J201, J202 N-Channel JFET

Features

- InterFET N0016SH Geometry
- Low Noise: 5 nV/√Hz Typical
- Low Ciss: 4pF Typical
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

Applications

- Audio Amplifiers
- Small Signal Amplifier
- Ultrahigh Impedance Pre-Amplifier
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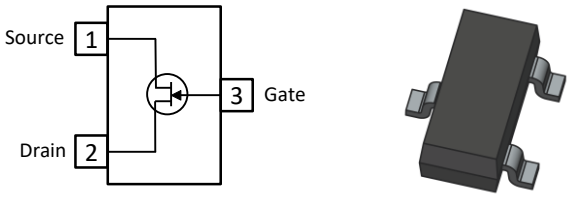
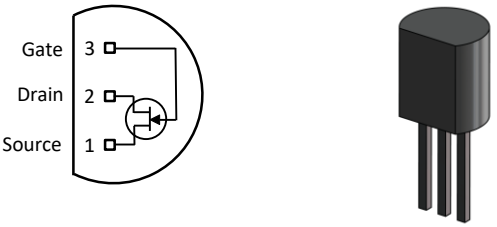
Description

The -40V InterFET J201 and J202 are targeted for sensitive amplifier stages for mid-frequencies designs. Gate leakages are typically less than 10pA at room temperatures.

SOT23 Top View



TO-92 Bottom View



Product Summary

Parameters		J201 Min	J202 Min	Unit
BV_{GSS}	Gate to Source Breakdown Voltage	-40	-40	V
I_{DSS}	Drain to Source Saturation Current	0.2	0.9	mA
$V_{GS(off)}$	Gate to Source Cutoff Voltage	-0.3	-0.8	V
G_{FS}	Forward Transconductance	500	1000	µS

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
J201; J202	Through-Hole	TO-92	Bulk
SMPJ201; SMPJ202	Surface Mount	SOT23	Bulk
SMPJ201TR; SMPJ202TR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
J201COT; J202COT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
J201CFT; J202CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters		Value	Unit
V_{RGS}	Reverse Gate Source and Gate Drain Voltage	-40	V
I_{FG}	Continuous Forward Gate Current	50	mA
P_D	Continuous Device Power Dissipation	360	mW
P	Power Derating	3.27	mW/°C
T_J	Operating Junction Temperature	-55 to 125	°C
T_{STG}	Storage Temperature	-65 to 200	°C

Static Characteristics (@ TA = 25°C, Unless otherwise specified)

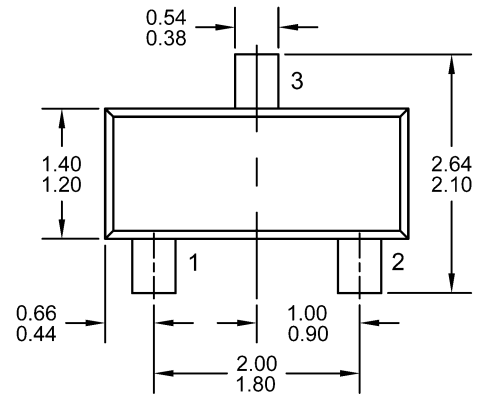
Parameters		Conditions	J201			J202			Unit
			Min	Typ	Max	Min	Typ	Max	
$V_{(BR)GSS}$	Gate to Source Breakdown Voltage	V_{DS} = 0V, I_G = -1µA	-40			-40			V
I_{GSS}	Gate to Source Reverse Current	V_{GS} = -20V, V_{DS} = 0V			-100			-100	pA
$V_{GS(OFF)}$	Gate to Source Cutoff Voltage	V_{DS} = 20V, I_D = 10nA	-0.3		-1.5	-0.8		-4	V
I_{DSS}	Drain to Source Saturation Current	V_{GS} = 0V, V_{DS} = 20V (Pulsed)	0.2		1	0.9		4.5	mA
I_G	Gate Operating Current	V_{DG} = 20V, I_D = $I_{DSS(min)}$		-10			-10		pA

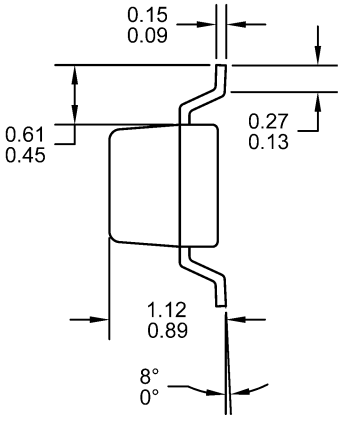
Dynamic Characteristics (@ TA = 25°C, Unless otherwise specified)

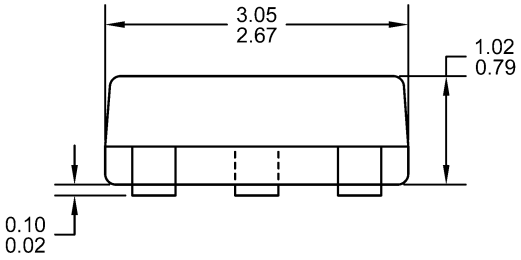
Parameters		Conditions	J201			J202			Unit
			Min	Typ	Max	Min	Typ	Max	
G_{FS}	Forward Transconductance	V_{DS} = 20V, V_{GS} = 0V, f = 1kHz	500			1000			µS
G_{OS}	Output Conductance	V_{DS} = 20V, V_{GS} = 0V, f = 1kHz		1			3.5		µS
C_{iss}	Input Capacitance	V_{DS} = 20V, V_{GS} = 0V, f = 1MHz		4			4		pF
C_{rss}	Reverse Transfer Capacitance	V_{DS} = 20V, V_{GS} = 0V, f = 1MHz		1			1		pF
e_n	Noise Voltage	V_{DS} = 10V, V_{GS} = 0V, f = 1kHz		5			5		nV/√Hz

SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data

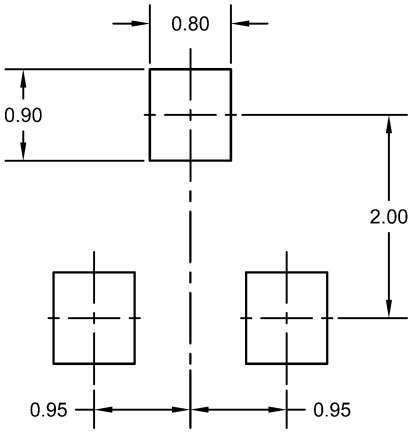






1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.