

J270, J271 P-Channel JFET

Features

- InterFET [P0099F Geometry](#)
- Low Noise: 6 nV/VHz Typical
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

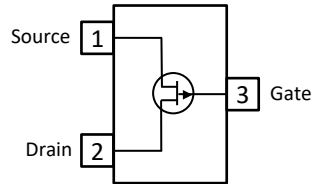
Applications

- Analog Switch
- Sample and Hold
- Low Noise, High Gain Amplifier

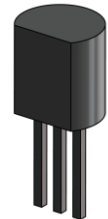
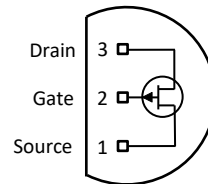
Description

The -30V InterFET J270 and J271 JFET is targeted for low noise high gain amplifiers and switch applications. The J270 has a cutoff voltage of less than 2.0V ideal for low-level power supplies.

SOT23 Top View



TO-92 Bottom View



Product Summary

Parameters	J270 Min	J271 Min	Unit
BV_{GSS} Gate to Source Breakdown Voltage	30	30	V
I_{DSS} Drain to Source Saturation Current	-2	-6	mA
$V_{GS(off)}$ Gate to Source Cutoff Voltage	0.5	1.5	V
G_{fs} Forward Transconductance	6	8	mS

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
J270; J271	Through-Hole	TO-92	Bulk
SMPJ270; SMPJ271	Surface Mount	SOT23	Bulk
SMPJ270TR; SMPJ271TR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
J270COT; J271COT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
J270CFT; J271CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack



Disclaimer: It is the Buyers responsibility for designing, validating and testing the end application under all field use cases and extreme use conditions. Guaranteeing the application meets required standards, regulatory compliance, and all safety and security requirements is the responsibility of the Buyer. These resources are subject to change without notice.

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters	Value	Unit
V _{RGS} Reverse Gate Source and Gate Drain Voltage	30	V
I _{FG} Continuous Forward Gate Current	50	mA
P _D Continuous Device Power Dissipation	360	mW
P Power Derating	2.8	mW/°C
T _J Operating Junction Temperature	-55 to 125	°C
T _{STG} Storage Temperature	-65 to 200	°C

Static Characteristics (@ T_A = 25°C, Unless otherwise specified)

Parameters	Conditions	J270		J271		Unit
		Min	Max	Min	Max	
V _{(BR)GSS} Gate to Source Breakdown Voltage	V _{DS} = 0V, I _G = 1μA	30		30		V
I _{GSS} Gate to Source Reverse Current	V _{GS} = 10V, V _{DS} = 0V		200		200	pA
V _{GS(OFF)} Gate to Source Cutoff Voltage	V _{DS} = -10V, V _{GS} = 0V	0.5	2	1.5	4.5	V
I _{DSS} Drain to Source Saturation Current	V _{GS} = 0V, V _{DS} = -10V (Pulsed)	-2	15	-6	-50	mA

Dynamic Characteristics (@ T_A = 25°C, Unless otherwise specified)

Parameters	Conditions	J270		J271		Unit
		Min	Max	Min	Max	
G _{FS} Forward Transconductance	V _{DS} = -10V, V _{GS} = 0V, f = 1kHz	6	15	8	18	mS
C _{iss} Input Capacitance	V _{DS} = -10V, V _{GS} = 0V, f = 1MHz		32		32	pF
C _{rss} Reverse Transfer Capacitance	V _{DS} = -10V, V _{GS} = 0V, f = 1MHz		4		4	pF
e _n Noise Voltage	V _{DS} = 10V, I _D = 5mA, f = 1kHz	6 (typ)		6 (typ)		nV/√Hz

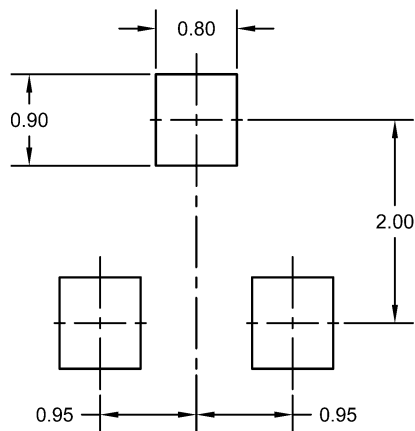
SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.