

PAD1, PAD2, PAD5 PicoAmp Diode

Features

- InterFET [N0001H Geometry](#)
- Low Leakage: 0.5pA Typical
- Low Capacitance: 0.8pF Typical
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

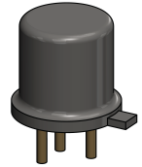
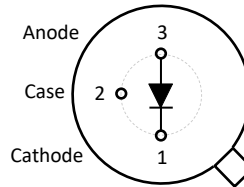
Applications

- High Impedance Protection Circuits
- Low Power Battery Circuitry
- High Impedance Diode Switching

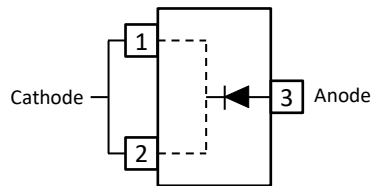
Description

The -45V InterFET PAD1 and PAD2 are targeted for low power and high impedance applications. Leakages are typically 0.5pA at room temperatures. The TO-18 package is hermetically sealed and suitable for military applications. For SOT23 functionality pins 1 and 2 must be externally shorted.

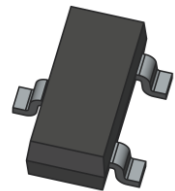
TO-18 Bottom View



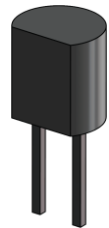
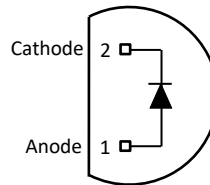
SOT23 Top View



Short Pins 1 and 2 Externally



TO-92 Bottom View



Product Summary

Parameters		PAD1 Min	PAD2 Min	PAD5 Min	Unit
BV _R	Breakdown Reverse Voltage	-45	-45	-45	V
I _R	Reverse Current	-1 (Max)	-2 (Max)	-5 (Max)	pA
V _F	Forward Voltage Drop	1.5 (Max)	1.5 (Max)	1.5 (Max)	V

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
PAD1; PAD2; PAD5	Through-Hole	TO-18	Bulk
PNPAD1; PNPAD2, PNPAD5	Through-Hole	TO-92-2L	Bulk
SMPPAD1; SMPPAD2; SMPPAD5	Surface Mount	SOT23	Bulk
SMPPAD1TR; SMPPAD2TR; SMPPAD5TR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
PAD1COT; PAD2COT; PAD5COT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
PAD1CFT; PAD2CFT; PAD5CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack



Disclaimer: It is the Buyers responsibility for designing, validating and testing the end application under all field use cases and extreme use conditions. Guaranteeing the application meets required standards, regulatory compliance, and all safety and security requirements is the responsibility of the Buyer. These resources are subject to change without notice.

Electrical Characteristics

Maximum Ratings (@ T_A = 25°C, Unless otherwise specified)

Parameters	Value	Unit
V _{RGS} Reverse Gate Source and Gate Drain Voltage	45	V
I _{FG} Continuous Forward Gate Current	50	mA
P _D Continuous Device Power Dissipation	225	mW
P Power Derating	1.8	mW/°C
T _J Operating Junction Temperature	-55 to 125	°C
T _{STG} Storage Temperature	-55 to 125	°C

Static Characteristics (@ T_A = 25°C, Unless otherwise specified)

Parameters	Conditions	PAD1			PAD2			PAD5			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
BV _R Breakdown Reverse Voltage	I _R = -1μA	-45			-45			-45			V
I _R Reverse Current	V _R = -20V			-1			-2			-5	μA
V _F Forward Voltage Drop	I _F = 5mA		0.8	1.5		0.8	1.5		0.8	1.5	V
C _R Capacitance	V _R = -5V, f = 1MHz			0.8			0.8			0.8	pF

SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

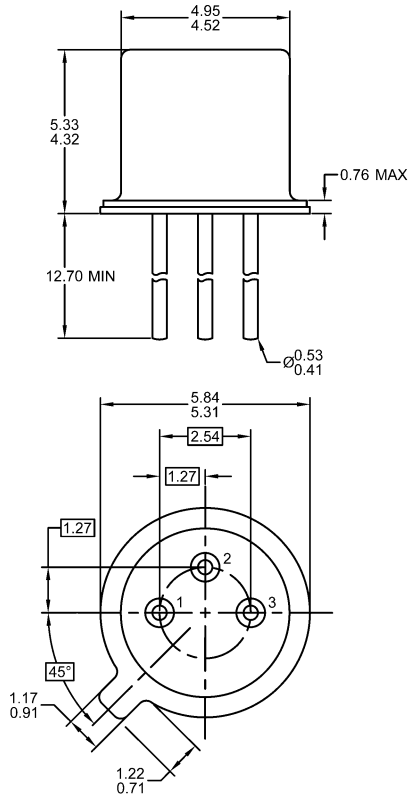
Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

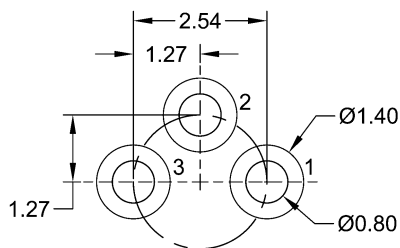
TO-18 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.29 grams
3. Bulk product is shipped in standard ESD shipping material
4. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.