

VCR3P P-Channel Voltage Controlled Resistor JFET

Features

- InterFET [P0099F Geometry](#)
- Low Leakage: 500pA Typical
- Low Input Capacitance: 18pF Typical
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

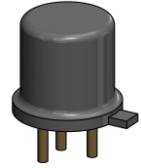
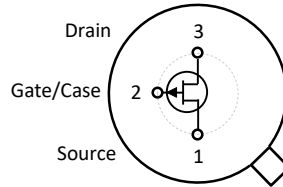
Applications

- Small Signal Attenuators
- Filters
- Amplifier Gain Control
- Oscillator Amplitude Control

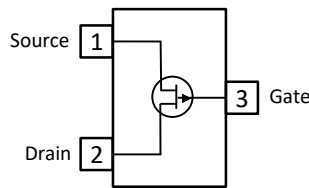
Description

The 15V InterFET VCR3P Voltage Controlled Resistor JFET is targeted for high input impedance applications. The resistance range of the VCR3P is 70 Ohms to 200 Ohms. The TO-18 package is hermetically sealed and suitable for military applications.

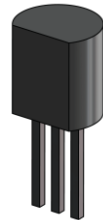
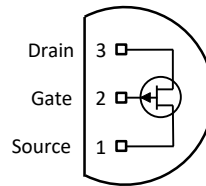
TO-18 Bottom View



SOT23 Top View



TO-92 Bottom View



Product Summary

Parameters	VCR3P Min	Unit
BV_{GSS} Gate to Source Breakdown Voltage	15	V
$V_{GS(off)}$ Gate to Source Cutoff Voltage	1	V
$r_{ds(on)}$ Drain to Source ON Resistance	70	Ω

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
VCR3P	Through-Hole	TO-18	Bulk
PNVCR3P	Through-Hole	TO-92	Bulk
SMPVCR3P	Surface Mount	SOT23	Bulk
SMPVCR3PTR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
VCR3PCOT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
VCR3PCFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack



Disclaimer: It is the Buyers responsibility for designing, validating and testing the end application under all field use cases and extreme use conditions. Guaranteeing the application meets required standards, regulatory compliance, and all safety and security requirements is the responsibility of the Buyer. These resources are subject to change without notice.

Electrical Characteristics

Maximum Ratings (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Value	Unit
V_{RGS} Reverse Gate Source and Gate Drain Voltage	15	V
I_{FG} Continuous Forward Gate Current	10	mA
P_D Continuous Device Power Dissipation	300	mW
P Power Derating	2.4	mW/ $^\circ\text{C}$
T_J Operating Junction Temperature	-55 to 125	$^\circ\text{C}$
T_{STG} Storage Temperature	-65 to 150	$^\circ\text{C}$

Static Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Conditions	VCR3P		Unit
		Min	Max	
$V_{(BR)GSS}$ Gate to Source Breakdown Voltage	$I_G = 1\mu\text{A}, V_{DS} = 0\text{V}$	15		V
I_{GSS} Gate to Source Reverse Current	$V_{GS} = 15\text{V}, V_{DS} = 0\text{V}$		20	nA
$V_{GS(OFF)}$ Gate to Source Cutoff Voltage	$V_{DS} = -10\text{V}, I_D = -1\mu\text{A}$	1	5	V

Dynamic Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Conditions	VCR3P		Unit
		Min	Max	
$r_{ds(on)}$ Drain to Source ON Resistance	$I_D = 0\text{A}, V_{GS} = 0\text{V}, f = 1\text{kHz}$	70	200	Ω
C_{dg} Drain Gate Capacitance	$V_{DG} = 10\text{V}, I_S = 0\text{A}, f = 1\text{MHz}$		25	pF
C_{sg} Source Gate Capacitance	$V_{GS} = 10\text{V}, I_D = 0\text{A}, f = 1\text{MHz}$		15	pF

SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

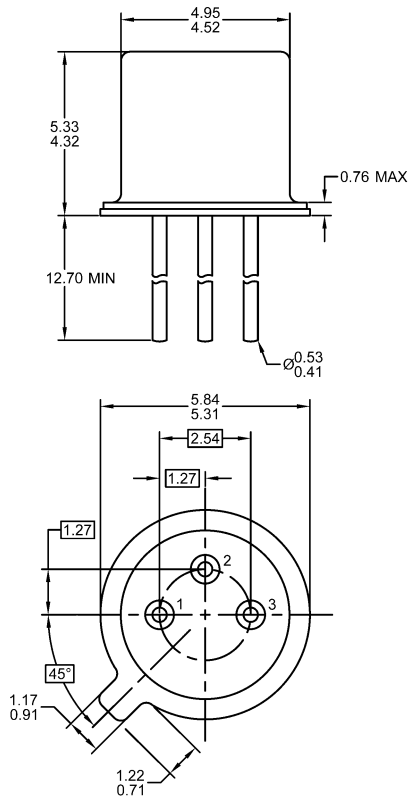
Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

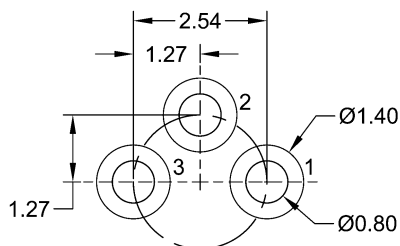
TO-18 Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.29 grams
3. Bulk product is shipped in standard ESD shipping material
4. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.