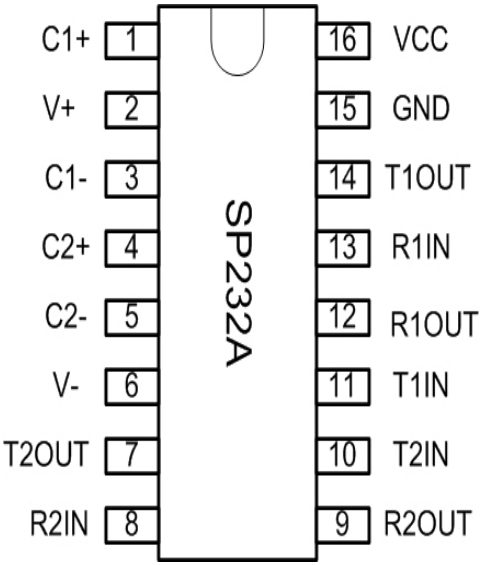
MAXLINEAR

SP232A

Enhanced RS-232 Line Drivers/Receivers

FEATURES

- Operates from a Single +5V Power Supply
- Meets all RS-232F and ITU V.28 Specifications
- Operates with 0.1µF Ceramic Capacitors
- High Data rate - 120kbps under load
- Low power CMOS Operation
- +/-2kV Human Body Model ESD Protection
- Lead Free packaging available



DESCRIPTION

The SP232A is a line driver and receiver pair that meets the specifications of RS-232 and V.28 serial protocols. This device is pin-to-pin compatible with popular industry standard pinouts. The SP232A offers 120kbps data rate under load, small ceramic type 0.1µF charge pump capacitors and overall ruggedness for comercial applications. The SP232A features Exar's BiCMOS design allowing for low power operation without sacrificing performance. This device is avaialble in plastic DIP, SOICW and nSOIC packages operating over the commercial and industrial temperature ranges.

SOICW and nSOIC versions available, PDIP versions are obsolete.

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below are not implied. Exposure to absolute maximum ratings conditions for extended periods of time may affect reliability.

Supply Voltage (V_{CC}).....+ 6V
V+..... (Vcc-0.3V) to +11.0V
V- .....-11.0V
Input Voltages
Tin.....-0.3V to (Vcc + 0.3V)
Rin.....+/-15V
Output Voltages
Tout.....(V+, +0.3V) to (V-, -0.3V
Rout.....-0.3V to (Vcc + 0.3V)

Short Circuit duration
Tout.....Continuous
Package Power Dissipation:
Plastic DIP.....375mW
(derate 7mW/°C above +70°C)
Small Outline.....375mW
(derate 7mW/°C above +70°C)
Storage Temperature.....-65°C to +150°C
Lead Temperature (soldering, 10s)..... +300°C

ELECTRICAL CHARACTERISTICS

Vcc=5V ±10%, 0.1µF charge pump capacitors, T_{MIN} to T_{MAX}, unless otherwise noted, Typical values are Vcc=5V and T_A=25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
TTL INPUT					
Logic Threshold LOW	TIN			0.8	Volts
Logic Threshold HIGH	TIN	2.0			Volts
Logic Pull-Up Current	TIN = 0V		15	200	µA
TTL OUTPUT					
Output Voltge LOW	I_{OUT} = 3.2 mA: Vcc = +5V			0.4	Volts
Output Voltage HIGH	I_{OUT} = -1.0 mA	3.5			Volts
RS-232 OUTPUT					
Output Voltage Swing	All Transmitter outputs loaded with 3k ohms to GND	+/-5.0	+/-6.5V		Volts
Output Resistance	Vcc = 0V, Vout = +/-2V	300			Ohms
Output Short Circuit Current	Infinite Duration		+/-18		mA
Maximum Data Rate	CL = 2500pF, RL = 3kΩ	120	240		kbps
RS-232 INPUT					
Voltage Range		-15		+15	Volts
Voltage Threshold LOW	Vcc = 5V, T_A=25°C	0.8	1.2		Volts
Voltage Threshold HIGH	Vcc = 5V, T_A=25°C		1.7	2.4	Volts
Hysteresis	Vcc = 5V, T_A=25°C	0.2	0.5	1.0	Volts
Resistance	T_A=25°C, -15V ≤ V_{IN} ≤ +15V	3	5	7	kΩ

ELECTRICAL CHARACTERISTICS

Vcc=5V ±10%, 0.1µF charge pump capacitors, TMIN to TMAX, unless otherwise noted, Typical values are Vcc=5V and TA=25°C

DYNAMIC CHARACTERISTICS					
Driver Propagation Delay	TTL to RS_232; CL = 50pF		1.5	3.0	µs
Receiver Propagation Delay	RS-232 to TTL,		0.1	1.0	µs
Instantaneous Slew Rate	CL = 10pF, RL = 3-7kΩ			30	V/ µs
Transition Region Slew Rate	CL = 2500pF, RL = 3kΩ; Measured from +3V to -3V or -3V to +3V		10		V/ µs
POWER REQUIREMENTS					
Vcc Power Supply Current	No Load, Vcc = 5V, TA=25°C		1.5	5	mA
Vcc Power Supply Current, Loaded	All Transmitters RL = 3kΩ, TA=25°C		11		mA

PIN ASSIGNMENTS

Pin Number	Pin Name	Pin Function
1	C1+	Positive terminal of the voltage doubler charge pump capacitor
2	V+	+6.5V generated by the charge pump
3	C1-	Negative terminal of the voltage doubler charge pump capacitor
4	C2+	Positive terminal of the inverting charge pump capacitor
5	C2-	Negative terminal of the inverting charge pump capacitor
6	V-	-6.7V generated by the charge pump
7	T2OUT	RS-232 driver output
8	R2IN	RS-232 receiver input
9	R2OUT	TTL/CMOS receiver output
10	T2IN	TTL/CMOS driver input
11	T1IN	TTL/CMOS driver input
12	R1OUT	TTL/CMOS receiver output
13	R1IN	RS-232 receiver input
14	T1OUT	RS-232 driver output
15	GND	Ground
16	Vcc	5V supply voltage

DETAILED DESCRIPTION

The SP232A transceiver is a two driver and two receiver device that meets the EIA/TIA- 232 and V.28 serial communication protocol. The device is pin-to-pin compatible with popular industry standard pinouts. The SP232A offers 120kbps data rate, 10V/μs slew rate and a regulated charge pump that operates from a single 5V supply. The proprietary on-board charge pump generates a regulated output of +/-6.5V for RS-232 compliant voltage levels.

Theory Of Operation

The SP232A is made up of three basic circuit blocks: 1. Driver, 2. Receiver, and 3. charge pump.

Drivers

The drivers are inverting level transmitters that convert TTL or CMOS logic levels to EIA/TIA-232 levels with an inverted sense relative to the input logic levels. Typically, the RS-232 output voltage swing is +/-6.5V with no load and +/-5.0V minimum when fully loaded. The driver outputs are protected against infinite short-circuits to ground without degradation in reliability.

The drivers can guarantee output data rates of 120Kbps under worst case loading of 3k ohms and 2500pF.

The driver output Slew Rate is internally limited to 30V/μs in order to meet the EIA standards (EIA-232F). Additionally, the driver output LOW to HIGH transition meet the monotonicity output requirements of the standard.

Receivers

The receivers convert EIA/TIA-232 signal levels to TTL or CMOS logic output levels. Since the input is usually from a transmission line, where long cable length and system interference can degrade the signal, the receiver inputs have a typical hysteresis margin of 500mV. This ensures that the receiver is virtually immune to noisy transmission lines. Should a input be left unconnected, an internal 5Kohm pull-down resistor to ground will commit the output of the receiver to a logic HIGH state. The input voltage range for the SP232A Receiver is +/-15V.

Charge pump

The charge pump is a patented design and uses a unique approach compared to older less efficient designs. The charge pump requires 4 external capacitors and uses a four phase voltage shifting technique. The internal power supply consists of a regulated dual charge pump that provides output voltages of +/-6.5V. This is important to maintain compliant RS-232 levels regardless of power supply fluctuations. The charge pump operates in a discontinous mode using an internal oscillator. If the voltages are less than a magnitude of 6.5V, the charge pump is enabled. If the output voltage exceed a magnitude of 6.5V then the charge pump is disabled. The internal oscillator controls the four phases of the voltage shifting. A description of each phase follows:

Phase 1

Vss charge store and double: The positive terminals of capacitors C1 and C2 are charged from Vcc with their negative terminals initially connected to ground. C1+ is then connected to ground and the stored charge from C1- is superimposed onto C2-. Since C2+ is still connected to Vcc the voltage potential across C2 is now 2 x Vcc.

Phase 2

Vss transfer and invert: Phase two connects the negative terminal of C2 to the Vss storage capacitor and the positive terminal of C2 to ground. This transfers the doubled and inverted (V-) voltage onto C4. Meanwhile, capacitor C1 is charged from Vcc in order to prepare it for its next phase.

Phase 3

Vdd charge store and double: Phase three is identical to the first phase. The positive terminals of C1 and C2 are charged from Vcc with their negative terminals initially connected to ground. C1+ is then connected to ground and the stored charge from C1- is superimposed onto C2-. Since C2+ is still connected to Vcc the voltage potential across capacitor C2 is now 2 x Vcc.

Phase 4

Vdd transfer. The fourth phase connects the negative terminal of C2 to ground and the positive terminal of C2 to the Vdd storage capacitor . This transfers the doubled (V+) voltage onto C3. Meanwhile, capacitor C1 is charged from Vcc to prepare it for its next phase.

Under lightly loaded conditions, the intelligent pump oscillator maximizes efficiency by running only as needed to maintain V+ and V- voltage levels. Since interface transceivers spend most of their time at idle, this power-efficient innovation can greatly reduce total power consumption. This improvement is made possible by the independent phase sequences of the Exar charge pump design.

The clock rate of the charge pump typically operates greater than 70kHz allowing the pump to operate efficiently with small 0.1uF capacitors. Efficient operation depends on rapid charging and discharging of C1 and C2. Therefore, the capacitors should be mounted as close as possible to the IC and have a low ESR (equivalent series resistance). Inexpensive, surface mount ceramic capacitors are ideal for use on charge pump. If polarized capacitors are used the positive and negative terminals should be connected as shown on the typical operating circuit. A diagram of the 4 individual phases is shown in Figure 1.

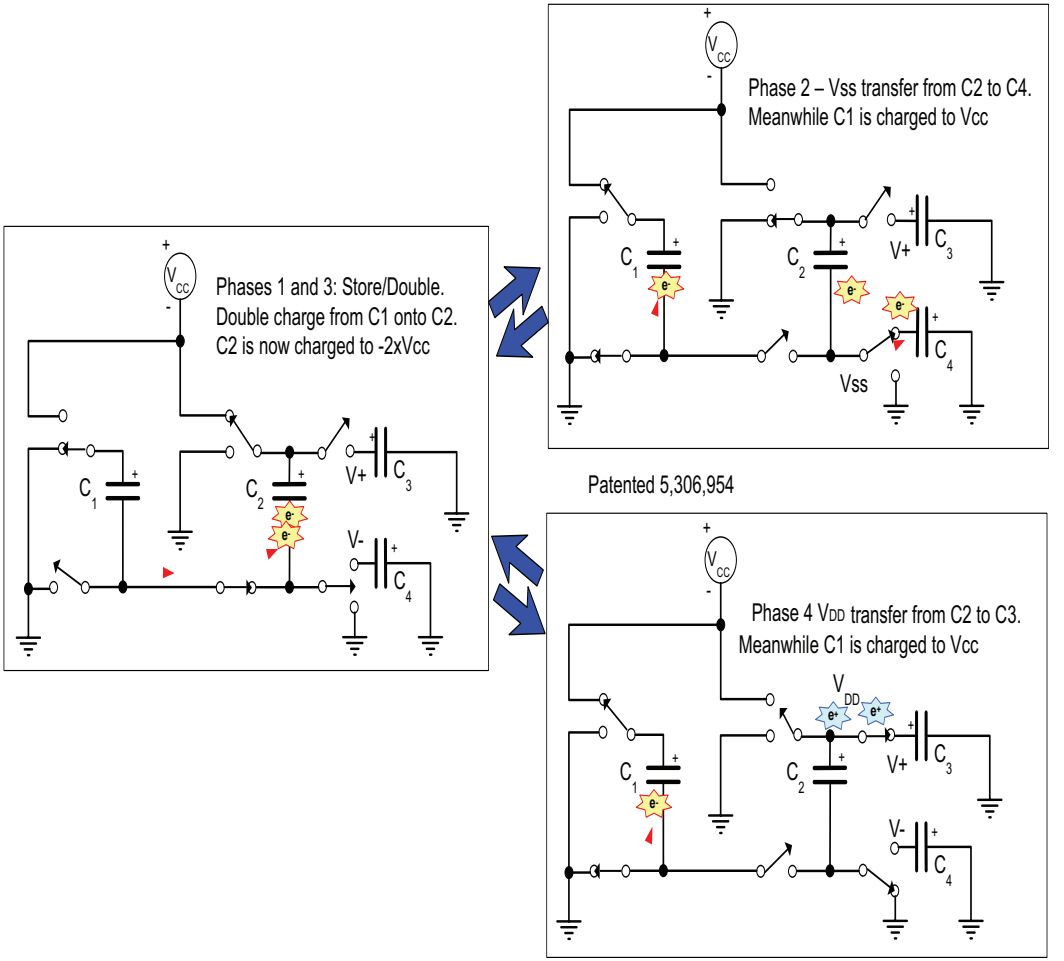


Figure 1. Charge pump phases

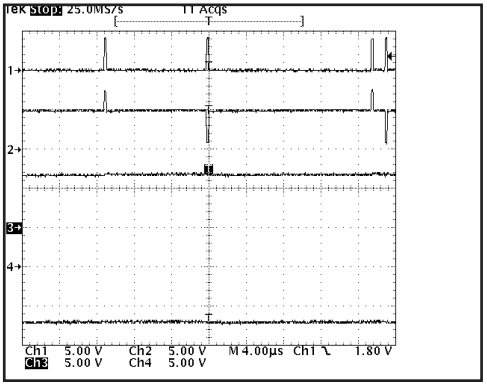


Figure 2, Charge pump waveforms with no load (1 = C1+, 2 = C2+, 3 = V+, 4 = V-).

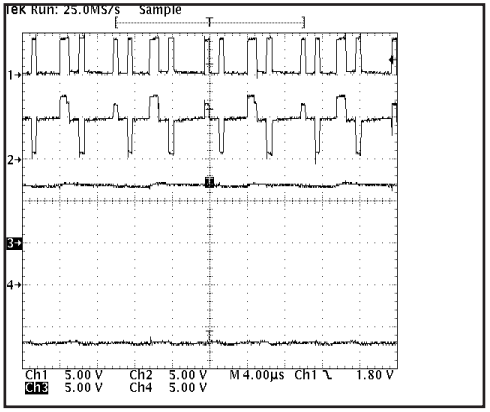


Figure 3, Charge pump waveforms when fully loaded with 3k ohms (1 = C1+, 2 = C2+, 3 = V+, 4 = V-).

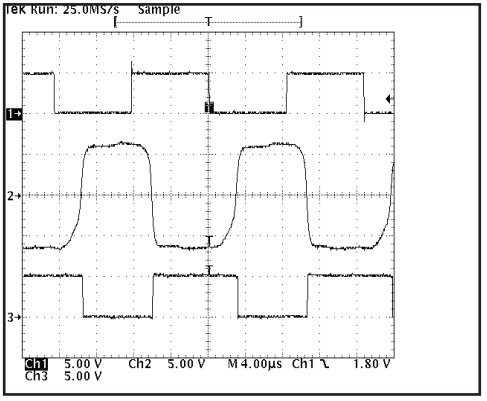


Figure 4, Loopback results at 60kHZ and 2500pF load (1 = TXin, 2 = TXout/RXin, 3 = RXout).

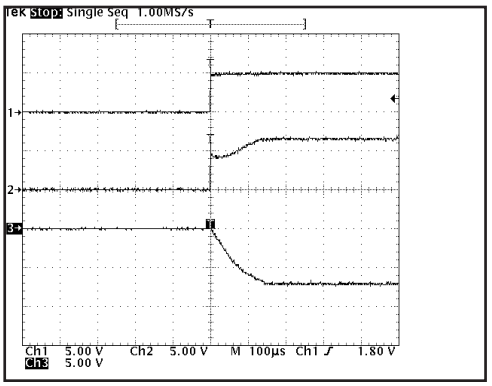


Figure 5, Charge pump outputs at start up (1 = Vcc, 2 = V+, 3 = V-).

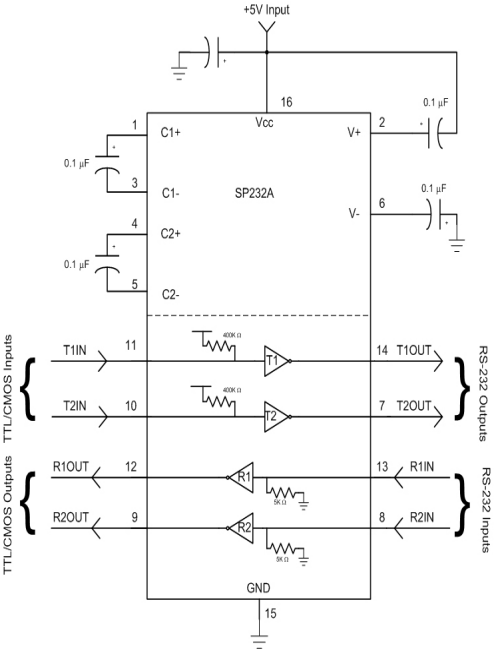
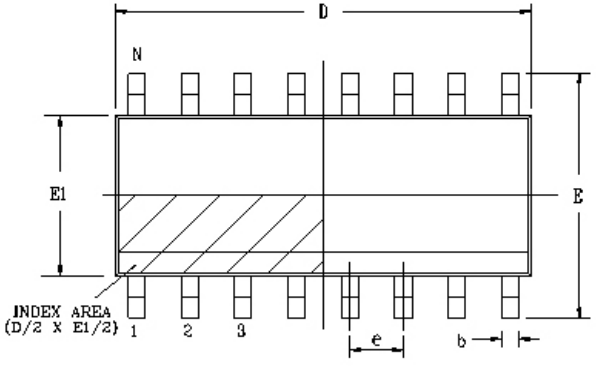


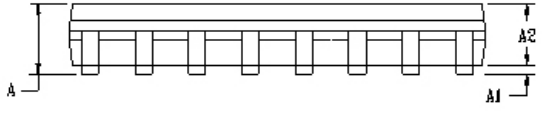
Figure 6, Typical Application circuit

REVISION HISTORY			
REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	10/12/05	JL
B	DRAWING FORMAT MODIFICATION	07/19/06	JL
C	CHANGE DRAWING LOGO AND COMPANY NAME	11/21/07	JL

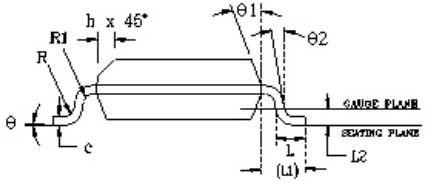


Top View

16 Pin SOICN JEDEC MS-012 Variation AC						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	—	1.75	0.053	—	0.069
A1	0.10	—	0.25	0.004	—	0.010
A2	1.25	—	1.65	0.049	—	0.065
b	0.31	—	0.51	0.012	—	0.020
c	0.17	—	0.25	0.007	—	0.010
E	6.00 BSC			0.236 BSC		
E1	3.90 BSC			0.154 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25	—	0.50	0.010	—	0.020
L	0.40	—	1.27	0.016	—	0.050
L1	1.04 REF			0.041 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	—	—	0.003	—	—
R1	0.07	—	—	0.003	—	—
θ	0°	—	8°	0°	—	8°
θ1	5°	—	15°	5°	—	15°
θ2	0°	—	—	0°	—	—
D	9.90 BSC			0.390 BSC		
N	16			16		



Side View

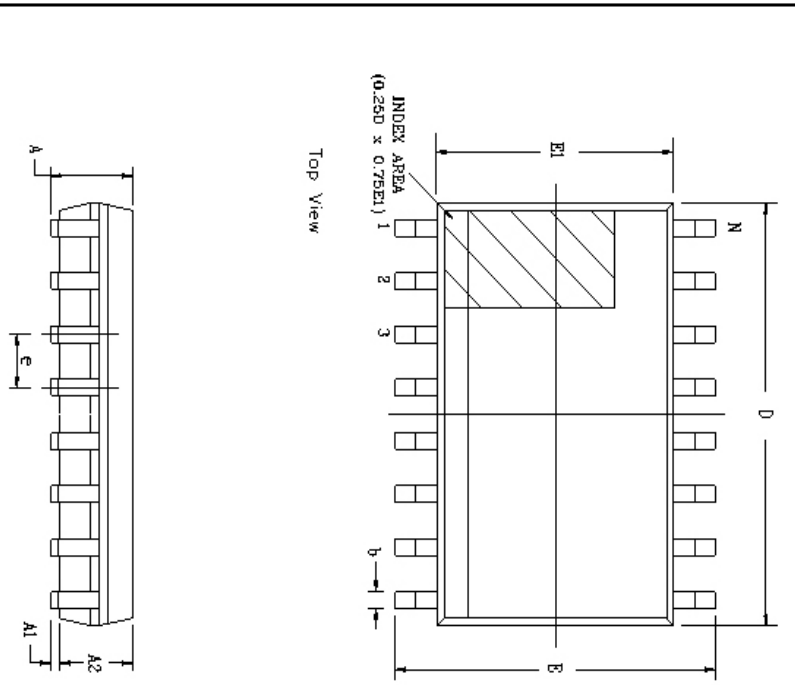


Front View

EXAR CORPORATION			
	16 PIN SOICN PACKAGE OUTLINE		
Packaging Approval:		Drawing No: 16-PIN SOICN	
By: JL	Date: 11/21/07	Revision: C	Sheet: 1 OF 1

16 pin PDIP versions are obsolete.

REVISION HISTORY			
REV.	DESCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	11/05/05	JL
B	DRAWING FORMAT MODIFICATION	09/15/08	JL
C	CHANGE DRAWING LOGO AND COMPANY NAME	11/21/07	JL



16 Pin SOICW JEDEC MS-013 Variation AA

SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.35	—	2.65	0.093	—	0.104
A1	0.10	—	0.30	0.004	—	0.012
A2	2.05	—	2.55	0.081	—	0.100
b	0.31	—	0.51	0.012	—	0.020
c	0.20	—	0.33	0.008	—	0.013
E	10.30 BSC			0.406 BSC		
E1	7.50 BSC			0.295 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25	—	0.75	0.010	—	0.030
L	0.40	—	1.27	0.016	—	0.050
L1	1.40 REF			0.055 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	—	—	0.003	—	—
R1	0.07	—	—	0.003	—	—
θ	0°	—	8°	0°	—	8°
θ1	5°	15°	5°	0°	—	15°
θ2	0°	—	—	0°	—	—
D	10.30 BSC			0.405 BSC		
N	16			16		

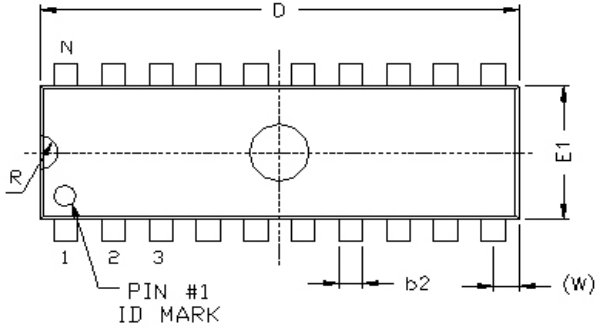
EXAR CORPORATION

16 PIN SOICW PACKAGE OUTLINE

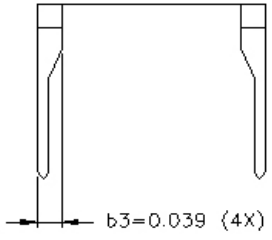
Packaging Approval:		Drawing No:	16-PIN SOICW
Drn: JL	Date: 11/21/07	Revision: C	Sheet: 1 OF 1

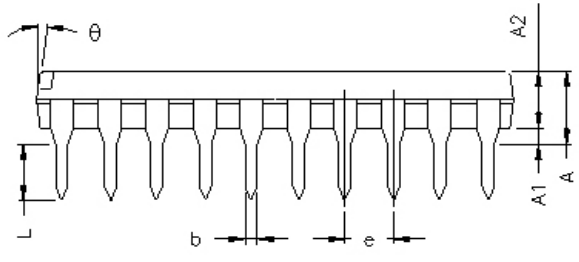
REVISION HISTORY			
REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	11/21/05	JL
B	DRAWING FORMAT MODIFICATION	04/26/06	JL
C	CHANGE DRAWING LOGO AND COMPANY NAME	11/21/07	JL

REMARKS:
FOR 8LD AND 16LD
ALL END LEADS (4X)
ARE HALF LEAD TYPES

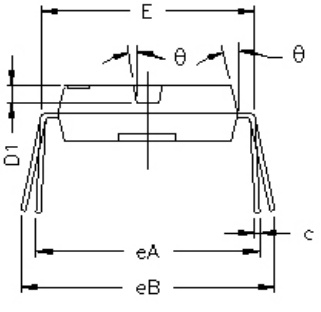


Top View





Side View



Front View

16 Pin PDIP JEDEC MS-001 Variation BB						
SYMBOLS	DIMENSIONS IN INCH (Control Unit)			DIMENSIONS IN MM (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	0.210	—	—	5.33
A1	0.015	—	—	0.38	—	—
A2	0.115	0.130	0.195	2.92	3.30	4.95
b	0.014	0.018	0.022	0.36	0.46	0.56
b2	0.045	0.060	0.070	1.14	1.52	1.78
c	0.008	0.010	0.014	0.20	0.25	0.36
D1	0.030	—	0.060	0.76	—	1.52
E	0.300	0.310	0.325	7.62	7.87	8.26
E1	0.240	0.250	0.280	6.10	6.35	7.11
e	0.100 BSC			2.54 BSC		
eA	0.300 BSC			7.62 BSC		
eB	—	—	0.430	—	—	10.92
L	0.115	0.130	0.150	2.92	3.30	3.81
W	0.075 REF			1.91 REF		
R	0.030 BSC			0.76 BSC		
θ	4°	7°	10°	4°	7°	10°
D	0.735	0.755	0.775	18.67	19.18	19.69
N	16			16		

EXAR CORPORATION

16 PIN PDIP PACKAGE OUTLINE

Packaging Approval:		Drawing No:	16-PIN PDIP
By: JL	Date: 11/21/07	Revision: C	Sheet: 1 OF 1