SP332

RS-232/RS-485 Multi-Mode Serial Transceiver

Description

The SP332 is a monolithic device that contains both RS-232 and RS-485 line drivers and receivers. The configuration of the SP332 can be changed at any time by changing the logic state of two control pins. The device also includes a loop back function which internally connects driver outputs to receiver inputs for a chip self test. An MaxLinear-patented charge pump allows 5V-only operation.

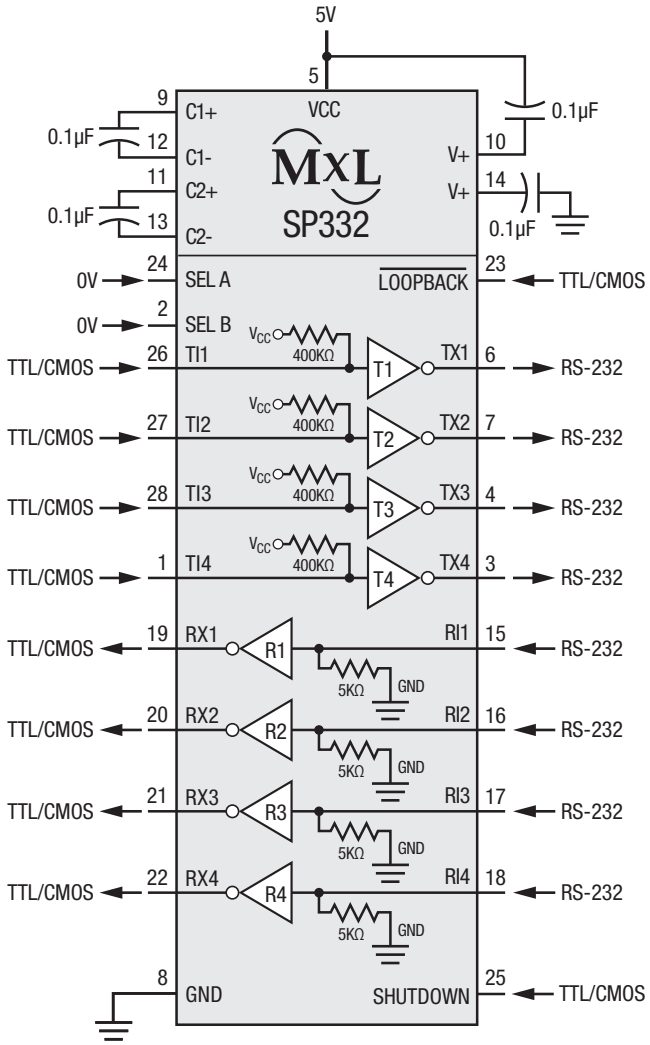
FEATURES

- 5V only single supply operation
- Software programmable RS-232 or RS-485 selection
- 4 drivers, 4 receivers RS-232
- 2 drivers, 2 receivers RS-485
- Loop back function for self test
- 28-pin WSOIC package

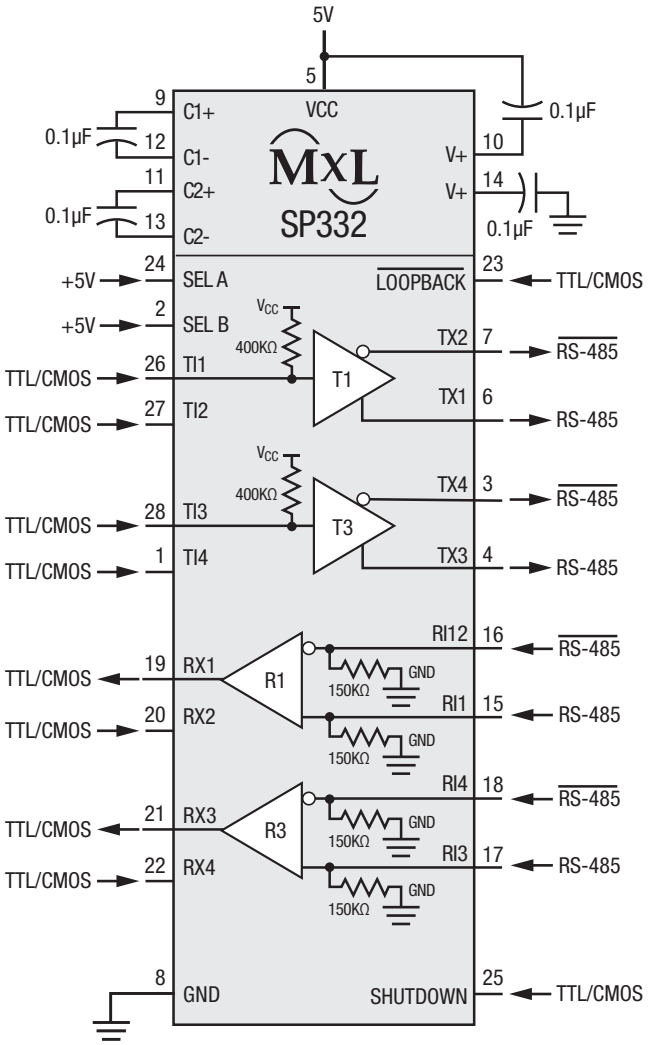
Ordering Information - Back Page

Typical Applications Circuit

RS-232 Mode



Full Duplex RS-485 Mode Mode



Absolute Maximum Ratings

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections to the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC} 7V

Input Voltages

Logic ..... -0.5V to (V_{CC} + 0.5V)

Drivers ..... -0.5V to (V_{CC} + 0.5V)

Receivers.....±30V @ ≤100mA

Driver Outputs .....±15V

Maximum Data Rate..... 8Mbps(1)

Storage Temperature ..... -65°C to 150°C

Power Dissipation

28-pin WSOIC 1000mW

Power Derating, $ø_{JA}$

28-pin WSOIC ..... 40°C/W

Electrical Characteristics

Limits are specified at T_A = 25°C and V_{CC} = 5.0V unless otherwise noted.

Parameters	Min.	Typ.	Max.	Units	Conditions
RS-485 Driver DC Characteristics					
Differential output voltage			Vcc	Volts	Unloaded; R = ∞Ω; See Figure 1
Differential output voltage	2.0		5.0	Volts	With load; R = 50Ω (RS-422); See Figure 1
Differential output voltage	1.5		5.0	Volts	With load; R = 27Ω (RS-485); See Figure 1
Change in magnitude of driver differential output voltage for complementary states			0.2	Volts	R = 27Ω or R = 50Ω; See Figure 1
Driver common-mode output voltage			3	Volts	R = 27Ω or R = 50Ω; See Figure 1
Input high voltage	2.0			Volts	Applies to transmitter inputs, SEL A, SEL B, SD and $\overline{LB}$
Input low voltage			0.8	Volts	Applies to transmitter inputs, SEL A, SEL B, SD and $\overline{LB}$
Input current			±10	µA	Applies to transmitter inputs, SEL A, SEL B, SD and $\overline{LB}$
Pull-up current		1.5		µA	
Pull-down current		3.0		µA	
Driver short circuit current V_{OUT} = HIGH	35		250	mA	-7V ≤ V_O ≤ 10V
Driver short circuit current V_{OUT} = LOW	35		250	mA	-7V ≤ V_O ≤ 10V
RS-485 Driver AC Characteristics					
Driver data rate	10			Mbps	
Driver data rate			8	Mbps	T_A = 85°C(1)
Driver input to output t_{PLH}		70	180	ns	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF; see Figures 3 and 5
Driver input to output t_{PHL}		70	180	ns	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF; see Figures 3 and 5
Driver skew		5	10	ns	From output to output; see Figures 3 and 5
Driver rise or fall time	3	15	40	ns	From 10% to 90%; R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF; see Figures 3 and 5

Electrical Characteristics (Continued)

Limits are specified at T_A = 25°C and V_{CC} = 5.0V unless otherwise noted.

Parameters	Min.	Typ.	Max.	Units	Conditions
RS-485 Receiver DC Characteristics					
Differential input threshold	-0.2		0.2	Volts	-7V ≤ V_{CM} ≤ 12V
Input hysteresis		70		mV	V_{CM} = 0V
Output voltage HIGH	3.5			Volts	I_O = -4mA, V_{ID} = 200mV
Output voltage LOW			0.4	Volts	I_O = 4mA, V_{ID} = -200mV
Input resistance	12	15		kΩ	-7V ≤ V_{CM} ≤ 12V
Input current (A, B); V_{IN} = 12V			1.5	mA	V_{IN} = 12V, A is the non-inverting receiver input. B is the inverting receiver input
Input current (A, B); V_{IN} = -7V			-0.8	mA	V_{IN} = -7V
Short circuit current			85	mA	0V ≤ V_{CM} ≤ V_{CC}
RS-485 Receiver AC Characteristics					
Receiver data rate	10			Mbps	
Receiver data rate			8	Mbps	T_A = 85°C(1)
Receiver input to output t_{PLH}		130	250	ns	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF; Figures 3 and 6
Receiver input to output t_{PHL}		130	250	ns	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF; Figures 3 and 6
Differential receiver skew $\lvert t_{PHL} - t_{PLH} \rvert$		13		ns	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF; Figures 3 and 6
RS-232 Driver DC Characteristics					
TTL input level V_{IL}			0.8	Volts	Applies to transmitter inputs, SEL A, SEL B, SD and $\overline{LB}$
TTL input level V_{IH}	2.0			Volts	Applies to transmitter inputs, SEL A, SEL B, SD and $\overline{LB}$
High level voltage output	5.0		15.0	Volts	R_L = 3kΩ to GND
Low level voltage output	-15.0		-5.0	Volts	R_L = 3kΩ to GND
Open circuit output			±15	Volts	R_L = ∞
Short circuit current			±100	mA	V_{OUT} = 0V
Power off impedance	300			Ω	V_{CC} = 0V; V_{OUT} = ±2V
RS-232 Driver AC Characteristics					
Transmission rate	120			kbps	
Transition time			1.56	µs	Rise/fall time, 3V to -3V; -3V to 3V, R_L = 3kΩ, C_L = 2500pF
Propagation delay; t_{PHL}		2	4	µs	R_L = 3kΩ, C_L = 2500pF, from 1.5V of T_{IN} to 50% of V_{OUT}
Propagation delay; t_{PLH}		2	4	µs	R_L = 3kΩ, C_L = 2500pF, from 1.5V of T_{IN} to 50% of V_{OUT}
Slew rate		10	30	V/µs	R_L = 3kΩ, C_L = 50pF; From 3V to -3V or -3V to 3V

Electrical Characteristics (Continued)

Limits are specified at T_A = 25°C and V_{CC} = 5.0V unless otherwise noted.

Parameters	Min.	Typ.	Max.	Units	Conditions
RS-232 Receiver DC Characteristics					
TTL output level; V_{OL}			0.4	Volts	I_{SINK} = 4mA
TTL output level; V_{OH}	3.5			Volts	I_{SOURCE} = -4mA
Input high threshold		2.1	3.0	Volts	
Input low threshold	0.8	1.6		Volts	
Input voltage range	-15		15	Volts	
Input impedance	3	5	7	kΩ	V_{IN} = ±15V
Hysteresis	0.2	0.5	1.0	Volts	V_{CC} = 5V
RS-232 Receiver AC Characteristics					
Transmission rate	120			kbps	
Transition time		50		ns	Rise/fall time, 10% to 90%
Propagation delay t_{PHL}		100	300	ns	From 50% of V_{IN} to 1.5V of R_{OUT}
Propagation delay t_{PLH}		100	200	ns	
Power Requirements					
No load supply current		19	25	mA	No load; V_{CC} = 5.0V; T_A = 25°C
Full load supply current		90	120	mA	RS-232 drivers R_L = 3kΩ to GND, DC input RS-485 drivers R_L = 54Ω from A to B; DC input
Shutdown supply current		5	50	µA	T_A = 25°C, V_{CC} = 5.0V

NOTE

1. Exceeding the maximum data rate may damage the device.

Test Circuits

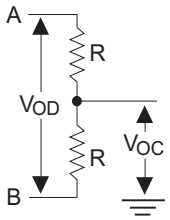


Figure 1: RS-485 Driver DC Test Load Circuit

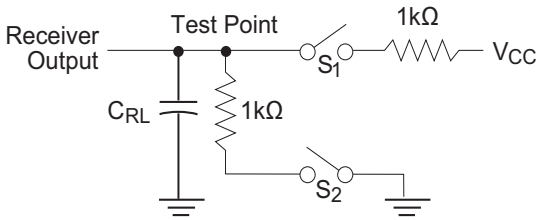


Figure 2. Receiver Timing Test Load Circuit

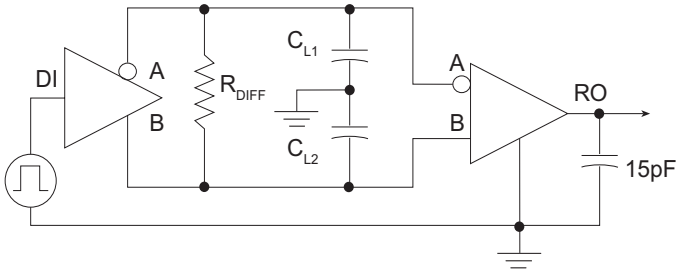


Figure 3: RS-485 Driver/Receiver Timing Test Circuit

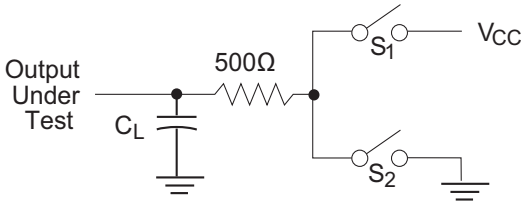


Figure 4: RS-485 Driver Timing Test Load #2 Circuit

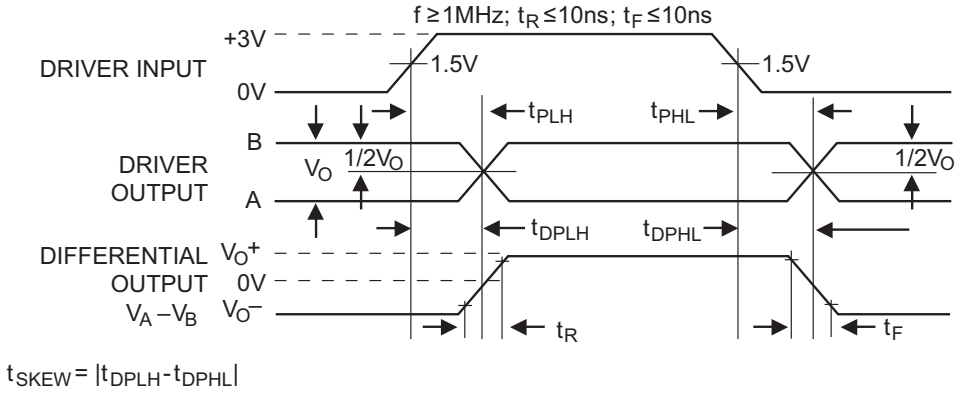


Figure 5: RS-485 Driver Propagation Delays

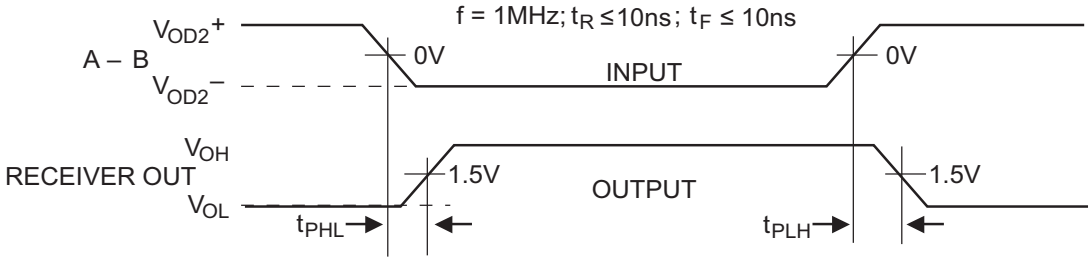
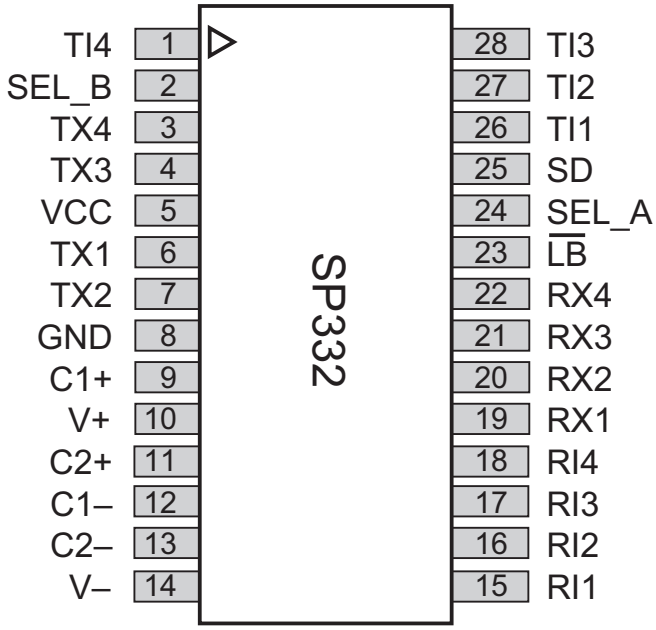


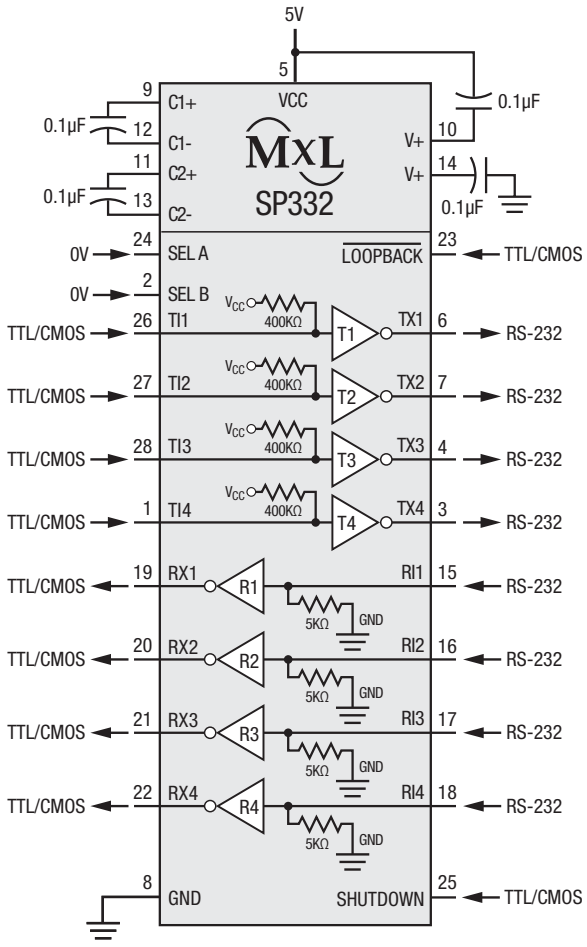
Figure 6: RS-485 Receiver Propagation Delays

Pin Configuration

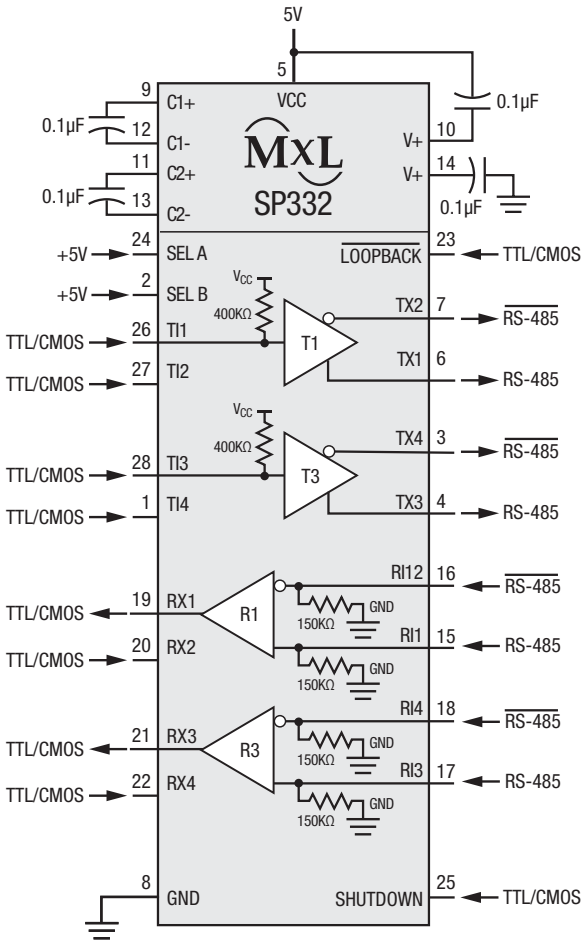


Typical Applications Circuits

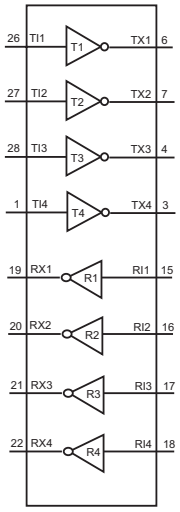
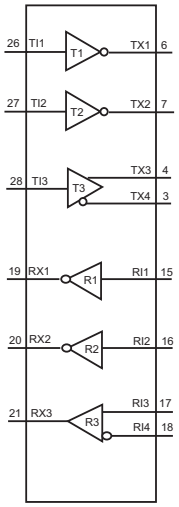
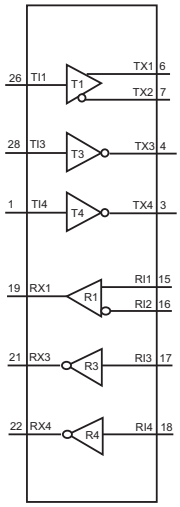
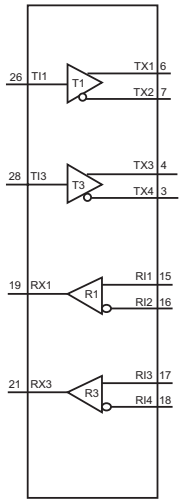
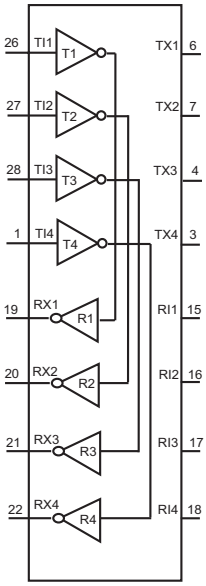
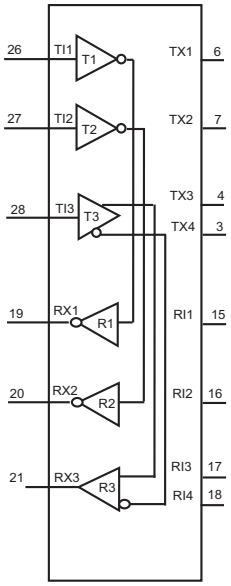
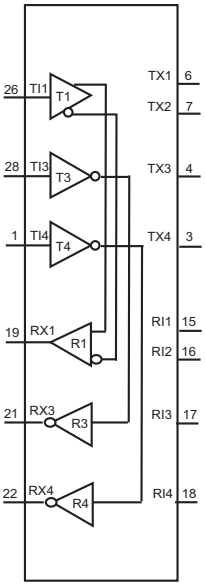
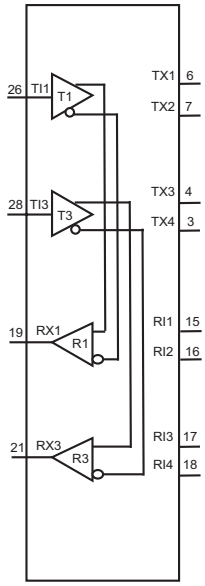
RS-232 Mode



Full Duplex RS-485 Mode Mode



SP332 Control Logic Configuration

SEL A	0	0	1	1
SEL B	0	1	0	1
$\overline{LB}$	1	1	1	1
SD	0	0	0	0
				
SEL A	0	0	1	1
SEL B	0	1	0	1
$\overline{LB}$	0	0	0	0
SD	0	0	0	0
				

Receiver Inputs are inactive in Loopback Mode ($\overline{LOOPBACK}$ = 0)

Driver Outputs are Tri-stated in Loopback Mode ($\overline{LOOPBACK}$ = 0)

Unused Outputs are Tri-stated

Functional Description

The SP332 is single chip device that can be configured via software for either RS-232, RS-485 or both interface modes at any time. The SP332 is made up of three basic circuit elements, single-ended drivers and receivers, differential drivers and receivers and charge pump.

Differential Driver/Receiver

RS-485, RS-422 Drivers

The differential drivers and receivers comply with the RS-485 and RS-422 standards. The driver circuits are able to drive a minimum of 1.5V when terminated with a 54Ω resistor across the two outputs. The typical propagation delay from driver input to output is 60ns. The driver outputs are current limited to less than 250mA, and can tolerate shorts to ground, or to any voltage within a 10V to -7V range with no damage.

RS-485, RS-422 Receivers

The differential receivers of the SP332 comply with the RS-485 and RS-422 standards. The input to the receiver is equipped with a common mode range of 12V to -7V. The input threshold over this range is a minimum of ±200mV. The differential receivers can receive data up to 10Mbps. The typical propagation delay from the receiver input to output is 90ns.

Single Ended Driver / Receiver

RS-232 (V.28) Drivers

The single-ended drivers and receivers comply with the RS-232 and V.28 standards. The drivers are inverting transmitters which accept either TTL or CMOS inputs and output the RS-232 signals with an inverted sense relative to the input logic levels. Typically, the RS-232 driver output voltage swing is ±9V with no load and is guaranteed to be greater than ±5V under full load. The drivers rely on the V+ and V- voltages generated by the on-chip charge pump to maintain proper RS-232 output levels. With worst case load conditions of 3kΩ and 2500pF, the four RS-232 drivers can still maintain ±5V output levels. The drivers can operate up to 120kbps; the propagation delay from input to output is typically 2µs.

RS-232 (V.28) Receivers

The RS-232 receivers convert RS-232 input signals to inverted TTL signals. Each of the four receivers features 500mV of hysteresis margin to minimize the affects of noisy transmission lines. The inputs also have a 5kΩ resistor to ground, in an open circuit situation the input of the receiver will be forced low, committing the output to a logic high state. The input resistance will maintain 3kΩ to 7kΩ over a ±15V range. The maximum operating voltage range for the receiver is ±30V, under these conditions the input current to the receiver must be limited to less than 100mA. Due to the on-chip ESD protection circuitry, the receiver inputs will be clamped to ±15V levels. The RS-232 receivers can operate up to 120kbps.

Charge–Pump

The charge pump is a MaxLinear–patented design (U.S. 5,306,954) and uses a unique approach compared to older less efficient designs. The charge pump still requires four external capacitors, but uses a four–phase voltage shifting technique to attain symmetrical 10V power supplies. Figure 7(a) shows the waveform found on the positive side of capacitor C_2, and Figure 7(b) shows the negative side of capacitor C_2. There is a free–running oscillator that controls the four phases of the voltage shifting. A description of each phase follows.

Phase 1 — V_{SS} charge storage

During this phase of the clock cycle, the positive side of capacitors C_1 and C_2 are initially charged to 5V. C_{I^+} is then switched to ground and charge on C_{1^-} is transferred to C_{2^-}. Since C_{2^+} is connected to 5V, the voltage potential across capacitor C_2 is now 10V.

Phase 2 — V_{SS} transfer

Phase two of the clock connects the negative terminal of C_2 to the V_{SS} storage capacitor and the positive terminal of C_2 to ground, and transfers the generated –10V to C_3. Simultaneously, the positive side of capacitor C_1 is switched to 5V and the negative side is connected to ground.

Phase 3 — V_{DD} charge storage

The third phase of the clock is identical to the first phase — the charge transferred in C_1 produces –5V in the negative terminal of C_1, which is applied to the negative side of capacitor C_2. Since C_{2^+} is at +5V, the voltage potential across C_2 is 10V.

Phase 4 — V_{DD} transfer

The fourth phase of the clock connects the negative terminal of C_2 to ground and transfers the generated 10V across C_2 to C_4, the V_{DD} storage capacitor. Again, simultaneously with this, the positive side of capacitor C_1 is switched to 5V and the negative

side is connected to ground, and the cycle begins again.

Since both V+ and V^- are separately generated from V_{CC} in a no–load condition, V+ and V^- will be symmetrical. Older charge pump approaches that generate V^- from V+ will show a decrease in the magnitude of V^- compared to V+ due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 15kHz. The external capacitors must be 0.1µF with a 16V breakdown rating.

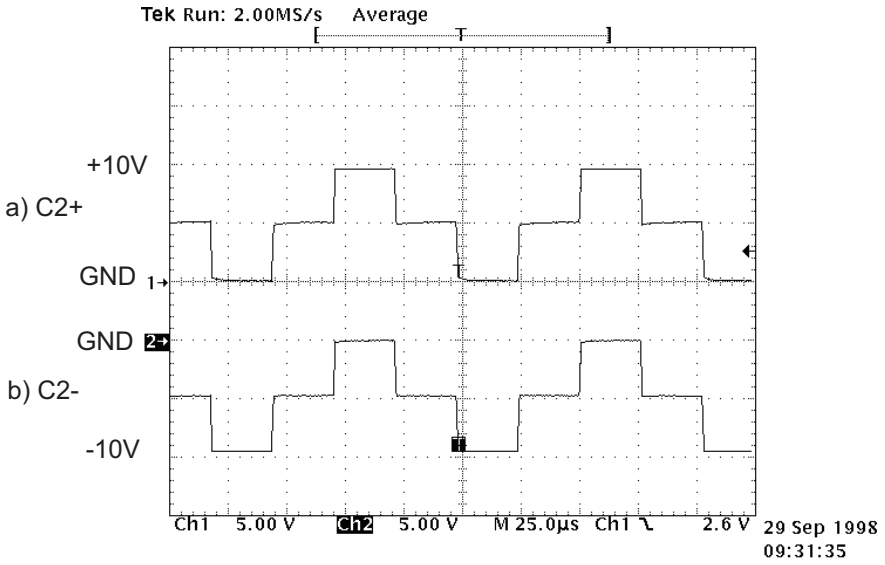


Figure 7: Charge Pump Waveforms

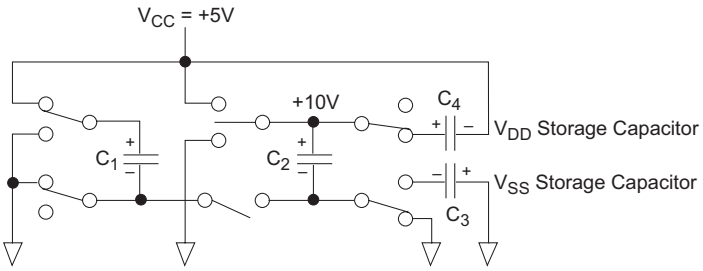


Figure 8: Charge Pump Phase 1

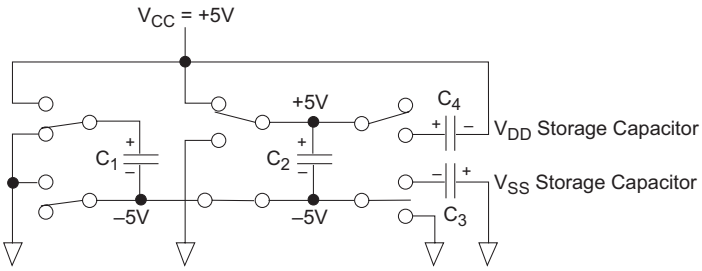


Figure 9: Charge Pump Phase 3

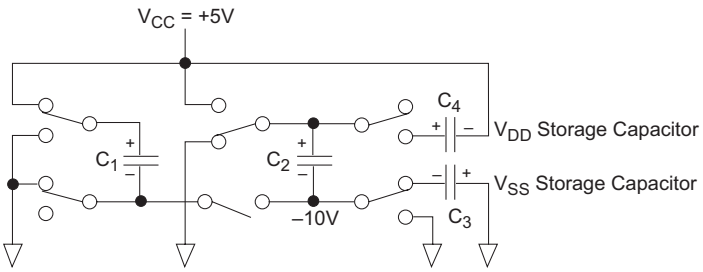


Figure 10: Charge Pump Phase 2

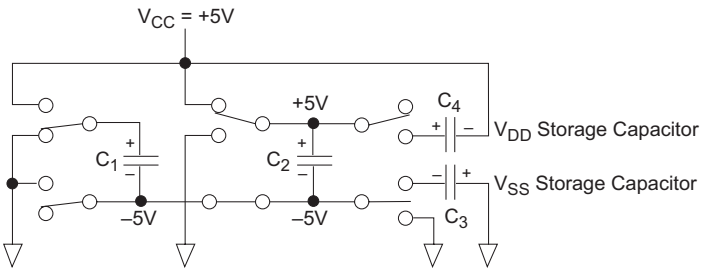
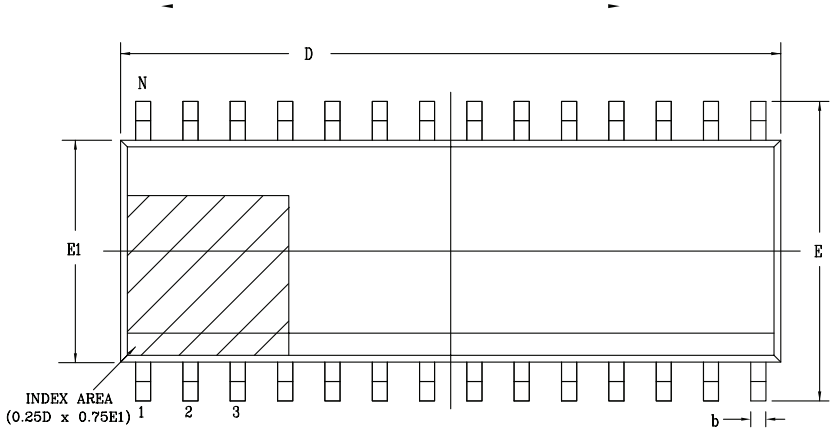


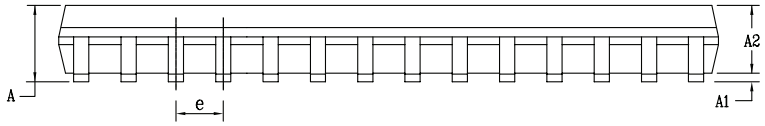
Figure 11: Charge Pump Phase 4

Package Description

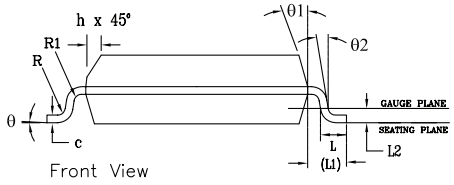
WSOIC28

Top View





Side View



Front View

PACKAGE OUTLINE SOIC .300" BODY JEDEC MS-013 VARIATION AE						
SYMBOLS	COMMON DIMENSIONS IN MM (Control Unit)			COMMON DIMENSIONS IN MM (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.35	—	2.65	0.093	—	0.104
A1	0.10	—	0.30	0.004	—	0.012
A2	2.05	—	2.55	0.081	—	0.100
b	0.31	—	0.51	0.012	—	0.020
c	0.20	—	0.33	0.008	—	0.013
E	10.30 BSC			0.406 BSC		
E1	7.50 BSC			0.295 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25	—	0.75	0.010	—	0.030
L	0.40	—	1.27	0.016	—	0.050
L1	1.40 REF			0.055 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	—	—	0.003	—	—
R1	0.07	—	—	0.003	—	—
θ	0°	—	8°	0°	—	8°
θ1	5°	—	15°	5°	—	15°
θ2	0°	—	—	0°	—	—
D	17.90 BSC			0.705 BSC		
N	28					

Drawing No: POD-00000106

Revision: A