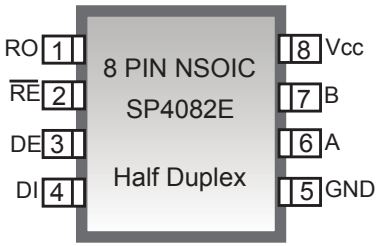
SP4082E

5V RS-485/RS-422 Transceivers
1/8th Unit Load, Slew-Rate Limited, ±15kV ESD-Protected

FEATURES

- 5.0V single supply operation
- Receiver failsafe on open or shorted lines
- 1/8th Unit Load, 256 transceivers on bus
- Robust ESD protection for RS-485 pins
  ±15kV Human Body Model
- Controlled driver slew rates
  115kbps, Low EMI
- Driver short circuit current limit and thermal shutdown for overload protection
- Industry standard package footprints



APPLICATIONS

- Motor Control
- Building Automation
- Security Systems
- Remote Meter Reading
- Long or un-terminated transmission lines

DESCRIPTION

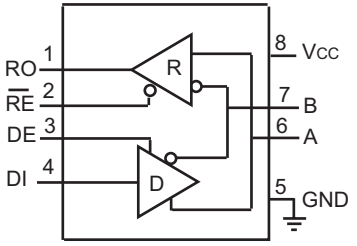
The SP4082E is designed for reliable, bidirectional communication on multipoint bus transmission lines. The device contains one differential driver and one differential receiver. It is a half-duplex device. The device complys with TIA/EIA-485 and TIA/EIA-422 standards. Lead-free and RoHS compliant packages are available.

This device is ruggedized for use in harsh operating conditions over the entire common-mode voltage range from -7V to +12V. Receivers are specially designed to fail-safe to a logic high output state if the inputs are un-driven or shorted. All RS-485 bus-pins are protected against severe ESD events up to ±15kV (Human Body Model). Drivers are protected from excess current flow caused by bus contention or output short-circuits by both an internal current limit and a thermal-overload shutdown. Devices are rated for industrial (-40 to +85ºC) operating temperatures. Receivers have exceptionally high input impedance, which places only 1/8th the standard load on a shared bus. Up to 256 transceivers may coexist while preserving full signal margin.

The device operates from a single 5.0V power supply and draws negligible quiescent power. The device has an independent enable and disable for the driver and receiver and will enter a low power shutdown mode if both driver and receiver are disabled. All outputs maintain high impedance during shutdown or when powered-off.

Pin Number	Pin Name	Pin Function
1	RO	Receiver Output. When $\overline{RE}$ is low and if (A – B) ≥ -40mV, RO is high. If (A – B) ≤ - 200mV, RO is low.
2	$\overline{RE}$	Receiver Output Enable. When $\overline{RE}$ is low, RO is enabled. When $\overline{RE}$ is high, RO is high impedance. Drive $\overline{RE}$ high and DE low to enter shutdown mode.
3	DE	Driver Output Enable. When DE is high, outputs are enabled. When DE is low, outputs are high impedance. Drive DE low and $\overline{RE}$ high to enter shutdown mode.
4	DI	Driver Input. With DE high, a low level on DI forces non-inverting output low and inverting output high. A high level on DI forces non-inverting output high and inverting output low.
5	GND	Ground
6	A	Non-inverting Receiver Input and Non-inverting Driver Output
7	B	Inverting Receiver Input and Inverting Driver Output
8	Vcc	Positive Supply V_{CC}. Bypass to GND with a 0.1uF capacitor.

DEVICE ARCHITECTURE AND BLOCK DIAGRAM



8-Pin Half Duplex

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Supply Voltage (V_{CC}).....+ 7.0V
Input voltage at control input pins ($\overline{RE}$, DE) ..... -0.3V to Vcc+0.3V
Driver input voltage (DI) .....-0.3V to Vcc+0.3V
Driver output voltage (A, B, Y, and Z) .....+/-13V
Receiver output voltage (RO) .....-0.3V to (Vcc + 0.3V)
Receiver input voltage (A, B) .....+/-13V
Package Power Dissipation:
Maximum Junction Temperature 150°C
8-Pin SO $\varnothing_{JA}$ = 128.4°C/W
Storage Temperature.....-65°C to +150°C
Lead Temperature (soldering, 10s)..... +300°C

RECOMMENDED OPERATING CONDITIONS

Vcc=5V ±5%, T_{MIN} to T_{MAX}, unless otherwise noted, Typical values are Vcc=5V and T_A=25°C

Recommended Operating Conditions		Min.	Nom.	Max.	Unit
Supply Voltage, Vcc		4.5	5	5.5	V
Input Voltage on A and B pins		-7		12	V
High-level input voltage (DI, DE or $\overline{RE}$), V_{IH}		2		Vcc	V
Low-level input voltage (DI, DE or $\overline{RE}$), V_{IH}		0		0.8	V
Output Current	Driver	-60		60	mA
	Receiver	-8		8	
Operating Free Air Temperature, T_A	Industrial Grade (E)	-40		85	°C

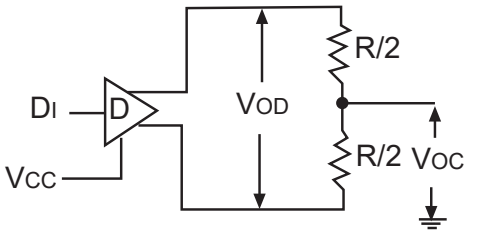
Note: The least positive (most negative) limit is designated as the maxium value.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Digital Input Signals: DI, DE, $\overline{RE}$							
Logic input thresholds		High, V_{IH}		2.0			V
		Low, V_{IL}				0.8	
Logic Input Current		T_A = 25°C, after first transition				±1	µA
Input Hysteresis		T_A = 25°C			100		mV
Driver							
Differential Driver Output (V_{OD})		No Load				Vcc	V
Differential Driver Output, Test 1		R_L=100Ω (RS-422)		2		Vcc	V
		R_L=54Ω (RS-485)		1.5	2.7	Vcc	
Differential Driver Output, Test 2		V_{CM} = -7 to +12V		1.5		Vcc	
Change in Magnitude of Differential Output Voltage (ΔV_{OD}) (Note 1)		R_L=54 or 100Ω				±0.2	V
Driver Common Mode Output Voltage (Voc)		R_L=54 or 100Ω		1		3	V
Change in Common Mode Output Voltage (ΔVoc)		R_L=54 or 100Ω				±0.2	V
Driver Short Circuit Current Limit		-7V ≤ V_{OUT} ≤ +12V				±250	mA
Output Leakage Current		DE=0, $\overline{RE}$=0, Vcc=0 or 5.5V	V_{OUT}=12V			125	µA
			V_{OUT}= -7V	-100			
Receiver							
Receiver Input Resistance		-7V ≤ V_{CM} ≤ 12V		96			KΩ
Input Current (A, B pins)		DE=0, $\overline{RE}$=0, Vcc=0 or 5.5V	V_{IN}= 12V			125	µA
			V_{IN}= -7V	-100			
Receiver Differential Threshold (VA-VB)		-7V ≤ V_{CM} ≤ 12V		-200	-125	-40	mV
Receiver Input Hysteresis					25		mV
Receiver Output Voltage	V_{OH}	I_{OUT} = -8mA, V_{ID} = -40mV		Vcc-1.5			V
	V_{OL}	I_{OUT} = 8mA, V_{ID} = -200mV				0.4	
High-Z Receiver Output Current		Vcc =5.5V, 0 ≤ V_{OUT} ≤ Vcc				± 1	µA
Receiver Output Short Circuit Current		0V ≤ V_{RO} ≤ Vcc				± 95	mA
Supply and Protection							
Supply Current	IQ, Active Mode	No load, DI=0 or Vcc			400	900	µA
	Shutdown Mode, Note 2	DE=0, $\overline{RE}$=Vcc, DI=Vcc				1	µA
Thermal Shutdown Temperature		Junction temperature			165		°C
Thermal Shutdown Hysteresis					15		

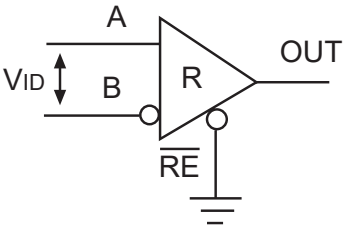
Notes:
1. Change in Magnitude of Differential Output Voltage and Change in Magnitude of Common Mode Output Voltage are the changes in output voltage when DI input changes state.
2. The transceivers are put into shutdown by bringing $\overline{RE}$ high and DE low. If the inputs are in this state for less than 50ns the device does not enter shutdown. If the enable inputs are held in this state for at least 600ns the device is assured to be in shutdown. In this low power mode most circuitry is disabled and supply current is typically 1nA.
3.Characterized, not 100% tested.

Unless otherwise noted Vcc= +5.0±0.5V, ambient temperature TA from -40 to +85ºC

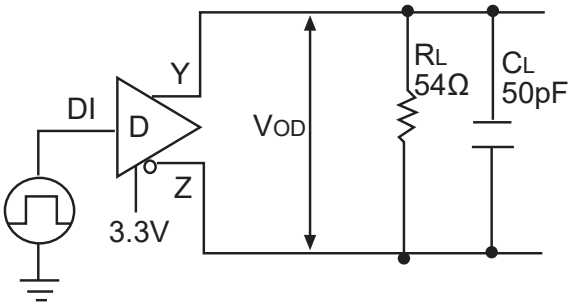
DRIVER CHARACTERISTICS:	Conditions	Min.	Typ.	Max.	Unit
Data Signaling Rate (1 / t_{UI})	Duty Cycle 40 to 60%	115			Kbps
Driver Propagation Delay (t_{PHL}, t_{PLH})	R_L = 54Ω, C_L = 50pF,			3500	ns
Driver Output Rise/Fall Time (t_R, t_F)		667	1200	2500	ns
Driver Differential Skew (t_{PLH} – t_{PHL})				±500	ns
Driver Enable to Output High (t_{DZH})				3500	ns
Driver Enable to Output Low (t_{DZL})				3500	ns
Driver Disable from Output High (t_{DHZ})				100	ns
Driver Disable from Output Low (t_{DLZ})				100	ns
Shutdown to Driver Output Valid (t_{DZV})				6000	ns
RECEIVER CHARACTERISTICS:	Conditions	Min.	Typ.	Max	Unit
Receiver Propagation Delay	C_L = 15pF, V_{ID} = ±2V			250	ns
Prop. Delay Skew (t_{PLH} – t_{PHL})				±50	ns
Receiver Output Rise / Fall Time (t_R, t_F)	C_L = 15pF			50	ns
Receiver Enable to Output High (t_{ZH})				100	ns
Receiver Enable to Output Low (t_{ZL})				100	ns
Receiver Disable from Output High (t_{HZ})				100	ns
Receiver Disable from Output Low (t_{LZ})				100	ns
Shutdown to Receiver Output Valid (t_{ROV})				3500	ns
Time to Shutdown (Note 2,3)		50		600	ns



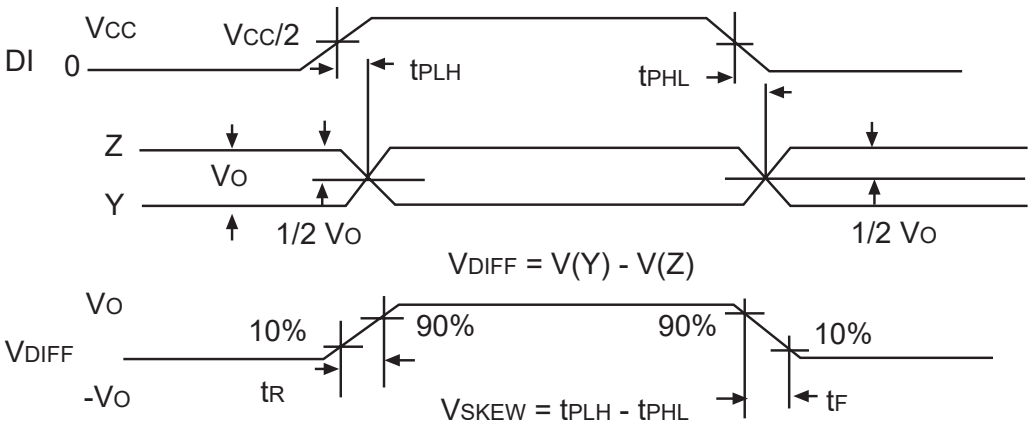
Driver DC Test Circuit



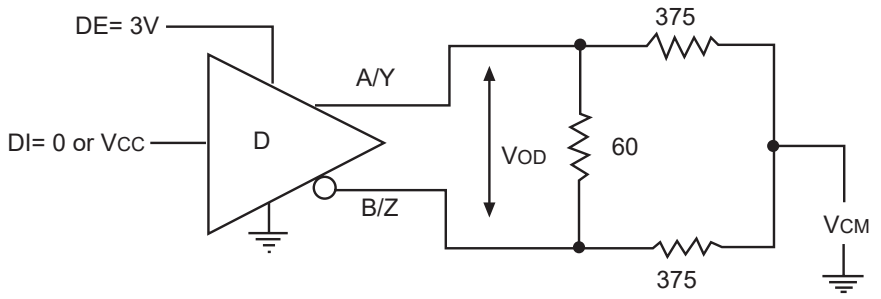
Receiver DC Test Circuit



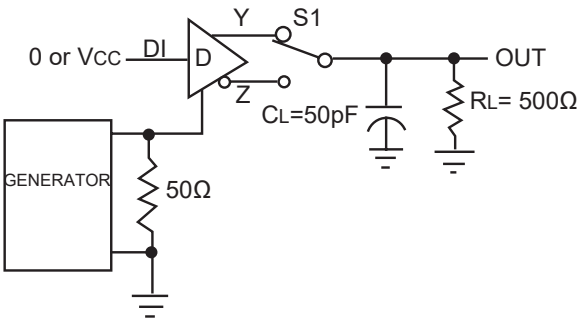
Driver Propagation Delay Time Test Circuit and Timing Diagram

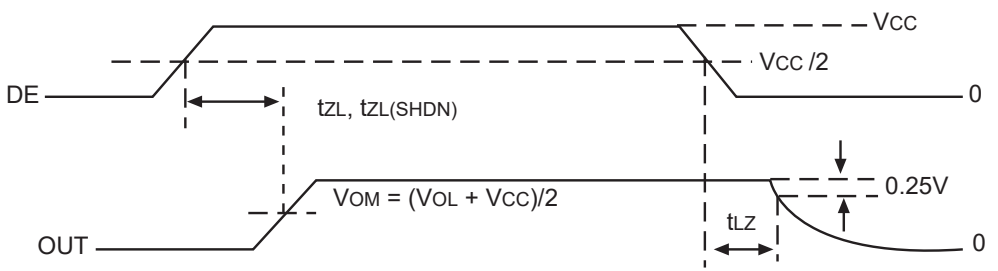


Driver Differential Output Test Circuit

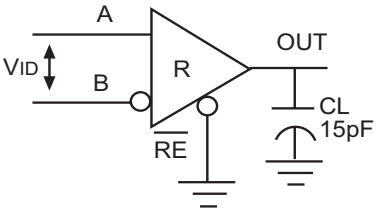


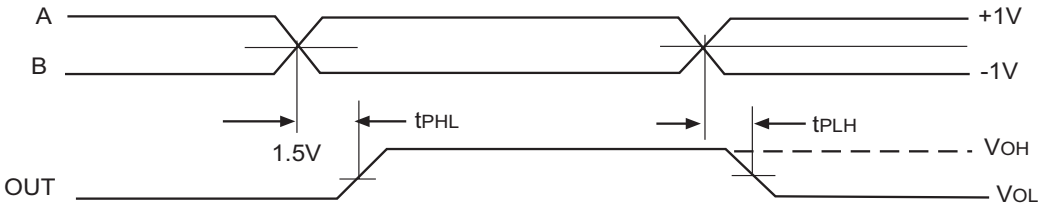
Driver Enable and Disable Times Test Circuit and Timing Diagram



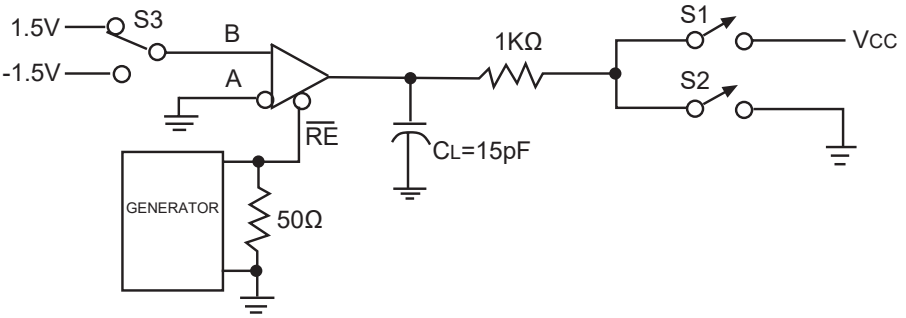


Receiver Propagation Delay Test Circuit and Timing Diagram

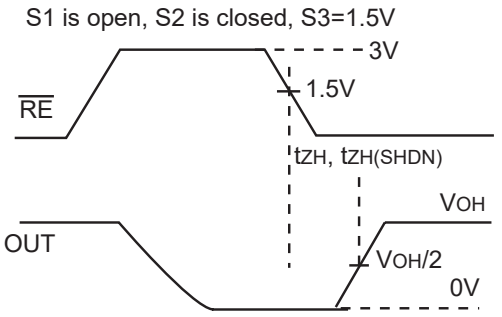


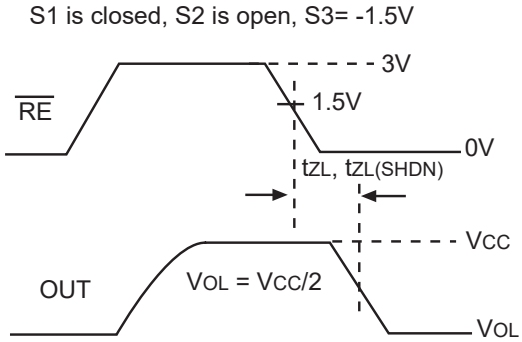


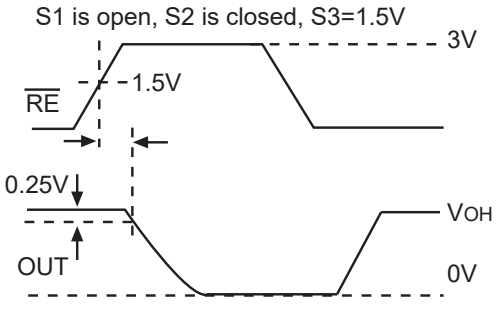
Receiver Enable and Disable Times Test Circuit

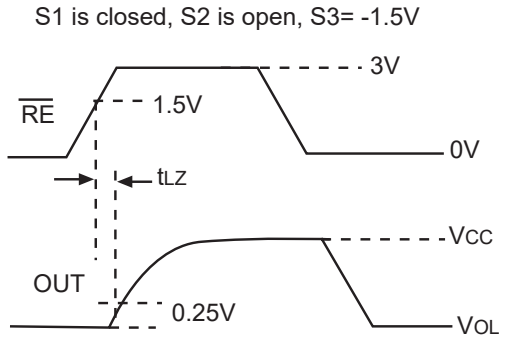


Receiver Enable and DisableTiming Diagram









Transmitting				
Inputs			Outputs	
$\overline{RE}$	DE	DI	A	B
X	1	1	1	0
X	1	0	0	1
0	0	X	High-Z	
1	0	X	Shutdown	

Receiving			
Inputs			Output
$\overline{RE}$	DE	$V_A - V_B$	RO
0	X	≥ -40mV	1
0	X	≤-200mV	0
0	X	Open/shorted	1
1	1	X	High-Z
1	0	X	Shutdown

Note: Receiver inputs -200mV < VA - VB < -40mV, should be considered indeterminate

DETAILED DESCRIPTION

The SP4082E is a 5V half-duplex RS-485 transceiver.

The SP4082E contains one driver and one receiver. These devices feature fail-safe circuitry that will guarantee a logic-high receiver output when the receiver inputs are open or shorted.

The SP4082E features reduced slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free data transmission up to 115kbps.

It operates from a single 5.0V supply. Drivers are output short-circuit current limited. Thermal-shutdown circuitry protects drivers against excessive power dissipation. When activated, the thermal-shutdown circuitry places the driver outputs into a high-impedance state.

Receiver FAILSAFE

Ordinary RS-485 differential receivers will be in an indeterminate state whenever A - B is less than ±200mV. This situation can occur whenever the data bus is not being actively driven. The Failsafe feature guarantees a logic-high receiver output if the receiver's differential inputs are shorted or open-circuit.

The receiver thresholds of the SP4082E are very precise and offset by at least a 40mV noise margin from ground. This results in a logic-high receiver output at zero volts input differential while maintaining compliance with the EIA/TIA-485 standard of ±200mV.

±15KV ESD PROTECTION

ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver output and receiver inputs have extra protection against static electricity. Sipex uses state of the art structures to protect these pins against ESD of ±15kV without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown, and powered down. After an ESD event, the SP4082E keeps working without latch-up or damage.

ESD protection can be tested in various ways. The transmitter outputs and receiver inputs of the SP4082E is characterized for protection to the following limits:

±15kV using the Human Body Model

ESD TEST CONDITIONS

ESD performance depends on a variety of conditions. Contact Sipex for a reliability report that documents test setup, methodology and results.

MACHINE MODEL

The machine model for ESD tests all pins using a 200pF storage capacitor and zero discharge resistance. The objective is to emulate the stress caused when I/O pins are contacted by handling equipment during test and assembly.

256 TRANSCEIVERS ON THE BUS

The standard RS-485 receiver input impedance is 12kΩ (1 unit load). A standard driver can drive up to 32 unit loads. The SP4032E has only a 1/8th unit load receiver input impedance (96kΩ), thereby allowing eight times as many, up to 256, transceivers to be connected in parallel on a communication line. Any combination of these devices and other RS-485 transceivers up to a total of 32 unit loads may be connected to the line.

LOW POWER SHUTDOWN MODE

Low-power shutdown mode is initiated by bringing both $\overline{RE}$ high and DE low simultaneously. While in shutdown devices typically draw only 50nA of supply current. DE and $\overline{RE}$ may be tied together and driven by a single control signal. Devices are guaranteed not to enter shutdown if $\overline{RE}$ is high and DE is low for less than 50ns. If the inputs are in this state for at least 600ns, the parts are shutdown.

Enable times t_{ZH} and t_{ZL} apply when the part is not in low-power shutdown state. Enable times $t_{ZH}(\overline{SHDN})$ and $t_{ZL}(\overline{SHDN})$ apply when the parts are shut down. The drivers and receivers take longer to become enabled from low power shutdown mode $t_{ZL}(\overline{SHDN})$ and $t_{ZL}(\overline{SHDN})$ than from driver/receiver-disable mode (t_{ZH}, t_{ZL}).

DRIVER OUTPUT PROTECTION

Two mechanisms prevent excessive output current and power dissipation caused by faults or by bus contention. First, a driver current limit on the output stage provides immediate protec-

tion against short circuits over the whole common-mode voltage range. Second, a thermal-shutdown circuit forces the driver outputs into a high-impedance state if junction temperature becomes excessive.

LINE LENGTH, EMI, AND REFLECTIONS

It features controlled slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables.

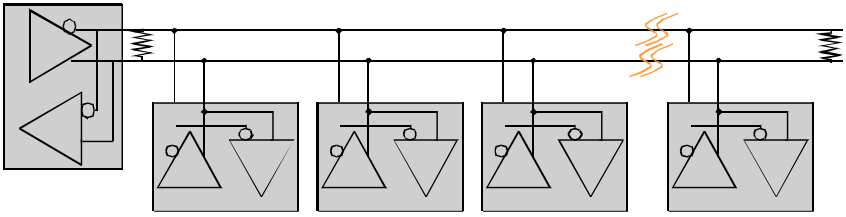
Driver rise and fall times are limited to no faster than 667ns, allowing error-free data transmission up to 115kbps.

The RS-485/RS-422 standard covers line lengths up to 4,000ft. Maximum achievable line length is a function of signal attenuation and noise. Use of slew-controlled drivers may help to reduce crosstalk interference and permit communication over longer transmission lines.

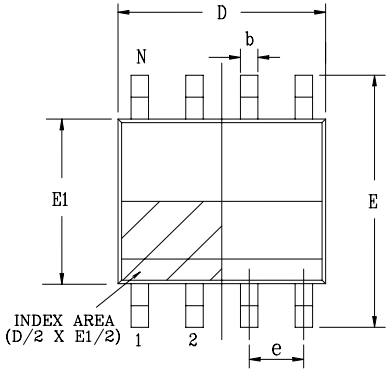
Termination prevents reflections by eliminating the impedance mismatches on a transmission line. Line termination is typically used if rise and fall times are shorter than the round-trip signal propagation time. Slew-limited drivers may reduce or eliminate the need for cable termination in many applications.

TYPICAL APPLICATIONS:

Half-Duplex Network

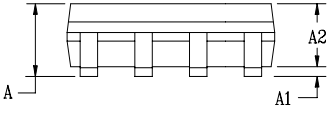


REVISION HISTORY			
REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	08/16/05	JL
B	DRAWING FORMAT MODIFICATION	07/19/06	JL
C	CHANGE DRAWING LOGO	11/16/07	JL

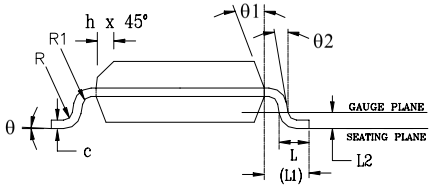


Top View

8 Pin SOICN JEDEC MS-012 Variation AA						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	—	1.75	0.053	—	0.069
A1	0.10	—	0.25	0.004	—	0.010
A2	1.25	—	1.65	0.049	—	0.065
b	0.31	—	0.51	0.012	—	0.020
c	0.17	—	0.25	0.007	—	0.010
E	6.00 BSC			0.236 BSC		
E1	3.90 BSC			0.154 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25	—	0.50	0.010	—	0.020
L	0.40	—	1.27	0.016	—	0.050
L1	1.04 REF			0.041 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	—	—	0.003	—	—
R1	0.07	—	—	0.003	—	—
θ	0°	—	8°	0°	—	8°
θ1	5°	—	15°	5°	—	15°
θ2	0°	—	—	0°	—	—
D	4.90 BSC			0.193 BSC		
N	8			8		



Side View



Front View

EXAR Powering Connectivity	EXAR CORPORATION		
	8 PIN SOICN PACKAGE OUTLINE		
Packaging Approval:		Drawing No: 8-PIN SOICN	
By: JL	Date: 11/16/07	Revision: C	Sheet: 1 OF 1