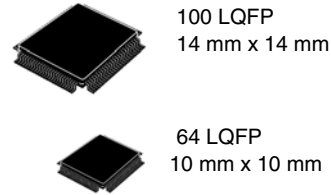


## MPC5604E



## MPC5604E Microcontroller Data Sheet

- Single issue, 32-bit CPU core complex (e200z0h)
  - Compliant with Power Architecture<sup>®</sup> embedded category
  - Variable Length Encoding (VLE) only
- Memory
  - 512 KB on-chip Code Flash with ECC and erase/program controller
  - additional 64 (4 × 16) KB on-chip Data Flash with ECC for EEPROM emulation
  - 96 KB on-chip SRAM with ECC
- Fail-safe protection
  - Programmable watchdog timer
  - Non-maskable interrupt
  - Fault collection unit
- Nexus 2+ interface
- Interrupts and events
  - 16-channel eDMA controller
  - 16 priority level controller
  - Up to 32 external interrupts for 100-pin LQFP<sup>1</sup>
  - Upto 22 external interrupts for 64-pin LQFP
  - PIT implements four 32-bit timers
  - 120 interrupts are routed via INTC
- General purpose I/Os
  - Individually programmable as input, output or special function
  - 39 on LQFP64
  - 71 on LQFP100<sup>1</sup>
- 1 general purpose eTimer unit
  - 6 timers each with up/down capabilities
  - 16-bit resolution, cascadeable counters
- Quadrature decode with rotation direction flag
- Double buffer input capture and output compare
- Communications interfaces
  - 2 LINFlex channels (1 × Master/Slave, 1 × Master Only)
  - 3 DSPI controllers with automatic chip select generation (up to 2/2/4 chip selects)
  - 1 FlexCAN interface (2.0B Active) with 32 message buffers
- One 10-bit analog-to-digital converter (ADC)
  - 7 input channels
    - 4 channels routed to the pins
    - 3 internal connections: 1x temperature sensor, 1x core voltage, 1x IO voltage
  - Conversion time < 1 μs including sampling time at full precision
  - 4 analog watchdogs with interrupt capability
- On-chip CAN/UART bootstrap loader with Boot Assist Module (BAM)
- On-chip TSENS
- 100 MBit Fast Ethernet Controller (FEC)
  - Supports precision timestamps
  - MII on 100-pin LQFP package<sup>1</sup>
  - MII-lite on 64-pin LQFP package
- JPEG/MJPEG 8/12bit Encoder
- 6 x stereo channels audio interface
- 2x I<sup>2</sup>C controller module
- CRC module

<sup>1</sup>.The 100-pin package is not a production package. It is used for software development only.

# Table of Contents

|       |  |    |         |  |    |
|-------|--|----|---------|--|----|
| 1     | Overview   | 3  | 3.14    | Analog-to-Digital Converter (ADC) electrical characteristics | 37 |
| 1.1   | Device summary   | 3  | 3.14.1  | Input impedance and ADC accuracy                             | 37 |
| 1.2   | Block diagram  | 4  | 3.14.2  | ADC conversion characteristics                               | 41 |
| 2     | Package pinouts and signal descriptions                          | 6  | 3.15    | Temperature sensor electrical characteristics                | 42 |
| 2.1   | Package pinouts  | 6  | 3.16    | Flash memory electrical characteristics                      | 42 |
| 2.2   | Signal descriptions  | 8  | 3.17    | NMI filter functional specification                          | 44 |
| 2.2.1 | Power supply and reference voltage pins                          | 8  | 3.18    | AC specifications  | 44 |
| 2.2.2 | System pins  | 9  | 3.18.1  | Pad AC specifications  | 44 |
| 2.2.3 | Pin muxing   | 10 | 3.19    | AC timing characteristics                                    | 47 |
| 3     | Electrical characteristics                                       | 21 | 3.19.1  | Generic timing diagrams                                      | 47 |
| 3.1   | Introduction   | 21 | 3.19.2  | $\overline{\text{RESET}}$ pin characteristics                | 49 |
| 3.2   | Parameter classification   | 21 | 3.19.3  | Nexus and JTAG timing  | 50 |
| 3.3   | Absolute maximum ratings   | 22 | 3.19.4  | GPIO timing  | 52 |
| 3.4   | Recommended operating conditions                                 | 23 | 3.19.5  | External interrupt timing (IRQ pin)                          | 53 |
| 3.5   | Thermal characteristics  | 24 | 3.19.6  | FlexCAN timing   | 53 |
| 3.5.1 | General notes for specifications at maximum junction temperature | 25 | 3.19.7  | LINFlex timing   | 53 |
| 3.6   | Electromagnetic Interference (EMI) characteristics               | 26 | 3.19.8  | DSPI timing  | 54 |
| 3.7   | Electrostatic Discharge (ESD) characteristics                    | 27 | 3.19.9  | Video interface timing                                       | 59 |
| 3.8   | Power management electrical characteristics                      | 27 | 3.19.10 | Fast ethernet interface                                      | 60 |
| 3.8.1 | Power Management Overview  | 27 | 3.19.11 | $^{\circ}\text{C}$ timing                                    | 62 |
| 3.8.2 | Voltage regulator electrical characteristics                     | 30 | 3.19.12 | SAI timing   | 63 |
| 3.8.3 | Voltage monitor electrical characteristics                       | 31 | 4       | Package mechanical data                                      | 66 |
| 3.9   | Power Up/Down reset sequencing                                   | 31 | 4.1     | 100 LQFP mechanical outline drawing                          | 66 |
| 3.10  | DC electrical characteristics                                    | 33 | 4.2     | 64 LQFP mechanical outline drawing                           | 70 |
| 3.11  | Main oscillator electrical characteristics                       | 34 | 5       | Ordering information   | 73 |
| 3.12  | FMPLL electrical characteristics                                 | 35 | 6       | Document revision history                                    | 74 |
| 3.13  | 16 MHz RC oscillator electrical characteristics                  | 36 |         |  |    |

# 1 Overview

This document provides electrical specifications, pin assignments, and package diagrams for the MPC5604E series of microcontroller units (MCUs).

MPC5604E microcontrollers are members of a new family of next generation microcontrollers built on the Power Architecture. This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the devices.

The MPC5604E microcontroller is a gateway system designed to move data from different sources via Ethernet to a receiving system and vice versa. The supported data sources and sinks are:

- Video data (with 8/10/12 bits per data word)
- Audio data (6× stereo channels)
- RADAR data (2 × 12 bit with <1μs per sample, digitized externally and read in via SPI)
- Other serial communication interfaces including CAN, LIN, and SPI

The Ethernet module has a bandwidth of 10/100 Mbits/sec and supports precision time stamps (IEEE1588). Unshielded twisted pair cables are used to transfer data (via Ethernet) in the car, resulting in a significant reduction of wiring costs by providing inexpensive high bandwidth data links.

## 1.1 Device summary

The following table summarizes the MPC5604E device.

### NOTE

The 100-pin package is not a production package. It is used for software development only.

**Table 1. Device summary**

| Feature            | MPC5604E   |                    |
|--------------------|--|--------------------|
|                    | 100-pin LQFP <sup>1</sup>  | 64-pin LQFP        |
| CPU                | e200z0h, 64 MHz, VLE only, no SPE  |                    |
| Flash with ECC     | CFlash: 512 KB (LC) DFlash: 64 KB (LC, area optimized)                     |                    |
| RAM with ECC       | 96 KB  |                    |
| DMA                | 16 channels  |                    |
| PIT                | yes  |                    |
| SWT                | yes  |                    |
| FCU                | yes  |                    |
| Ethernet           | 100 Mbits MII  | 100 Mbits MII-Lite |
| Video Encoder      | 8bpp/12bpp   |                    |
| Audio Interface    | 6x Stereo (4x synchronous + 2x synchronous/asynchronous)                   |                    |
| ADC (10-bit)       | 1× 4 channels + V <sub>DD_IO</sub> + V <sub>DDCore</sub> + TSens           |                    |
| Timer I/O (eTimer) | 1×6 channels   |                    |
| SCI (LINFlex)      | 2×   |                    |
| SPI (DSPI)         | DSPI_0: 2 chip selects<br>DSPI_1: 2 chip selects<br>DSPI_2: 4 chip selects |                    |

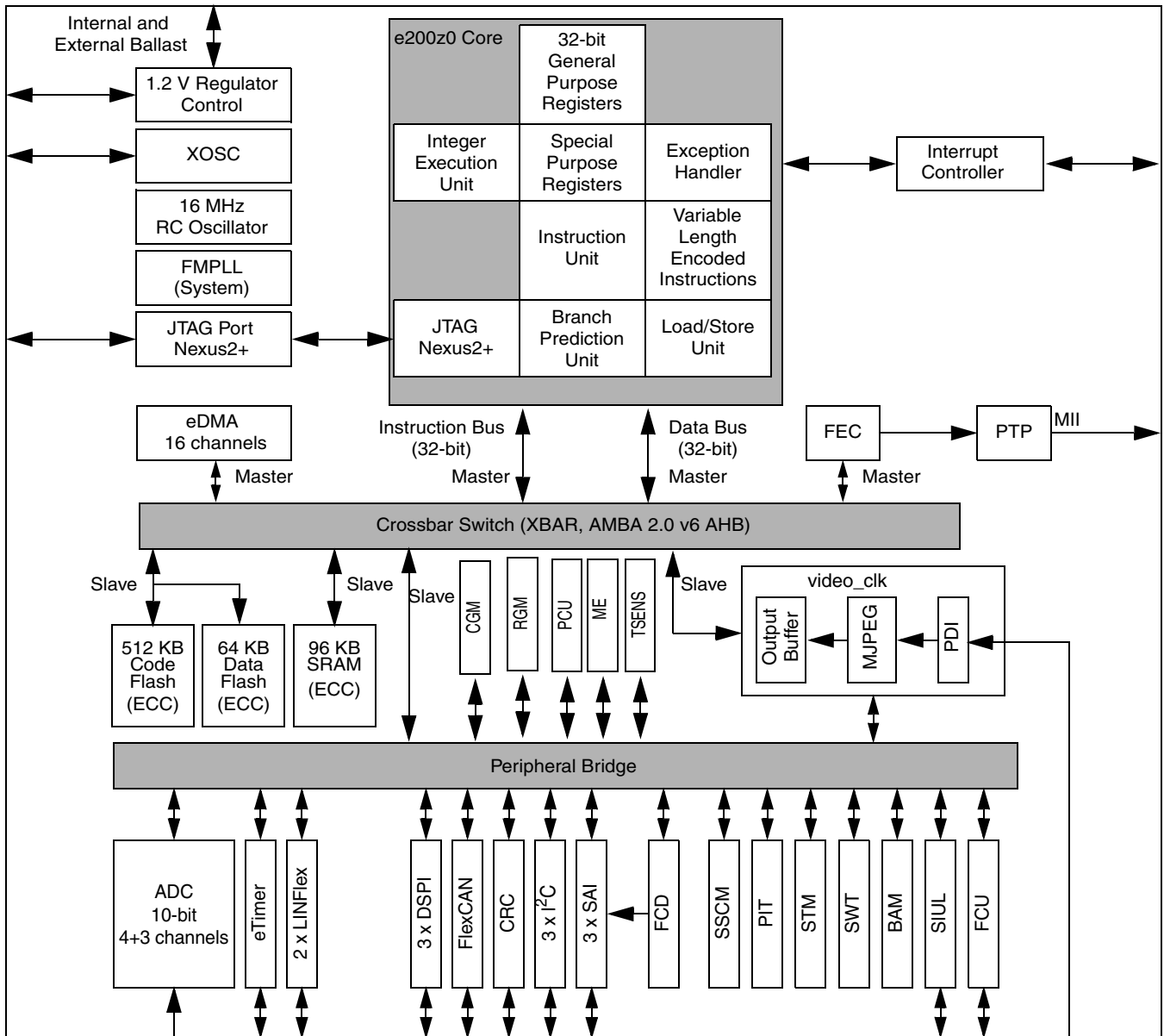
Table 1. Device summary (continued)

| Feature                     | MPC5604E  |             |
|-----------------------------|---|-------------|
|                             | 100-pin LQFP <sup>1</sup>   | 64-pin LQFP |
| CAN (FlexCAN)               | 1×  |             |
| IIC                         | 2×  |             |
| Supply                      | 3.3 V IO<br>1.2V Core with dedicated ballast source pin in two modes: <ul style="list-style-type: none"> <li>• internal ballast or</li> <li>• external supply (using power on reset pin)</li> </ul> |             |
| Phase Lock Loop (PLL)       | 1× FMPLL  |             |
| Internal RC Oscillator      | 16 MHz  |             |
| External crystal Oscillator | 4 MHz - 40 MHz  |             |
| CRC                         | yes   |             |
| Debug                       | JTAG, Nexus2+   | JTAG        |
| Ambient Temperature         | -40 to 125 °C   |             |

<sup>1</sup> The 100-pin package is not a production package. It is used for software development only.

## 1.2 Block diagram

Figure 1 shows a top-level block diagram of the MPC5604E MCU.



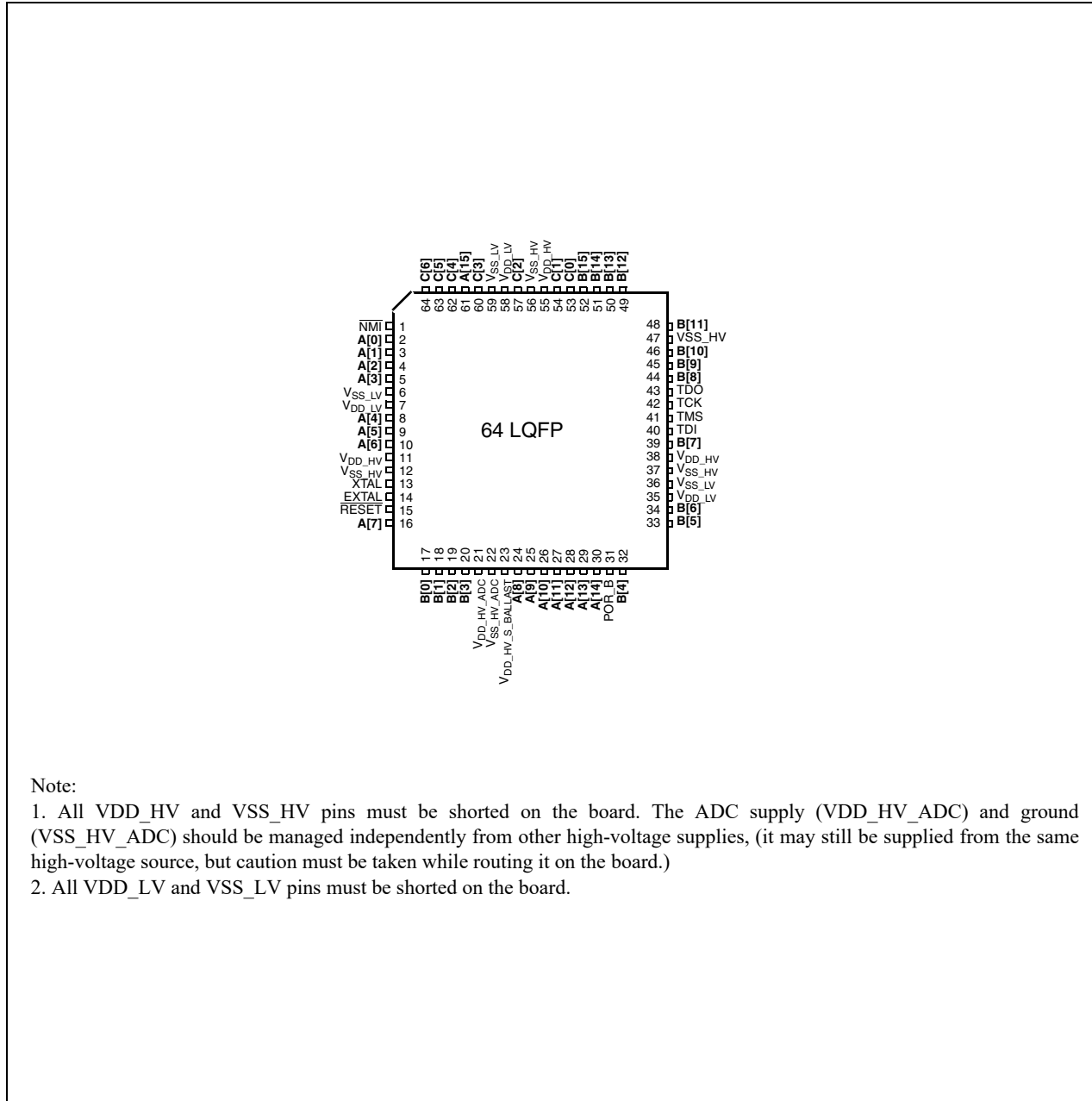
- |         |  |        |  |
|---------|--|--------|--|
| ADC     | Analog-to-Digital Converter                  | CGM    | Clock Generation Module                |
| BAM     | Boot Assist Module                           | PCU    | Power Control Unit                     |
| CRC     | Cyclic Redundancy Check                      | RGM    | Reset Generation Module                |
| DSPi    | Deserial Serial Peripheral Interface         | TSSENS | Temperature sensor                     |
| eDMA    | Enhanced Direct Memory Access                | MJPEG  | 12-bit Motion JPEG Encoder             |
| eTimer  | Enhanced Timer                               | PDI    | Parallel Data Interface (image sensor) |
| FCD     | Fractional Clock Divider                     | PIT    | Periodic Interrupt Timer               |
| FCU     | Fault Collection Unit                        | PTP    | IEEE 1588 Precision Time Stamps        |
| FEC     | Fast Ethernet Controller                     | SIUL   | System Integration Unit                |
| FlexCAN | Flexible Controller Area Network             | SRAM   | Static Random-Access Memory            |
| FMPLL   | Frequency-Modulated Phase-Locked Loop        | SSCM   | System Status and Configuration Module |
| I2C     | Inter-Integrated Circuit serial interface    | STM    | System Timer Module                    |
| SAI     | Serial Audio Interface 6xStereo              | SWT    | Software Watchdog Timer                |
| LINFlex | Serial Communication Interface (LIN support) |        |  |
| ME      | Mode Entry Module                            |        |  |

Figure 1. MPC5604E block diagram

## 2 Package pinouts and signal descriptions

### 2.1 Package pinouts

The LQFP pinouts are shown in the following figures.



Note:

1. All VDD\_HV and VSS\_HV pins must be shorted on the board. The ADC supply (VDD\_HV\_ADC) and ground (VSS\_HV\_ADC) should be managed independently from other high-voltage supplies, (it may still be supplied from the same high-voltage source, but caution must be taken while routing it on the board.)
2. All VDD\_LV and VSS\_LV pins must be shorted on the board.

Figure 2. 64-pin LQFP pinout (top view)

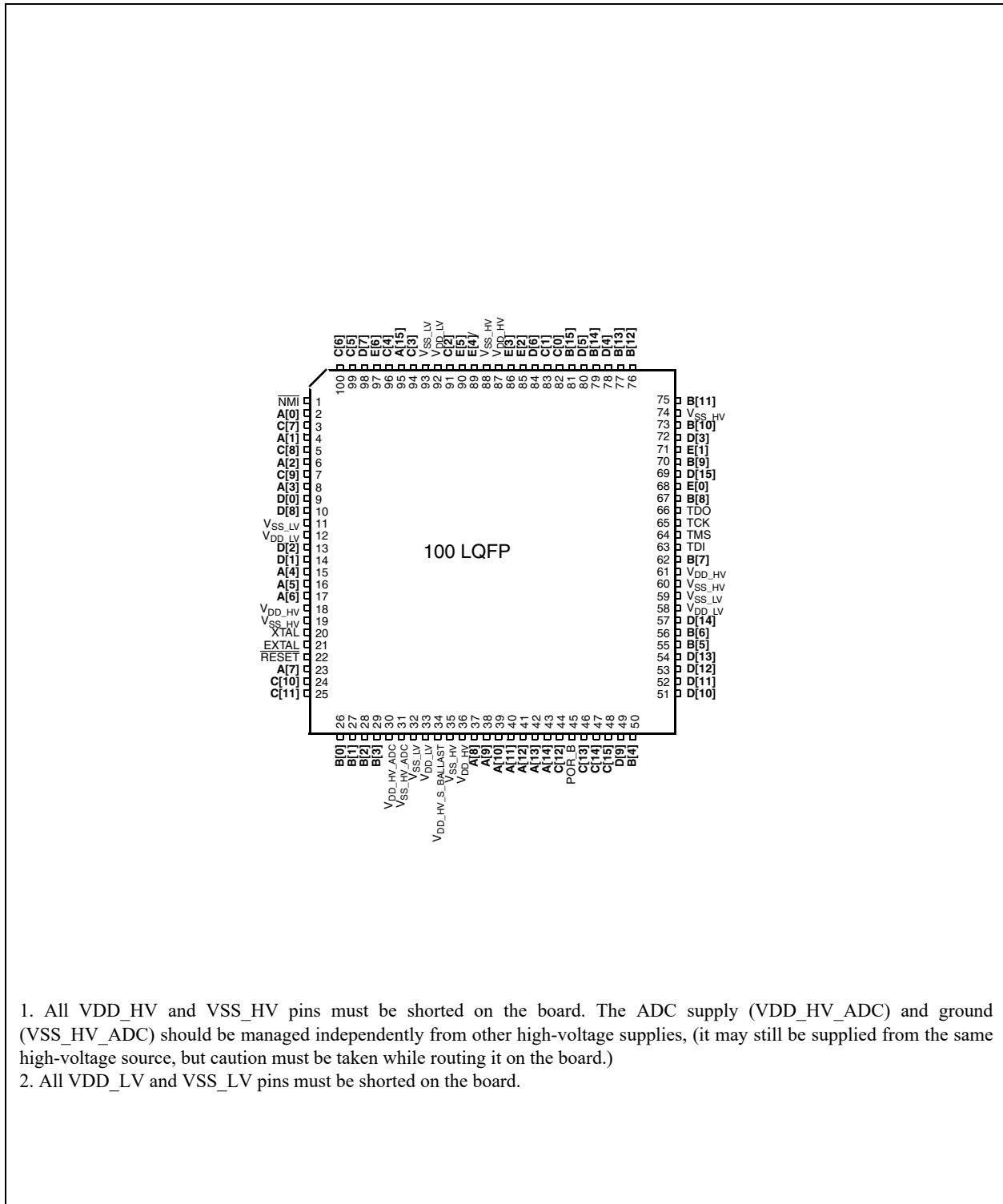


Figure 3. 100-pin LQFP pinout (top view)<sup>1</sup>

1. The 100-pin package is not a production package. It is used for software development only.

## 2.2 Signal descriptions

The following sections provide signal descriptions and related information about the functionality and configuration of the MPC5604E devices.

### 2.2.1 Power supply and reference voltage pins

Table 2 lists the power supply and reference voltage for the MPC5604E devices.

**Table 2. Supply pins**

| Supply  |                                    |  | Pin    |                      |
|---|------------------------------------|--|--------|----------------------|
| Port Pin  | Multi-bonded Power Supplies/Ground | Description  | 64-pin | 100-pin <sup>1</sup> |
| VREG control and power supply pins. Pins available on 64-pin and 100-pin package. |                                    |  |        |                      |
| V <sub>DD_HV_S_BALLAST</sub>  | V <sub>DD_HV_S_BALLAST0</sub>      | Ballast Source/Supply Voltage  | 23     | 34                   |
|   | V <sub>DD_HV_S_BALLAST1</sub>      | Ballast Source/Supply Voltage  |        |                      |
| ADC0 reference and supply voltage. Pins available on 64-pin and 100-pin package.  |                                    |  |        |                      |
| V <sub>DD_HV_ADC</sub>  | V <sub>DD_HV_ADC0</sub>            | ADC0 supply voltage with respect to ground (V <sub>SS_HV_ADC</sub> )         | 21     | 30                   |
|   | V <sub>DD_HV_ADC0</sub>            | ADC0 high reference voltage with respect to ground (V <sub>SS_HV_ADC</sub> ) |        |                      |
| V <sub>SS_HV_ADC</sub>  | V <sub>SS_HV_ADC0</sub>            | ADC0 ground voltage with respect to ground                                   | 22     | 31                   |
|   | V <sub>SS_HV_ADC0</sub>            | ADC0 low reference voltage with respect to ground                            |        |                      |
| Power supply pins (3.3 V). Pins available on 64-pin and 100-pin package.          |                                    |  |        |                      |
| V <sub>DD_HV</sub>  | V <sub>DD_HV_IO0_0</sub>           | Input/output ground voltage  | 11     | 18                   |
|   | V <sub>DD_HV_OSC0</sub>            | Crystal oscillator amplifier supply voltage                                  |        |                      |
|   | V <sub>DD_HV_IO0_2</sub>           | 3.3 V Input/Output Supply Voltage (supply)                                   | 38     | 61                   |
|   | V <sub>DD_HV_FLA1</sub>            | Code and data flash supply voltage   |        |                      |
|   | V <sub>DD_HV_IO0_3</sub>           | 3.3 V Input/Output Supply Voltage (supply)                                   | 55     | 87                   |
|   | V <sub>DD_HV_FLA0</sub>            | Code and data flash supply voltage   |        |                      |
|   | V <sub>DD_HV</sub>                 | HV Supply  | -      | 36                   |
| V <sub>SS_HV</sub>  | V <sub>SS_HV_IO0_0</sub>           | Input/output ground voltage  | 12     | 19                   |
|   | V <sub>SS_HV_OSC0</sub>            | Crystal oscillator amplifier ground  |        |                      |
|   | V <sub>SS_HV_IO0_2</sub>           | Input/output ground voltage  | 37     | 60                   |
|   | V <sub>ss_HV_FLA1</sub>            | Code and data flash supply ground  |        |                      |
|   | V <sub>ss_IO0_4</sub>              | Input/output ground voltage  | 56     | 35                   |
|   | V <sub>ss_HV_FLA0</sub>            | Code and data flash supply voltage   |        |                      |
|   | V <sub>SS_HV</sub>                 | HV Ground  | 47     | 74                   |



Table 2. Supply pins (continued)

| Supply   |                                    |   | Pin    |                      |
|--|------------------------------------|---|--------|----------------------|
| Port Pin   | Multi-bonded Power Supplies/Ground | Description   | 64-pin | 100-pin <sup>1</sup> |
| Power supply pins (1.2 V). Pins available on 64-pin and 100-pin package. |                                    |   |        |                      |
| V <sub>DD_LV</sub>   | V <sub>DD_LV_COR0_3</sub>          | 1.2 V supply pins for core logic and code Flash. Decoupling capacitor must be connected between these pins and the nearest V <sub>SS_LV_COR0_3</sub> pin. | 7      | 12                   |
|  | V <sub>DD_LV_PLL0</sub>            | 1.2 V PLL supply voltage  |        |                      |
|  | V <sub>DD_LV_COR0_2</sub>          | 1.2 V supply pins for core logic and code Flash. Decoupling capacitor must be connected between these pins and the nearest V <sub>SS_LV_COR0_2</sub> pin. | 58     | 92                   |
|  | V <sub>DD_LV_FLA0</sub>            | Code and data flash supply voltage  |        |                      |
|  | V <sub>DD_LV_COR0_1</sub>          | 1.2 V supply pins for core logic and code Flash. Decoupling capacitor must be connected between these pins and the nearest V <sub>SS_LV_COR0_1</sub> pin. | 35     | 58                   |
|  | V <sub>DD_LV_FLA1</sub>            | Code and data flash supply voltage  |        |                      |
|  | V <sub>DD_LV</sub>                 | Core supply   | -      | 33                   |
| V <sub>SS_LV</sub>   | V <sub>SS_LV_COR0_3</sub>          | 1.2 V supply pins for core logic and code Flash. Decoupling capacitor must be connected between these pins and the nearest V <sub>DD_LV_COR0_3</sub> pin. | 6      | 11                   |
|  | V <sub>SS_LV_PLL0</sub>            | PLL supply ground   |        |                      |
|  | V <sub>SS_LV_COR0_2</sub>          | 1.2 V supply pins for core logic and code Flash. Decoupling capacitor must be connected between these pins and the nearest V <sub>DD_LV_COR0_2</sub> pin. | 59     | 93                   |
|  | V <sub>SS_LV_FLA0</sub>            | Code and data flash supply ground   |        |                      |
|  | V <sub>SS_LV_COR0_1</sub>          | 1.2 V supply pins for core logic and data Flash. Decoupling capacitor must be connected between these pins and the nearest V <sub>DD_LV_COR0_1</sub> pin. | 36     | 59                   |
|  | V <sub>SS_LV_FLA1</sub>            | Code and data flash supply ground   |        |                      |
|  | V <sub>SS_LV</sub>                 | Core ground   | -      | 32                   |

<sup>1</sup> The 100-pin package is not a production package. It is used for software development only.

## 2.2.2 System pins

Table 3 and Table 4 contain information on pin functions for the MPC5604E devices. The pins listed in Table 3 are single-function pins. The pins shown in Table 4 are multi-function pins, programmable via their respective Pad Configuration Register (PCR) values.

**Table 3. System pins**

| Symbol                    | Description   | Direction     | Pad speed <sup>1</sup> |         | Pin    |                      |
|---------------------------|---|---------------|------------------------|---------|--------|----------------------|
|                           |   |               | SRC = 0                | SRC = 1 | 64-pin | 100-pin <sup>2</sup> |
| Dedicated pins            |   |               |                        |         |        |                      |
| $\overline{\text{NMI}}$   | Non-maskable Interrupt  | Input only    | Slow                   | —       | 1      | 1                    |
| XTAL                      | Oscillator amplifier output   | Output only   | —                      | —       | 13     | 20                   |
| EXTAL                     | Input for oscillator amplifier circuit and internal clock generator       | Input only    | —                      | —       | 14     | 21                   |
| TDI <sup>3</sup>          | JTAG test data input  | Input only    | Slow                   | Medium  | 40     | 63                   |
| TMS <sup>3</sup>          | JTAG state machine control  | Input only    | Slow                   | Medium  | 41     | 64                   |
| TCK <sup>3</sup>          | JTAG clock  | Input only    | Slow                   | —       | 42     | 65                   |
| TDO <sup>3</sup>          | JTAG test data output   | Output only   | Slow                   | Medium  | 43     | 66                   |
| Reset pin                 |   |               |                        |         |        |                      |
| $\overline{\text{RESET}}$ | Bidirectional reset with Schmitt trigger characteristics and noise filter | Bidirectional | Medium                 | —       | 15     | 22                   |
| POR_B                     | Power-on reset  | Input only    | —                      | —       | 31     | 45                   |

<sup>1</sup> SRC values refer to the value assigned to the Slew Rate Control bits of the pad configuration register.

<sup>2</sup> The 100-pin package is not a production package. It is used for software development only.

<sup>3</sup> Additional board pull resistors are recommended when JTAG pins are not being used on the board or application.

## 2.2.3 Pin muxing

Table 4 defines the pin list and muxing for the MPC5604E devices.

Each row of Table 4 shows all the possible ways of configuring each pin, via “alternate functions”. The default function assigned to each pin after reset is the ALT0 function. Pins marked as external interrupt capable can also be used to resume from STOP and HALT mode.

MPC5604E devices provide four main I/O pad types depending of the associated functions:

- *Slow pads* are the most common, providing a compromise between transition time and low electromagnetic emission.
- *Medium pads* provide fast enough transition for serial communication channels with controlled current to reduce electromagnetic emission.
- *Fast pads* provide maximum speed. They are used for improved Nexus debugging capability.

Medium and Fast pads can be used in slow configuration to reduce the electromagnetic emissions, at the cost of reducing AC performance.

Table 4. Pin muxing

| Port pin        | PCR register | Alternate function <sup>1,2,8</sup>         | Functions   | Peripheral <sup>3</sup>                                 | I/O direction <sup>4</sup>              | Pad speed <sup>5</sup> |         | Pin <sup>6</sup> |                      |
|-----------------|--------------|---|---|---|---|------------------------|---------|------------------|----------------------|
|                 |              |   |   |   |   | SRC = 0                | SRC = 1 | 64-pin           | 100-pin <sup>7</sup> |
| Port A (16-bit) |              |   |   |   |   |                        |         |                  |                      |
| A[0]            | PCR[0]       | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—<br>— | GPIO[0]<br>D[0]<br>—<br>—<br>D[11]<br>SIN<br>EIRQ[0]        | SIUL<br>SAI0<br>—<br>—<br>VID<br>DSPI 1<br>SIUL         | I/O<br>I/O<br>—<br>—<br>I<br>I<br>I     | Slow                   | Medium  | 2                | 2                    |
| A[1]            | PCR[1]       | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—      | GPIO[1]<br>D[1]<br>SOUT<br>—<br>D[10]<br>EIRQ[1]            | SIUL<br>SAI0<br>DSPI1<br>—<br>VID<br>SIUL               | I/O<br>I/O<br>O<br>—<br>I<br>I          | Slow                   | Medium  | 3                | 4                    |
| A[2]            | PCR[2]       | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—<br>— | GPIO[2]<br>D[2]<br>SCK<br>D[0]<br>D[9]<br>ETC[5]<br>EIRQ[2] | SIUL<br>SAI0<br>DSPI1<br>SAI1<br>VID<br>ETIMER0<br>SIUL | I/O<br>I/O<br>I/O<br>I/O<br>I<br>I<br>I | Slow                   | Medium  | 4                | 6                    |
| A[3]            | PCR[3]       | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—<br>— | GPIO[3]<br>D[3]<br>—<br>D[0]<br>D[8]<br>SIN<br>EIRQ[3]      | SIUL<br>SAI0<br>—<br>SAI2<br>VID<br>DSPI2<br>SIUL       | I/O<br>I/O<br>—<br>I/O<br>I<br>I<br>I   | Slow                   | Medium  | 5                | 8                    |
| A[4]            | PCR[4]       | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—<br>— | GPIO[4]<br>SYNC<br>SOUT<br>—<br>D[7]<br>ETC[3]<br>EIRQ[4]   | SIUL<br>SAI0<br>DSPI2<br>—<br>VID<br>ETIMER0<br>SIUL    | I/O<br>I/O<br>O<br>—<br>I<br>I<br>I     | Slow                   | Medium  | 8                | 15                   |
| A[5]            | PCR[5]       | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—<br>— | GPIO[5]<br>SYNC<br>SCK<br>D[0]<br>CLK<br>ETC[4]<br>EIRQ[5]  | SIUL<br>SAI1<br>DSPI2<br>SAI1<br>VID<br>ETIMER0<br>SIUL | I/O<br>I/O<br>I/O<br>I/O<br>I<br>I<br>I | Medium                 | Fast    | 9                | 16                   |

Table 4. Pin muxing (continued)

| Port pin | PCR register | Alternate function <sup>1,2,8</sup>              | Functions   | Peripheral <sup>3</sup>                                     | I/O direction <sup>4</sup>                 | Pad speed <sup>5</sup> |         | Pin <sup>6</sup> |                      |
|----------|--------------|--|---|---|--|------------------------|---------|------------------|----------------------|
|          |              |  |   |   |  | SRC = 0                | SRC = 1 | 64-pin           | 100-pin <sup>7</sup> |
| A[6]     | PCR[6]       | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—<br>—<br>— | GPIO[6]<br>SYNC<br>CS0<br>—<br>VSYNC<br>D[0]<br>ETC[1]<br>EIRQ[6] | SIUL<br>SAI2<br>DSPI2<br>—<br>VID<br>VID<br>ETIMER0<br>SIUL | I/O<br>I/O<br>I/O<br>—<br>I<br>I<br>I<br>I | Slow                   | Medium  | 10               | 17                   |
| A[7]     | PCR[7]       | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—<br>—<br>— | GPIO[7]<br>BCLK<br>CS1<br>—<br>HREF<br>D[1]<br>ETC[2]<br>EIRQ[7]  | SIUL<br>SAI0<br>DSPI2<br>—<br>VID<br>VID<br>ETIMER0<br>SIUL | I/O<br>I/O<br>I/O<br>—<br>I<br>I<br>I<br>I | Slow                   | Medium  | 16               | 23                   |
| A[8]     | PCR[8]       | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—<br>—      | GPIO[8]<br>BCLK<br>CS0<br>D[0]<br>D[6]<br>RX<br>EIRQ[8]           | SIUL<br>SAI1<br>DSPI1<br>SAI2<br>VID<br>LIN1<br>SIUL        | I/O<br>I/O<br>I/O<br>I/O<br>I<br>I<br>I    | Slow                   | Medium  | 24               | 37                   |
| A[9]     | PCR[9]       | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—           | GPIO[9]<br>BCLK<br>CS1<br>TX<br>D[5]<br>EIRQ[9]                   | SIUL<br>SAI2<br>DSPI1<br>LIN1<br>VID<br>SIUL                | I/O<br>I/O<br>I/O<br>O<br>I<br>I           | Slow                   | Medium  | 25               | 38                   |
| A[10]    | PCR[10]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—<br>—      | GPIO[10]<br>MCLK<br>ETC[5]<br>—<br>D[4]<br>SIN<br>EIRQ[10]        | SIUL<br>SAI2<br>ETIMER0<br>—<br>VID<br>DSPI0<br>SIUL        | I/O<br>I/O<br>I/O<br>—<br>I<br>I<br>I      | Slow                   | Medium  | 26               | 39                   |
| A[11]    | PCR[11]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—<br>—      | GPIO[11]<br>TX<br>CS1<br>CS0<br>D[3]<br>RX<br>RX                  | SIUL<br>CAN0<br>DSPI0<br>DSPI1<br>VID<br>LIN0<br>LIN1       | I/O<br>O<br>O<br>I/O<br>I<br>I<br>I        | Slow                   | Medium  | 27               | 40                   |

Table 4. Pin muxing (continued)

| Port pin        | PCR register | Alternate function <sup>1,2,8</sup>         | Functions  | Peripheral <sup>3</sup>   | I/O direction <sup>4</sup>            | Pad speed <sup>5</sup> |         | Pin <sup>6</sup> |                      |
|-----------------|--------------|---|--|---|---------------------------------------|------------------------|---------|------------------|----------------------|
|                 |              |   |  |   |                                       | SRC = 0                | SRC = 1 | 64-pin           | 100-pin <sup>7</sup> |
| A[12]           | PCR[12]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—<br>— | GPIO[12]<br>TX<br>CS0<br>TX<br>D[2]<br>RX<br>EIRQ[11]        | SIUL<br>LIN0<br>DSPI0<br>LIN1<br>VID<br>CAN0<br>SIUL            | I/O<br>O<br>I/O<br>O<br>I<br>I<br>I   | Slow                   | Medium  | 28               | 41                   |
| A[13]           | PCR[13]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—           | GPIO[13]<br>CLK<br>F[0]<br>CS0<br>EIRQ[12]                   | SIUL<br>IIC1<br>FCU0<br>DSPI0<br>SIUL                           | I/O<br>I/O<br>O<br>I/O<br>I           | Slow                   | Medium  | 29               | 42                   |
| A[14]           | PCR[14]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—      | GPIO[14]<br>DATA<br>F[1]<br>CS1<br>SIN<br>EIRQ[13]           | SIUL<br>IIC1<br>FCU0<br>DSPI0<br>DSPI0<br>SIUL                  | I/O<br>I/O<br>O<br>O<br>I<br>I        | Slow                   | Medium  | 30               | 43                   |
| A[15]           | PCR[15]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—<br>— | GPIO[15]<br>SCK<br>PPS3<br>MCLK<br>SCK<br>ETC[0]<br>EIRQ[18] | SIUL<br>DSPI0<br>CE_RTC<br>SAI1<br>DSPI1<br>ETIMER0<br>SIUL     | I/O<br>I/O<br>O<br>I/O<br>I<br>I<br>I | Slow                   | Medium  | 61               | 95                   |
| Port B (16-bit) |              |   |  |   |                                       |                        |         |                  |                      |
| B[0]            | PCR[16]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—           | GPIO[16]<br>TX<br>ALARM2<br>BCLK<br>AN[0]                    | SIUL<br>CAN0<br>CE_RTC<br>SAI1<br>ADC0 <sup>8</sup>             | I/O<br>O<br>O<br>I/O<br>I             | Slow                   | Medium  | 17               | 26                   |
| B[1]            | PCR[17]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—<br>— | GPIO[17]<br>—<br>—<br>D[0]<br>AN[1]<br>RX<br>TRIGGER2        | SIUL<br>—<br>—<br>SAI1<br>ADC0 <sup>8</sup><br>CAN0<br>CE_RTC   | I/O<br>—<br>—<br>I/O<br>I<br>I<br>I   | Slow                   | Medium  | 18               | 27                   |
| B[2]            | PCR[18]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—      | GPIO[18]<br>TX<br>PPS2<br>ALARM1<br>AN[2]<br>TRIGGER1        | SIUL<br>LIN0<br>CE_RTC<br>CE_RTC<br>ADC0 <sup>8</sup><br>CE_RTC | I/O<br>O<br>O<br>O<br>I<br>I          | Slow                   | Medium  | 19               | 28                   |

Table 4. Pin muxing (continued)

| Port pin | PCR register | Alternate function <sup>1,2,8</sup>         | Functions   | Peripheral <sup>3</sup>   | I/O direction <sup>4</sup>            | Pad speed <sup>5</sup> |         | Pin <sup>6</sup> |                      |
|----------|--------------|---|---|---|---------------------------------------|------------------------|---------|------------------|----------------------|
|          |              |   |   |   |                                       | SRC = 0                | SRC = 1 | 64-pin           | 100-pin <sup>7</sup> |
| B[3]     | PCR[19]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—<br>— | GPIO[19]<br>ETC[2]<br>SOUT<br>PPS1<br>AN[3]<br>RX<br>EIRQ[14] | SIUL<br>ETIMER0<br>DSPIO<br>CE_RTC<br>ADC0 <sup>8</sup><br>LIN0<br>SIUL | I/O<br>I/O<br>I/O<br>O<br>I<br>I<br>I | Slow                   | Medium  | 20               | 29                   |
| B[4]     | PCR[20]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—           | GPI[20]<br>—<br>—<br>—<br>RX_DV                               | SIUL<br>—<br>—<br>—<br>FEC  | I<br>—<br>—<br>—<br>I                 | Slow                   | Medium  | 32               | 50                   |
| B[5]     | PCR[21]      | ALT0<br>ALT1<br>ALT2<br>ALT3                | GPIO[21]<br>TX_D0<br>DEBUG[0]<br>—                            | SIUL<br>FEC<br>SSCM<br>—  | I/O<br>O<br>I/O<br>—                  | Slow                   | Medium  | 33               | 55                   |
| B[6]     | PCR[22]      | ALT0<br>ALT1<br>ALT2<br>ALT3                | GPIO[22]<br>TX_D1<br>DEBUG[1]<br>—                            | SIUL<br>FEC<br>SSCM<br>—  | I/O<br>O<br>I/O<br>—                  | Slow                   | Medium  | 34               | 56                   |
| B[7]     | PCR[23]      | ALT0<br>ALT1<br>ALT2<br>ALT3                | GPIO[23]<br>TX_D2<br>DEBUG[2]<br>—                            | SIUL<br>FEC<br>SSCM<br>—  | I/O<br>O<br>I/O<br>—                  | Slow                   | Medium  | 39               | 62                   |
| B[8]     | PCR[24]      | ALT0<br>ALT1<br>ALT2<br>ALT3                | GPIO[24]<br>TX_D3<br>DEBUG[3]<br>—                            | SIUL<br>FEC<br>SSCM<br>—  | I/O<br>O<br>I/O<br>—                  | Slow                   | Medium  | 44               | 67                   |
| B[9]     | PCR[25]      | ALT0<br>ALT1<br>ALT2<br>ALT3                | GPIO[25]<br>TX_EN<br>DEBUG[4]<br>—                            | SIUL<br>FEC<br>SSCM<br>—  | I/O<br>O<br>I/O<br>—                  | Slow                   | Medium  | 45               | 70                   |
| B[10]    | PCR[26]      | ALT0<br>ALT1<br>ALT2<br>ALT3                | GPIO[26]<br>MDC<br>DEBUG[5]<br>—                              | SIUL<br>FEC<br>SSCM<br>—  | I/O<br>O<br>I/O<br>—                  | Slow                   | Medium  | 46               | 73                   |
| B[11]    | PCR[27]      | ALT0<br>ALT1<br>ALT2<br>ALT3                | GPIO[27]<br>MDIO<br>DEBUG[6]<br>—                             | SIUL<br>FEC<br>SSCM<br>—  | I/O<br>I/O<br>I/O<br>—                | Slow                   | Medium  | 48               | 75                   |
| B[12]    | PCR[28]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—           | GPIO[28]<br>—<br>DEBUG[7]<br>—<br>TX_CLK                      | SIUL<br>—<br>SSCM<br>—<br>FEC   | I/O<br>—<br>I/O<br>—<br>I             | Slow                   | Medium  | 49               | 76                   |

Table 4. Pin muxing (continued)

| Port pin                                | PCR register | Alternate function <sup>1,2,8</sup>         | Functions  | Peripheral <sup>3</sup>                                  | I/O direction <sup>4</sup>            | Pad speed <sup>5</sup> |         | Pin <sup>6</sup> |                      |
|---|--------------|---|--|--|---------------------------------------|------------------------|---------|------------------|----------------------|
|   |              |   |  |  |                                       | SRC = 0                | SRC = 1 | 64-pin           | 100-pin <sup>7</sup> |
| B[13]                                   | PCR[29]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—           | GPI[29]<br>—<br>—<br>—<br>RX_D0                            | SIUL<br>—<br>—<br>—<br>FEC                               | I<br>—<br>—<br>—<br>I                 | Slow                   | Medium  | 50               | 77                   |
| B[14]                                   | PCR[30]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—           | GPI[30]<br>—<br>—<br>—<br>RX_D1                            | SIUL<br>—<br>—<br>—<br>FEC                               | I<br>—<br>—<br>—<br>I                 | Slow                   | Medium  | 51               | 79                   |
| B[15]                                   | PCR[31]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—           | GPI[31]<br>—<br>—<br>—<br>RX_D2                            | SIUL<br>—<br>—<br>—<br>FEC                               | I<br>—<br>—<br>—<br>I                 | Slow                   | Medium  | 52               | 81                   |
| Port C (64-pin: 7-bit; 100-pin: 16-bit) |              |   |  |  |                                       |                        |         |                  |                      |
| C[0]                                    | PCR[32]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—           | GPI[32]<br>—<br>—<br>—<br>RX_D3                            | SIUL<br>—<br>—<br>—<br>FEC                               | I<br>—<br>—<br>—<br>I                 | Slow                   | Medium  | 53               | 82                   |
| C[1]                                    | PCR[33]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—      | GPI[33]<br>—<br>—<br>—<br>RX_CLK<br>EIRQ[15]               | SIUL<br>—<br>—<br>—<br>FEC<br>SIUL                       | I<br>—<br>—<br>—<br>I<br>I            | Slow                   | Medium  | 54               | 83                   |
| C[2]                                    | PCR[34]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—<br>— | GPIO[34]<br>ETC[0]<br>TX<br>PPS1<br>D[0]<br>RX<br>EIRQ[16] | SIUL<br>ETIMER0<br>CAN0<br>CE_RTC<br>VID<br>LIN0<br>SIUL | I/O<br>I/O<br>O<br>O<br>I<br>I<br>I   | Slow                   | Medium  | 57               | 91                   |
| C[3]                                    | PCR[35]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—<br>— | GPIO[35]<br>ETC[1]<br>TX<br>SYNC<br>D[1]<br>RX<br>EIRQ[17] | SIUL<br>ETIMER0<br>LIN0<br>SAI1<br>VID<br>CAN0<br>SIUL   | I/O<br>I/O<br>O<br>I/O<br>I<br>I<br>I | Slow                   | Medium  | 60               | 94                   |

Table 4. Pin muxing (continued)

| Port pin | PCR register | Alternate function <sup>1,2,8</sup>         | Functions   | Peripheral <sup>3</sup>                                       | I/O direction <sup>4</sup>            | Pad speed <sup>5</sup> |         | Pin <sup>6</sup> |                      |
|----------|--------------|---|---|---|---------------------------------------|------------------------|---------|------------------|----------------------|
|          |              |   |   |   |                                       | SRC = 0                | SRC = 1 | 64-pin           | 100-pin <sup>7</sup> |
| C[4]     | PCR[36]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—<br>— | GPIO[36]<br>CLK_OUT<br>ETC[4]<br>MCLK<br>TRIGGER1<br>ABS[0]<br>EIRQ[19] | SIUL<br>MC_CGL<br>ETIMER0<br>SAI0<br>CE_RTC<br>MC_RGM<br>SIUL | I/O<br>O<br>I/O<br>I/O<br>I<br>I<br>I | Medium                 | Fast    | 62               | 96                   |
| C[5]     | PCR[37]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—      | GPIO[37]<br>CLK<br>ETC[3]<br>CS2<br>ABS[2]<br>EIRQ[20]                  | SIUL<br>IIC0<br>ETIMER0<br>DSPI2<br>MC_RGM<br>SIUL            | I/O<br>—<br>I/O<br>O<br>I<br>I        | Slow                   | Medium  | 63               | 99                   |
| C[6]     | PCR[38]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—      | GPIO[38]<br>DATA<br>CS0<br>CS3<br>FAB<br>EIRQ[21]                       | SIUL<br>IIC0<br>DSPI1<br>DSPI2<br>MC_RGM<br>SIUL              | I/O<br>—<br>I/O<br>O<br>I<br>I        | Slow                   | Medium  | 64               | 100                  |
| C[7]     | PCR[39]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—           | GPIO[39]<br>TXD<br>—<br>—<br>RXD  | SIUL<br>LIN0<br>—<br>—<br>LIN1                                | I/O<br>O<br>—<br>—<br>I               | Slow                   | Medium  | —                | 3                    |
| C[8]     | PCR[40]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—      | GPIO[40]<br>TXD<br>—<br>—<br>RXD<br>EIRQ[22]                            | SIUL<br>LIN1<br>—<br>—<br>LIN0<br>SIUL                        | I/O<br>O<br>—<br>—<br>I<br>I          | Slow                   | Medium  | —                | 5                    |
| C[9]     | PCR[41]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—      | GPI[41]<br>—<br>—<br>—<br>SIN<br>EIRQ[23]                               | SIUL<br>—<br>—<br>—<br>DSPI0<br>SIUL                          | I<br>—<br>—<br>—<br>I<br>I            | Slow                   | Medium  | —                | 7                    |
| C[10]    | PCR[42]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—      | GPIO[42]<br>ETC[5]<br>ETC[4]<br>—<br>SIN<br>EIRQ[24]                    | SIUL<br>ETIMER0<br>ETIMER0<br>—<br>DSPI1<br>SIUL              | I/O<br>I/O<br>I/O<br>—<br>I<br>I      | Slow                   | Medium  | —                | 24                   |
| C[11]    | PCR[43]      | ALT0<br>ALT1<br>ALT2<br>ALT3                | GPIO[43]<br>ETC[2]<br>ETC[1]<br>ETC[3]                                  | SIUL<br>ETIMER0<br>ETIMER0<br>ETIMER0                         | I/O<br>I/O<br>I/O<br>I/O              | Slow                   | Medium  | —                | 25                   |



Table 4. Pin muxing (continued)

| Port pin                         | PCR register | Alternate function <sup>1,2,8</sup>         | Functions  | Peripheral <sup>3</sup>  | I/O direction <sup>4</sup>        | Pad speed <sup>5</sup> |         | Pin <sup>6</sup> |                      |
|----------------------------------|--------------|---|--|--|-----------------------------------|------------------------|---------|------------------|----------------------|
|                                  |              |   |  |  |                                   | SRC = 0                | SRC = 1 | 64-pin           | 100-pin <sup>7</sup> |
| C[12]                            | PCR[44]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—<br>— | GPIO[44]<br>PPS1<br>PPS2<br>ALARM1<br>TRIGGER1<br>TRIGGER2<br>EIRQ[25] | SIUL<br>CE_RTC<br>CE_RTC<br>CE_RTC<br>CE_RTC<br>CE_RTC<br>SIUL | I/O<br>O<br>O<br>O<br>I<br>I<br>I | Slow                   | Medium  | —                | 44                   |
| C[13]                            | PCR[45]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—      | GPIO[45]<br>—<br>—<br>—<br>D[1]<br>EIRQ[26]                            | SIUL<br>—<br>—<br>—<br>VID<br>SIUL                             | I/O<br>—<br>—<br>—<br>I<br>I      | Slow                   | Medium  | —                | 46                   |
| C[14]                            | PCR[46]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—      | GPIO[46]<br>—<br>—<br>—<br>D[0]<br>EIRQ[27]                            | SIUL<br>—<br>—<br>—<br>VID<br>SIUL                             | I/O<br>—<br>—<br>—<br>I<br>I      | Slow                   | Medium  | —                | 47                   |
| C[15]                            | PCR[47]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—           | GPI[47]<br>—<br>—<br>—<br>COL  | SIUL<br>—<br>—<br>—<br>FEC                                     | I<br>—<br>—<br>—<br>I             | Slow                   | Medium  | —                | 48                   |
| Port D (100-pin package: 16-bit) |              |   |  |  |                                   |                        |         |                  |                      |
| D[0]                             | PCR[48]      | ALT0<br>ALT1<br>ALT2<br>ALT3                | GPIO[48]<br>MDO0<br>—<br>—   | SIUL<br>NEXUS<br>—<br>—  | I/O<br>O<br>—<br>—                | Slow                   | Medium  | —                | 9                    |
| D[1]                             | PCR[49]      | ALT0<br>ALT1<br>ALT2<br>ALT3                | GPIO[49]<br>MCK0<br>—<br>—   | SIUL<br>NEXUS<br>—<br>—  | I/O<br>O<br>—<br>—                | Slow                   | Medium  | —                | 14                   |
| D[2]                             | PCR[50]      | ALT0<br>ALT1<br>ALT2<br>ALT3                | GPIO[50]<br>EVTO<br>—<br>—   | SIUL<br>NEXUS<br>—<br>—  | I/O<br>O<br>—<br>—                | Slow                   | Medium  | —                | 13                   |
| D[3]                             | PCR[51]      | ALT0<br>ALT1<br>ALT2<br>ALT3                | GPIO[51]<br>MSEO1<br>—<br>—  | SIUL<br>NEXUS<br>—<br>—  | I/O<br>O<br>—<br>—                | Slow                   | Medium  | —                | 72                   |
| D[4]                             | PCR[52]      | ALT0<br>ALT1<br>ALT2<br>ALT3                | GPIO[52]<br>MSEO0<br>—<br>—  | SIUL<br>NEXUS<br>—<br>—  | I/O<br>O<br>—<br>—                | Slow                   | Medium  | —                | 78                   |

Table 4. Pin muxing (continued)

| Port pin | PCR register | Alternate function <sup>1,2,8</sup>    | Functions  | Peripheral <sup>3</sup>                         | I/O direction <sup>4</sup>       | Pad speed <sup>5</sup> |         | Pin <sup>6</sup> |                      |
|----------|--------------|--|--|---|----------------------------------|------------------------|---------|------------------|----------------------|
|          |              |  |  |   |                                  | SRC = 0                | SRC = 1 | 64-pin           | 100-pin <sup>7</sup> |
| D[5]     | PCR[53]      | ALT0<br>ALT1<br>ALT2<br>ALT3           | GPIO[53]<br>MDO3<br>—<br>—                           | SIUL<br>NEXUS<br>—<br>—                         | I/O<br>O<br>—<br>—               | Slow                   | Medium  | —                | 80                   |
| D[6]     | PCR[54]      | ALT0<br>ALT1<br>ALT2<br>ALT3           | GPIO[54]<br>MDO2<br>—<br>—                           | SIUL<br>NEXUS<br>—<br>—                         | I/O<br>O<br>—<br>—               | Slow                   | Medium  | —                | 84                   |
| D[7]     | PCR[55]      | ALT0<br>ALT1<br>ALT2<br>ALT3           | GPIO[55]<br>MDO1<br>—<br>—                           | SIUL<br>NEXUS<br>—<br>—                         | I/O<br>—<br>—<br>—               | Slow                   | Medium  | —                | 98                   |
| D[8]     | PCR[56]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—      | GPI[56]<br>—<br>—<br>—<br>EVTI                       | SIUL<br>—<br>—<br>—<br>NEXUS                    | I<br>—<br>—<br>—<br>I            | Slow                   | Medium  | —                | 10                   |
| D[9]     | PCR[57]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>— | GPIO[57]<br>ETC[3]<br>ETC[2]<br>—<br>RXD<br>EIRQ[28] | SIUL<br>ETIMER0<br>ETIMER0<br>—<br>CAN0<br>SIUL | I/O<br>I/O<br>I/O<br>—<br>I<br>I | Slow                   | Medium  | —                | 49                   |
| D[10]    | PCR[58]      | ALT0<br>ALT1<br>ALT2<br>ALT3           | GPIO[58]<br>TXD<br>—<br>—                            | SIUL<br>CAN0<br>—<br>—                          | I/O<br>O<br>—<br>—               | Slow                   | Medium  | —                | 51                   |
| D[11]    | PCR[59]      | ALT0<br>ALT1<br>ALT2<br>ALT3           | GPIO[59]<br>ETC[0]<br>ETC[5]<br>ETC[4]               | SIUL<br>ETIMER0<br>ETIMER0<br>ETIMER0           | I/O<br>I/O<br>I/O<br>I/O         | Slow                   | Medium  | —                | 52                   |
| D[12]    | PCR[60]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—      | GPIO[60]<br>ETC[1]<br>ETC[0]<br>—<br>SIN             | SIUL<br>ETIMER0<br>ETIMER0<br>—<br>DSPI0        | I/O<br>I/O<br>I/O<br>—<br>I      | Slow                   | Medium  | —                | 53                   |
| D[13]    | PCR[61]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>— | GPI[61]<br>—<br>—<br>—<br>CRS<br>EIRQ[29]            | SIUL<br>—<br>—<br>—<br>FEC<br>SIUL              | I<br>—<br>—<br>—<br>I<br>I       | Slow                   | Medium  | —                | 54                   |

Table 4. Pin muxing (continued)

| Port pin                        | PCR register | Alternate function <sup>1,2,8</sup>         | Functions   | Peripheral <sup>3</sup>                                    | I/O direction <sup>4</sup>        | Pad speed <sup>5</sup> |         | Pin <sup>6</sup> |                      |
|---------------------------------|--------------|---|---|--|-----------------------------------|------------------------|---------|------------------|----------------------|
|                                 |              |   |   |  |                                   | SRC = 0                | SRC = 1 | 64-pin           | 100-pin <sup>7</sup> |
| D[14]                           | PCR[62]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—      | GPI[62]<br>—<br>—<br>—<br>RX_ER<br>EIRQ[30]           | SIUL<br>—<br>—<br>—<br>FEC<br>SIUL                         | I<br>—<br>—<br>—<br>I<br>I        | Slow                   | Medium  | —                | 57                   |
| D[15]                           | PCR[63]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—      | GPIO[63]<br>F[0]<br>—<br>—                            | SIUL<br>FCU0<br>—<br>—                                     | I/O<br>O<br>—<br>—                | Slow                   | Medium  | —                | 69                   |
| Port E (100-pin package: 7-bit) |              |   |   |  |                                   |                        |         |                  |                      |
| E[0]                            | PCR[64]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—      | GPIO[64]<br>F[1]<br>—<br>—                            | SIUL<br>FCU0<br>—<br>—                                     | I/O<br>O<br>—<br>—                | Slow                   | Medium  | —                | 68                   |
| E[1]                            | PCR[65]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—      | GPIO[65]<br>TX_ER<br>—<br>—                           | SIUL<br>FEC<br>—<br>—                                      | I/O<br>O<br>—<br>—                | Slow                   | Medium  | —                | 71                   |
| E[2]                            | PCR[66]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—      | GPI[66]<br>—<br>—<br>—<br>RXD<br>EIRQ[31]             | SIUL<br>—<br>—<br>—<br>LIN1<br>SIUL                        | I<br>—<br>—<br>—<br>I<br>I        | Slow                   | Medium  | —                | 85                   |
| E[3]                            | PCR[67]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—      | GPIO[67]<br>TXD<br>—<br>—                             | SIUL<br>LIN1<br>—<br>—                                     | I/O<br>O<br>—<br>—                | Slow                   | Medium  | —                | 86                   |
| E[4]                            | PCR[68]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—      | GPIO[68]<br>CS0<br>CS0<br>CS0                         | SIUL<br>DSPI0<br>DSPI1<br>DSPI2                            | I/O<br>I/O<br>I/O<br>I/O          | Slow                   | Medium  | —                | 89                   |
| E[5]                            | PCR[69]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—      | GPIO[69]<br>SCK<br>SCK<br>SCK                         | SIUL<br>DSPI0<br>DSPI1<br>DSPI2                            | I/O<br>I/O<br>I/O<br>I/O          | Slow                   | Medium  | —                | 90                   |
| E[6]                            | PCR[70]      | ALT0<br>ALT1<br>ALT2<br>ALT3<br>—<br>—<br>— | GPIO[70]<br>SOUT<br>SOUT<br>SOUT<br>SIN<br>SIN<br>SIN | SIUL<br>DSPI0<br>DSPI1<br>DSPI2<br>DSPI0<br>DSPI2<br>DSPI2 | I/O<br>O<br>O<br>O<br>I<br>I<br>I | Slow                   | Medium  | —                | 97                   |

<sup>1</sup> ALT0 is the primary (default) function for each port after reset.

## Package pinouts and signal descriptions

- <sup>2</sup> Alternate functions are chosen by setting the values of the PCR.PA bitfields inside the SIU module. PCR.PA = 00 → ALT0; PCR.PA = 01 → ALT1; PCR.PA = 10 → ALT2; PCR.PA = 11 → ALT3. This is intended to select the output functions; to use one of the input functions, the PCR.IBE bit must be written to '1', regardless of the values selected in the PCR.PA bitfields. For this reason, the value corresponding to an input only function is reported as "—".
- <sup>3</sup> Module included on the MCU.
- <sup>4</sup> Multiple inputs are routed to all respective modules internally. The input of some modules must be configured by setting the values of the PSMIO.PADSELx bitfields inside the SIUL module.
- <sup>5</sup> Programmable via the SRC (Slew Rate Control) bits in the respective Pad Configuration Register.
- <sup>6</sup> Additional board pull resistors are recommended when JTAG pins are not being used on the board or application.
- <sup>7</sup> The 100-pin package is not a production package. It is used for software development only.
- <sup>8</sup> Do not use ALT multiplexing when ADC channels are used.

## 3 Electrical characteristics

### 3.1 Introduction

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level ( $V_{DD}$  or  $V_{SS}$ ). This can be done by the internal pull-up or pull-down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

### CAUTION

All of the following figures are indicative and must be confirmed during either silicon validation, silicon characterization or silicon reliability trial.

### 3.2 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in [Table 5](#) are used and the parameters are tagged accordingly in the tables where appropriate.

**Table 5. Parameter classifications**

| Classification tag | Tag description  |
|--------------------|--|
| P                  | Those parameters are guaranteed during production testing on each individual device.   |
| C                  | Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.  |
| T                  | Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category. |
| D                  | Those parameters are derived mainly from simulations.  |

### NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

### 3.3 Absolute maximum ratings

Table 6. Absolute Maximum Ratings<sup>1</sup>

| Symbol                               | Parameter  | Conditions   | Min                         | Max <sup>2</sup>            | Unit |
|--------------------------------------|--|--|-----------------------------|-----------------------------|------|
| V <sub>SS</sub>                      | SR Device ground   | —  | V <sub>SS</sub>             | V <sub>SS</sub>             | V    |
| V <sub>DD_HV_IO</sub>                | SR 3.3 V Input/Output Supply Voltage (supply).<br>Code Flash supply with V <sub>DD_HV_IO3</sub> and Data Flash with V <sub>DD_HV_IO2</sub> | —  | V <sub>SS</sub> – 0.3       | V <sub>SS</sub> + 6.0       | V    |
| V <sub>SS_HV_IO</sub>                | SR 3.3 V Input/Output Supply Voltage (ground).<br>Code Flash ground with V <sub>SS_HV_IO3</sub> and Data Flash with V <sub>SS_HV_IO2</sub> | —  | V <sub>SS</sub> – 0.1       | V <sub>SS</sub> + 0.1       | V    |
| V <sub>DD_HV_OSC</sub>               | SR 3.3 V Crystal Oscillator Amplifier Supply voltage (supply)  | The oscillator and flash supply segments are double-bounded with the V <sub>DD_HV_IO</sub> segments. See V <sub>DD_HV_IO</sub> and V <sub>SS_HV_IO</sub> specifications. |                             |                             | —    |
| V <sub>SS_HV_OSC</sub>               | SR 3.3 V Crystal Oscillator Amplifier Supply voltage (ground)  |  |                             |                             |      |
| V <sub>DD_HV_ADC0</sub> <sup>3</sup> | SR 3.3 V ADC_0 Supply and High Reference voltage   | —  | V <sub>SS</sub> – 0.3       | V <sub>SS</sub> + 6.0       | V    |
| V <sub>SS_HV_ADC0</sub>              | SR 3.3 V ADC_0 Ground and Low Reference voltage  | —  | V <sub>SS</sub> – 0.1       | V <sub>SS</sub> + 0.1       | V    |
| V <sub>DD_HV_REG</sub>               | SR 3.3 V Voltage Regulator Supply voltage  | —  | V <sub>SS</sub> – 0.3       | V <sub>SS</sub> + 6.0       | V    |
| TV <sub>DD</sub>                     | SR Slope characteristics on all VDD during power up <sup>4</sup>   | —  | —                           | 0.1                         | V/us |
| V <sub>DD_LV_COR</sub>               | SR 1.2 V supply pins for core logic (supply)   | —  | V <sub>SS</sub> – 0.3       | V <sub>SS</sub> + 1.4       | V    |
| V <sub>SS_LV_COR</sub>               | SR 1.2 V supply pins for core logic (ground)   | —  | V <sub>SS</sub> – 0.1       | V <sub>SS</sub> + 0.1       | V    |
| V <sub>IN</sub>                      | SR Voltage on any pin with respect to ground (V <sub>SS_HV_IO</sub> )  | —  | V <sub>SS_HV_IO</sub> – 0.3 | V <sub>DD_HV_IO</sub> + 0.5 | V    |
| I <sub>INPAD</sub>                   | SR Input current on any pin during overload condition  | —  | –10                         | 10                          | mA   |
| I <sub>INJSUM</sub>                  | SR Absolute sum of all input currents during overload condition  | —  | –50                         | 50                          | mA   |
| T <sub>STORAGE</sub>                 | SR Storage temperature   | —  | –55                         | 150                         | °C   |
| T <sub>J</sub>                       | SR Junction temperature under bias   | —  | –40                         | 150                         | °C   |
| T <sub>A</sub>                       | SR Ambient temperature under bias  | f <sub>CPU</sub> < 64 MHz  | –40                         | 125                         | °C   |
|                                      |  | f <sub>CPU</sub> < 64 MHz<br>Video use case with internal supply   | –40                         | 105                         | °C   |

<sup>1</sup> Functional operating conditions are given in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

- <sup>2</sup> Absolute maximum voltages are currently maximum burn-in voltages. Absolute maximum specifications for device stress have not yet been determined.
- <sup>3</sup> MPC5604E's I/O, flash, and oscillator circuit supplies are interconnected. The ADC supply managed independently from other supplies.
- <sup>4</sup> Guaranteed by device validation.

### 3.4 Recommended operating conditions

Table 7. Recommended operating conditions

| Symbol                               |    | Parameter  | Conditions  | Min             | Max <sup>1</sup> | Unit |
|--------------------------------------|----|--|---|-----------------|------------------|------|
| V <sub>SS</sub>                      | SR | Device ground  | —   | V <sub>SS</sub> | V <sub>SS</sub>  | V    |
| V <sub>DD_HV_IO</sub>                | SR | 3.3 V input/output supply voltage                          | —   | 3.0             | 3.6              | V    |
| V <sub>SS_HV_IO</sub>                | SR | Input/output ground voltage                                | —   | 0               | 0                | V    |
| V <sub>DD_HV_OSC</sub>               | SR | 3.3 V Crystal Oscillator Amplifier Supply voltage (supply) | The oscillator and flash supply segments are double-bounded with the V <sub>DD_HV_IOx</sub> segments. See V <sub>DD_HV_IOx</sub> and V <sub>SS_HV_IOx</sub> specifications. |                 |                  | —    |
| V <sub>SS_HV_OSC</sub>               | SR | 3.3 V Crystal Oscillator Amplifier Supply voltage (ground) |   |                 |                  |      |
| V <sub>DD_HV_ADC0</sub> <sup>2</sup> | SR | 3.3 V ADC_0 Supply and High Reference voltage              | —   | 3.0             | 3.6              | V    |
| V <sub>DD_HV_REG</sub>               | SR | 3.3 V voltage regulator supply voltage                     | —   | 3.0             | 3.6              | V    |
| V <sub>DD_LV_EXTCOR</sub>            | SR | Externally supplied core voltage                           | —   | 1.15            | 1.32             | V    |
| V <sub>DD_LV_REGCOR</sub>            | SR | Internal supply voltage                                    | —   | —               | —                | V    |
| V <sub>SS_LV_REGCOR</sub>            | SR | Internal reference voltage                                 | —   | 0               | 0                | V    |
| V <sub>DD_LV_COR</sub>               | SR | Internal supply voltage                                    | —   | —               | —                | V    |
| V <sub>SS_LV_COR</sub>               | SR | Internal reference voltage                                 | —   | 0               | 0                | V    |
| V <sub>SS_HV_ADC0</sub>              | SR | Ground and Low Reference voltage                           | —   | 0               | 0                | V    |
| T <sub>J</sub>                       | SR | Junction temperature under bias                            |   | −40             | 150              | °C   |
| T <sub>A</sub>                       | SR | Ambient temperature under bias                             | f <sub>CPU</sub> <64 MHz  | −40             | 125              | °C   |
|                                      |    |  | f <sub>CPU</sub> <64 MHz<br>Video use case<br>with internal<br>supply   | −40             | 105              | °C   |

<sup>1</sup> Full functionality cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed.

<sup>2</sup> MPC5604E's I/O, flash, and oscillator circuit supplies are interconnected. The ADC supply managed independently from other supplies.

### 3.5 Thermal characteristics

**Table 8. Thermal characteristics for 100-pin LQFP<sup>1</sup>**

| Symbol             | Parameter   | Conditions  | Typical value | Unit |
|--------------------|---|---|---------------|------|
| $R_{\theta JA}$    | Thermal resistance junction-to-ambient, natural convection <sup>2</sup> | Single layer board—1s                               | 51            | °C/W |
|                    |   | Four layer board—2s2p                               | 38            | °C/W |
| $R_{\theta JMA}$   | Thermal resistance junction-to-ambient <sup>2</sup>                     | @ 200 ft./min. <sup>3</sup> , single layer board—1s | 41            | °C/W |
|                    |   | @ 200 ft./min. <sup>3</sup> , four layer board—2s2p | 32            | °C/W |
| $R_{\theta JB}$    | Thermal resistance junction to board <sup>4</sup>                       | —   | 23            | °C/W |
| $R_{\theta JCTop}$ | Thermal resistance junction to case (top) <sup>5</sup>                  | —   | 11            | °C/W |
| $\Psi_{JT}$        | Junction to package top natural convection <sup>6</sup>                 | —   | 2             | °C/W |

<sup>1</sup> Thermal characteristics are targets based on simulation that are subject to change per device characterization.

<sup>2</sup> Junction-to-Ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

<sup>3</sup> Flow rate of forced air flow.

<sup>4</sup> Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

<sup>5</sup> Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

<sup>6</sup> Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

**Table 9. Thermal characteristics for 64-pin LQFP<sup>1</sup>**

| Symbol             | Parameter   | Conditions  | Typical value | Unit |
|--------------------|---|---|---------------|------|
| $R_{\theta JA}$    | Thermal resistance junction-to-ambient, natural convection <sup>2</sup> | Single layer board—1s                               | 64            | °C/W |
|                    |   | Four layer board—2s2p                               | 45            | °C/W |
| $R_{\theta JMA}$   | Thermal resistance junction-to-ambient <sup>2</sup>                     | @ 200 ft./min. <sup>3</sup> , single layer board—1s | 52            | °C/W |
|                    |   | @ 200 ft./min. <sup>3</sup> , four layer board—2s2p | 39            | °C/W |
| $R_{\theta JB}$    | Thermal resistance junction to board <sup>4</sup>                       | —   | 28            | °C/W |
| $R_{\theta JCTop}$ | Thermal resistance junction to case (top) <sup>5</sup>                  | —   | 14            | °C/W |
| $\Psi_{JT}$        | Junction to package top natural convection <sup>6</sup>                 | —   | 3             | °C/W |

<sup>1</sup> Thermal characteristics are targets based on simulation that are subject to change per device characterization.

<sup>2</sup> Junction-to-Ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.



- <sup>3</sup> Flow rate of forced air flow.
- <sup>4</sup> Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
- <sup>5</sup> Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
- <sup>6</sup> Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

### 3.5.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature,  $T_J$ , can be obtained from [Equation 1](#):

$$T_J = T_A + (R_{\theta JA} * P_D) \quad \text{Eqn. 1}$$

where:

- $T_A$  = ambient temperature for the package (°C)
- $R_{\theta JA}$  = junction to ambient thermal resistance (°C/W)
- $P_D$  = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. There are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in [Equation 2](#) as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \text{Eqn. 2}$$

where:

- $R_{\theta JA}$  = junction to ambient thermal resistance (°C/W)
- $R_{\theta JC}$  = junction to case thermal resistance (°C/W)
- $R_{\theta CA}$  = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$  is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance,  $R_{\theta CA}$ . For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter ( $\Psi_{JT}$ ) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using [Equation 3](#):

$$T_J = T_T + (\Psi_{JT} * P_D) \quad \text{Eqn. 3}$$

where:

- $T_T$  = thermocouple temperature on top of the package (°C)
- $\Psi_{JT}$  = thermal characterization parameter (°C/W)
- $P_D$  = power dissipation in the package (W)

## Electrical characteristics

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International  
 3081 Zanker Road  
 San Jose, CA 95134 U.S.A.  
 (408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at <http://www.jedec.org>.

1. C.E. Triplett and B. Joiner, *An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module*, Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.
2. G. Kromann, S. Shidore, and S. Addison, *Thermal Modeling of a PBGA for Air-Cooled Applications*, Electronic Packaging and Production, pp. 53-58, March 1998.
3. B. Joiner and V. Adams, *Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling*, Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

## 3.6 Electromagnetic Interference (EMI) characteristics

Table 10. EMI Testing Specifications<sup>1</sup>

| Symbol             | Parameter        | Conditions  | Clocks   | Frequency Range | Level (Typ) | Unit       |
|--------------------|------------------|---|--|-----------------|-------------|------------|
| Radiated emissions | V <sub>EME</sub> | V <sub>DD</sub> = 3.3 V<br>T <sub>A</sub> = +25 °C<br><br>Device Configuration, test conditions and EM testing per standard IEC61967-2. | Oscillator Frequency = 8 MHz;<br>System Bus Frequency = 64 MHz;<br>CPU Freq = 64MHZ<br>No PLL Frequency Modulation | 150 kHz–50 MHz  | 2           | dB $\mu$ V |
|                    |                  |   |  | 50–150 MHz      | 14          |            |
|                    |                  |   |  | 150–500 MHz     | 11          |            |
|                    |                  |   |  | 500–1000 MHz    | 7           |            |
|                    |                  |   |  | IEC Level       | M           |            |
|                    |                  |   | External Oscillator Freq = 8 MHz<br>System Bus Freq = 64 MHz<br>CPU Freq = 64MHZ<br><br>2% PLL Freq Modulation     | 150 kHz–50 MHz  | 1           | dB $\mu$ V |
|                    |                  |   |  | 50–150 MHz      | 11          |            |
|                    |                  |   |  | 150–500 MHz     | 7           |            |
|                    |                  |   |  | 500–1000 MHz    | 1           |            |
|                    |                  |   |  | IEC Level       | N           |            |

<sup>1</sup> EMI testing and I/O port waveforms per standard IEC61967-2.

## 3.7 Electrostatic Discharge (ESD) characteristics

Table 11. ESD ratings<sup>1,2</sup>

| Symbol         |    | Parameter                                      | Conditions | Value         | Unit |
|----------------|----|--|------------|---------------|------|
| $V_{ESD(HBM)}$ | SR | Electrostatic discharge (Human Body Model)     | —          | 2000          | V    |
| $V_{ESD(CDM)}$ | SR | Electrostatic discharge (Charged Device Model) | —          | 750 (corners) | V    |
|                |    |  |            | 500 (other)   |      |

<sup>1</sup> All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

<sup>2</sup> A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification

## 3.8 Power management electrical characteristics

### 3.8.1 Power Management Overview

The device supports the following power modes:

- Internal voltage regulation mode
- External voltage regulation mode

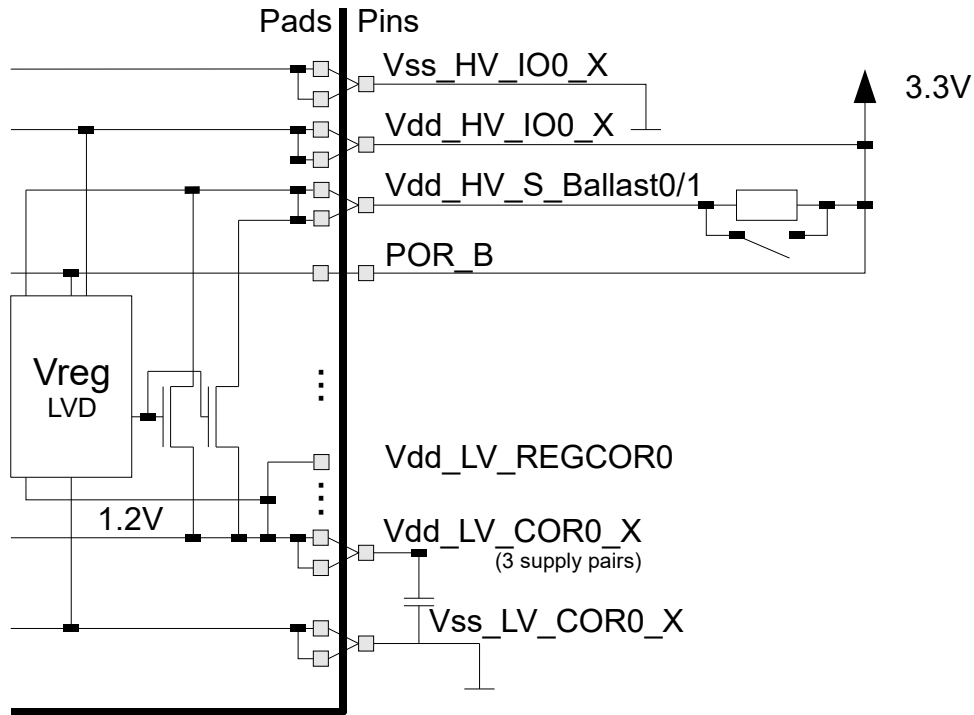
#### 3.8.1.1 Internal voltage regulation mode

In this mode, the following supplies are involved:

- $V_{DD\_HV\_IO}$  (3.3V) — This is the main supply provided externally.

## Electrical characteristics

- $V_{DD\_LV\_COR}$  (1.2V) — This is the core logic supply. In the internal regulation mode, the core supply is derived from the main supply via an on-chip linear regulator driving an internal PMOS ballast transistor. The PMOS ballast transistors are located in the pad ring and their source connectors are directly bonded to a dedicated pin. See [Figure 4](#).



**Figure 4. Internal Regulation Mode**

The core supply can also be provided externally. [Table 12](#) shows how to connect  $V_{DD\_HV\_S\_BALLAST}$  pin for internal and external core supply mode.

### NOTE

$V_{DD\_HV\_S\_BALLAST}$  pin is the supply pin, which carries the entire core logic current in the internal regulation mode, while in external regulation mode it is used as a signal to bypass the regulator.

**Table 12. Core Supply Select**

| Mode   | $V_{DD\_HV\_S\_Ballast}$ |
|--|--------------------------|
| Internal supply mode (via internal PMOS ballast transistors) | $V_{DD\_HV\_IO}$ (3.3V)  |
| External supply mode (e.g., via external switched regulator) | $V_{DD\_LV\_COR}$ (1.2V) |

### 3.8.1.2 External voltage regulation mode

In the external regulation mode, the core supply is provided externally using a switched regulator. This saves on-chip power consumption by avoiding the voltage drop over the ballast transistor. The external supply mode is selected via a board level supply change at the  $V_{DD\_HV\_S\_BALLAST}$  pin.

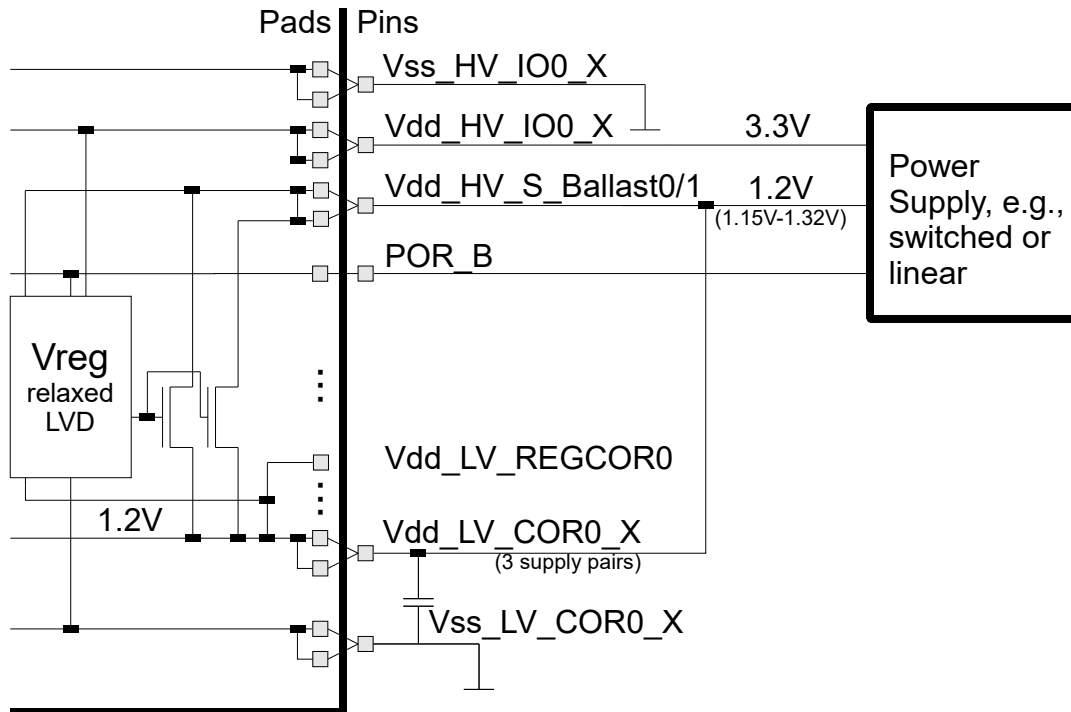


Figure 5. External Regulation Mode

#### NOTE

"In external regulation mode, POR\_B pin should be used to control the power on RESET for the device. POR\_B should be kept low (asserted) as long as the input supplies are unstable or below the specified operating range. Failure to do so may lead to unexpected device operation and erratic reset recovery"

### 3.8.1.3 Recommended power supply sequencing<sup>1</sup>

For MPC5604E, the external supplies need to be maintained as per the following relations:

- $V_{DD\_HV\_IO}$  should be always greater or equal to  $V_{DD\_HV\_S\_Ballast}$
- $V_{DD\_HV\_IO}$  should be always greater than  $V_{DD\_LV\_COR0\_X}$
- $V_{DD\_HV\_IO}$  should be always greater than  $V_{DD\_HV\_ADC}$

<sup>1</sup>Investigations are in process to relax power supply sequencing recommendation.

### 3.8.2 Voltage regulator electrical characteristics

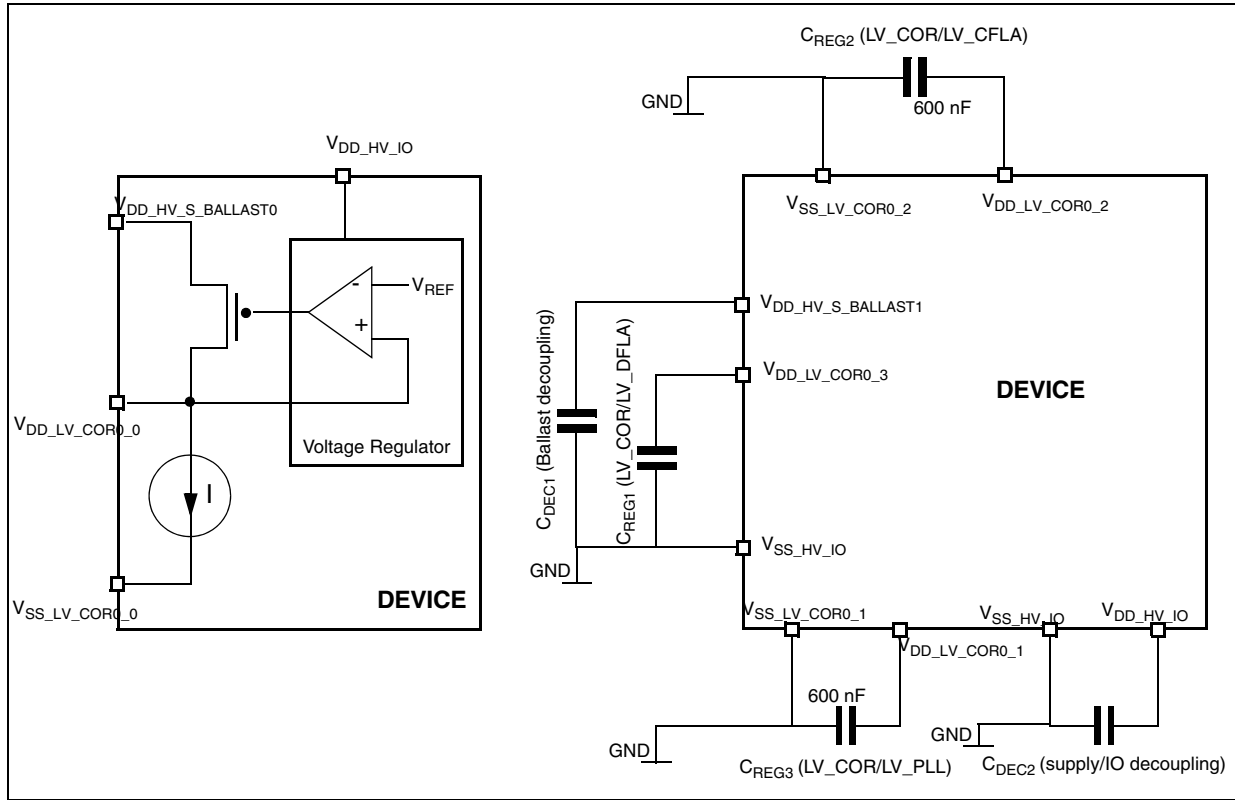


Figure 6. Voltage regulator capacitance connection

Table 13. Voltage regulator electrical characteristics

| Symbol       | C  | Parameter  | Conditions <sup>1</sup>   | Value            |                  |      | Unit     |
|--------------|----|--|---------------------------|------------------|------------------|------|----------|
|              |    |  |                           | Min              | Typ              | Max  |          |
| $C_{REGn}^2$ | SR | Internal voltage regulator external capacitance        | —                         | 200              | —                | 600  | nF       |
| $R_{REG}$    | SR | Stability capacitor equivalent serial resistance       | —                         | 0.05             | —                | 0.2  | $\Omega$ |
| $C_{DEC1}$   | SR | Decoupling capacitance <sup>3</sup> ballast            | —                         | 100 <sup>4</sup> | 470 <sup>5</sup> | —    | nF       |
|              |    |  | —                         | 400              |                  | —    |          |
| $C_{DEC2}$   | SR | Decoupling capacitance regulator supply                | —                         | 100 nF           | 1 $\mu$ F        | —    | —        |
| $V_{MREG}$   | CC | Main regulator output voltage                          | Before exiting from reset | —                | 1.32             | —    | V        |
|              |    |  | After trimming            | 1.15             | 1.28             | 1.32 |          |
| $I_{MREG}$   | SR | Main regulator current provided to $V_{DD\_LV}$ domain | —                         | —                | —                | 150  | mA       |

Table 13. Voltage regulator electrical characteristics (continued)

| Symbol               | C  | Parameter  | Conditions <sup>1</sup>    | Value |     |                 | Unit |
|----------------------|----|--|----------------------------|-------|-----|-----------------|------|
|                      |    |  |                            | Min   | Typ | Max             |      |
| I <sub>MREGINT</sub> | CC | Main regulator module current consumption                          | I <sub>MREG</sub> = 200 mA | —     | —   | 2               | mA   |
|                      |    |  | I <sub>MREG</sub> = 0 mA   | —     | —   | 1               |      |
| I <sub>DD_BV</sub>   | CC | In-rush current on V <sub>DD_BV</sub> during power-up <sup>6</sup> | —                          | —     | —   | 40 <sup>7</sup> | mA   |

<sup>1</sup> V<sub>DD</sub> = 3.3 V ± 10%, T<sub>A</sub> = -40 to 125 °C, unless otherwise specified

<sup>2</sup> It is required by the device in internal voltage regulation mode only.

<sup>3</sup> This capacitance value is driven by the constraints of the external voltage regulator that supplies the V<sub>DD\_BV</sub> voltage. A typical value is in the range of 470 nF. This capacitance should be placed close to the device pin.

<sup>4</sup> This value is acceptable to guarantee operation from 3.0 V to 3.6 V

<sup>5</sup> External regulator and capacitance circuitry must be capable of providing I<sub>DD\_BV</sub> while maintaining supply V<sub>DD\_BV</sub> in operating range.

<sup>6</sup> In-rush current is seen only for short time during power-up and on standby exit (max 20 μs, depending on external LV capacitances to be load)

<sup>7</sup> The duration of the in-rush current depends on the capacitance placed on LV pins. BV decaps must be sized accordingly. Refer to IMREG value for minimum amount of current to be provided in cc.

### 3.8.3 Voltage monitor electrical characteristics

The device implements a POR module to ensure correct power-up initialization, as well as three low voltage detectors to monitor the V<sub>DD\_HV</sub> and the V<sub>DD\_LV</sub> voltage while device is supplied:

- POR monitors V<sub>DD\_HV</sub> during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors V<sub>DD\_HV</sub> to ensure device reset below minimum functional supply
- LVDLVCOR monitors low voltage digital power domain

Table 14. Low voltage monitor electrical characteristics

| Symbol                    | C | Parameter  | Conditions <sup>1</sup> | Value |       | Unit |
|---------------------------|---|--|-------------------------|-------|-------|------|
|                           |   |  |                         | Min   | Max   |      |
| V <sub>PORH</sub>         | T | Power-on reset threshold                               | —                       | 1.5   | 2.7   | V    |
| V <sub>PORUP</sub>        | D | Supply for functional POR module                       | T <sub>A</sub> = 25°C   | 1.0   | —     | V    |
| V <sub>DDHVLVDMOK_H</sub> | P | V <sub>DD_HV</sub> low voltage detector high threshold | —                       | —     | 2.95  | V    |
| V <sub>DDHVLVDMOK_L</sub> | P | V <sub>DD_HV</sub> low voltage detector low threshold  | —                       | 2.6   | —     | V    |
| V <sub>MLVDDOK_H</sub>    | P | Digital supply low voltage detector high               | —                       | —     | 1.135 | V    |
| V <sub>MLVDDOK_L</sub>    | P | Digital supply low voltage detector low                | —                       | 1.095 | —     | V    |

<sup>1</sup> V<sub>DD\_HV</sub> = 3.3V ± 10% T<sub>A</sub> = -40 °C to T<sub>A MAX</sub>, unless otherwise specified

### 3.9 Power Up/Down reset sequencing

The MPC5604E implements a precise sequence to ensure each module is started only when all conditions for switching it ON are available. This prevents overstress event or miss-functionality within and outside the device:

## Electrical characteristics

- A POR module working on voltage regulator supply is controlling the correct start-up of the regulator. This is a key module ensuring safe configuration for all Voltage regulator functionality when supply is below 1.5 V. Associated POR (or POR) signal is active low.
- Several Low Voltage Detectors, working on voltage regulator supply are monitoring the voltage of the critical modules (Voltage regulator, I/Os, Flash and Low voltage domain). LVDs are gated low when POWER\_ON is active.
- A POWER\_OK signal is generated when all critical supplies monitored by the LVD are available. This signal is active high and released to all modules including I/Os, Flash and RC16 oscillator needed during power-up phase and reset phase. When POWER\_OK is low the associated module are set into a safe state.

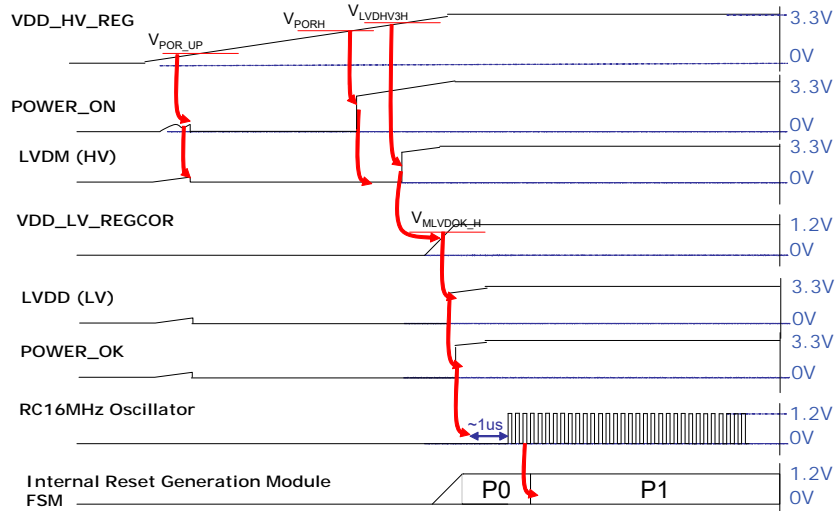


Figure 7. Power-up typical sequence

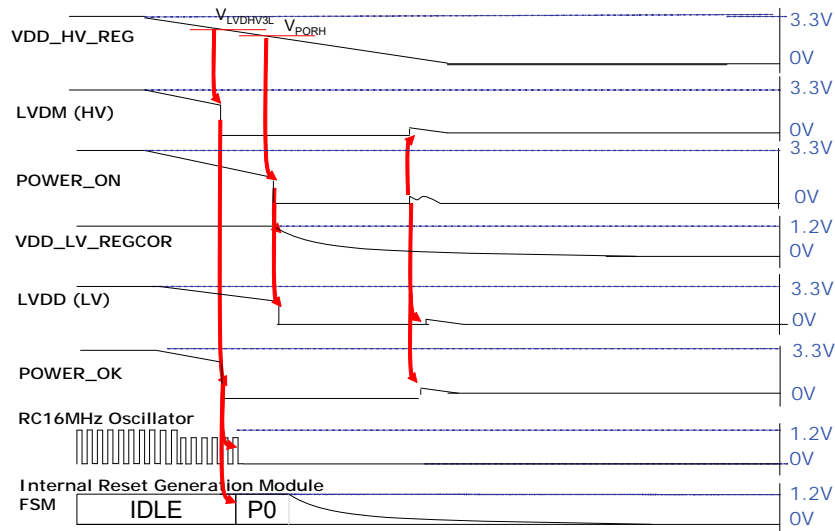


Figure 8. Power-down typical sequence



### 3.10 DC electrical characteristics

Table 15 gives the DC electrical characteristics at 3.3 V ( $3.0\text{ V} < V_{DD\_HV\_IO} < 3.6\text{ V}$ ).

Table 15. DC electrical characteristics (3.3 V)<sup>1</sup>

| Symbol            |   | Parameter  | Conditions                        | Min                        | Max                                      | Unit |
|-------------------|---|--|-----------------------------------|----------------------------|--|------|
| V <sub>IL</sub>   | D | Minimum low level input voltage                              | —                                 | -0.4 <sup>2</sup>          | —  | V    |
| V <sub>IL</sub>   | P | Maximum low level input voltage                              | —                                 | —                          | 0.35 V <sub>DD_HV_IO</sub>               | V    |
| V <sub>IH</sub>   | P | Minimum high level input voltage                             | —                                 | 0.65 V <sub>DD_HV_IO</sub> | —  | V    |
| V <sub>IH</sub>   | D | Maximum high level input voltage                             | —                                 | —                          | V <sub>DD_HV_IO</sub> + 0.4 <sup>2</sup> | V    |
| V <sub>HYS</sub>  | T | Schmitt trigger hysteresis                                   | —                                 | 0.1 V <sub>DD_HV_IO</sub>  | —  | V    |
| V <sub>OL_S</sub> | P | Slow, low level output voltage                               | I <sub>OL</sub> = 2 mA            | —                          | 0.1V <sub>DD_HV_IO</sub>                 | V    |
| V <sub>OH_S</sub> | P | Slow, high level output voltage                              | I <sub>OH</sub> = -2 mA           | 0.8V <sub>DD_HV_IO</sub>   | —  | V    |
| V <sub>OL_M</sub> | P | Medium, low level output voltage                             | I <sub>OL</sub> = 2 mA            | —                          | 0.1V <sub>DD_HV_IO</sub>                 | V    |
| V <sub>OH_M</sub> | P | Medium, high level output voltage                            | I <sub>OH</sub> = -3 mA           | 0.8V <sub>DD_HV_IO</sub>   | —  | V    |
| V <sub>OL_F</sub> | P | Fast, high level output voltage                              | I <sub>OL</sub> = 11 mA           | —                          | 0.1V <sub>DD_HV_IO</sub>                 | V    |
| V <sub>OH_F</sub> | P | Fast, high level output voltage                              | I <sub>OH</sub> = -11 mA          | 0.8V <sub>DD_HV_IO</sub>   | —  | V    |
| I <sub>PU</sub>   | P | Equivalent pull-up current                                   | V <sub>IN</sub> = V <sub>IL</sub> | -95                        | —  | μA   |
| I <sub>PD</sub>   | P | Equivalent pull-down current                                 | V <sub>IN</sub> = V <sub>IH</sub> | —                          | 95                                       |      |
| I <sub>IL</sub>   | P | Input leakage current (all bidirectional ports)              | T <sub>A</sub> = -40 to 125 °C    | —                          | 1  | μA   |
| I <sub>IL</sub>   | P | Input leakage current (all ADC input-only ports)             | T <sub>A</sub> = -40 to 125 °C    | —                          | 0.5                                      | μA   |
| V <sub>ILR</sub>  | D | Minimum $\overline{\text{RESET}}$ , low level input voltage  | —                                 | -0.4 <sup>2</sup>          | —  | V    |
| V <sub>ILR</sub>  | P | Maximum $\overline{\text{RESET}}$ , low level input voltage  | —                                 | —                          | 0.35 V <sub>DD_HV_IO</sub>               | V    |
| V <sub>IHR</sub>  | P | Minimum $\overline{\text{RESET}}$ , high level input voltage | —                                 | 0.65 V <sub>DD_HV_IO</sub> | —  | V    |
| V <sub>IHR</sub>  | D | Maximum $\overline{\text{RESET}}$ , high level input voltage | —                                 | —                          | V <sub>DD_HV_IO</sub> + 0.4 <sup>2</sup> | V    |
| V <sub>HYSR</sub> | D | $\overline{\text{RESET}}$ , Schmitt trigger hysteresis       | —                                 | 0.1 V <sub>DD_HV_IO</sub>  | —  | V    |
| V <sub>OLR</sub>  | D | $\overline{\text{RESET}}$ , low level output voltage         | I <sub>OL</sub> = 0.5 mA          | —                          | 0.1V <sub>DD_HV_IO</sub>                 | V    |
| I <sub>PU</sub>   | D | $\overline{\text{RESET}}$ , equivalent pull-up current       | V <sub>IN</sub> = V <sub>IL</sub> | -130                       | —  | μA   |
|                   |   |  | V <sub>IN</sub> = V <sub>IH</sub> | —                          | -10                                      |      |
| C <sub>IN</sub>   | D | Input capacitance  | —                                 | —                          | 10                                       | pF   |

<sup>1</sup> These specifications are design targets and subject to change per device characterization.

<sup>2</sup> “SR” parameter values must not exceed the absolute maximum ratings shown in Table 6.

Table 16. Supply current

| Symbol                  |   | Parameter      |   | Conditions   | Value <sup>1</sup> |      |     | Unit |  |
|-------------------------|---|----------------|---|--|--------------------|------|-----|------|--|
|                         |   |                |   |  | Min                | Typ  | Max |      |  |
| I <sub>DD_LV_CORE</sub> | C |                | RUN Mode, I/O currents not included, worst case over temperature for system clock |  | —                  | 75   | 120 | mA   |  |
|                         | P |                | HALT Mode <sup>2</sup>  | V <sub>DD_LV_CORx</sub> externally forced at 1.3 V   | —                  | 4    | 25  |      |  |
|                         | P |                | STOP Mode <sup>3</sup>  | V <sub>DD_LV_CORx</sub> externally forced at 1.3 V   | —                  | 4    | 25  |      |  |
| I <sub>DD_FLASH</sub>   | C | Supply current | <b>Code Flash</b>   |  |                    |      |     |      |  |
|                         |   |                | FLASH supply current during read  | V <sub>DD_HV_IO</sub> at 3.3 V                       | —                  | 4    | 7   |      |  |
|                         |   |                | FLASH supply current during erase operation on 1 Flash module                     | V <sub>DD_HV_IO</sub> at 3.3 V                       | —                  | 9    | 14  |      |  |
|                         |   |                | <b>Data Flash</b>   |  |                    |      |     |      |  |
|                         |   |                | FLASH supply current during read  | V <sub>DD_HV_IO</sub> at 3.3 V                       | —                  | 3.5  | 6   |      |  |
|                         |   |                | FLASH supply current during erase operation on 1 Flash module                     | V <sub>DD_HV_IO</sub> at 3.3 V                       | —                  | 7.5  | 12  |      |  |
| I <sub>DD_ADC</sub>     | C |                | ADC supply current  | V <sub>DD_HV_ADC0</sub> at 3.3 V<br>ADC Freq = 16MHz | —                  | 1.8  | 3   |      |  |
| I <sub>DD_OSC</sub>     | C |                | OSC supply current  | V <sub>DD_HV_OSC</sub> at 3.3 V<br>16 MHz            | —                  | 0.74 | 4   |      |  |

<sup>1</sup> All values to be confirmed after characterization/data collection.

<sup>2</sup> Halt mode configurations: Code fetched from SRAM, Code Flash and Data Flash in low power mode, OSC/PLL0 are OFF, Core clock frozen, all peripherals are disabled.

<sup>3</sup> STOP "P" mode DUT configuration: Code fetched from SRAM, Code Flash and Data Flash off, OSC/PLL0 are OFF, Core clock frozen, all peripherals are disabled.

### 3.11 Main oscillator electrical characteristics

The MPC5604E provides an oscillator/resonator driver.

Table 17. Main oscillator electrical characteristics

| Symbol             |    | Parameter                         | Min | Max    | Unit |
|--------------------|----|-----------------------------------|-----|--------|------|
| f <sub>OSC</sub>   | SR | Oscillator frequency              | 4   | 40     | MHz  |
| g <sub>m</sub>     | P  | Transconductance                  | 4   | 15.846 | mA/V |
| V <sub>OSC</sub>   | T  | Oscillation amplitude on XTAL pin | 1.3 | 2.25   | V    |
| t <sub>OSCSU</sub> | T  | Start-up time <sup>1,2</sup>      | —   | 5      | ms   |

<sup>1</sup> The start-up time is dependent upon crystal characteristics, board leakage, etc., high ESR and excessive capacitive loads can cause long start-up time.

<sup>2</sup> Value captured when amplitude reaches 90% of XTAL

**Table 18. Input clock characteristics**

| Symbol            |    | Parameter                | Min  | Typ | Max  | Unit |
|-------------------|----|--------------------------|------|-----|------|------|
| f <sub>OSC</sub>  | SR | Oscillator frequency     | 4    | —   | 40   | MHz  |
| f <sub>CLK</sub>  | SR | Frequency in bypass      | —    | —   | 100  | MHz  |
| t <sub>rCLK</sub> | SR | Rise/fall time in bypass | —    | —   | 1    | ns   |
| t <sub>DC</sub>   | SR | Duty cycle               | 47.5 | 50  | 52.5 | %    |

### 3.12 FMPLL electrical characteristics

**Table 19. PLLMRFM electrical specifications<sup>1</sup>**  
(V<sub>DDPLL</sub> = 3.0 V to 3.6 V, V<sub>SS</sub> = V<sub>SSPLL</sub> = 0 V, T<sub>A</sub> = T<sub>L</sub> to T<sub>H</sub>)

| Symbol   |   | Parameter   |  | Conditions               | Value                |     | Unit               |
|--|---|---|--|--------------------------|----------------------|-----|--------------------|
|  |   |   |  |                          | Min                  | Max |                    |
| f <sub>ref_crystal</sub><br>f <sub>ref_ext</sub> | D | PLL reference frequency range <sup>2</sup>                              |  | Crystal reference        | 4                    | 40  | MHz                |
| f <sub>pll_in</sub>                              | D | Phase detector input frequency range (after pre-divider)                |  | —                        | 4                    | 16  | MHz                |
| f <sub>FMPLL_0</sub><br>PCS                      | D | Clock frequency range in normal mode                                    |  | —                        | 4                    | 128 | MHz                |
| f <sub>FMPLL_0</sub><br>_CLK                     | D | PLL output frequency  |  | —                        | 4                    | 256 | MHz                |
| f <sub>VCO</sub>                                 | P | VCO frequency   |  | —                        | 256                  | 512 | MHz                |
| f <sub>sys</sub>                                 | D | On-chip PLL frequency <sup>2</sup>                                      |  | —                        | 16                   | 64  | MHz                |
| t <sub>CYC</sub>                                 | D | System clock period   |  | —                        | 1 / f <sub>sys</sub> |     | ns                 |
| f <sub>SCM</sub>                                 | D | Self-clocked mode frequency (VCO free running frequency) <sup>3,4</sup> |  | —                        | 20                   | 150 | MHz                |
| CLKOU<br>T <sub>JITTER</sub>                     | T | CLKOUT period jitter <sup>5,6,7,8</sup>                                 | Peak-to-peak (clock edge to clock edge)    | f <sub>sys</sub> Maximum | -500                 | 500 | ps                 |
|  |   |   | Long-term jitter (avg. over 2 ms interval) |                          | -6                   | 6   | ns                 |
| t <sub>pll</sub>                                 | D | PLL lock time <sup>9, 10</sup>  |  | —                        | —                    | 200 | μs                 |
| t <sub>dc</sub>                                  | D | Duty cycle of reference   |  | —                        | 40                   | 60  | %                  |
| f <sub>LCK</sub>                                 | D | Frequency LOCK range  |  | —                        | -6                   | 6   | % f <sub>sys</sub> |

**Table 19. PLLMRFM electrical specifications<sup>1</sup>**  
 ( $V_{DDPLL} = 3.0\text{ V to }3.6\text{ V}$ ,  $V_{SS} = V_{SSPLL} = 0\text{ V}$ ,  $T_A = T_L\text{ to }T_H$ ) (continued)

| Symbol               |   | Parameter                          | Conditions    | Value      |                | Unit        |
|----------------------|---|------------------------------------|---------------|------------|----------------|-------------|
|                      |   |                                    |               | Min        | Max            |             |
| $f_{UL}$             | D | Frequency un-LOCK range            | —             | -18        | 18             | % $f_{sys}$ |
| $f_{CS}$<br>$f_{DS}$ | D | Modulation Depth                   | Center spread | $\pm 0.25$ | $\pm 4.0^{11}$ | % $f_{sys}$ |
|                      |   |                                    | Down Spread   | -0.5       | -8.0           |             |
| $f_{MOD}$            | D | Modulation frequency <sup>12</sup> | —             | —          | 100            | kHz         |

- <sup>1</sup> All values given are initial design targets and subject to change.
- <sup>2</sup> Considering operation with PLL not bypassed.
- <sup>3</sup> Self clocked mode frequency is the frequency that the PLL operates at when the PLL reference frequency falls.
- <sup>4</sup>  $f_{scm}$  represents PLL0 VCO frequency in free running (when the PLL reference clock is disconnected).
- <sup>5</sup> This value is determined by the crystal manufacturer and board design.
- <sup>6</sup> Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum  $f_{sys}$ . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via  $V_{DDPLL}$  and  $V_{SSPLL}$  and variation in crystal oscillator frequency increase the  $C_{JITTER}$  percentage for a given interval.
- <sup>7</sup> Proper PC board layout procedures must be followed to achieve specifications.
- <sup>8</sup> Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of  $C_{JITTER}$  and either  $f_{CS}$  or  $f_{DS}$  (depending on whether center spread or down spread modulation is enabled).
- <sup>9</sup> This value is determined by the crystal manufacturer and board design. For 4 MHz to 20 MHz crystals specified for this PLL, load capacitors should not exceed these limits.
- <sup>10</sup> This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).
- <sup>11</sup> This value is true when operating at frequencies above 60 MHz, otherwise  $f_{CS}$  is 2% (above 64 MHz).
- <sup>12</sup> Modulation depth will be attenuated from depth setting when operating at modulation frequencies above 50 kHz.

### 3.13 16 MHz RC oscillator electrical characteristics

**Table 20. 16 MHz RC oscillator electrical characteristics**

| Symbol             |   | Parameter  | Conditions                       | Min | Typ | Max | Unit |
|--------------------|---|--|----------------------------------|-----|-----|-----|------|
| $f_{RC}$           | C | RC oscillator frequency  | $T_A = 25\text{ }^\circ\text{C}$ | 8.5 | 16  | 24  | MHz  |
| $\Delta_{RCMVAR}$  | P | Fast internal RC oscillator variation in temperature and supply with respect to $f_{RC}$ at $T_A = 55\text{ }^\circ\text{C}$ in high-frequency configuration | —                                | -5  | —   | 5   | %    |
| $\Delta_{RCMTRIM}$ | T | Post Trim Accuracy: The variation of the PTF <sup>1</sup> from the 16 MHz oscillator   | $T_A = 25\text{ }^\circ\text{C}$ | -2  | —   | 2   | %    |

<sup>1</sup> PTF = Post Trimming Frequency: The frequency of the output clock after trimming at typical supply voltage and temperature

### 3.14 Analog-to-Digital Converter (ADC) electrical characteristics

The device provides a 10-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

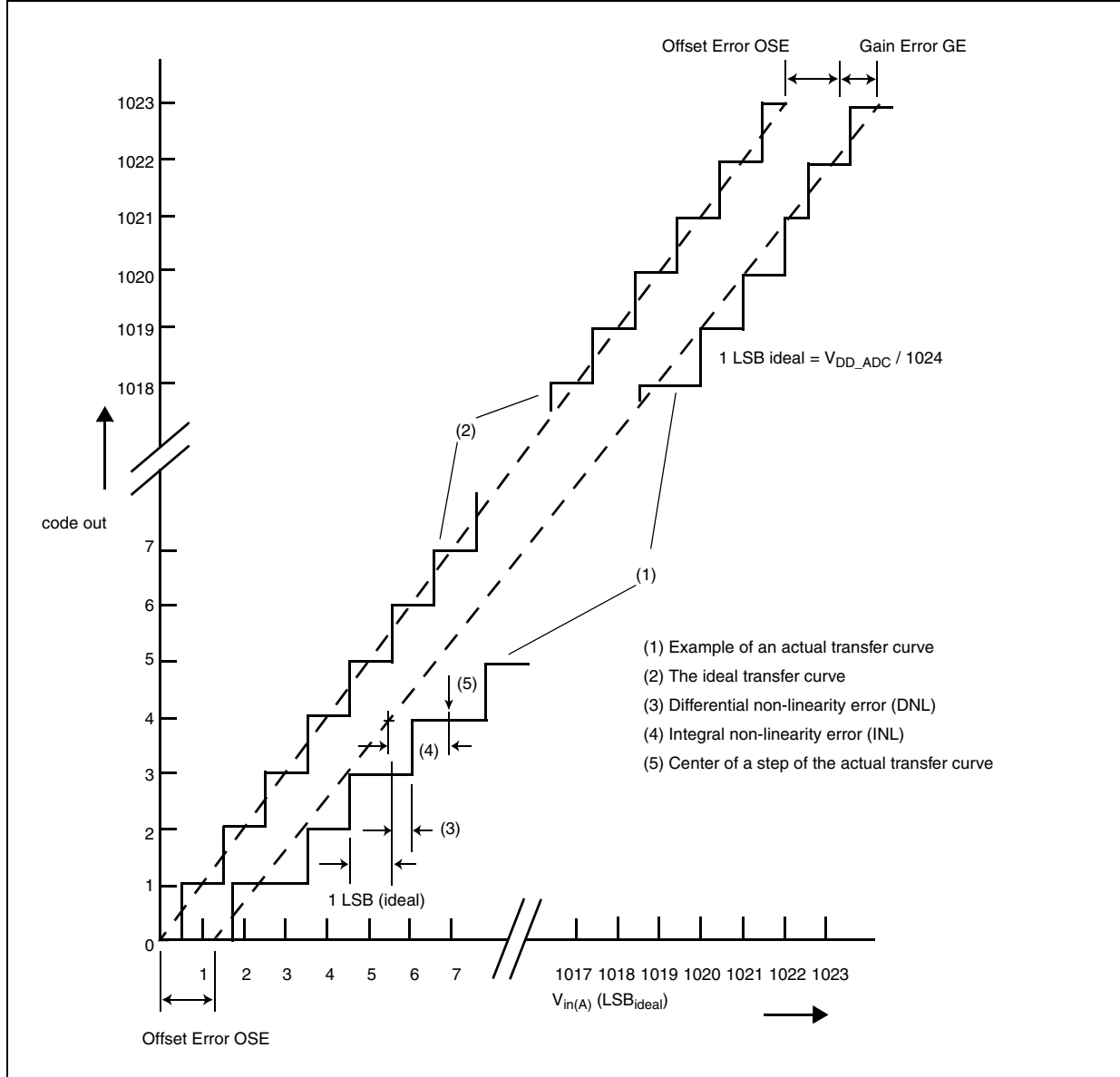


Figure 9. ADC characteristics and error definitions

#### 3.14.1 Input impedance and ADC accuracy

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; further, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to

## Electrical characteristics

be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance:  $C_S$  being substantially a switched capacitance, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with  $C_S$  equal to 3 pF, a resistance of 330 k $\Omega$  is obtained ( $R_{EQ} = 1 / (fc \times C_S)$ , where  $fc$  represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on  $C_S$ ) and the sum of  $R_S + R_F + R_L + R_{SW} + R_{AD}$ , the external circuit must be designed to respect the [Equation 4](#):

$$V_A \cdot \frac{R_S + R_F + R_L + R_{SW} + R_{AD}}{R_{EQ}} < \frac{1}{2} \text{LSB} \quad \text{Eqn. 4}$$

[Equation 4](#) generates a constraint for external network design, in particular on resistive path. Internal switch resistances ( $R_{SW}$  and  $R_{AD}$ ) can be neglected with respect to external resistances.

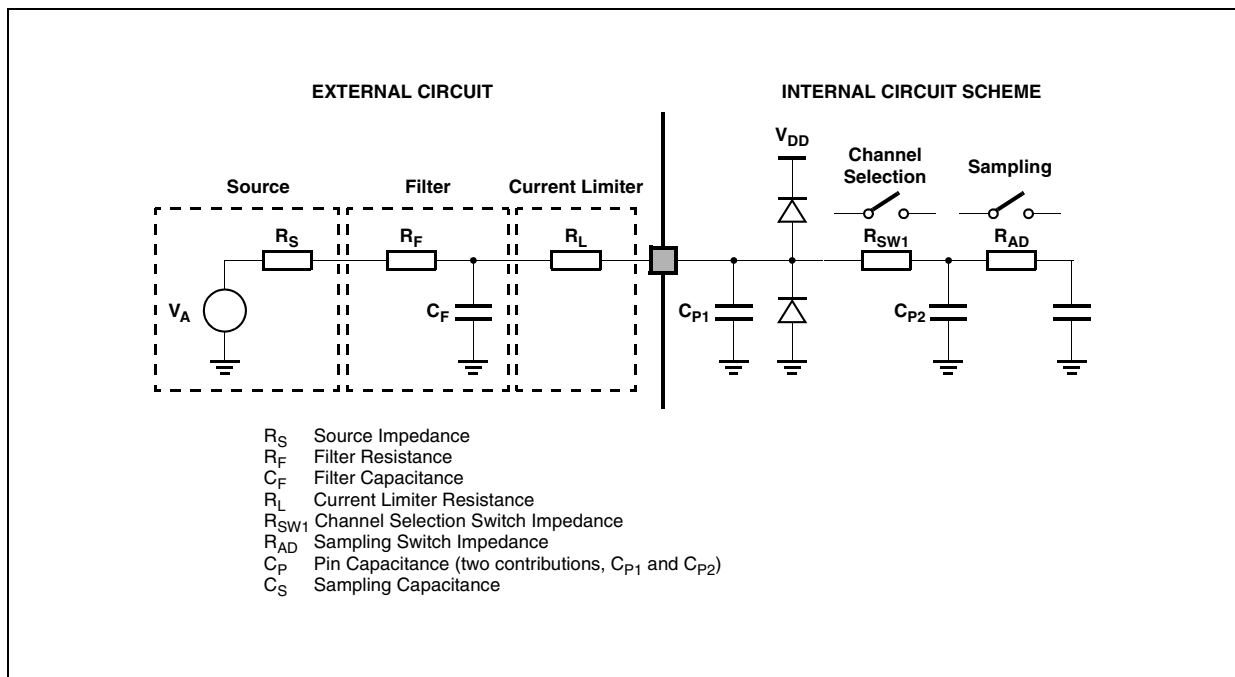
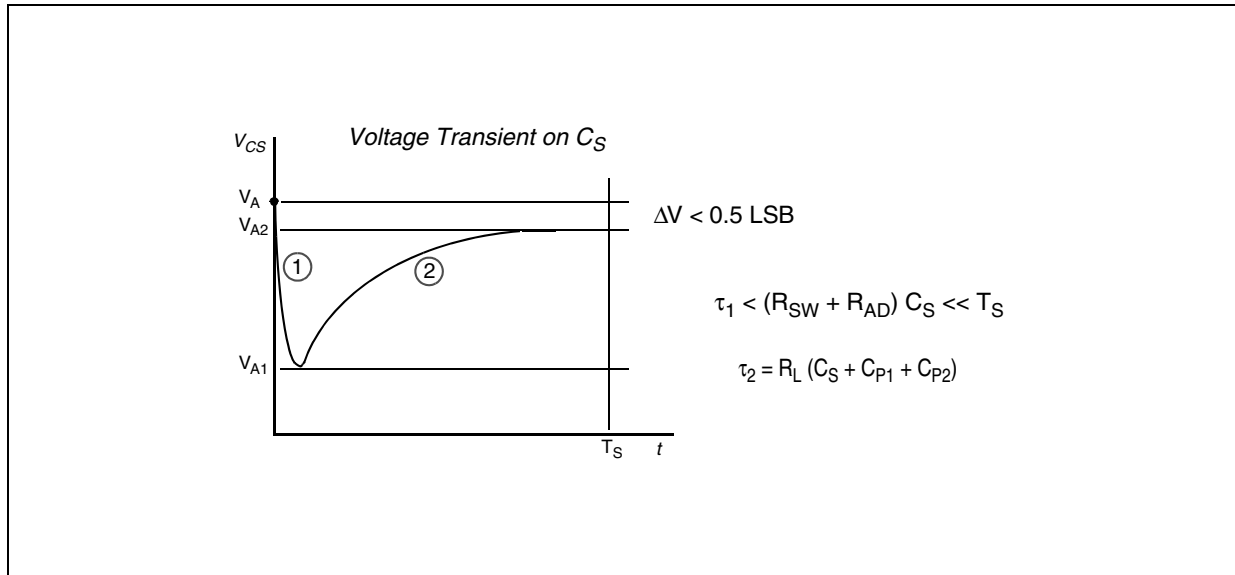


Figure 10. Input equivalent circuit

A second aspect involving the capacitance network shall be considered. Assuming the three capacitances  $C_F$ ,  $C_{P1}$  and  $C_{P2}$  are initially charged at the source voltage  $V_A$  (refer to the equivalent circuit reported in [Figure 10](#)): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).



**Figure 11. Transient behavior during sampling phase**

In particular two different transient periods can be distinguished:

- A first and quick charge transfer from the internal capacitance  $C_{P1}$  and  $C_{P2}$  to the sampling capacitance  $C_S$  occurs ( $C_S$  is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which  $C_{P2}$  is reported in parallel to  $C_{P1}$  (call  $C_P = C_{P1} + C_{P2}$ ), the two capacitances  $C_P$  and  $C_S$  are in series, and the time constant is

$$\tau_1 = (R_{SW} + R_{AD}) \cdot \frac{C_P \cdot C_S}{C_P + C_S} \quad \text{Eqn. 5}$$

Equation 5 can again be simplified considering only  $C_S$  as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time  $T_S$  is always much longer than the internal time constant:

$$\tau_1 < (R_{SW} + R_{AD}) \cdot C_S \ll T_S \quad \text{Eqn. 6}$$

The charge of  $C_{P1}$  and  $C_{P2}$  is redistributed also on  $C_S$ , determining a new value of the voltage  $V_{A1}$  on the capacitance according to Equation 7:

$$V_{A1} \cdot (C_S + C_{P1} + C_{P2}) = V_A \cdot (C_{P1} + C_{P2}) \quad \text{Eqn. 7}$$

- A second charge transfer involves also  $C_F$  (that is typically bigger than the on-chip capacitance) through the resistance  $R_L$ : again considering the worst case in which  $C_{P2}$  and  $C_S$  were in parallel to  $C_{P1}$  (since the time constant in reality would be faster), the time constant is:

$$\tau_2 < R_L \cdot (C_S + C_{P1} + C_{P2}) \quad \text{Eqn. 8}$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time  $T_S$ , a constraints on  $R_L$  sizing is obtained:

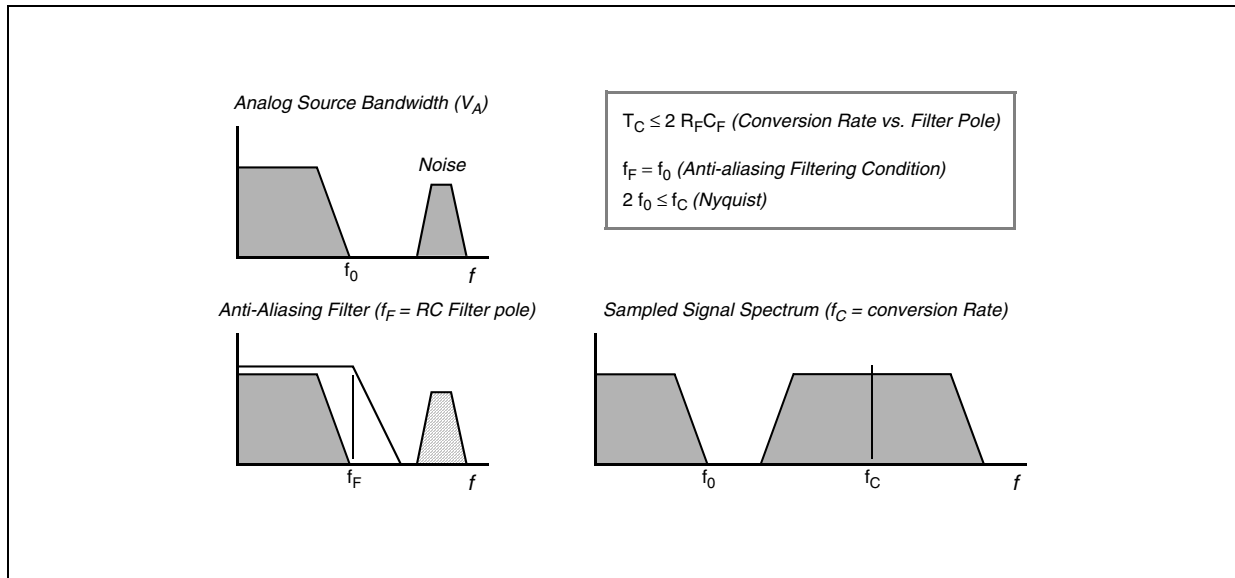
$$10 \cdot \tau_2 = 10 \cdot R_L \cdot (C_S + C_{P1} + C_{P2}) < T_S \quad \text{Eqn. 9}$$

## Electrical characteristics

Of course,  $R_L$  shall be sized also according to the current limitation constraints, in combination with  $R_S$  (source impedance) and  $R_F$  (filter resistance). Being  $C_F$  definitively bigger than  $C_{P1}$ ,  $C_{P2}$  and  $C_S$ , then the final voltage  $V_{A2}$  (at the end of the charge transfer transient) will be much higher than  $V_{A1}$ . Equation 10 must be respected (charge balance assuming now  $C_S$  already charged at  $V_{A1}$ ):

$$V_{A2} \cdot (C_S + C_{P1} + C_{P2} + C_F) = V_A \cdot C_F + V_{A1} \cdot (C_{P1} + C_{P2} + C_S) \quad \text{Eqn. 10}$$

The two transients above are not influenced by the voltage source that, due to the presence of the  $R_F C_F$  filter, is not able to provide the extra charge to compensate the voltage drop on  $C_S$  with respect to the ideal source  $V_A$ ; the time constant  $R_F C_F$  of the filter is very high with respect to the sampling time ( $T_S$ ). The filter is typically designed to act as anti-aliasing.



**Figure 12. Spectral representation of input signal**

Calling  $f_0$  the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter,  $f_F$ ), according to the Nyquist theorem the conversion rate  $f_C$  must be at least  $2f_0$ ; it means that the constant time of the filter is greater than or at least equal to twice the conversion period ( $T_C$ ). Again the conversion period  $T_C$  is longer than the sampling time  $T_S$ , which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter  $R_F C_F$  is definitively much higher than the sampling time  $T_S$ , so the charge level on  $C_S$  cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on  $C_S$ ; from the two charge balance equations above, it is simple to derive Equation 11 between the ideal and real sampled voltage on  $C_S$ :

$$\frac{V_A}{V_{A2}} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S} \quad \text{Eqn. 11}$$

From this formula, in the worst case (when  $V_A$  is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on  $C_F$  value:

$$C_F > 2048 \cdot C_S \quad \text{Eqn. 12}$$



## 3.14.2 ADC conversion characteristics

Table 21. ADC conversion characteristics

| Symbol                 |    | Parameter  | Conditions <sup>1</sup>  | Value |         |                  | Unit       |
|------------------------|----|--|--|-------|---------|------------------|------------|
|                        |    |  |  | Min   | Typ     | Max              |            |
| $f_{CK}$               | SR | ADC clock frequency<br>(depends on ADC configuration)<br>(The duty cycle depends on ADCClk <sup>2</sup> frequency) | —  | 1     | —       | 64               | MHz        |
| $f_s$                  | SR | Sampling frequency   | —  | —     | —       | 1.53             | MHz        |
| $t_{ADC\_S}$           | D  | Sample time <sup>3</sup>   | $f_{ADC} = 20$ MHz,<br>ADC_conf_sample_input = 17  | 500   | —       | —                | ns         |
|                        |    |  | $f_{ADC} = 9$ MHz,<br>INPSAMP = 255  | —     | —       | 28.2             | $\mu$ s    |
| $t_{ADC\_C}$           | P  | Conversion time <sup>4</sup>   | $f_{ADC} = 20$ MHz <sup>5</sup> ,<br>ADC_conf_comp = 3   | 500   | —       | —                | ns         |
| $C_S$ <sup>6</sup>     | D  | ADC input sampling capacitance   | —  | —     | —       | 2.5              | pF         |
| $C_{P1}$ <sup>6</sup>  | D  | ADC input pin capacitance 1  | —  | —     | —       | 0.8 <sup>7</sup> | pF         |
| $C_{P2}$ <sup>6</sup>  | D  | ADC input pin capacitance 2  | —  | —     | —       | 1                | pF         |
| $R_{SW1}$ <sup>6</sup> | D  | Internal resistance of analog source   | —  | —     | —       | 0.6              | k $\Omega$ |
| $R_{AD}$ <sup>6</sup>  | D  | Internal resistance of analog source   | —  | —     | —       | 2                | k $\Omega$ |
| $I_{INJ}$              | T  | Input current injection  | Current injection on one ADC input, different from the converted one. Remains within TUE specification | -5    | —       | 5                | mA         |
| INL                    | P  | Integral Non Linearity   | No overload  | -1.5  | —       | 1.5              | LSB        |
| DNL                    | P  | Differential Non Linearity   | No overload  | -1.0  | —       | 1.0              | LSB        |
| OFS                    | T  | Offset error   | —  | —     | $\pm 1$ | —                | LSB        |
| GNE                    | T  | Gain error   | —  | —     | $\pm 1$ | —                | LSB        |
| TUE                    | P  | Total unadjusted error without current injection   | —  | -3    | —       | 3                | LSB        |
| TUE                    | T  | Total unadjusted error with current injection  | —  | -3    | —       | 3                | LSB        |
| TUE                    | P  | Total unadjusted error   | —  | -3    | —       | 3                | LSB        |
| TUEP                   | CC | Total Unadjusted Error for precise channels, input only pins   | No overload  | -2    | —       | 2                | LSB        |
|                        |    |  | overload conditions on adjacent channel  | —     | —       | —                | LSB        |
| TUEX                   | CC | Total Unadjusted Error for extended channel,   | No overload  | -3    | —       | 3                | LSB        |
|                        |    |  | overload conditions on adjacent channel  | —     | —       | —                | LSB        |

## Electrical characteristics

- <sup>1</sup>  $V_{DD} = 3.3\text{ V to }3.6\text{ V}$ ,  $T_A = -40\text{ to }+125\text{ }^\circ\text{C}$ , unless otherwise specified and analog input voltage from  $V_{AGND}$  to  $V_{AREF}$
- <sup>2</sup> ADCClk clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.
- <sup>3</sup> During the sample time the input capacitance  $C_S$  can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within  $t_{ADC\_S}$ . After the end of the sample time  $t_{ADC\_S}$ , changes of the analog input voltage have no effect on the conversion result. Values for the sample clock  $t_{ADC\_S}$  depend on programming.
- <sup>4</sup> This parameter does not include the sample time  $t_{ADC\_S}$ , but only the time for determining the digital result and the time to load the result register with the conversion result.
- <sup>5</sup> 20 MHz ADC clock. Specific prescaler is programmed on MC\_PLL\_CLK to provide 20 MHz clock to the ADC.
- <sup>6</sup> See [Figure 10](#).
- <sup>7</sup> Does not include packaging and bonding capacitances

## 3.15 Temperature sensor electrical characteristics

Table 22. Temperature sensor electrical characteristics

| Symbol | C  | Parameter | Conditions                   | Value   |         |     | Unit                       |
|--------|----|-----------|------------------------------|---|---------|-----|----------------------------|
|        |    |           |                              | min   | typical | max |                            |
| —      | CC | C         | Temperature monitoring range | —   | —       | 150 | $^\circ\text{C}$           |
| —      | CC | C         | Sensitivity                  | —   | 5.14    | —   | $\text{mV}/^\circ\text{C}$ |
| —      | CC | C         | Accuracy                     | $T_J = -40\text{ to }25\text{ }^\circ\text{C}$  | —       | 10  | $^\circ\text{C}$           |
| —      | CC | C         |                              | $T_J = -25\text{ to }125\text{ }^\circ\text{C}$ | —       | 10  | $^\circ\text{C}$           |

## 3.16 Flash memory electrical characteristics

Table 23. Code flash program and erase specifications<sup>1</sup>

| Symbol       | Parameter                             | Min Value | Typical Value <sup>2</sup><br>(0 Cycles) | Initial Max <sup>3</sup><br>(100 Cycles) | Max <sup>4</sup><br>(100000 Cycles) | Unit          |
|--------------|---------------------------------------|-----------|--|--|-------------------------------------|---------------|
| $T_{DWPRG}$  | Double Word Program <sup>5</sup>      | —         | 22                                       | 50                                       | 500                                 | $\mu\text{s}$ |
| $T_{BKPRG}$  | Bank Program (512 KB) <sup>5, 6</sup> | —         | 1.45                                     | 1.65                                     | 33                                  | s             |
| $T_{ER8K}$   | Sector Erase (8KB)                    | —         | 0.2                                      | 0.4                                      | 5.0                                 | s             |
| $T_{ER16K}$  | Sector Erase (16KB)                   | —         | 0.3                                      | 0.5                                      | 5.0                                 | s             |
| $T_{ER32K}$  | Sector Erase (32KB)                   | —         | 0.3                                      | 0.6                                      | 5.0                                 | s             |
| $T_{ER64K}$  | Sector Erase (64KB)                   | —         | 0.6                                      | 0.9                                      | 5.0                                 | s             |
| $T_{ER128K}$ | Sector Erase (128KB)                  | —         | 0.8                                      | 1.3                                      | 7.5                                 | s             |
| $T_{ER512K}$ | Bank Erase (512KB)                    | —         | 4.8                                      | 7.6                                      | 55                                  | s             |
| $T_{PABT}$   | Program Abort Latency                 | —         | —  | 10                                       | 10                                  | $\mu\text{s}$ |
| $T_{EABT}$   | Erase Abort Latency                   | —         | —  | 30                                       | 30                                  | $\mu\text{s}$ |

Table 23. Code flash program and erase specifications<sup>1</sup>

| Symbol            | Parameter                      | Min Value | Typical Value <sup>2</sup><br>(0 Cycles) | Initial Max <sup>3</sup><br>(100 Cycles) | Max <sup>4</sup><br>(100000 Cycles) | Unit    |
|-------------------|--------------------------------|-----------|--|--|-------------------------------------|---------|
| T <sub>EABT</sub> | Erase Suspend Latency          | —         | —  | 30                                       | 30                                  | μs      |
| T <sub>EABT</sub> | Erase Suspend Request Rate     | 10        | —  | —  | —                                   | ms      |
| NER               | Endurance (8KB, 16KB sectors)  | 100       | —  | —  | —                                   | Kcycles |
|                   | Endurance (32KB, 64KB sectors) | 10        | —  | —  | —                                   |         |
|                   | Endurance (128KB sectors)      | 1         | —  | —  | —                                   |         |
| T <sub>DR</sub>   | Data Retention at 1K cycles    | 20        | —  | —  | —                                   | Years   |
|                   | Data Retention at 10K cycles   | 10        | —  | —  | —                                   |         |
|                   | Data Retention at 100K cycles  | 5         | —  | —  | —                                   |         |

<sup>1</sup> TBC = To be confirmed

<sup>2</sup> Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

<sup>3</sup> Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

<sup>4</sup> The maximum program & erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.

<sup>5</sup> Actual hardware programming times. This does not include software overhead.

<sup>6</sup> Typical Bank programming time assumes that all cells are programmed in a single pulse. In reality some cells will require more than one pulse, adding a small overhead to total bank programming time (see Initial Max column).

Table 24. Data flash program and erase specifications<sup>1</sup>

| Symbol              | Parameter                            | Min Value | Typical Value <sup>2</sup><br>(0 Cycles) | Initial Max <sup>3</sup><br>(100 Cycles) | Max <sup>4</sup><br>(100000 Cycles) | Unit           |
|---------------------|--------------------------------------|-----------|--|--|-------------------------------------|----------------|
| T <sub>DWPRG</sub>  | Word Program <sup>5</sup>            | —         | 30                                       | TBC                                      | TBC                                 | μs             |
| T <sub>BKPRG</sub>  | Bank Program (64 KB) <sup>5, 6</sup> | —         | 0.49                                     | TBC                                      | TBC                                 | s              |
| T <sub>ER16K</sub>  | Sector Erase (16KB)                  | —         | 0.7                                      | TBC                                      | TBC                                 | s              |
| T <sub>ER512K</sub> | Bank Erase (64KB)                    | —         | 1.9                                      | TBC                                      | TBC                                 | s              |
| T <sub>PABT</sub>   | Program Abort Latency                | —         | —  | 12                                       | 12                                  | μs             |
| T <sub>EABT</sub>   | Erase Abort Latency                  | —         | —  | 30                                       | 30                                  | μs             |
| T <sub>EABT</sub>   | Erase Suspend Latency                | —         | —  | 30                                       | 30                                  | μs             |
| T <sub>EABT</sub>   | Erase Suspend Request Rate           | 10        | —  | —  | —                                   | ms             |
| NER                 | Endurance (16KB sectors)             | 100       | —  | —  | —                                   | K cycles       |
| T <sub>DR</sub>     | Data Retention at 1K cycles          | 20        | —  | —  | —                                   | Years<br>@ 85C |
|                     | Data Retention at 10K cycles         | 10        | —  | —  | —                                   |                |
|                     | Data Retention at 100K cycles        | 1         | —  | —  | —                                   |                |

<sup>1</sup> TBC = To be confirmed

<sup>2</sup> Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.

## Electrical characteristics

- <sup>3</sup> Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.
- <sup>4</sup> The maximum program & erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.
- <sup>5</sup> Actual hardware programming times. This does not include software overhead.
- <sup>6</sup> Typical Bank programming time assumes that all cells are programmed in a single pulse. In reality some cells will require more than one pulse, adding a small overhead to total bank programming time (see Initial Max column).

**Table 25. Flash read access timing**

| Symbol | C | Parameter  | Conditions <sup>1</sup> | Max | Unit |
|--------|---|--|-------------------------|-----|------|
| Fmax   | C | Maximum working frequency for Code Flash at given number of WS in worst conditions | 2 wait states           | 66  | MHz  |
|        |   |  | 0 wait states           | 18  |      |
| Fmax   | C | Maximum working frequency for Data Flash at given number of WS in worst conditions | 8 wait states           | 66  | MHz  |

<sup>1</sup> VDD\_HV = 3.3 V ± 10%, TA = -40 to 125 °C, unless otherwise specified

## 3.17 NMI filter functional specification

**Table 26. NMI filter functional specification**

| Pulse Width                          | Value | Units |
|--------------------------------------|-------|-------|
| Maximum pulse width that is rejected | 40    | ns    |
| Minimum pulse width that is accepted | 205   | ns    |

The pulses shorter than “Maximum pulse width that is rejected” are blocked. The Pulses wider than “Minimum pulse width that is passed” are allowed. When the pulses lengths are between they may be blocked or passed. This is due to tolerance of analog circuit.

## 3.18 AC specifications

### 3.18.1 Pad AC specifications

Table 27 gives the AC electrical characteristics at 3.3 V ( $3.0\text{ V} < V_{\text{DD\_HV\_IO}} < 3.6\text{ V}$ ) operation.

Table 27. Pad AC specifications (3.3 V, INVUSRO[PAD3V5V] = 1)

| Pad    | Symbol       | Parameter  | Load drive (pF) | Rise/Fall <sup>1</sup> (ns) |     |     | Unit  |
|--------|--------------|--|-----------------|-----------------------------|-----|-----|-------|
|        |              |  |                 | Min                         | Typ | Max |       |
| Slow   | Tswitchon    | Propagation delay from vdd/2 of internal signal to Pchannel / Nchannel switch on condition | 25              | 3                           | —   | 40  | ns    |
|        |              |  | 50              | 3                           | —   | 40  | ns    |
|        |              |  | 100             | 3                           | —   | 40  | ns    |
|        |              |  | 200             | 3                           | —   | 40  | ns    |
|        | tr/tf        | Slope at rising/falling edge   | 25              | 4                           | —   | 40  | ns    |
|        |              |  | 50              | 6                           | —   | 50  | ns    |
|        |              |  | 100             | 10                          | —   | 75  | ns    |
|        |              |  | 200             | 14                          | —   | 100 | ns    |
|        | Freq         | Frequency of Operation   | 25              | —                           | —   | 4   | MHz   |
|        |              |  | 50              | —                           | —   | 2   | MHz   |
|        |              |  | 100             | —                           | —   | 2   | MHz   |
|        |              |  | 200             | —                           | —   | 2   | MHz   |
|        | Current Slew | Slew rate at rising edge of current  | 25              | 0.01                        | —   | 2   | mA/ns |
|        |              |  | 50              | 0.01                        | —   | 2   | mA/ns |
|        |              |  | 100             | 0.01                        | —   | 2   | mA/ns |
|        |              |  | 200             | 0.01                        | —   | 2   | mA/ns |
| Medium | Tswitchon    | Propagation delay from vdd/2 of internal signal to Pchannel / Nchannel switch on condition | 25              | 1                           | —   | 15  | ns    |
|        |              |  | 50              | 1                           | —   | 15  | ns    |
|        |              |  | 100             | 1                           | —   | 15  | ns    |
|        |              |  | 200             | 1                           | —   | 15  | ns    |
|        | tr/tf        | Slope at rising/falling edge   | 25              | 2                           | —   | 12  | ns    |
|        |              |  | 50              | 4                           | —   | 25  | ns    |
|        |              |  | 100             | 8                           | —   | 40  | ns    |
|        |              |  | 200             | 14                          | —   | 70  | ns    |
|        | Freq         | Frequency of Operation   | 25              | —                           | —   | 40  | MHz   |
|        |              |  | 50              | —                           | —   | 20  | MHz   |
|        |              |  | 100             | —                           | —   | 13  | MHz   |
|        |              |  | 200             | —                           | —   | 7   | MHz   |
|        | Current Slew | Slew rate at rising edge of current  | 25              | 2.5                         | —   | 7   | mA/ns |
|        |              |  | 50              | 2.5                         | —   | 7   | mA/ns |
|        |              |  | 100             | 2.5                         | —   | 7   | mA/ns |
|        |              |  | 200             | 2.5                         | —   | 7   | mA/ns |

Table 27. Pad AC specifications (3.3 V, INVUSRO[PAD3V5V] = 1)

| Pad       | Symbol         | Parameter  | Load drive (pF) | Rise/Fall <sup>1</sup> (ns) |     |     | Unit  |
|-----------|----------------|--|-----------------|-----------------------------|-----|-----|-------|
|           |                |  |                 | Min                         | Typ | Max |       |
| Fast      | Tswitchon      | Propagation delay from vdd/2 of internal signal to Pchannel / Nchannel switch on condition | 25              | 1                           | —   | 6   | ns    |
|           |                |  | 50              | 1                           | —   | 6   | ns    |
|           |                |  | 100             | 1                           | —   | 6   | ns    |
|           |                |  | 200             | 1                           | —   | 6   | ns    |
|           | tr/tf          | Slope at rising/falling edge   | 25              | 1                           | —   | 4   | ns    |
|           |                |  | 50              | 1.5                         | —   | 7   | ns    |
|           |                |  | 100             | 3                           | —   | 12  | ns    |
|           |                |  | 200             | 5                           | —   | 18  | ns    |
|           | Freq           | Frequency of Operation   | 25              | —                           | —   | 72  | MHz   |
|           |                |  | 50              | —                           | —   | 55  | MHz   |
|           |                |  | 100             | —                           | —   | 40  | MHz   |
|           |                |  | 200             | —                           | —   | 25  | MHz   |
|           | Current Slew   | Slew rate at rising edge of current  | 25              | 3                           | —   | 40  | mA/ns |
|           |                |  | 50              | 3                           | —   | 40  | mA/ns |
|           |                |  | 100             | 3                           | —   | 40  | mA/ns |
|           |                |  | 200             | 3                           | —   | 40  | mA/ns |
| Symmetric | Tswitchon      | Propagation delay from vdd/2 of internal signal to Pchannel / Nchannel switch on condition | 25              | 1                           | —   | 8   | ns    |
|           | tr/tf          | Slope at rising/falling edge   | 25              | 1                           | —   | 5   | ns    |
|           | TRise/TFall    | Delay at rising/falling edge   | 25              | 3                           | —   | 12  | ns    |
|           | ITRise - TFall | Delay between rising and falling edge  | 25              | 0.05                        | —   | 1   | ns    |
|           | Freq           | Frequency of Operation   | 25              | —                           | —   | 50  | MHz   |
|           | Current Slew   | Slew rate at rising edge of current  | 25              | 3                           | —   | 25  | mA/ns |

<sup>1</sup> Slope at rising/falling edge

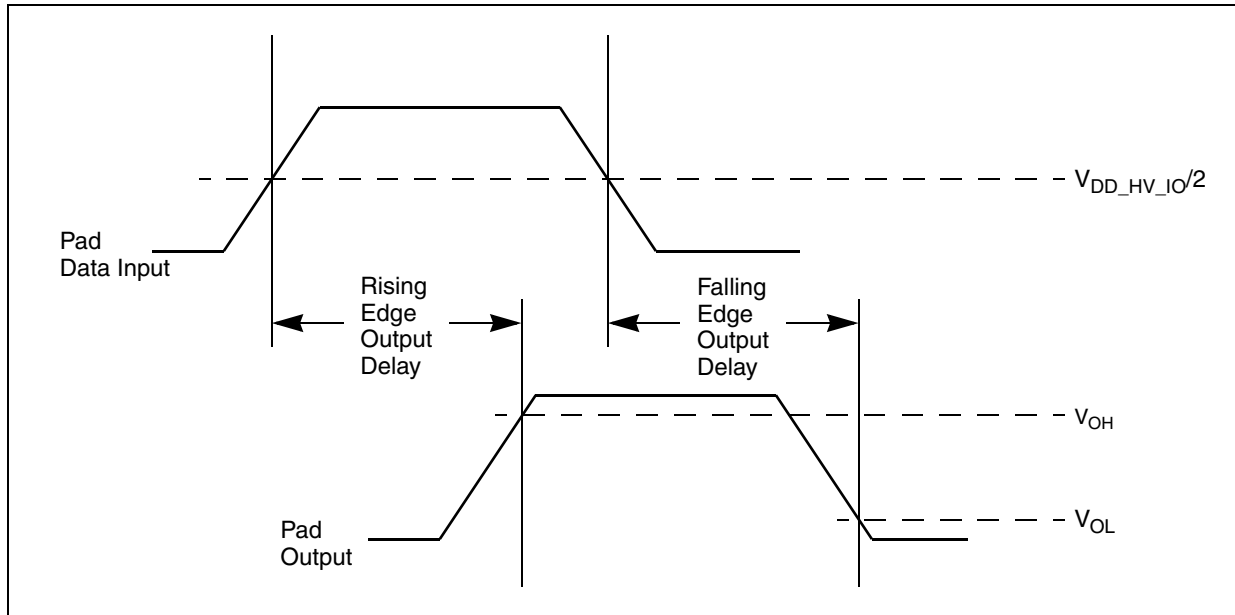


Figure 13. Pad output delay

## 3.19 AC timing characteristics

### 3.19.1 Generic timing diagrams

The generic timing diagrams in [Figure 14](#) and [Figure 15](#) apply to all I/O pins with pad types fast, slow and medium. See [Section 2.2, “Signal descriptions”](#) for the pad type for each pin.

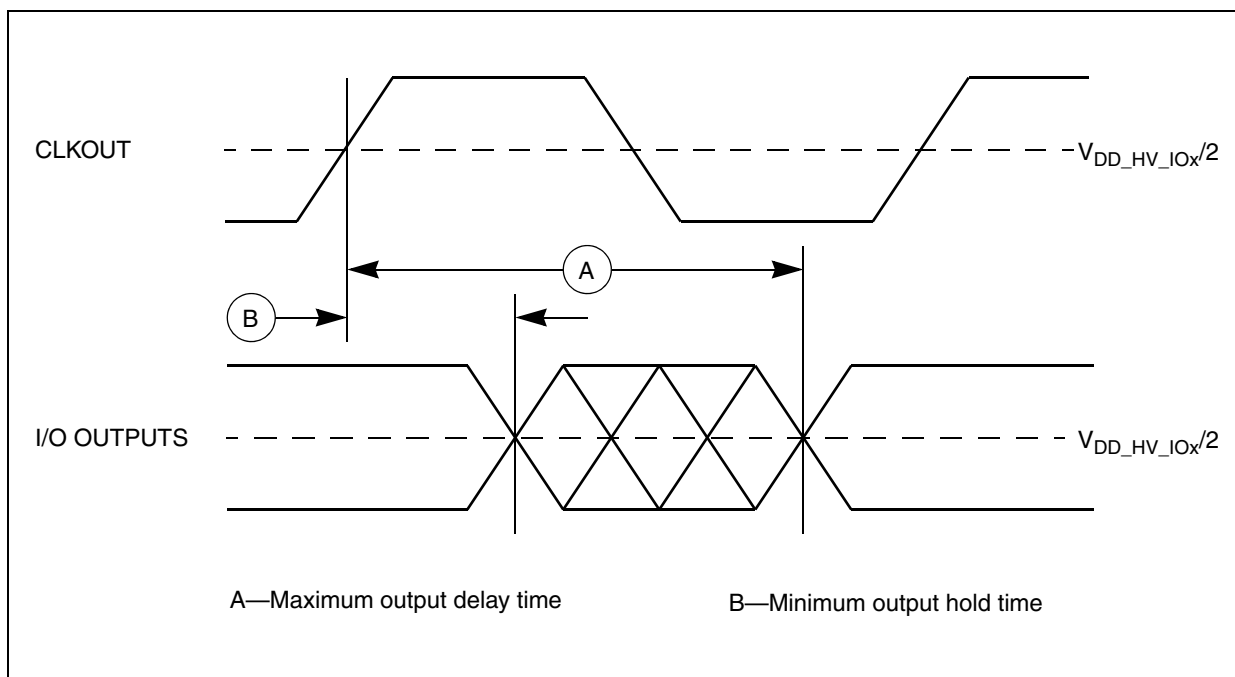


Figure 14. Generic output delay/hold timing

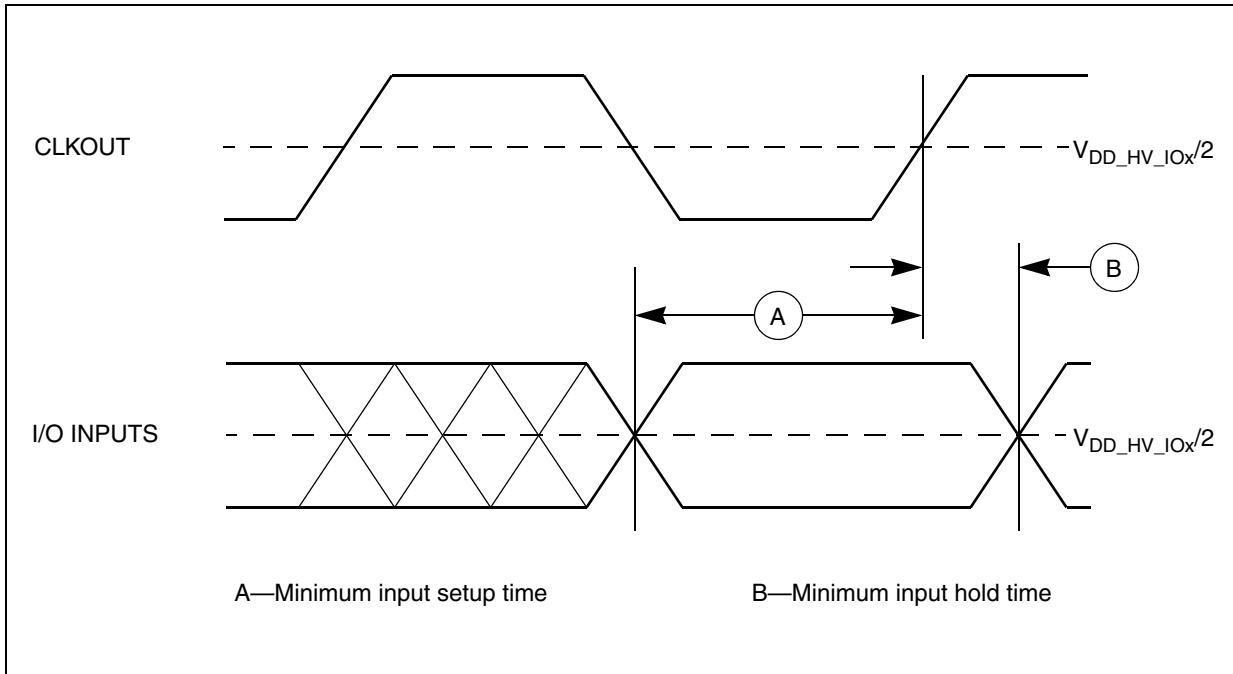


Figure 15. Generic Input setup/hold timing



### 3.19.2 $\overline{\text{RESET}}$ pin characteristics

The MPC5604E implements a dedicated bidirectional  $\overline{\text{RESET}}$  pin.

Figure 16. Start-up reset requirements

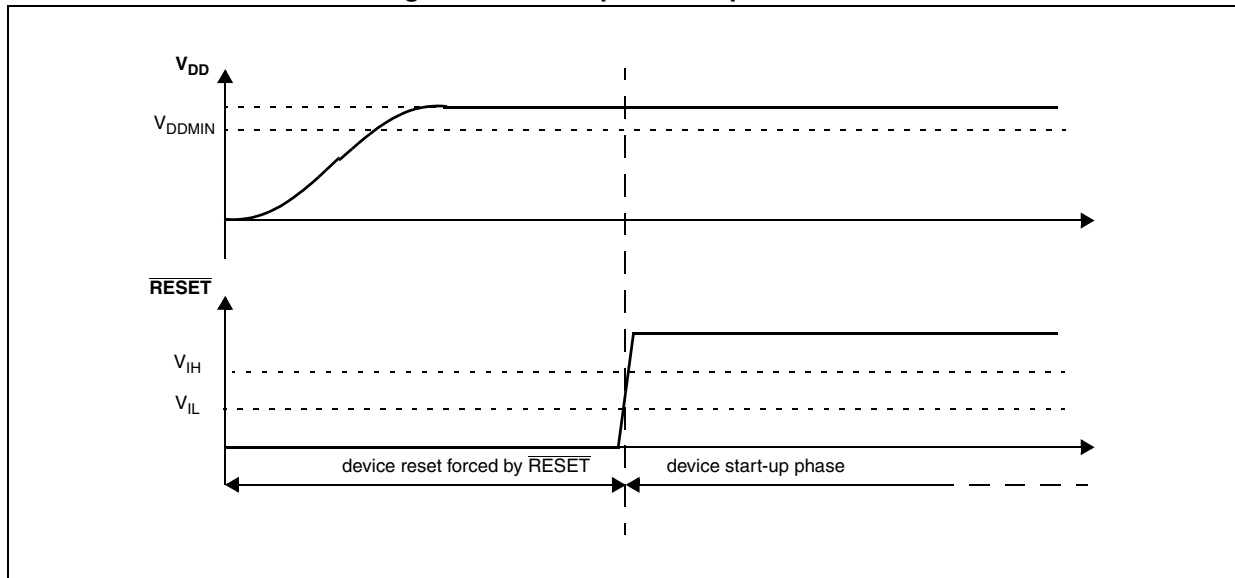


Figure 17. Noise filtering on reset signal

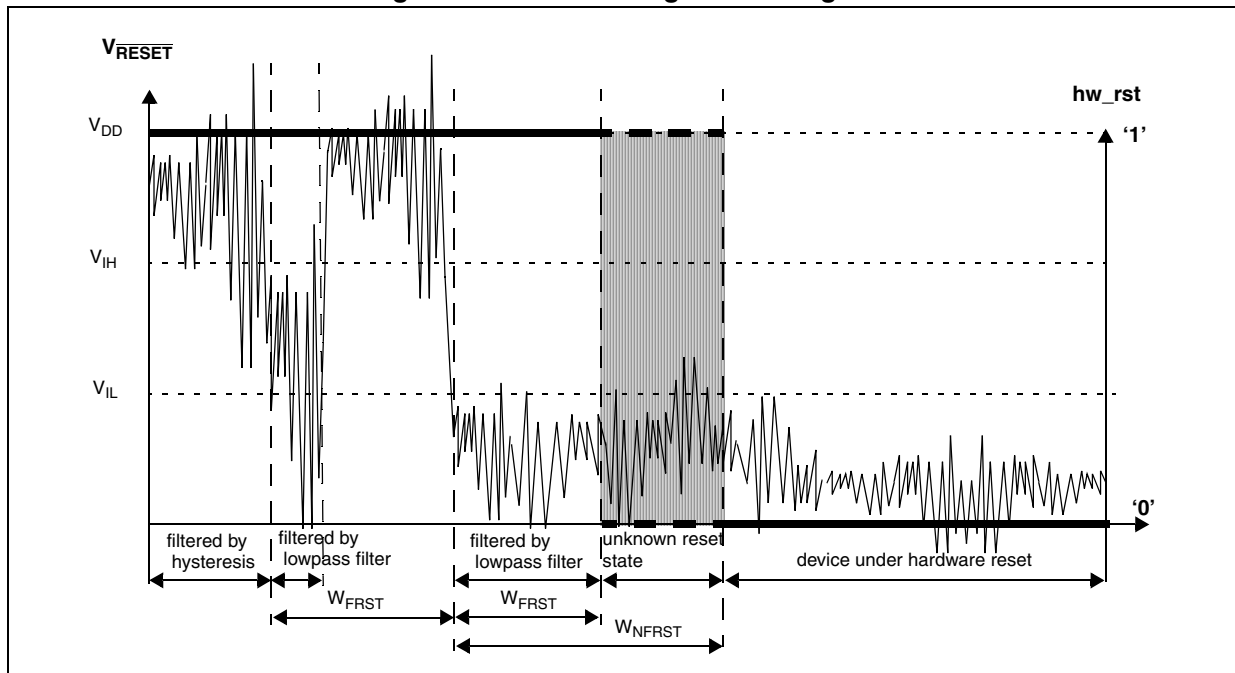


Table 28.  $\overline{\text{RESET}}$  electrical characteristics

| Symbol             | C  | Parameter | Conditions <sup>1</sup>  | Value <sup>2</sup>                                       |     |     | Unit |    |
|--------------------|----|-----------|--|--|-----|-----|------|----|
|                    |    |           |  | Min  | Typ | Max |      |    |
| V <sub>IH</sub>    | SR | P         | Input High Level CMOS (Schmitt Trigger)                                | —  | —   | —   | V    |    |
| V <sub>IL</sub>    | SR | P         | Input low Level CMOS (Schmitt Trigger)                                 | —  | —   | —   | V    |    |
| V <sub>HYS</sub>   | CC | C         | Input hysteresis CMOS (Schmitt Trigger)                                | —  | —   | —   | V    |    |
| V <sub>OL</sub>    | CC | P         | Output low level   | Push Pull, I <sub>OL</sub> = 3 mA,                       | —   | —   | V    |    |
| T <sub>tr</sub>    | CC | D         | Output transition time output pin <sup>3</sup><br>MEDIUM configuration | C <sub>L</sub> = 25 pF,<br>V <sub>DD</sub> = 3.3 V ± 10% | —   | —   | 12   | ns |
|                    |    |           | C <sub>L</sub> = 50 pF,<br>V <sub>DD</sub> = 3.3 V ± 10%               | —  | —   | 25  |      |    |
|                    |    |           | C <sub>L</sub> = 100 pF,<br>V <sub>DD</sub> = 3.3 V ± 10%              | —  | —   | 40  |      |    |
| W <sub>FRST</sub>  | SR | P         | $\overline{\text{RESET}}$ input filtered pulse                         | —  | —   | —   | ns   |    |
| W <sub>NFRST</sub> | SR | P         | $\overline{\text{RESET}}$ input not filtered pulse                     | —  | —   | —   | ns   |    |
| I <sub>WPU</sub>   | CC | P         | Weak pull-up current absolute value                                    | V <sub>DD</sub> = 3.3 V ± 10%                            | 10  | —   | 150  | μA |

<sup>1</sup> V<sub>DD</sub> = 3.3 V ± 10% / 5.0 V ± 10%, T<sub>A</sub> = -40 to 125 °C, unless otherwise specified

<sup>2</sup> All values need to be confirmed during device validation.

<sup>3</sup> C<sub>L</sub> includes device and package capacitance (C<sub>PKG</sub> < 5 pF).

### 3.19.3 Nexus and JTAG timing

Table 29. Nexus debug port timing<sup>1</sup>

| No. | Symbol              | C  | Parameter | Value   |      |     | Unit |                   |
|-----|---------------------|----|-----------|---|------|-----|------|-------------------|
|     |                     |    |           | Min   | Typ  | Max |      |                   |
| 1   | t <sub>MCYC</sub>   | CC | D         | MCKO Cycle Time   | 2    | —   | 8    | t <sub>CYC</sub>  |
| 2A  | t <sub>MCYCP</sub>  | CC | D         | MCKO cycle period   | 15   | —   | —    | ns                |
| 2B  | t <sub>MDC</sub>    | CC | D         | MCKO duty cycle   | 48   | —   | 52   | %                 |
| 3   | t <sub>MDOV</sub>   | CC | D         | MCKO low to MDO data valid <sup>2</sup>                       | -0.1 | —   | 0.22 | t <sub>MCYC</sub> |
| 4   | t <sub>MSEOV</sub>  | CC | D         | MCKO low to $\overline{\text{MSEO}}$ data valid <sup>2</sup>  | -0.1 | —   | 0.22 | t <sub>MCYC</sub> |
| 5   | t <sub>EVT OV</sub> | CC | D         | MCKO low to $\overline{\text{EVT O}}$ data valid <sup>2</sup> | -0.1 | —   | 0.22 | t <sub>MCYC</sub> |
| 6   | t <sub>TCYC</sub>   | CC | D         | TCK cycle time  | 50   | —   | —    | ns                |
| 7   | t <sub>TDC</sub>    | CC | D         | TCK Duty Cycle  | 40   | —   | 60   | %                 |

Table 29. Nexus debug port timing<sup>1</sup> (continued)

| No. | Symbol      | C  | Parameter | Value                       |     |     | Unit |            |
|-----|-------------|----|-----------|-----------------------------|-----|-----|------|------------|
|     |             |    |           | Min                         | Typ | Max |      |            |
| 8   | $t_{NTDIS}$ | CC | D         | TDI data setup time         | 0.2 | —   | —    | $t_{TCYC}$ |
|     | $t_{NTMSS}$ | CC | D         | TMS data setup time         | 0.2 | —   | —    | $t_{TCYC}$ |
| 9   | $t_{NTDIH}$ | CC | D         | TDI data hold time          | 0.1 | —   | —    | $t_{TCYC}$ |
|     | $t_{NTMSH}$ | CC | D         | TMS data hold time          | 0.1 | —   | —    | $t_{TCYC}$ |
| 10  | $t_{TDOV}$  | CC | D         | TCK low to TDO data valid   | —   | —   | 25   | ns         |
| 11  | $t_{TDOV}$  | CC | D         | TCK low to TDO data invalid | 0.1 | —   | —    | $t_{TCYC}$ |

<sup>1</sup> All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal.

<sup>2</sup> MDO,  $\overline{\text{MSEO}}$ , and  $\overline{\text{EVT0}}$  data is held valid until next MCKO low cycle.

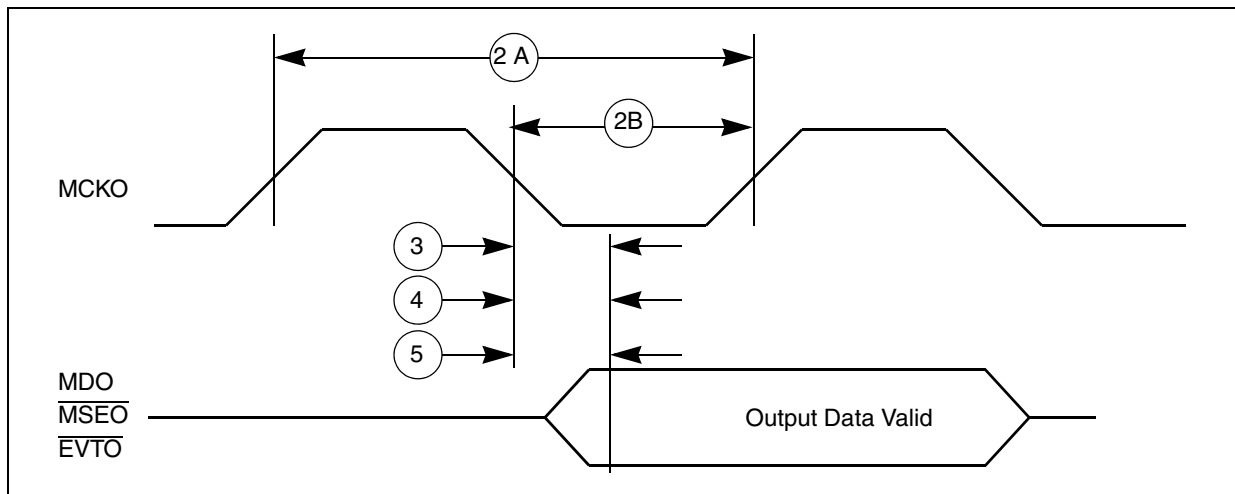


Figure 18. Nexus output timing

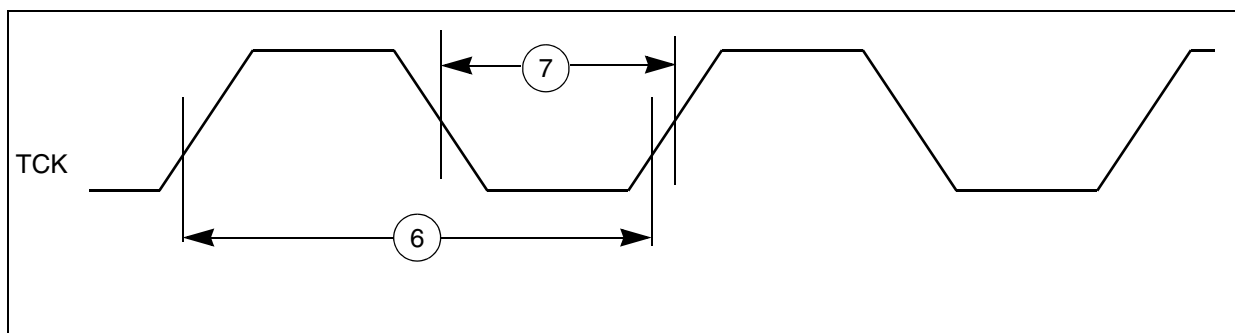


Figure 19. Nexus event trigger and test clock timings

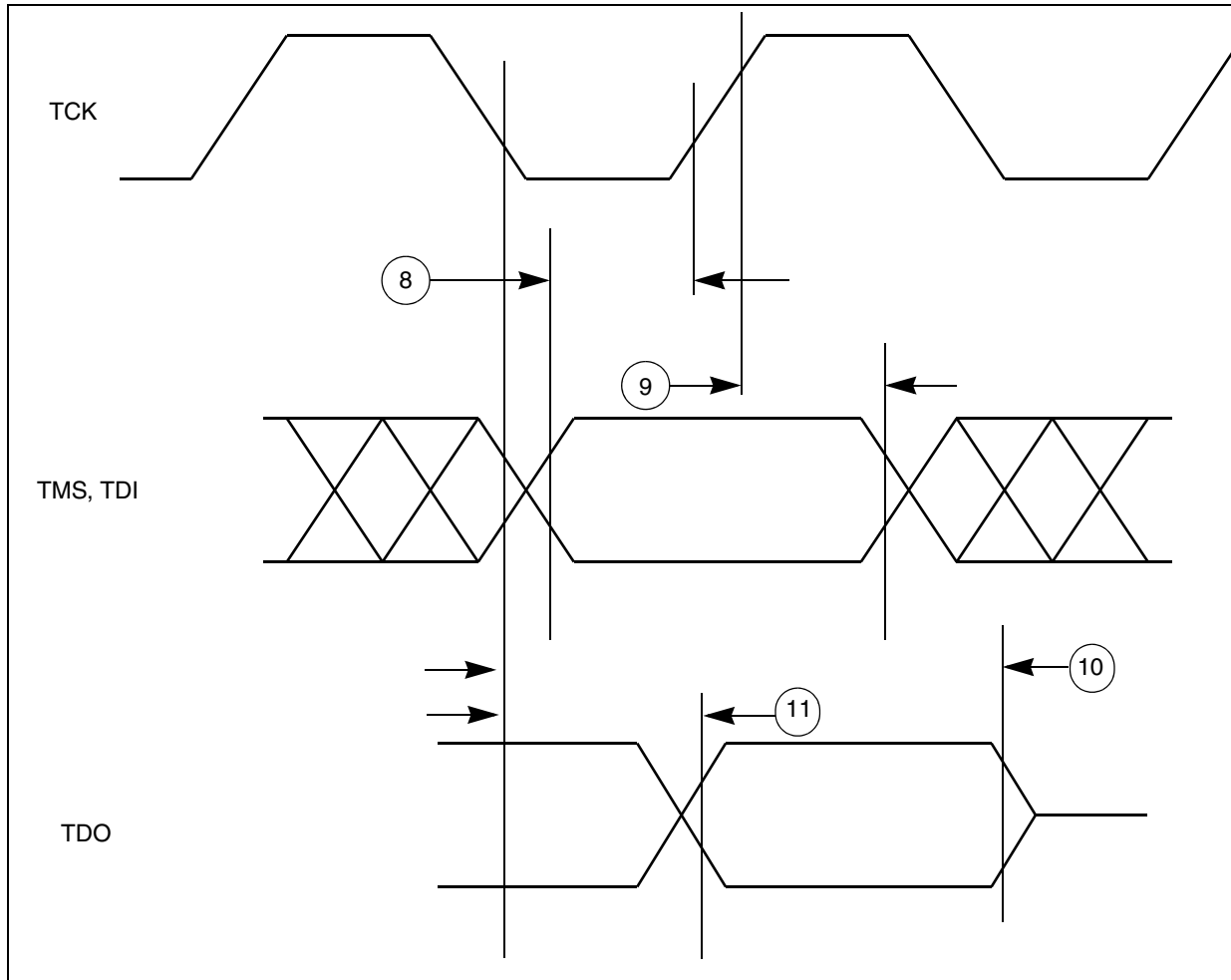


Figure 20. Nexus TDI, TMS, TDO Timing

### 3.19.4 GPIO timing

The GPIO specifications for setup time and output valid relative to CLKOUT are the same for all pins on the device regardless of the primary pin function.

Table 30. GPIO Timing

| No. | Symbol             | Characteristic  | Min. | Max. | Unit             |
|-----|--------------------|-----------------|------|------|------------------|
| 1   | $t_{\text{READ}}$  | GPIO Read Time  | 5    | —    | $t_{\text{CYC}}$ |
| 2   | $t_{\text{WRITE}}$ | GPIO Write Time | 6    | —    | $t_{\text{CYC}}$ |

### 3.19.5 External interrupt timing (IRQ pin)

Table 31. External interrupt timing<sup>1</sup>

| No. | Symbol     | C  | D | Parameter                          | Conditions | Min     | Max | Unit      |
|-----|------------|----|---|------------------------------------|------------|---------|-----|-----------|
| 1   | $t_{IPWL}$ | CC | D | IRQ pulse width low                | —          | 4       | —   | $t_{CYC}$ |
| 2   | $t_{IPWH}$ | CC | D | IRQ pulse width high               | —          | 4       | —   | $t_{CYC}$ |
| 3   | $t_{ICYC}$ | CC | D | IRQ edge to edge time <sup>2</sup> | —          | $4+N^3$ | —   | $t_{CYC}$ |

<sup>1</sup> IRQ timing specified at  $f_{SYS} = 64$  MHz and  $V_{DD\_HV\_IOx} = 3.0$  V,  $T_A = T_L$  to  $T_H$ , and  $CL = 200$  pF with  $SRC = 0b00$ .

<sup>2</sup> Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

<sup>3</sup>  $N =$  ISR time to clear the flag

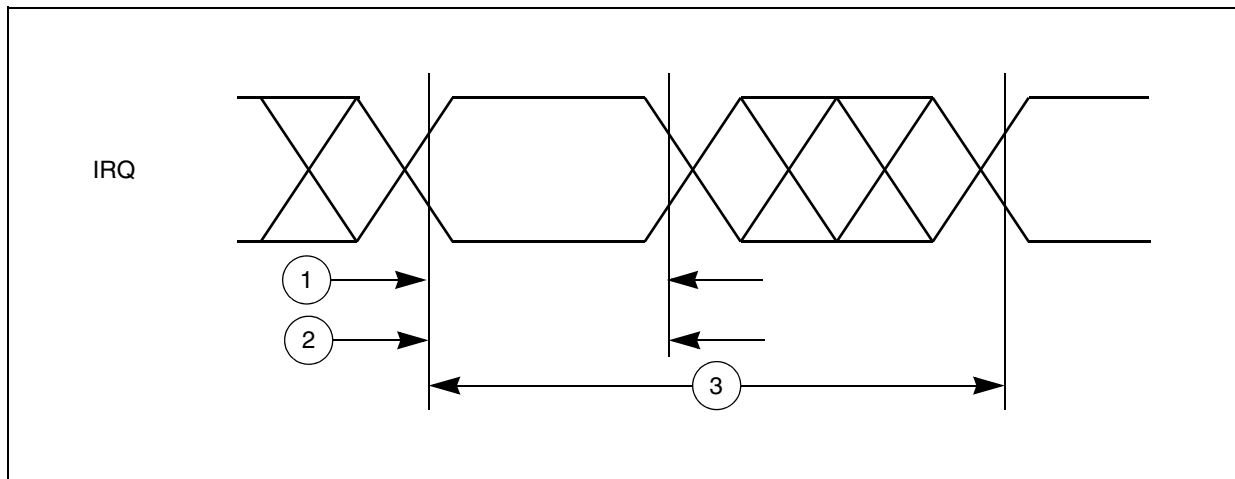


Figure 21. External interrupt timing

### 3.19.6 FlexCAN timing

Table 32. FlexCAN timing<sup>1</sup>

| Num | Characteristic  | Symbol      | Min. Value | Max. Value | Unit |
|-----|---|-------------|------------|------------|------|
| 1   | CTNX Output Valid after CLKOUT Rising Edge (Output Delay) | $t_{CANOV}$ | —          | 26.0       | ns   |
| 2   | CNRX Input Valid to CLKOUT Rising Edge (Setup Time)       | $t_{CANSU}$ | —          | 9.8        | ns   |

<sup>1</sup> FlexCAN timing specified at  $f_{SYS} = 64$  MHz,  $V_{DD} = 1.35$  V to  $1.65$  V,  $VDDEH = 3.0$  V to  $5.5$  V,  $VRC33$  and  $VDDPLL = 3.0$  V to  $3.6$  V,  $T_A = T_L$  to  $T_H$ , and  $CL = 50$  pF with  $SRC = 0b00$ .

### 3.19.7 LINFlex timing

Minimum design target for interface frequency is 2 MBit/s.

## 3.19.8 DSPI timing

Table 33. DSPI timing

| No. | Symbol            | C  | Parameter | Conditions                     | Min  | Max                    | Unit                   |    |
|-----|-------------------|----|-----------|--------------------------------|--|------------------------|------------------------|----|
| 1   | t <sub>SCK</sub>  | CC | D         | DSPI cycle time                | Master (MTFE = 0)                                  | 62.5                   | —                      | ns |
|     |                   |    |           |                                | Slave (MTFE = 0)                                   | 128                    | —                      |    |
|     |                   |    |           |                                | Master (MTFE = 1, CPHA=1)                          | 31.25                  | —                      |    |
| 2   | t <sub>CSC</sub>  | CC | D         | CS to SCK delay                | —  | 16                     | —                      | ns |
| 3   | t <sub>ASC</sub>  | CC | D         | After SCK delay                | —  | 16                     | —                      | ns |
| 4   | t <sub>SDC</sub>  | CC | D         | SCK duty cycle                 | —  | 0.4 * t <sub>SCK</sub> | 0.6 * t <sub>SCK</sub> | ns |
| 5   | t <sub>A</sub>    | CC | D         | Slave access time              | $\overline{SS}$ active to SOUT valid               | —                      | 40                     | ns |
| 6   | t <sub>DIS</sub>  | CC | D         | Slave SOUT disable time        | $\overline{SS}$ inactive to SOUT High-Z or invalid | —                      | 10                     | ns |
| 7   | t <sub>PCSC</sub> | CC | D         | PCSx to $\overline{PCSS}$ time | —  | 13                     | —                      | ns |
| 8   | t <sub>PASC</sub> | CC | D         | $\overline{PCSS}$ to PCSx time | —  | 13                     | —                      | ns |
| 9   | t <sub>SUI</sub>  | CC | D         | Data setup time for inputs     | Master (MTFE = 0)                                  | 12                     | —                      | ns |
|     |                   |    |           |                                | Slave  | 2                      | —                      |    |
|     |                   |    |           |                                | Master (MTFE = 1, CPHA = 0)                        | NA <sup>1</sup>        |                        |    |
|     |                   |    |           |                                | Master (MTFE = 1, CPHA = 1)                        | 12                     | —                      |    |
| 10  | t <sub>HI</sub>   | CC | D         | Data hold time for inputs      | Master (MTFE = 0)                                  | -5                     | —                      | ns |
|     |                   |    |           |                                | Slave  | 4                      | —                      |    |
|     |                   |    |           |                                | Master (MTFE = 1, CPHA = 0)                        | NA <sup>1</sup>        |                        |    |
|     |                   |    |           |                                | Master (MTFE = 1, CPHA = 1)                        | -5                     | —                      |    |
| 11  | t <sub>SUO</sub>  | CC | D         | Data valid (after SCK edge)    | Master (MTFE = 0)                                  | —                      | 4                      | ns |
|     |                   |    |           |                                | Slave  | —                      | 33                     |    |
|     |                   |    |           |                                | Master (MTFE = 1, CPHA = 0)                        | NA <sup>1</sup>        |                        |    |
|     |                   |    |           |                                | Master (MTFE = 1, CPHA = 1)                        | —                      | 11                     |    |
| 12  | t <sub>HO</sub>   | CC | D         | Data hold time for outputs     | Master (MTFE = 0)                                  | -2                     | —                      | ns |
|     |                   |    |           |                                | Slave  | 6                      | —                      |    |
|     |                   |    |           |                                | Master (MTFE = 1, CPHA = 0)                        | NA <sup>1</sup>        |                        |    |
|     |                   |    |           |                                | Master (MTFE = 1, CPHA = 1)                        | -2                     | —                      |    |

<sup>1</sup> This mode is not feasible at 32 MHz.

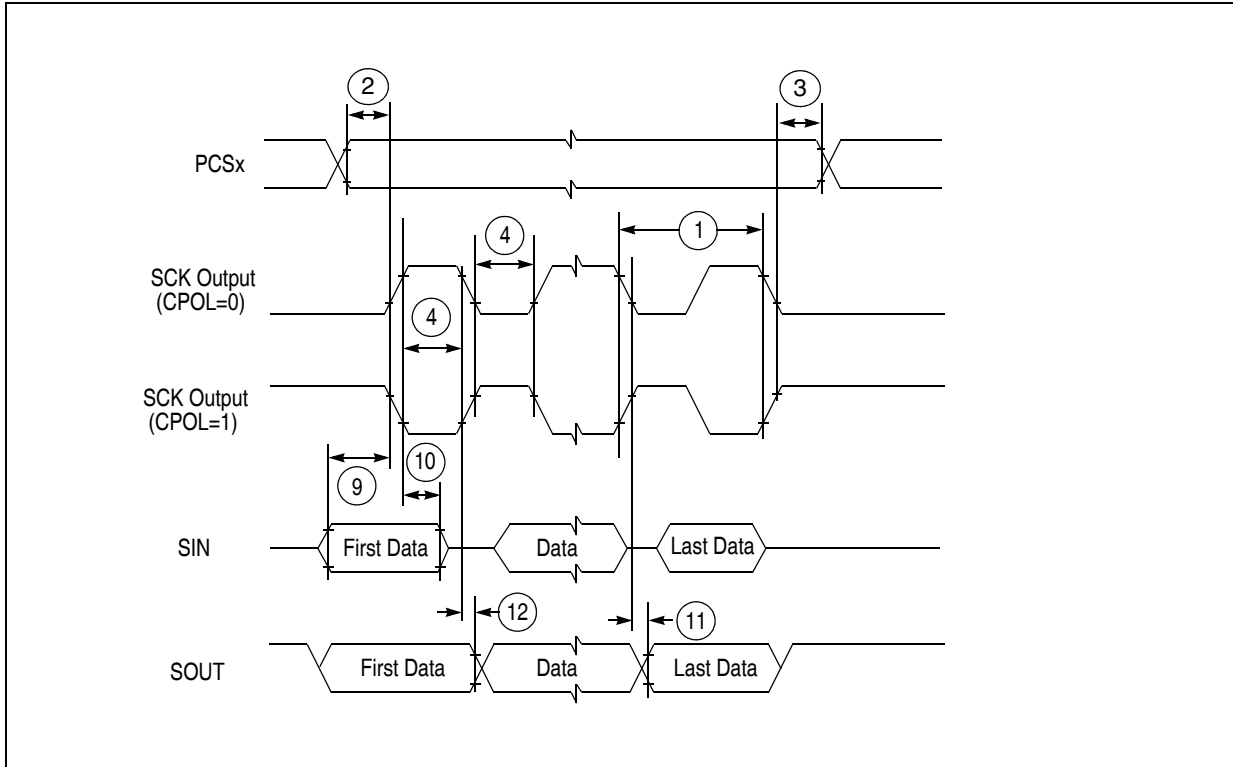


Figure 22. DSPI classic SPI timing — Master, CPHA = 0

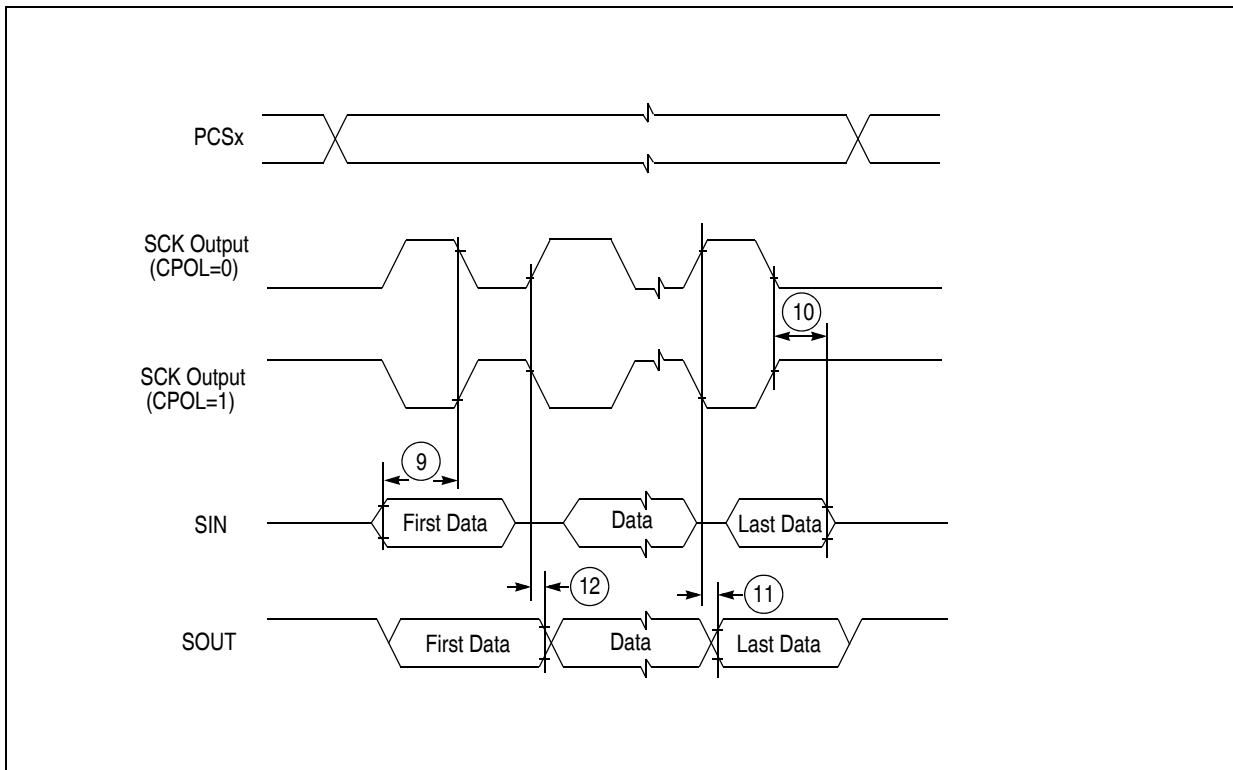


Figure 23. DSPI classic SPI timing — Master, CPHA = 1

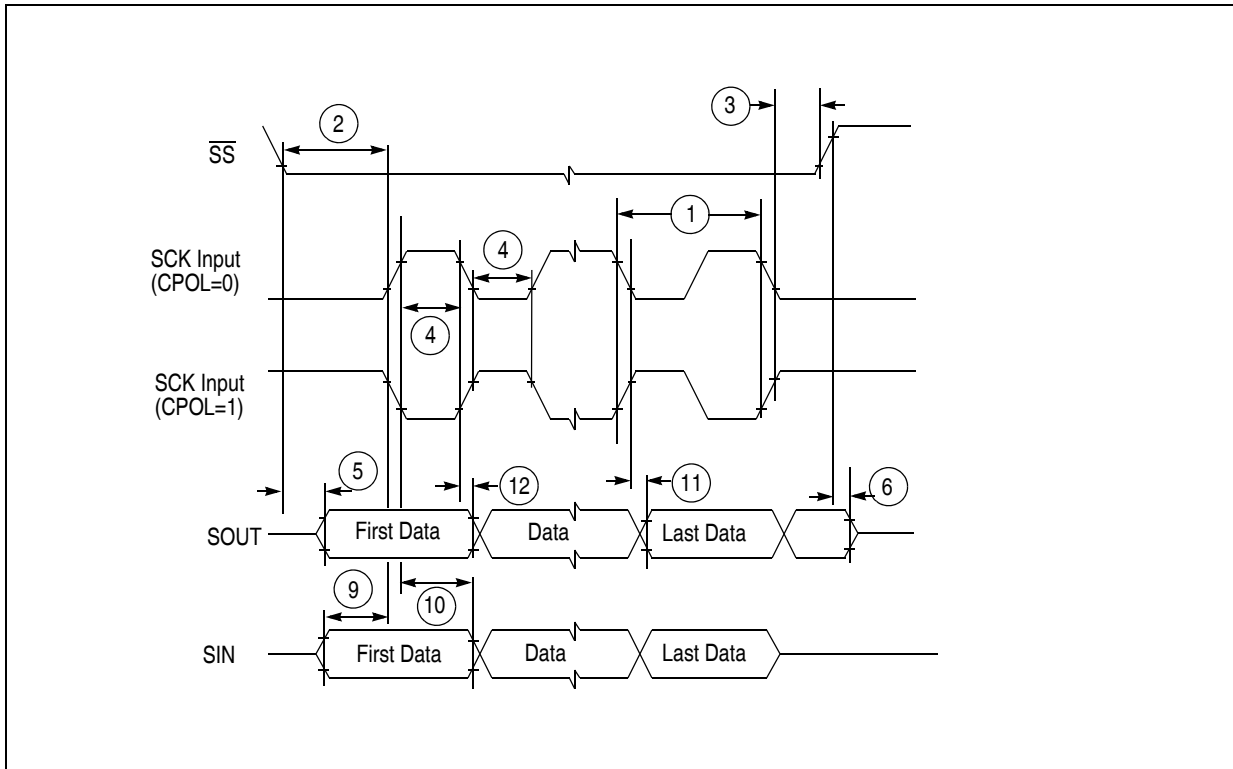


Figure 24. DSPI classic SPI timing — Slave, CPHA = 0

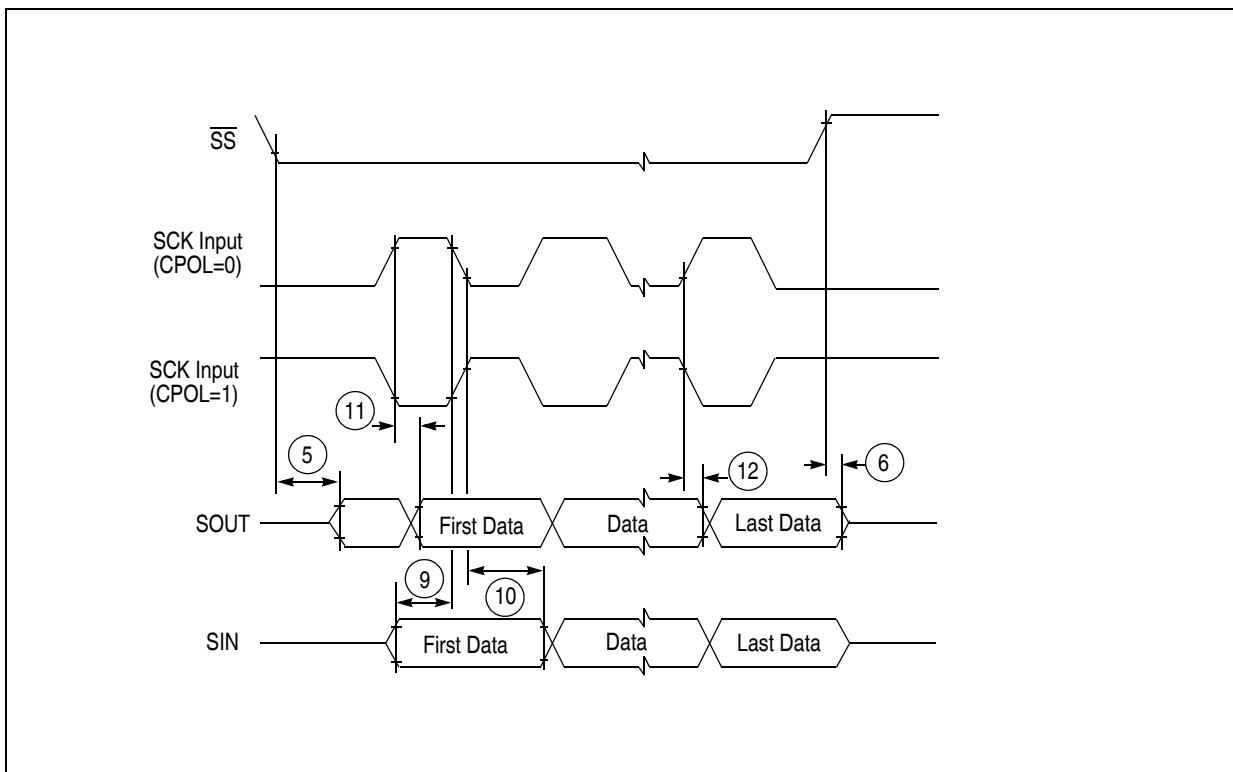


Figure 25. DSPI classic SPI timing — Slave, CPHA = 1



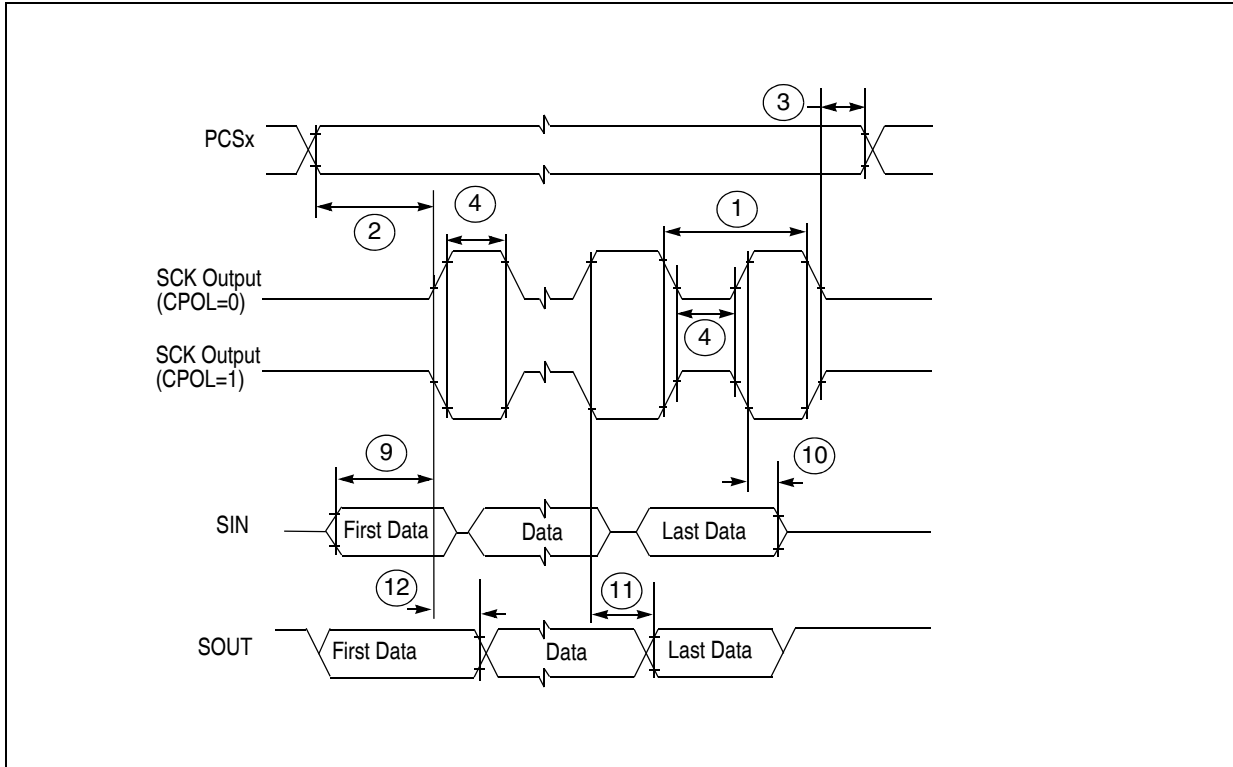


Figure 26. DSPI modified transfer format timing — Master, CPHA = 0

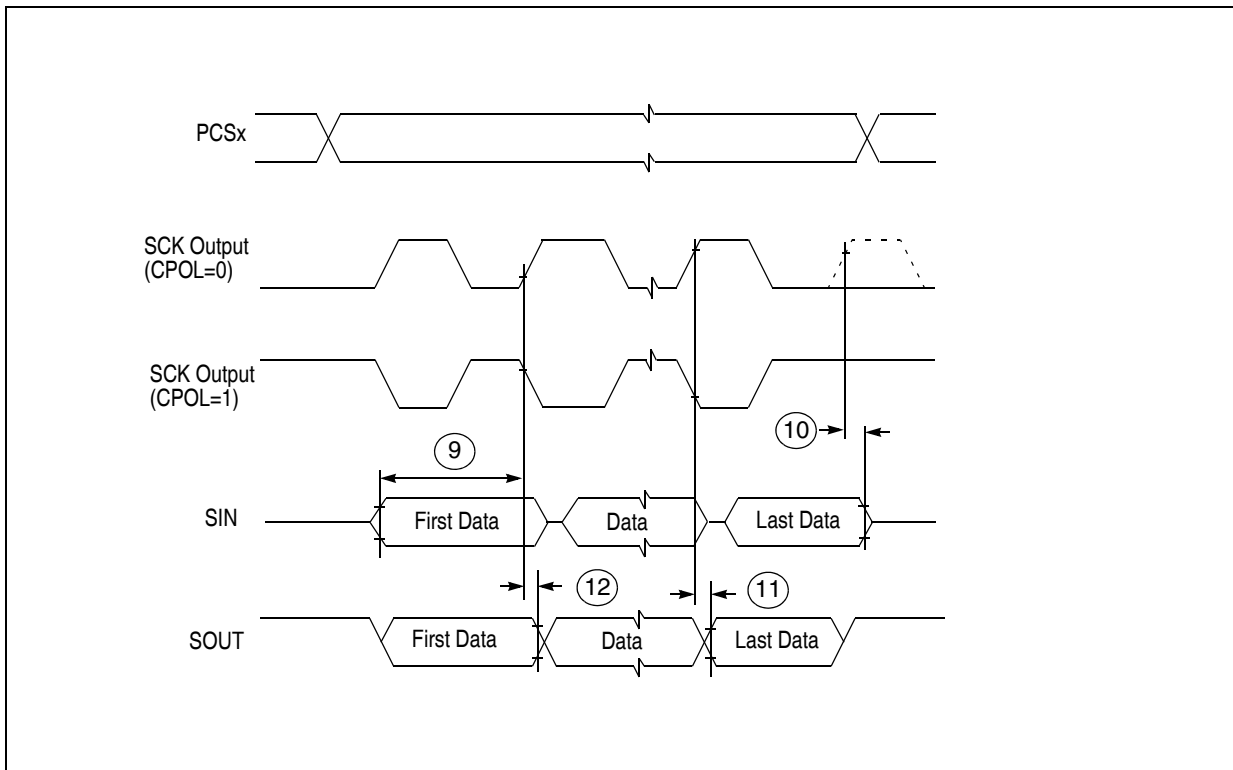


Figure 27. DSPI modified transfer format timing — Master, CPHA = 1

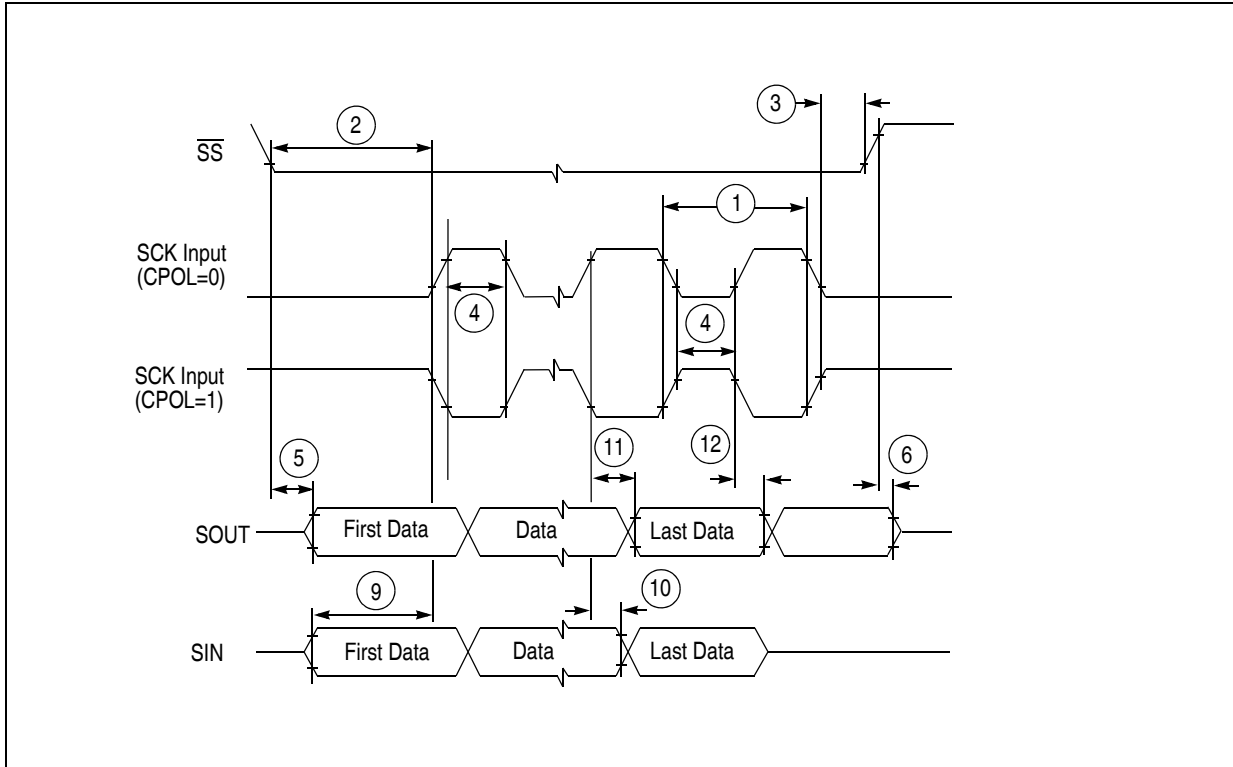


Figure 28. DSPI modified transfer format timing — Slave, CPHA = 0

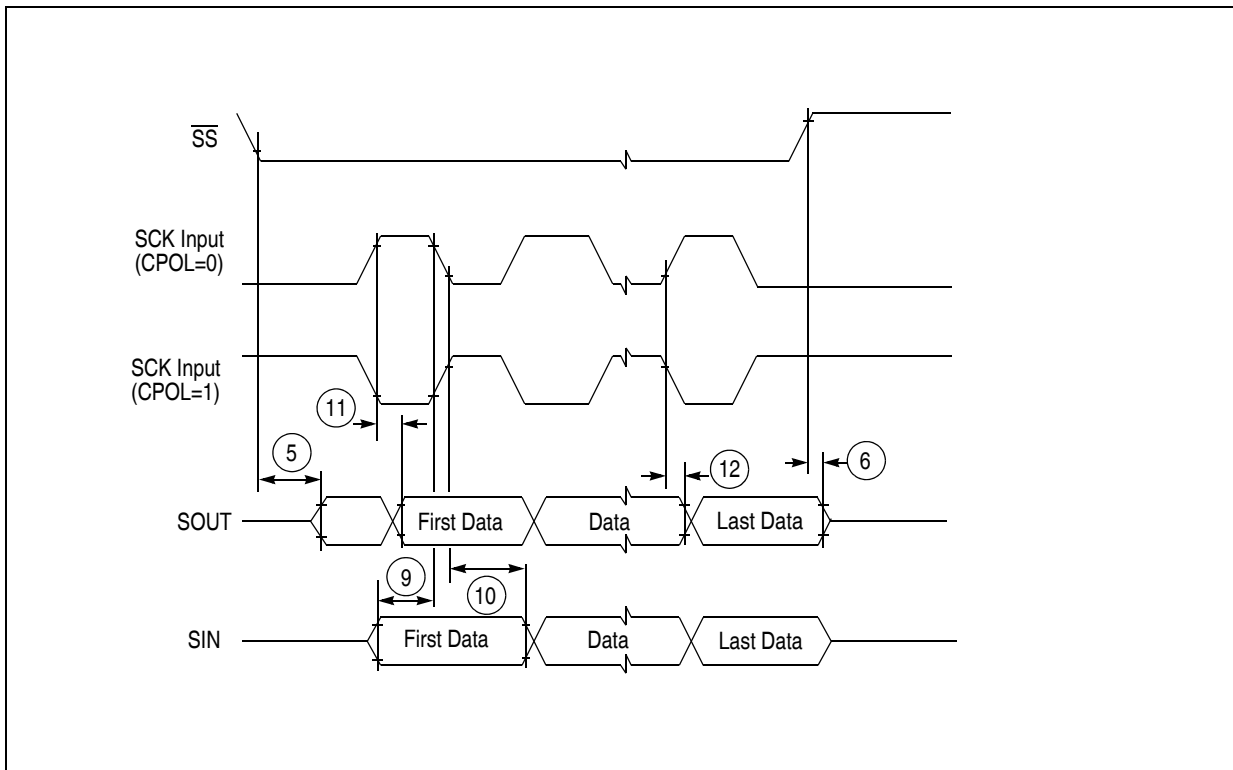
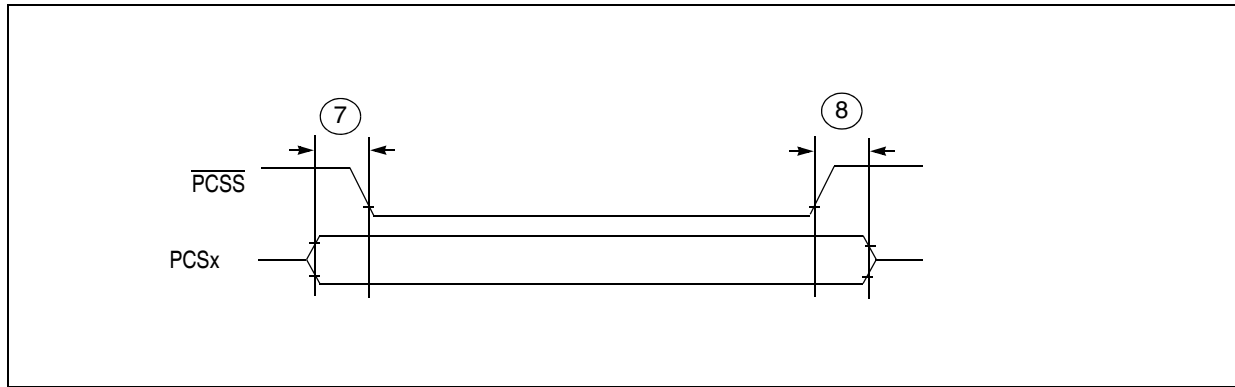


Figure 29. DSPI modified transfer format timing — Slave, CPHA = 1

Figure 30. DSPI PCS Strobe ( $\overline{\text{PCSS}}$ ) timing

### 3.19.9 Video interface timing

Table 34 details the MPC5604E's video encoder block's pixel input clocking requirement.

Table 34. Input pixel clock characteristics

| No. | Parameter                   | Min | Max | Unit |
|-----|-----------------------------|-----|-----|------|
| 1   | PDI Clock Period            | 10  | —   | ns   |
| 2   | PDI Clock Duty Cycle        | 50  | 50  | %    |
| 3   | Input setup time            | 2   | —   | ns   |
| 4   | Input Hold Time             | 2   | —   | ns   |
| 5   | Input Pixel Clock Slew Rate | —   | 2   | ns   |

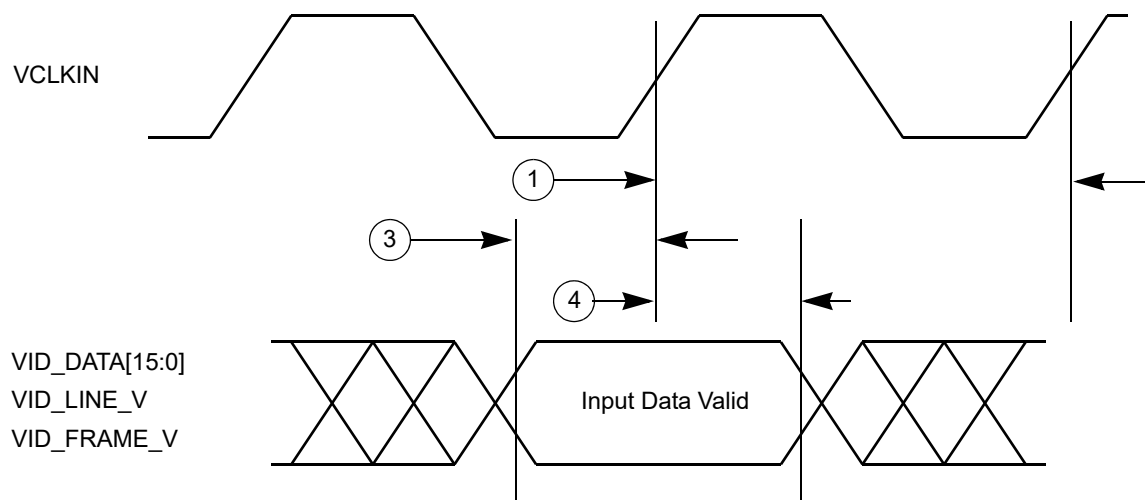


Figure 31. Video interface timing

### 3.19.10 Fast ethernet interface

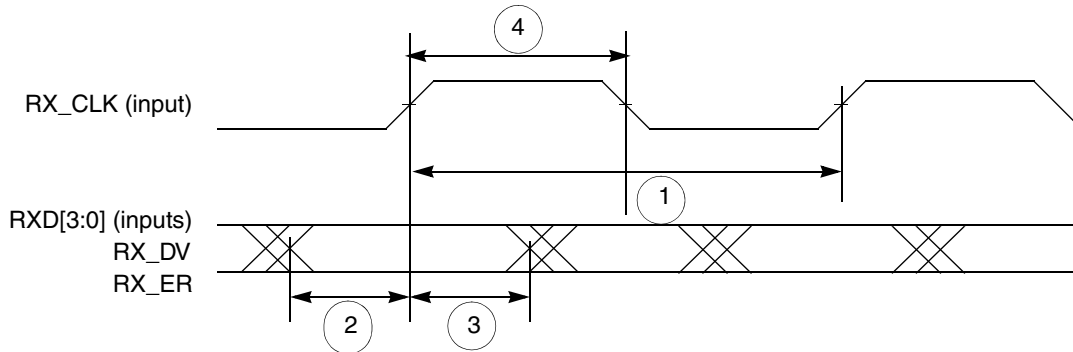
MII signals use CMOS signal levels compatible with devices operating at either 5.0 V or 3.3 V. Signals are not TTL compatible. They follow the CMOS electrical characteristics.

#### 3.19.10.1 MII receive signal timing (RXD[3:0], RX\_DV, RX\_ER, and RX\_CLK)

The receiver functions correctly up to a RX\_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the system clock frequency must exceed four times the RX\_CLK frequency.

**Table 35. MII receive signal timing**

| No. | Parameter                              | Min | Max | Unit |
|-----|--|-----|-----|------|
| 1   | Rx Clock Period                        | 40  | —   | ns   |
| 2   | RXD[3:0], RX_DV, RX_ER to RX_CLK setup | 5   | —   | ns   |
| 3   | RX_CLK to RXD[3:0], RX_DV, RX_ER hold  | 5   | —   | ns   |
| 4   | Rx Clock Duty Cycle                    | 40  | 60  | %    |



**Figure 32. MII receive signal timing diagram**

#### 3.19.10.2 MII transmit signal timing (TXD[3:0], TX\_EN, TX\_ER, TX\_CLK)

The transmitter functions correctly up to a TX\_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the system clock frequency must exceed four times the TX\_CLK frequency.

The transmit outputs (TXD[3:0], TX\_EN, TX\_ER) can be programmed to transition from either the rising or falling edge of TX\_CLK, and the timing is the same in either case. This options allows the use of non-compliant MII PHYs.

Refer to the Ethernet chapter for details of this option and how to enable it.

**Table 36. MII transmit signal timing<sup>1</sup>**

| No. | Parameter                                | Min | Max | Unit |
|-----|--|-----|-----|------|
| 5   | TX Clock Period                          | 40  | —   | ns   |
| 6   | TX_CLK to TXD[3:0], TX_EN, TX_ER invalid | 5   | —   | ns   |
| 7   | TX_CLK to TXD[3:0], TX_EN, TX_ER valid   | —   | 25  | ns   |
| 8   | TX Clock Duty Cycle                      | 40  | 60  | %    |

<sup>1</sup> Output pads configured with SRC = 0b11.

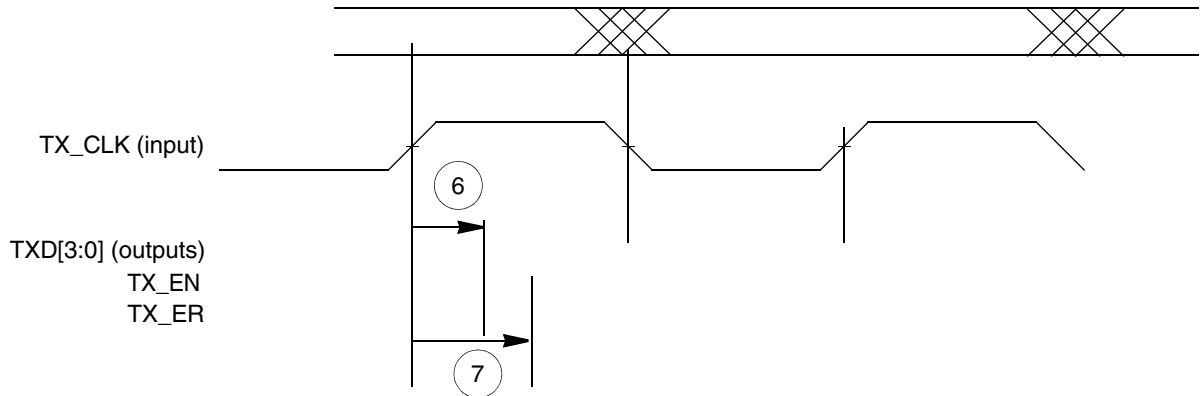


Figure 33. MII transmit signal timing diagram

### 3.19.10.3 MII async inputs signal timing (CRS and COL)

Table 37. MII async inputs signal timing<sup>1</sup>

| No. | Parameter                    | Min | Max | Unit          |
|-----|------------------------------|-----|-----|---------------|
| 9   | CRS, COL minimum pulse width | 1.5 | —   | TX_CLK period |

<sup>1</sup> Output pads configured with SRC = 0b11.

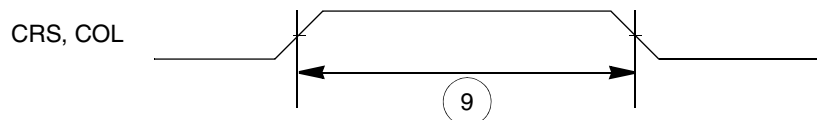


Figure 34. MII async inputs timing diagram

### 3.19.10.4 MII serial management channel timing (MDIO and MDC)

The FEC functions correctly with a maximum MDC frequency of 5 MHz.

Table 38. MII serial management channel timing (MDIO and MDC)

| No. | Parameter                 | Min | Max | Unit |
|-----|---------------------------|-----|-----|------|
| 1   | MDIO Input delay setup    | 28  | —   | ns   |
| 2   | MDIO Input delay hold     | 0   | —   | ns   |
| 3   | MDIO Output delay valid   | —   | 25  | ns   |
| 4   | MDIO Output delay Invalid | 0   | —   | ns   |
| 5   | MDC clock period          | 100 | —   | ns   |
| 6   | MDC Duty Cycle            | 40  | 60  | %    |

### 3.19.11 I<sup>2</sup>C timing

Table 39. I<sup>2</sup>C SCL and SDA input timing specifications

| No. | Symbol | Parameter  | Value |     | Unit                      |
|-----|--------|--|-------|-----|---------------------------|
|     |        |  | Min   | Max |                           |
| 1   | —      | D Start condition hold time                                      | 2     | —   | IP bus cycle <sup>1</sup> |
| 2   | —      | D Clock low time   | 8     | —   | IP bus cycle <sup>1</sup> |
| 4   | —      | D Data hold time   | 0.0   | —   | ns                        |
| 6   | —      | D Clock high time  | 4     | —   | IP bus cycle <sup>1</sup> |
| 7   | —      | D Data setup time  | 0.0   | —   | ns                        |
| 8   | —      | D Start condition setup time (for repeated start condition only) | 2     | —   | IP bus cycle <sup>1</sup> |
| 9   | —      | D Stop condition setup time                                      | 2     | —   | IP bus cycle <sup>1</sup> |

<sup>1</sup> Inter Peripheral Clock is the clock at which the I<sup>2</sup>C peripheral is working in the device. It is equal to the system clock (Sys\_clk).

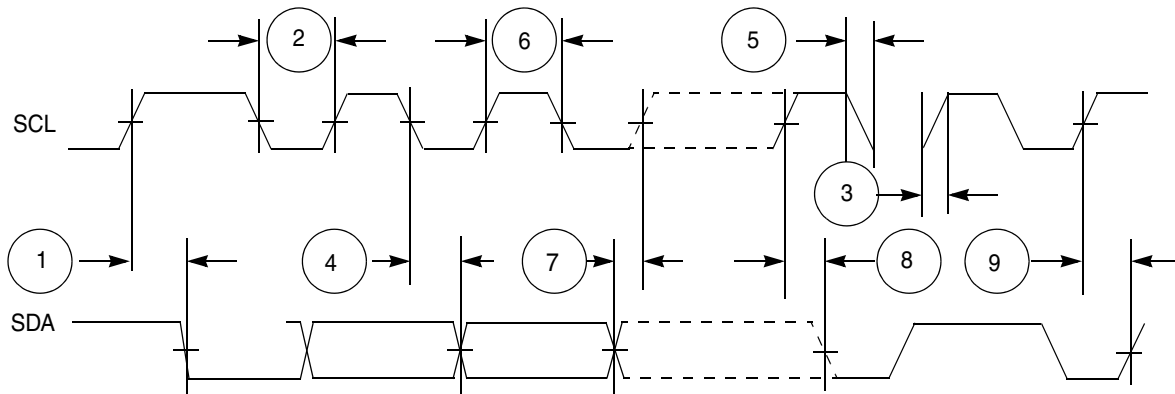
Table 40. I<sup>2</sup>C SCL and SDA output timing specifications

| No.            | Symbol | Parameter  | Value |      | Unit                      |
|----------------|--------|--|-------|------|---------------------------|
|                |        |  | Min   | Max  |                           |
| 1 <sup>1</sup> | —      | D Start condition hold time                                      | 6     | —    | IP bus cycle <sup>2</sup> |
| 2 <sup>1</sup> | —      | D Clock low time   | 10    | —    | IP bus cycle <sup>1</sup> |
| 3 <sup>3</sup> | —      | D SCL/SDA rise time  | —     | 99.6 | ns                        |
| 4 <sup>1</sup> | —      | D Data hold time   | 7     | —    | IP bus cycle <sup>1</sup> |
| 5 <sup>1</sup> | —      | D SCL/SDA fall time  | —     | 99.5 | ns                        |
| 6 <sup>1</sup> | —      | D Clock high time  | 10    | —    | IP bus cycle <sup>1</sup> |
| 7 <sup>1</sup> | —      | D Data setup time  | 2     | —    | IP bus cycle <sup>1</sup> |
| 8 <sup>1</sup> | —      | D Start condition setup time (for repeated start condition only) | 20    | —    | IP bus cycle <sup>1</sup> |
| 9 <sup>1</sup> | —      | D Stop condition setup time                                      | 10    | —    | IP bus cycle <sup>1</sup> |

<sup>1</sup> Programming IBFD (I<sup>2</sup>C bus Frequency Divider) with the maximum frequency results in the minimum output timings listed. The I<sup>2</sup>C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed in IFDR.

<sup>2</sup> Inter Peripheral Clock is the clock at which the I<sup>2</sup>C peripheral is working in the device.

<sup>3</sup> Because SCL and SDA are open-drain-type outputs, which the processor can only actively drive low, the time SCL or SDA takes to reach a high level depends on external signal capacitance and pull-up resistor values.

Figure 35. I<sup>2</sup>C input/output timing

### 3.19.12 SAI timing

All timing requirements are specified relative to the clock period or to the minimum allowed clock period of a device.

Table 41. Master Mode SAI Timing

| No. | Parameter                                  | Value |     | Unit        |
|-----|--|-------|-----|-------------|
|     |  | Min   | Max |             |
|     | Operating voltage                          | 2.7   | 3.6 | V           |
| S1  | SAI_MCLK cycle time                        | 31.25 | —   | ns          |
| S2  | SAI_MCLK pulse width high/low              | 45%   | 55% | MCLK period |
| S3  | SAI_BCLK cycle time                        | 62.5  | —   | ns          |
| S4  | SAI_BCLK pulse width high/low              | 45%   | 55% | BCLK period |
| S5  | SAI_BCLK to SAI_FS output valid            | —     | 15  | ns          |
| S6  | SAI_BCLK to SAI_FS output invalid          | 0     | —   | ns          |
| S7  | SAI_BCLK to SAI_TXD valid                  | —     | 15  | ns          |
| S8  | SAI_BCLK to SAI_TXD invalid                | 0     | —   | ns          |
| S9  | SAI_RXD/SAI_FS input setup before SAI_BCLK | 28    | —   | ns          |
| S10 | SAI_RXD/SAI_FS input hold after SAI_BCLK   | 0     | —   | ns          |

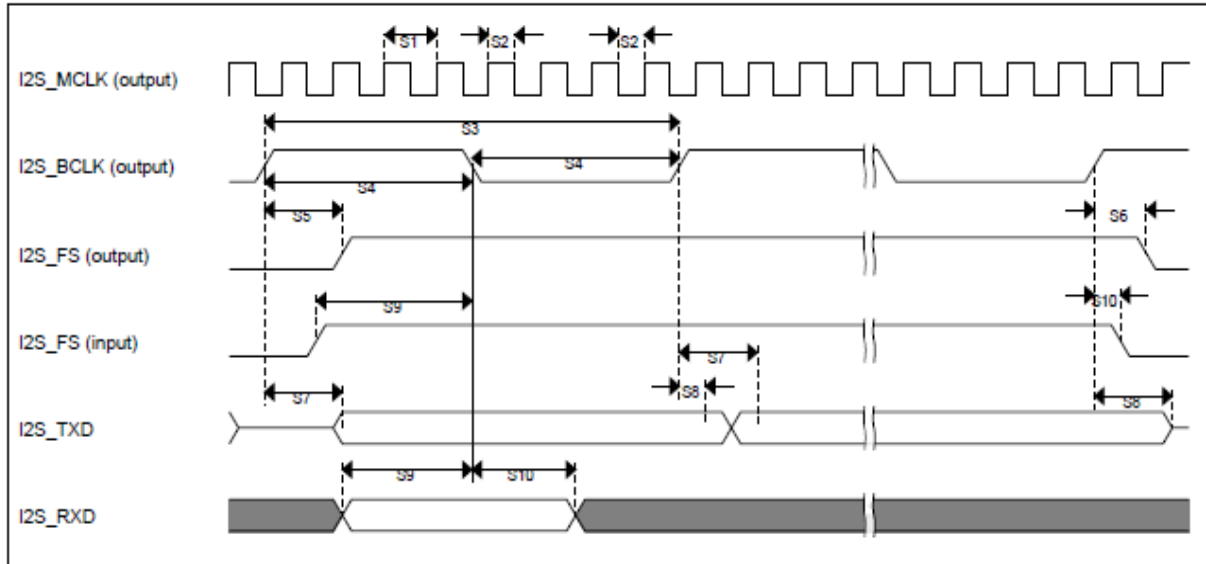


Figure 36. SAI timing master modes

Table 42. Slave Mode SAI Timing

| No. | Parameter                                 | Value |     | Unit        |
|-----|---|-------|-----|-------------|
|     |   | Min   | Max |             |
|     | Operating voltage                         | 2.7   | 3.6 | V           |
| S11 | SAI_BCLK cycle time (input)               | 80    | —   | ns          |
| S12 | SAI_BCLK pulse width high/low (input)     | 45%   | 55% | BCLK period |
| S13 | SAI_FS input setup before SAI_BCLK        | 10    | —   | ns          |
| S14 | SAI_FS input hold after SAI_BCLK          | 2     | —   | ns          |
| S15 | SAI_BCLK to SAI_TXD/SAI_FS output valid   | —     | 28  | ns          |
| S16 | SAI_BCLK to SAI_TXD/SAI_FS output invalid | 0     | —   | ns          |
| S17 | SAI_RXD setup before SAI_BCLK             | 10    | —   | ns          |
| S18 | SAI_RXD hold after SAI_BCLK               | 2     | —   | ns          |



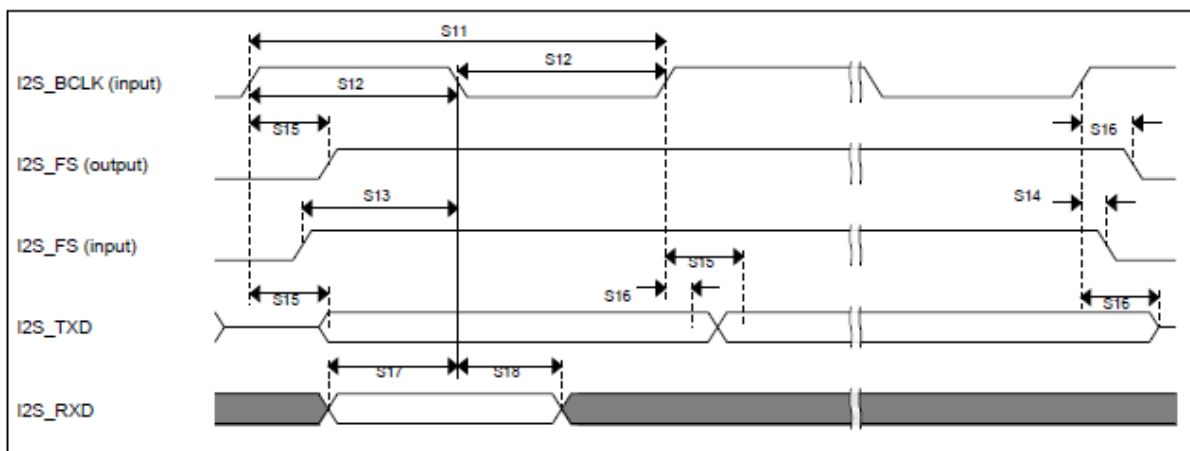


Figure 37. SAI timing slave modes

## **4 Package mechanical data**

### **4.1 100 LQFP mechanical outline drawing**

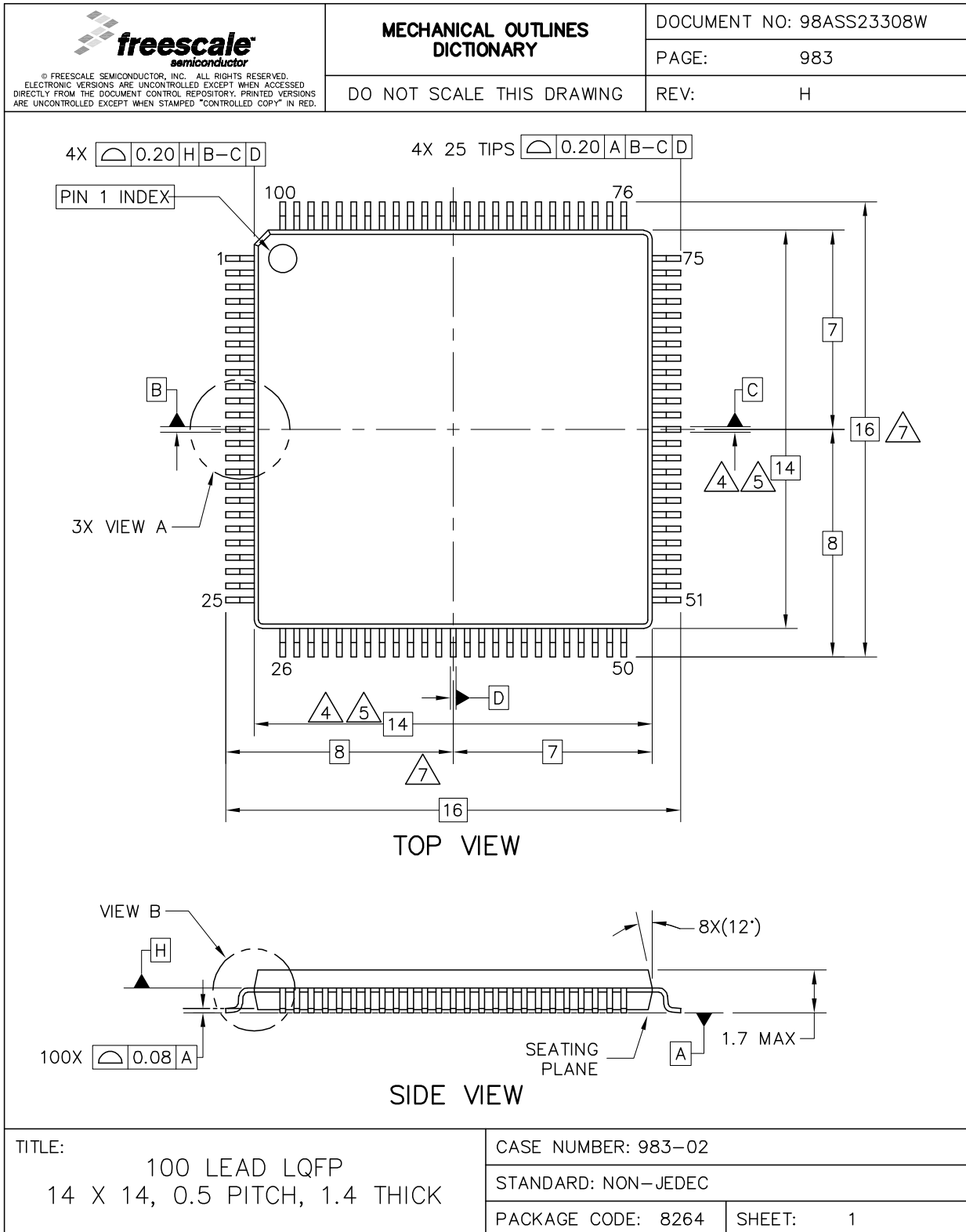


Figure 38. 100 LQFP package mechanical drawing (part 1)

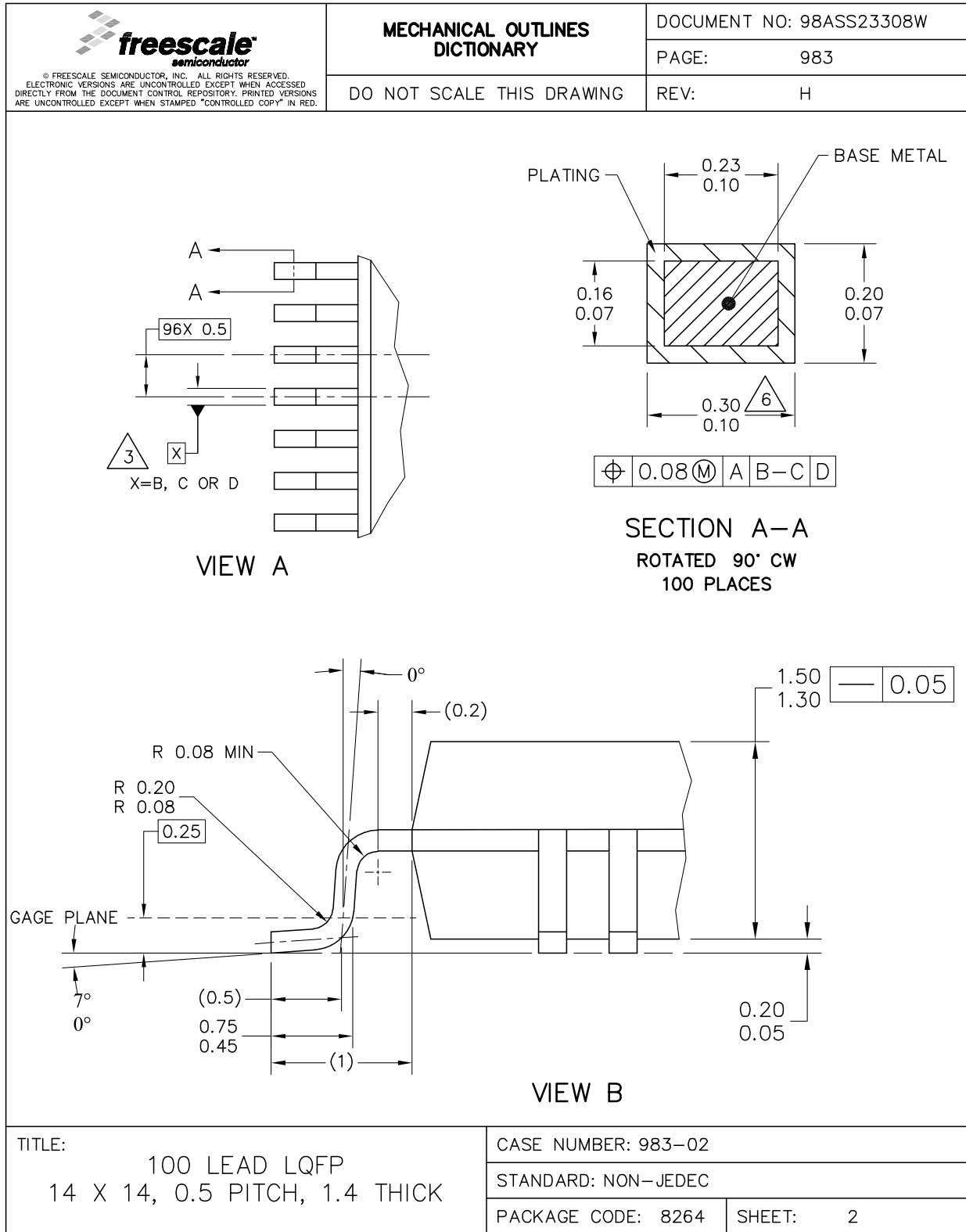


Figure 39. 100 LQFP package mechanical drawing (part 2)


|  |   |                     |                          |     |
|--|---|---------------------|--------------------------|-----|
|  <p>© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.<br/>ELECTRONIC VERSIONS ARE UNCONTROLLED EXCEPT WHEN ACCESSED<br/>DIRECTLY FROM THE DOCUMENT CONTROL REPOSITORY. PRINTED VERSIONS<br/>ARE UNCONTROLLED EXCEPT WHEN STAMPED "CONTROLLED COPY" IN RED.</p>   | <b>MECHANICAL OUTLINES<br/>DICTIONARY</b> |                     | DOCUMENT NO: 98ASS23308W |     |
|  |   |                     | PAGE:                    | 983 |
|  | DO NOT SCALE THIS DRAWING                 |                     | REV:                     | H   |
| <p>NOTES:</p> <ol style="list-style-type: none"> <li>1. ALL DIMENSIONS ARE IN MILLIMETERS.</li> <li>2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.</li> <li>3. DATUMS B, C AND D TO BE DETERMINED AT DATUM PLANE H.</li> <li>4. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY A MAXIMUM OF 0.1 MM.</li> <li>5. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSIONS. THE MAXIMUM ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THE DIMENSIONS ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.</li> <li>6. DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION. PROTRUSIONS SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL BE 0.07 MM.</li> <li>7. DIMENSIONS ARE DETERMINED AT THE SEATING PLANE, DATUM A.</li> </ol> |   |                     |                          |     |
| TITLE:   |   | CASE NUMBER: 983-02 |                          |     |
| 100 LEAD LQFP<br>14 X 14, 0.5 PITCH, 1.4 THICK   |   | STANDARD: NON-JEDEC |                          |     |
|  |   | PACKAGE CODE: 8264  | SHEET:                   | 3   |

Figure 40. 100 LQFP package mechanical drawing (part 3)

## 4.2 64 LQFP mechanical outline drawing

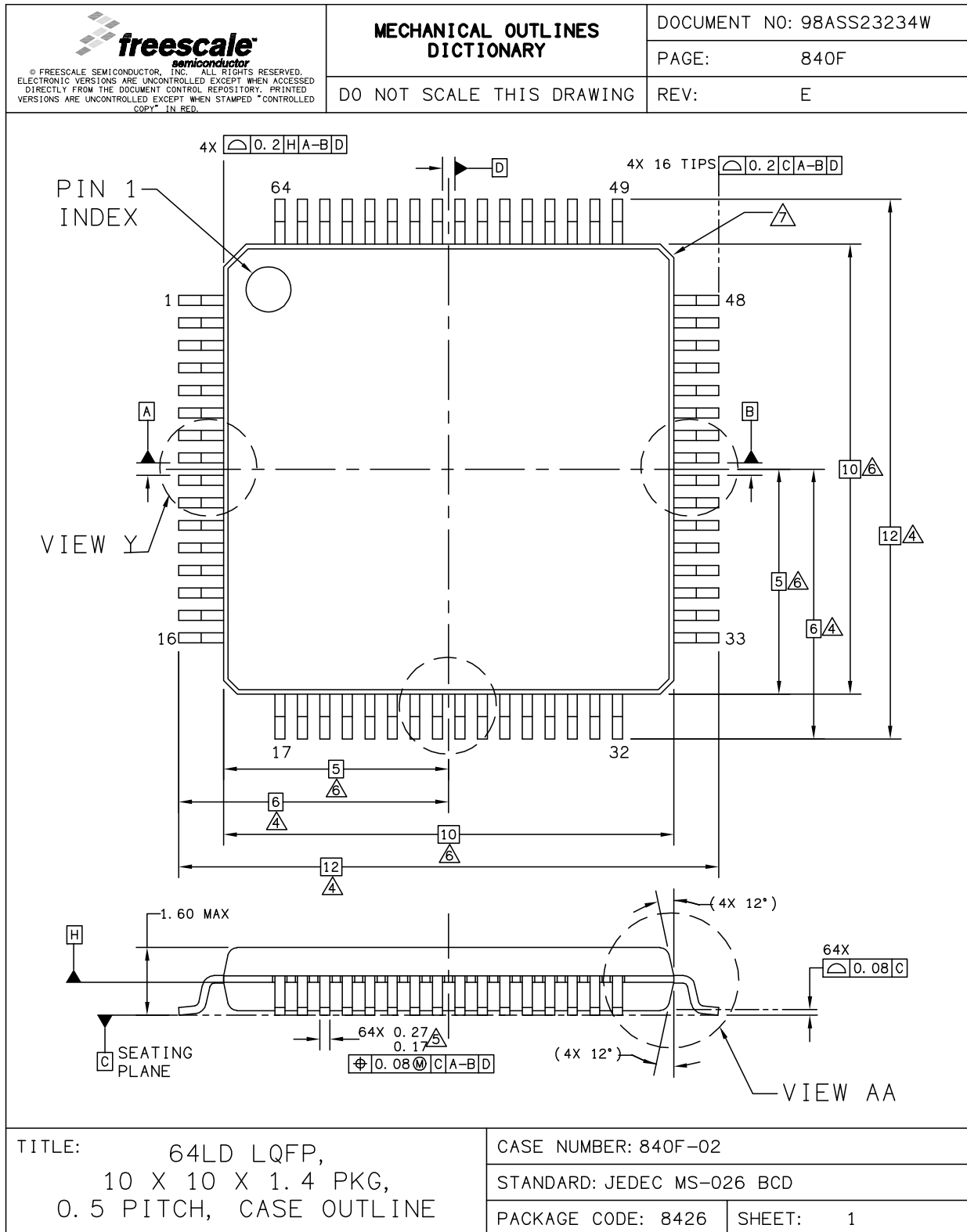


Figure 41. 64 LQFP package mechanical drawing (part 1)

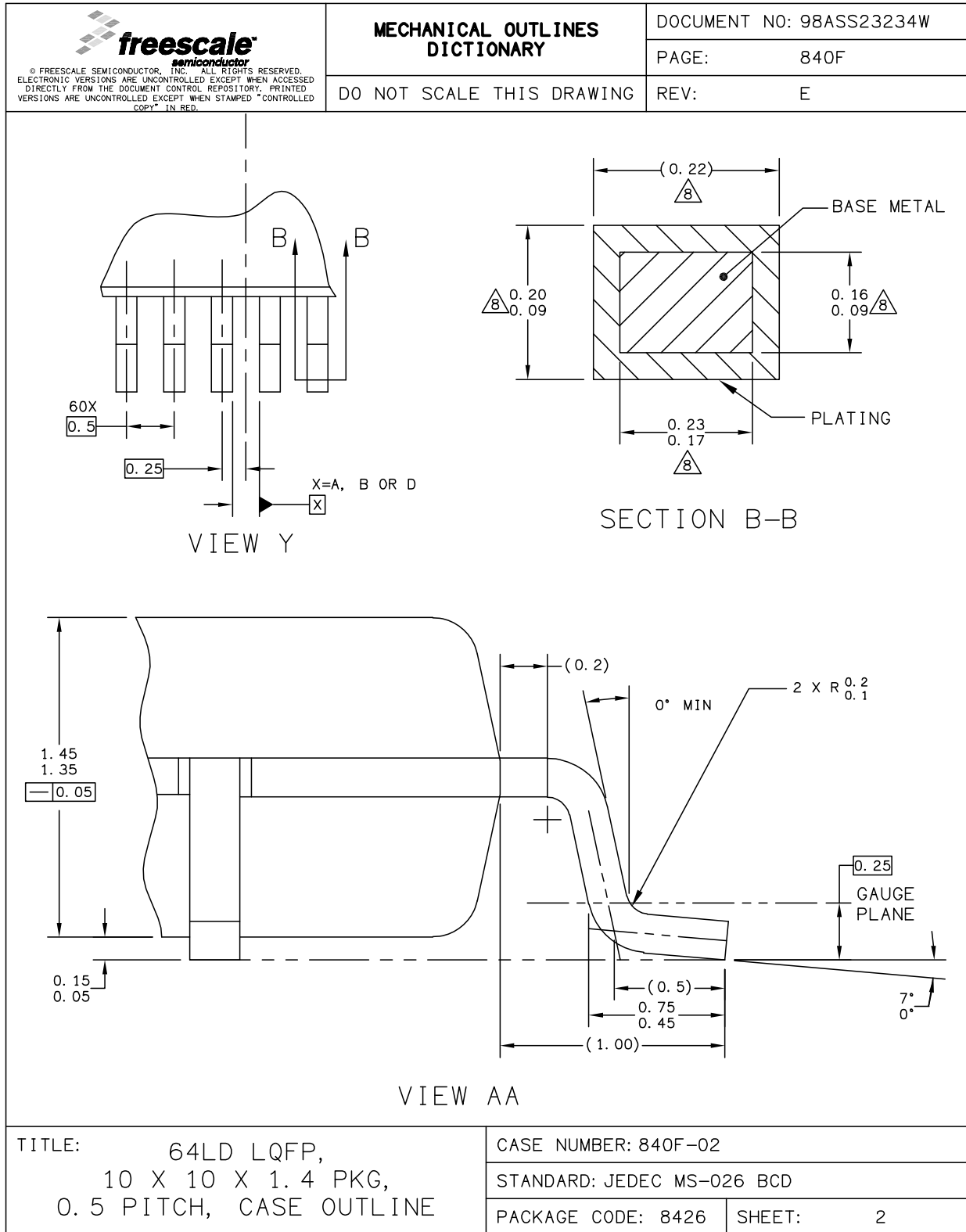


Figure 42. 64LQFP package mechanical drawing (part 2)

Package mechanical data


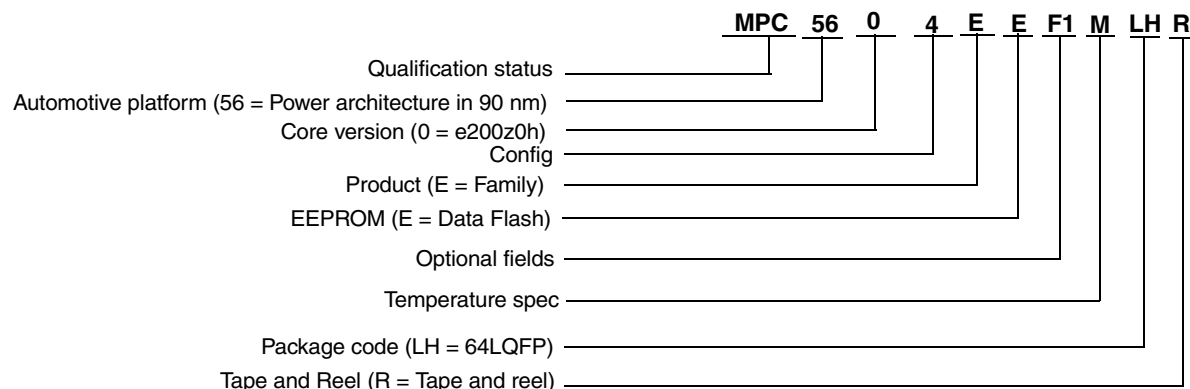
|   |   |                            |                          |      |
|---|---|----------------------------|--------------------------|------|
|  <p>© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.<br/>ELECTRONIC VERSIONS ARE UNCONTROLLED EXCEPT WHEN ACCESSED<br/>DIRECTLY FROM THE DOCUMENT CONTROL REPOSITORY. PRINTED<br/>VERSIONS ARE UNCONTROLLED EXCEPT WHEN STAMPED "CONTROLLED<br/>COPY" IN RED.</p>  | <b>MECHANICAL OUTLINES<br/>DICTIONARY</b> |                            | DOCUMENT NO: 98ASS23234W |      |
|   | DO NOT SCALE THIS DRAWING                 |                            | PAGE:                    | 840F |
|   |   |                            | REV:                     | E    |
| <p>NOTES:</p> <ol style="list-style-type: none"> <li>1. DIMENSIONS ARE IN MILLIMETERS.</li> <li>2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.</li> <li>3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.</li> <li>4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.</li> <li>5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.</li> <li>6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.</li> <li>7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.</li> <li>8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.</li> </ol> |   |                            |                          |      |
| TITLE: 64LD LQFP,<br>10 X 10 X 1.4 PKG,<br>0.5 PITCH, CASE OUTLINE  |   | CASE NUMBER: 840F-02       |                          |      |
|   |   | STANDARD: JEDEC MS-026 BCD |                          |      |
|   |   | PACKAGE CODE: 8426         | SHEET:                   | 3    |

Figure 43. 64LQFP package mechanical drawing (part 3)



# 5 Ordering information



**Qualification status**

M = MC status  
 S = Auto qualified  
 P = PC status

**Config**

4 = SAI + ENET + MJPEG  
 3 = SAI + ENET

**Optional fields**

F = ATMC  
 1 = Maskset revision 1  
 2 = Maskset revision 2

**Temperature spec**

C = - 40 to 85 °C  
 V = - 40 to 105 °C  
 M = - 40 to 125 °C

**Figure 44. Commercial product code structure**

**Table 43. Orderable part number summary**

| Part number <sup>1</sup>           | Flash/SRAM | Package | Speed  | Key Features       |
|------------------------------------|------------|---------|--------|--------------------|
| SPC5604EEF2MLH and SPC5604EEF2MLHR | 512K / 96K | 64 LQFP | 64 MHz | SAI + ENET + MJPEG |
| SPC5603EEF2MLH and SPC5603EEF2MLHR |            |         |        | SAI + ENET         |

<sup>1</sup> All packaged devices are PPC, rather than MPC or SPC, until product qualifications are complete. The unpackaged device prefix is PCC, rather than SCC, until product qualification is complete.

## 6 Document revision history

Table 44. Revision history

| Revision | Date         | Substantive changes  |
|----------|--------------|--|
| 1        | 15 Feb 2011  | Initial Release  |
| 2        | 13 June 2011 | <ul style="list-style-type: none"> <li>In the Recommended operating conditions table, changed the external supply voltage changed from 1.14 V to 1.15 V</li> <li>Added a footnote in the Device Summary table</li> <li>Changed the description of VDD_HV_S_BALLAST0 in the Supply pins table</li> </ul>  |
| 3        | 1 Nov 2011   | <ul style="list-style-type: none"> <li>Editorial changes and improvements</li> <li>In the Low voltage monitor electrical characteristics table, changed the marking of V<sub>PORUP</sub> from P to D</li> <li>In the DC electrical characteristics table, changed the I<sub>OL</sub> of the Medium, low level output voltage to 2 mA. From the same table, removed V<sub>OL_SYM</sub> and V<sub>OH_SYM</sub>. Revised the I<sub>PU</sub> and I<sub>PD</sub></li> <li>In the Main oscillator electrical characteristics table, changed the minimum value of transconductance to 4 mA/V</li> <li>In the 16 MHz RC oscillator electrical characteristics table, changed the marking of f<sub>RC</sub> from P to C and revised its minimum and value.</li> <li>In the ADC conversion characteristics table, changed the minimum and maximum value of TUE from TBD to -3 and 3</li> <li>In the Pin muxing table, C5 port ABS[2] assignment changed from SIUL to MC_RGM</li> <li>Revised the 64-pin and 100-pin package pinouts and added a footnote.</li> <li>In the Supply pins table, revised the description of ADC0 pins</li> <li>In the Supply pins table, added a column Port Pin and renamed the Symbol column</li> <li>Removed Power Supply segment table</li> <li>In the Pin Muxing table, clarified the peripherals in the following port pins: C5, A3, A8, A10, A12, A15, C3, C4, C5, C6, C12</li> <li>In the Low voltage monitor electrical characteristics table, changed the maximum value of VMLVDDOK_H</li> <li>In the ADC conversion characteristics, changed the ADC sampling time to 500 ns</li> </ul> |
| 3.1      | 2 Dec 2011   | <ul style="list-style-type: none"> <li>Inserted values for TBDs in the table EMI Testing Specifications</li> <li>From Supply Pins table, removed VDD_HV_ADV0</li> <li>In the PLLMRFM electrical specifications table, added the value of Self-clocked mode frequency</li> <li>In the ADC conversion characteristics table, added the value of INJ</li> </ul>   |
| 4        | 23 Jan 2012  | <ul style="list-style-type: none"> <li>System Pin table, swapped the description of XTAL and EXTAL</li> </ul>  |
| 5        | 03 Feb 2015  | <p>On the first page:</p> <ul style="list-style-type: none"> <li>added 32 external interrupts for 100-pin LQFP and updated 22 external interrupts for 64-pin LQFP.</li> <li>changed "8 input channels" to "7 input channels".</li> <li>changed "4 internal connection..." to "3 internal connection...".</li> <li>Removed "1 x VGate Current".</li> <li>In <a href="#">Table 1.</a>, "Device summary", removed VGate current from the equation for ADC (10-bit).</li> <li>In <a href="#">Figure 1.</a>, "MPC5604E block diagram": changed "4+4 channels" to "4+3 channels".</li> <li>Updated <a href="#">Table 2.</a>, "Supply pins".</li> <li>In <a href="#">Table 4.</a>, "Pin muxing", function of port pins B4, B13, B14, B15, C0, C1, C9, C15, D8, D13, D14, and E2 changed from GPIO to GPI.</li> <li>Added new section - <a href="#">Section 5</a>, "Ordering information".</li> <li>In <a href="#">Figure 2.</a>, "64-pin LQFP pinout (top view)", changed VSS (pin 47) to VSS_HV.</li> <li>In <a href="#">Figure 3.</a>, "100-pin LQFP pinout (top view)", changed VSS (pin 74) to VSS_HV.</li> <li>Updated "optional fields" entries in <a href="#">Figure 44.</a>, "Commercial product code structure".</li> </ul>  |

Table 44. Revision history (continued)

| Revision | Date            | Substantive changes  |
|----------|-----------------|--|
| 5.1      | 27 Jan 2016     | <ul style="list-style-type: none"> <li>Changed the DS document from Advanced Information to Technical Data</li> <li>Updated Figure 44., “Commercial product code structure” and Table 43., “Orderable part number summary”.</li> </ul>   |
| 6        | 16 October 2019 | <ul style="list-style-type: none"> <li>In Table 14., “Low voltage monitor electrical characteristics”, changed the max value of <math>V_{MLVDDOK\_H}</math> from 1.235 V to 1.135 V</li> <li>In Table 41., “Master Mode SAI Timing” <ul style="list-style-type: none"> <li>For SAI_MCLK changed the Min cycle time from 40 to 31.25.</li> <li>Changed the minimal value of SAI_BCLK cycle time from 80 to 62.5.</li> <li>Updated unit of SAI_BCLK cycle time from BCLK period to ns.</li> <li>Updated unit of SAI_BCLK pulse width high/low from ns to BCLK period.</li> </ul> </li> <li>In Table 19., “PLLMRFM electrical specifications (<math>V_{DDPLL} = 3.0\text{ V to }3.6\text{ V}</math>, <math>V_{SS} = V_{SSPLL} = 0\text{ V}</math>, <math>T_A = T_L\text{ to }T_H</math>)” changed the following: <ul style="list-style-type: none"> <li>Changed the name from <math>f_{FMPLL\_OUT}</math> to <math>f_{FMPLL\_PCS}</math> changed the Max value to 128</li> <li>Added PLL output frequency parameter row</li> <li>Changed the frequency of <math>f_{VCO}</math> Min range from 20 MHz to 256 MHz and Max range from 150 MHz to 512 MHz</li> <li>Changed the Min value of System clock period parameter to <math>1/f_{sys}</math></li> <li>Changed the name of Self-clocked mode frequency to Self-clocked mode frequency(VCO free running frequency)</li> <li>Updated the row for <math>C_{JITTER}</math></li> </ul> </li> <li>In section 3.8.1.2, “External voltage regulation mode”, under Figure 5., “External Regulation Mode”, added the following note: <ul style="list-style-type: none"> <li>In external regulation mode, POR_B pin should be used to control the power on RESET for the device. POR_B should be kept low (asserted) as long as the input supplies are unstable or below the specified operating range. Failure to do so may lead to unexpected device operation and erratic reset recovery.</li> </ul> </li> <li>Added section 3.17, “NMI filter functional specification”</li> <li>In Section Table 43., “Orderable part number summary”, changed the part number to “SPC5604EEF2MLH and SPC5604EEF2MLHR” and “SPC5603EEF2MLH and SPC5603EEF2MLHR”.</li> </ul> |