NXP Semiconductors
Data Sheet: Technical Data

Document Number MPC5746C
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MPC5746C

MPC5746C Microcontroller Datasheet

Features

- 1 × 160 MHz Power Architecture® e200z4 Dual issue, 32-bit CPU
  - Single precision floating point operations
  - 8 KB instruction cache and 4 KB data cache
  - Variable length encoding (VLE) for significant code density improvements
- 1 x 80 MHz Power Architecture® e200z2 Single issue, 32-bit CPU
  - Using variable length encoding (VLE) for significant code size footprint reduction
- End to end ECC
  - All bus masters, for example, cores, generate a single error correction, double error detection (SECDED) code for every bus transaction
  - SECDED covers 64-bit data and 29-bit address
- Memory interfaces
  - 3 MB on-chip flash memory supported with the flash memory controller
  - 3 x flash memory page buffers (3-port flash memory controller)
  - 384 KB on-chip SRAM across three RAM ports
- Clock interfaces
  - 8-40 MHz external crystal (FXOSC)
  - 16 MHz IRC (FIRC)
  - 128 KHz IRC (SIRC)
  - 32 KHz external crystal (SXOSC)
  - Clock Monitor Unit (CMU)
  - Frequency modulated phase-locked loop (FMPLL)
  - Real Time Counter (RTC)
- System Memory Protection Unit (SMPU) with up to 32 region descriptors and 16-byte region granularity
- 16 Semaphores to manage access to shared resources
- Interrupt controller (INTC) capable of routing interrupts to any CPU
- Crossbar switch architecture for concurrent access to peripherals, flash memory, and RAM from multiple bus masters
- 32-channel eDMA controller with multiple transfer request sources using DMAMUX
- Boot Assist Flash (BAF) supports internal flash programming via a serial link (SCI)
- Analog
  - Two analog-to-digital converters (ADC), one 10-bit and one 12-bit
  - Three analog comparators
  - Cross Trigger Unit to enable synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
- Communication
  - Four Deserial Serial Peripheral Interface (DSPI)
  - Four Serial Peripheral interface (SPI)
  - 16 serial communication interface (LIN) modules
  - Eight enhanced FlexCAN3 with FD support
  - Four inter-IC communication interface (I2C)
  - ENET complex (10/100 Ethernet) that supports Multi queue with AVB support, 1588, and MII/RMII
  - Dual-channel FlexRay controller
- Audio
  - Synchronous Audio Interface (SAI)
  - Fractional clock dividers (FCD) operating in conjunction with the SAI
- Configurable I/O domains supporting FlexCAN, LINFlexD, Ethernet, and general I/O
- Supports wake-up from low power modes via the WKPU controller
- On-chip voltage regulator (VREG)
- Debug functionality
  - e200z2 core:NDI per IEEE-ISTO 5001-2008 Class3+
  - e200z4 core: NDI per IEEE-ISTO 5001-2008 Class 3+

- Timer
  - 16 Periodic Interrupt Timers (PITs)
  - Two System Timer Modules (STM)
  - Three Software Watchdog Timers (SWT)
  - 64 Configurable Enhanced Modular Input Output Subsystem (eMIOS) channels
- Device/board boundary Scan testing supported with Joint Test Action Group (JTAG) of IEEE 1149.1 and IEEE 1149.7 (CJTAG)
- Security
  - Hardware Security Module (HSMv2)
  - Password and Device Security (PASS) supporting advanced censorship and life-cycle management
  - One Fault Collection and Control Unit (FCCU) to collect faults and issue interrupts
- Functional Safety
  - ISO26262 ASIL-B compliance
- Multiple operating modes
  - Includes enhanced low power operation

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1 Block diagram

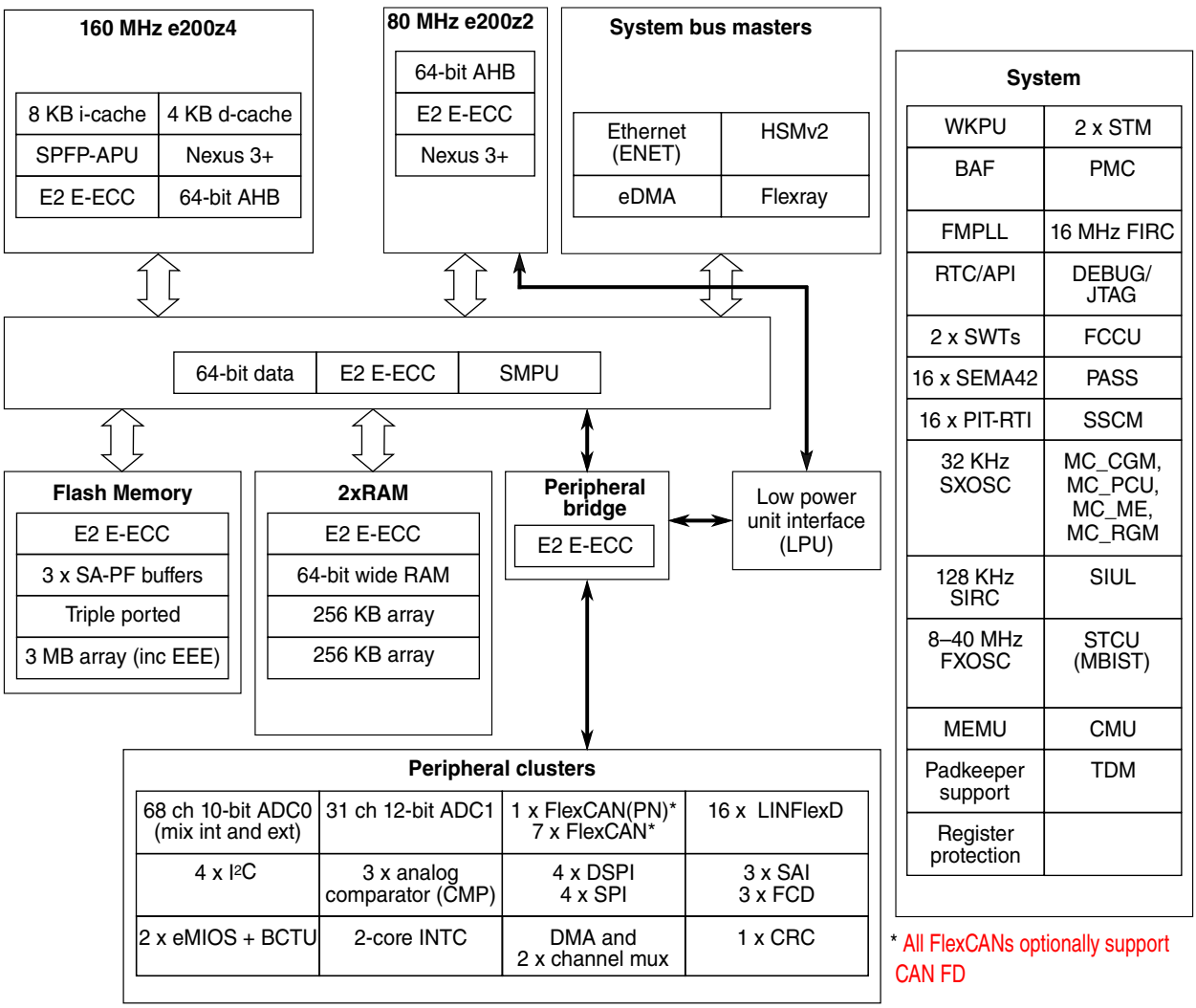


Figure 1. MPC5746C block diagram

2 Family comparison

The following table provides a summary of the different members of the MPC5746C family and their proposed features. This information is intended to provide an understanding of the range of functionality offered by this family. For full details of all of the family derivatives please contact your marketing representative.

NOTE

All optional features (Flash memory, RAM, Peripherals) start with lowest number or address (e.g., FlexCAN0) and end at highest available number or address (e.g., MPC574xB/C have 6 CAN, ending with FlexCAN5).

Table 1. MPC5746C Family Comparison[1]

Feature	MPC5745B	MPC5744B	MPC5746B	MPC5744C	MPC5745C	MPC5746C
CPUs	e200z4	e200z4	e200z4	e200z4 e200z2	e200z4 e200z2	e200z4 e200z2
FPU	e200z4	e200z4	e200z4	e200z4	e200z4	e200z4
Maximum Operating Frequency[2]	160MHz (Z4)	160MHz (Z4)	160MHz (Z4)	160MHz (Z4) 80MHz (Z2)	160MHz (Z4) 80MHz (Z2)	160MHz (Z4) 80MHz (Z2)
Flash memory	2 MB	1.5 MB	3 MB	1.5 MB	2 MB	3 MB
EEPROM support	Emulated up to 64K			Emulated up to 128K		
RAM	256 KB	192 KB	384 KB (Optional 512KB)[3]	192 KB	256 KB	384 KB (Optional 512KB)[3]
ECC	End to End					
SMPU	16 entry					
DMA	32 channels					
10-bit ADC	36 Standard channels 32 External channels					
12-bit ADC	15 Precision channels 16 Standard channels					
Analog Comparator	3					
BCTU	1					
SWT	1, SWT[0]			2[4]		
STM	1, STM[0]			2		
PIT-RTI	16 channels PIT 1 channels RTI					
RTC/API	1					
Total Timer I/O[5]	64 channels 16-bits					
LINFlexD	1 Master and Slave (LINFlexD[0], 11 Master (LINFlexD[1:11])			1 Master and Slave (LINFlexD[0], 15 Master (LINFlexD[1:15])		
FlexCAN	6 with optional CAN FD support (FlexCAN[0:5])			8 with optional CAN FD support (FlexCAN[0:7])		
DSPI/SPI	4 x DSPI 4 x SPI					

Table continues on the next page...

Table 1. MPC5746C Family Comparison[1] (continued)

Feature	MPC5745B	MPC5744B	MPC5746B	MPC5744C	MPC5745C	MPC5746C
I^2C	4	4	4	4		
SAI/I^2S	3	3	3	3		
FXOSC	8 - 40 MHz					
SXOSC	32 KHz					
FIRC	16 MHz					
SIRC	128 KHz					
FMPLL	1					
Low Power Unit (LPU)	Yes					
FlexRay 2.1 (dual channel)	Yes, 128 MB	Yes, 128 MB	Yes, 128 MB	Yes, 128 MB		
Ethernet (RMII, MII + 1588, Muti queue AVB support)	1	1	1	1		
CRC	1					
MEMU	2					
STCU2	1					
HSM-v2 (security)	Optional					
Censorship	Yes					
FCCU	1					
Safety level	Specific functions ASIL-B certifiable					
User MBIST	Yes					
I/O Retention in Standby	Yes					
GPI	1 (100 BGA), 17 (176 LQFP-EP), 18 (256 BGA), 18 (324 BGA)					
GPIO	65 (100 BGA), 129 (176 LQFP-EP), 178 (256 BGA), 246 (324 BGA)					
Debug	JTAGC, cJTAG					
Nexus	Z4 N3+ (Only available on 324BGA (development only)) Z2 N3+ (Only available on 324BGA (development only))					
Packages	176 LQFP-EP 256 BGA 100 BGA	176 LQFP-EP 256 BGA 100 BGA	176 LQFP-EP 256 BGA 100 BGA	176 LQFP-EP 256 BGA 100 BGA	176 LQFP-EP 256 BGA 100 BGA	176 LQFP-EP 256 BGA, 324 BGA (development only) 100 BGA

1. Feature set dependent on selected peripheral multiplexing, table shows example. Peripheral availability is package dependent.
2. Based on 125°C ambient operating temperature and subject to full device characterization.
3. Contact NXP representative for part number
4. Additional SWT included when HSM option selected

5. See device datasheet and reference manual for information on to timer channel configuration and functions.

Table 2. MPC5746C Family Comparison - NVM Memory Map 1

Start Address	End Address	Flash block	RWW partition	MPC5744	MPC5745	MPC5746
0x01000000	0x0103FFFF	256 KB code Flash block 0	6	available	available	available
0x01040000	0x0107FFFF	256 KB code Flash block 1	6	available	available	available
0x01080000	0x010BFFFF	256 KB code Flash block 2	6	available	available	available
0x010C0000	0x010FFFFF	256 KB code Flash block3	6	available	available	available
0x01100000	0x0113FFFF	256 KB code Flash block 4	6	not available	available	available
0x01140000	0x0117FFFF	256 KB code Flash block 5	7	not available	available	available
0x01180000	0x011BFFFF	256 KB code Flash block 6	7	not available	not available	available
0x011C0000	0x011FFFFF	256 KB code Flash block 7	7	not available	not available	available
0x01200000	0x0123FFFF	256 KB code Flash block 8	7	not available	not available	available
0x01240000	0x0127FFFF	256 KB code Flash block 9	7	not available	not available	available

Table 3. MPC5746C Family Comparison - NVM Memory Map 2

Start Address	End Address	Flash block	RWW partition	MPC5744B MPC5745B MPC5746B	MPC5744C MPC5745C MPC5746C
0x00F90000[1]	0x00F93FFF	16 KB data Flash	2	available	available[1]
0x00F94000	0x00F97FFF	16 KB data Flash	2	available	available[1]
0x00F98000	0x00F9BFFF	16 KB data Flash	2	available	available[1]
0x00F9C000	0x00F9FFFF	16 KB data Flash	2	available	available[1]
0x00FA0000	0x00FA3FFF	16 KB data Flash	3	not available	available[1]
0x00FA4000	0x00FA7FFF	16 KB data Flash	3	not available	available[1]
0x00FA8000	0x00FABFFF	16 KB data Flash	3	not available	available[1]
0x00FAC000	0x00FAFFFF	16 KB data Flash	3	not available	available[1]
0x00FB0000	0x00FB7FFF	32 KB data Flash	Reserved		
0x00FB8000	0x00FBFFFF	32 KB data Flash	Reserved		
0x00FC0000	0x00FC7FFF	32 KB data Flash	0	available	available
0x00FC8000	0x00FCFFFF	32 KB data Flash	1	available	available
0x00FD0000	0x00FD7FFF	32 KB data Flash	1	available	available
0x00FD8000	0x00FDFFFF	32 KB data Flash	1	available	available
0x00FE0000	0x00FEFFFF	64 KB data Flash	0	available	available
0x00FF0000	0x00FFFFFF	64 KB data Flash	1	available	available

1. Flexible patitions for boot and EEPROM

Table 4. MPC5748G Family Comparison - NVM Memory Map 3

Start Address	End Address	Flash block	RWW	MPC5744B MPC5745B MPC5746B	MPC5744C MPC5745C MPC5746C
0x00610000	0x0061FFFF	64 KB HSM Code block 2	0	available	available
0x00620000	0x0062FFFF	64 KB HSM Code block 3	1	available	available
HSM Data					
0x00630000	0x00F7FFFF	9536 KB	Reserved		
HSM Data					
0x00F80000	0x00F83FFF	16 KB HSM data block 0	4	available	available
0x00F84000	0x00F87FFF	16 KB HSM data block 1	5	available	available
0x00F88000	0x00F8BFFF	16 KB	Reserved		
Small HSM Code Block					
0x00F8C000	0x00F8FFFF	16 KB Code Flash block	0	available	available

Table 5. MPC5746C Family Comparison - RAM Memory Map

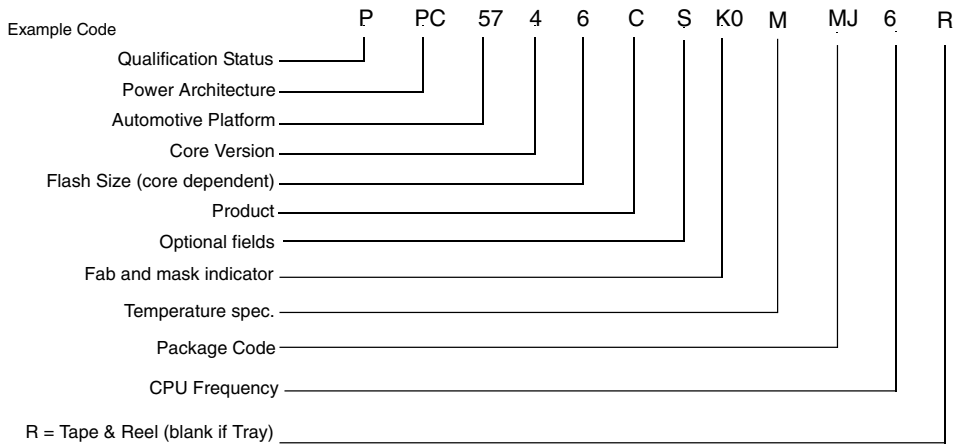
Start Address	End Address	Allocated size	Description	MPC5744	MPC5745	MPC5746
0x40000000	0x40001FFF	8 KB	SRAM0	available	available	available
0x40002000	0x4000FFFF	56 KB	SRAM1	available	available	available
0x40010000	0x4001FFFF	64 KB	SRAM2	available	available	available
0x40020000	0x4002FFFF	64 KB	SRAM3	available	available	available
0x40030000	0x4003FFFF	64 KB	SRAM4	not available	available	available
0x40040000	0x4004FFFF	64 KB	SRAM5	not available	not available	available
0x40050000	0x4005FFFF	64 KB	SRAM6	not available	not available	available
0x40060000	0x4006FFFF	64 KB	SRAM7	not available	not available	optional
0x40070000	0x4007FFFF	64 KB	SRAM8	not available	not available	optional

3 Ordering parts

3.1 Determining valid orderable parts

To determine the orderable part numbers for this device, go to www.nxp.com and perform a part number search for the following device number: MPC5746C.

3.2 Ordering Information



Qualification Status
P = Engineering samples
S = Automotive qualified

PC = Power Architecture

Automotive Platform
57 = Power Architecture in 55nm

Core Version
4 = e200z4 Core Version (highest core version in the case of multiple cores)

Flash Memory Size
4 = 1.5 MB
5 = 2 MB
6 = 3 MB

Product Version
B = Single core
C = Dual core

Optional fields
Blank = No optional feature
S = HSM (Security Module)
F = CAN FD
B = HSM + CAN FD
R = 512K RAM
T = HSM + 512K RAM
G* = CAN FD + 512K RAM
H* = HSM + CAN FD + 512K RAM
* G and H for 5746 B/C only

Fab and mask version indicator
K = TSMC Fab
#(0,1,etc.) = Version of the maskset, like rev. 0=0N65H

Temperature spec.
C = -40.C to +85.C Ta
V = -40.C to +105.C Ta
M = -40.C to +125.C Ta

Package Code
KU = 176 LQFP EP
MJ = 256 MAPBGA
MN = 324 MAPBGA
MH = 100MAPBGA

CPU Frequency
2 = Z4 operates upto 120 MHz
6 = Z4 operates upto 160 MHz

Shipping Method
R = Tape and reel
Blank = Tray

Note: Not all part number combinations are available as production product

4 General

4.1 Absolute maximum ratings

NOTE

Functional operating conditions appear in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maximum values is not guaranteed. See footnotes in Table 6 for specific conditions

Stress beyond the listed maximum values may affect device reliability or cause permanent damage to the device.

Table 6. Absolute maximum ratings

Symbol	Parameter	Conditions[1]	Min	Max	Unit
$V_{DD\_HV\_A}$, $V_{DD\_HV\_B}$, $V_{DD\_HV\_C}$[2, 3]	3.3 V - 5. 5V input/output supply voltage	—	–0.3	6.0	V
$V_{DD\_HV\_FLA}$[4, 5]	3.3 V flash supply voltage (when supplying from an external source in bypass mode)	—	–0.3	3.63	V
$V_{DD\_LP\_DEC}$[6]	Decoupling pin for low power regulators[7]	—	–0.3	1.32	V
$V_{DD\_HV\_ADC1\_REF}$[8]	3.3 V / 5.0 V ADC1 high reference voltage	—	–0.3	6	V
$V_{DD\_HV\_ADC0}$ $V_{DD\_HV\_ADC1}$	3.3 V to 5.5V ADC supply voltage	—	–0.3	6.0	V
$V_{SS\_HV\_ADC0}$ $V_{SS\_HV\_ADC1}$	3.3V to 5.5V ADC supply ground	—	–0.1	0.1	V
V_{DD_LV}[9, 10, 11, 12]	Core logic supply voltage	—	–0.3	1.32	V
V_{INA}	Voltage on analog pin with respect to ground (V_{SS_HV})	—	–0.3	Min ($V_{DD\_HV\_x}$, $V_{DD\_HV\_ADCx}$, $V_{DD\_ADCx\_REF}$) +0.3	V
V_{IN}	Voltage on any digital pin with respect to ground (V_{SS_HV})	Relative to $V_{DD\_HV\_A}$, $V_{DD\_HV\_B}$, $V_{DD\_HV\_C}$	–0.3	$V_{DD\_HV\_x}$ + 0.3	V
I_{INJPAD}	Injected input current on any pin during overload condition	Always	–5	5	mA
I_{INJSUM}	Absolute sum of all injected input currents during overload condition	—	–50	50	mA
T_{ramp}	Supply ramp rate	—	0.5 V / min	100V/ms	—
T_A[13]	Ambient temperature	—	-40	125	°C
T_{STG}	Storage temperature	—	–55	165	°C

1. All voltages are referred to VSS_HV unless otherwise specified
2. VDD_HV_B and VDD_HV_C are common together on the 176 LQFP-EP package.
3. Allowed $V_{DD\_HV\_x}$ = 5.5–6.0 V for 60 seconds cumulative time with no restrictions, for 10 hours cumulative time device in reset, T_J= 150 °C, remaining time at or below 5.5 V.
4. VDD_HV_FLA must be connected to VDD_HV_A when VDD_HV_A = 3.3V
5. VDD_HV_FLA must be disconnected from ANY power sources when VDD_HV_A = 5V
6. This pin should be decoupled with low ESR 1 µF capacitor.
7. Not available for input voltage, only for decoupling internal regulators
8. 10-bit ADC does not have dedicated reference and its reference is bonded to 10-bit ADC supply(VDD_HV_ADC0) inside the package.
9. Allowed 1.45 – 1.5 V for 60 seconds cumulative time at maximum T_J = 150 °C, remaining time as defined in footnotes 10 and 11.
10. Allowed 1.38 – 1.45 V– for 10 hours cumulative time at maximum T_J = 150 °C, remaining time as defined in footnote 11.
11. 1.32 – 1.38 V range allowed periodically for supply with sinusoidal shape and average supply value below 1.326 V at maximum T_J = 150 °C.
12. If HVD on core supply ($V_{HVD\_LV\_x}$) is enabled, it will generate a reset when supply goes above threshold.
13. T_J=150°C. Assumes T_A=125°C
    - Assumes maximum θJA for 2s2p board. See Thermal attributes

4.2 Recommended operating conditions

The following table describes the operating conditions for the device, and for which all specifications in the data sheet are valid, except where explicitly noted. The device operating conditions must not be exceeded in order to guarantee proper operation and reliability. The ranges in this table are design targets and actual data may vary in the given range.

NOTE

- For normal device operations, all supplies must be within operating range corresponding to the range mentioned in following tables. This is required even if some of the features are not used.
- If VDD_HV_A is in 5.0V range, VDD_HV_FLA should be externally supplied using a 3.3V source. If VDD_HV_A is in 3.3V range, VDD_HV_FLA should be shorted to VDD_HV_A.
- VDD_HV_A, VDD_HV_B and VDD_HV_C are all independent supplies and can each be set to 3.3V or 5V. The following tables: 'Recommended operating conditions (VDD_HV_x = 3.3 V)' and table 'Recommended operating conditions (VDD_HV_x = 5 V)' specify their ranges when configured in 3.3V or 5V respectively.

Table 7. Recommended operating conditions ($V_{DD\_HV\_x}$ = 3.3 V)

Symbol	Parameter	Conditions[1]	Min[2]	Max	Unit
$V_{DD\_HV\_A}$ $V_{DD\_HV\_B}$ $V_{DD\_HV\_C}$	HV IO supply voltage	—	3.15	3.6	V
$V_{DD\_HV\_FLA}$[3]	HV flash supply voltage	—	3.15	3.6	V
$V_{DD\_HV\_ADC1\_REF}$	HV ADC1 high reference voltage	—	3.0	5.5	V
$V_{DD\_HV\_ADC0}$ $V_{DD\_HV\_ADC1}$	HV ADC supply voltage	—	max(VDD_HV_A,VDD_HV_B,VDD_HV_C) - 0.05	3.6	V
$V_{SS\_HV\_ADC0}$ $V_{SS\_HV\_ADC1}$	HV ADC supply ground	—	-0.1	0.1	V
V_{DD_LV}[4, 5]	Core supply voltage	—	1.2	1.32	V
$V_{IN1\_CMP\_REF}$[6, 7]	Analog Comparator DAC reference voltage	—	3.15	3.6	V
I_{INJPAD}	Injected input current on any pin during overload condition	—	-3.0	3.0	mA

Table continues on the next page...

Table 7. Recommended operating conditions ($V_{DD\_HV\_x}$ = 3.3 V) (continued)

Symbol	Parameter	Conditions[1]	Min[2]	Max	Unit
T_A[8]	Ambient temperature under bias	f_{CPU} ≤ 160 MHz	–40	125	°C
T_J	Junction temperature under bias	—	–40	150	°C

1. All voltages are referred to V_{SS_HV} unless otherwise specified
2. Device will be functional down (and electrical specifications as per various datasheet parameters will be guaranteed) to the point where one of the LVD/HVD resets the device. When voltage drops outside range for an LVD/HVD, device is reset.
3. VDD_HV_FLA must be connected to VDD_HV_A when VDD_HV_A = 3.3V
4. Only applicable when supplying from external source.
5. VDD_LV supply pins should never be grounded (through a small impedance). If these are not driven, they should only be left floating.
6. VIN1_CMP_REF ≤ VDD_HV_A
7. This supply is shorted VDD_HV_A on lower packages.
8. T_J=150°C. Assumes T_A=125°C
   - Assumes maximum θJA of 2s2p board. See Thermal attributes

NOTE

If VDD_HV_A is in 5V range, it is necessary to use internal Flash supply 3.3V regulator. VDD_HV_FLA should not be supplied externally and should only have decoupling capacitor.

Table 8. Recommended operating conditions ($V_{DD\_HV\_x}$ = 5 V)

Symbol	Parameter	Conditions [1]	Min[2]	Max	Unit
$V_{DD\_HV\_A}$ $V_{DD\_HV\_B}$ $V_{DD\_HV\_C}$	HV IO supply voltage	—	4.5	5.5	V
$V_{DD\_HV\_FLA}$[3]	HV flash supply voltage	—	3.15	3.6	V
$V_{DD\_HV\_ADC1\_REF}$	HV ADC1 high reference voltage	—	3.15	5.5	V
$V_{DD\_HV\_ADC0}$ $V_{DD\_HV\_ADC1}$	HV ADC supply voltage	—	max(VDD_HV_A,VDD_HV_B,VDD_HV_C) - 0.05	5.5	V
$V_{SS\_HV\_ADC0}$ $V_{SS\_HV\_ADC1}$	HV ADC supply ground	—	-0.1	0.1	V
V_{DD_LV}[4]	Core supply voltage	—	1.2	1.32	V
$V_{IN1\_CMP\_REF}$[6]	Analog Comparator DAC reference voltage	—	3.15	5.5[5]	V
I_{INJPAD}	Injected input current on any pin during overload condition	—	-3.0	3.0	mA
T_A[7]	Ambient temperature under bias	f_{CPU} ≤ 160 MHz	–40	125	°C
T_J	Junction temperature under bias	—	–40	150	°C

1. All voltages are referred to V_{SS_HV} unless otherwise specified
2. Device will be functional down (and electrical specifications as per various datasheet parameters will be guaranteed) to the point where one of the LVD/HVD resets the device. When voltage drops outside range for an LVD/HVD, device is reset.
3. When VDD_HV is in 5 V range, VDD_HV_FLA cannot be supplied externally.This pin is decoupled with C_{flash_reg}.

4. VDD_LV supply pins should never be grounded (through a small impedance). If these are not driven, they should only be left floating
5. VIN1_CMP_REF ≤ VDD_HV_A
6. This supply is shorted VDD_HV_A on lower packages.
7. T_J=150°C. Assumes T_A=125°C
   - Assumes maximum θJA of 2s2p board. See Thermal attributes

4.3 Voltage regulator electrical characteristics

The voltage regulator is composed of the following blocks:

- Choice of generating supply voltage for the core area.
  - Control of external NPN ballast transistor
  - Generating core supply using internal ballast transistor
  - Connecting an external 1.25 V (nominal) supply directly without the NPN ballast
- Internal generation of the 3.3 V flash supply when device connected in 5V applications
- External bypass of the 3.3 V flash regulator when device connected in 3.3V applications
- Low voltage detector - low threshold (LVD_IO_A_LO) for $V_{DD\_HV\_IO\_A\ supply}$
- Low voltage detector - high threshold (LVD_IO_A_Hi) for $V_{DD\_HV\_IO\_A\ supply}$
- Low voltage detector (LVD_FLASH) for 3.3 V flash supply (VDD_HV_FLA)
- Various low voltage detectors (LVD_LV_x)
- High voltage detector (HVD_LV_cold) for 1.2 V digital core supply (VDD_LV)
- Power on Reset (POR_LV) for 1.25 V digital core supply (VDD_LV)
- Power on Reset (POR_HV) for 3.3 V to 5 V supply (VDD_HV_A)

The following bipolar transistors[1] are supported, depending on the device performance requirements. As a minimum the following must be considered when determining the most appropriate solution to maintain the device under its maximum power dissipation capability: current, ambient temperature, mounting pad area, duty cycle and frequency for Idd, collector voltage, etc

1. BCP56, MCP68 and MJD31are guaranteed ballasts.

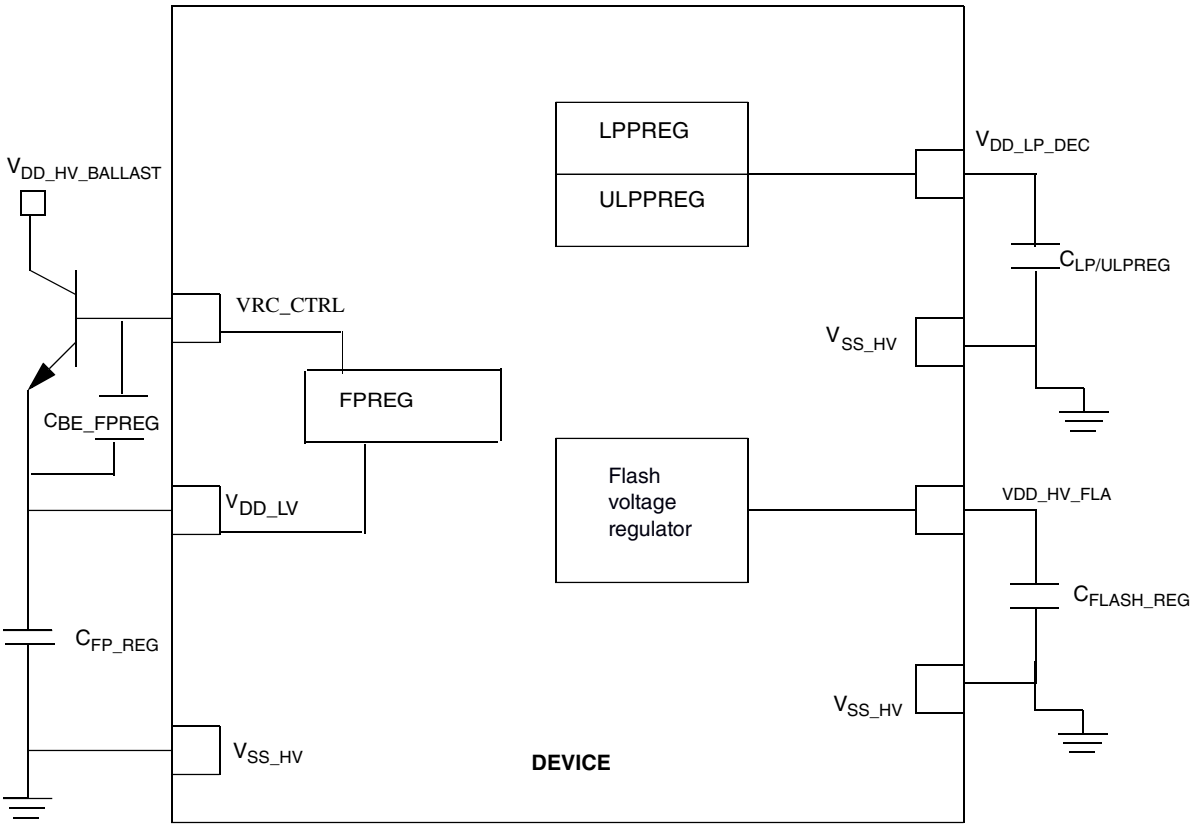


Figure 2. Voltage regulator capacitance connection

NOTE

On BGA, VSS_LV and VSS_HV have been joined on substrate and renamed as VSS.

Table 9. Voltage regulator electrical specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{fp_reg}[1]	External decoupling / stability capacitor	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1.32	2.2[2]	3	µF
	Combined ESR of external capacitor	—	0.001	—	0.03	Ohm
C_{lp/ulp_reg}	External decoupling / stability capacitor for internal low power regulators	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	0.8	1	1.4	µF
	Combined ESR of external capacitor	—	0.001	—	0.1	Ohm
C_{be_fpreg}[3]	Capacitor in parallel to base-emitter	BCP68 and BCP56		3.3		nF
		MJD31		4.7		

Table continues on the next page...

Table 9. Voltage regulator electrical specifications (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{flash_reg}[4]	External decoupling / stability capacitor for internal Flash regulators	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1.32	2.2	3	µF
	Combined ESR of external capacitor	—	0.001	—	0.03	Ohm
$C_{HV\_VDD\_A}$	VDD_HV_A supply capacitor [5]	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1	—	—	µF
$C_{HV\_VDD\_B}$	VDD_HV_B supply capacitor[5]	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1	—	—	µF
$C_{HV\_VDD\_C}$	VDD_HV_C supply capacitor[5]	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1	—	—	µF
C_{HV_ADC0} C_{HV_ADC1}	HV ADC supply decoupling capacitances	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1	—	—	µF
C_{HV_ADR}[6]	HV ADC SAR reference supply decoupling capacitances	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	0.47	—	—	µF
$V_{DD\_HV\_BALLAST}$[7]	FPREG Ballast collector supply voltage	When collector of NPN ballast is directly supplied by an on board supply source (not shared with VDD_HV_A supply pin) without any series resistance, that is, $R_{C\_BALLAST}$ less than 0.01 Ohm.	2.25	—	5.5	V
$R_{C\_BALLAST}$	Series resistor on collector of FPREG ballast	When VDD_HV_BALLAST is shorted to VDD_HV_A on the board	—	—	0.1	Ohm
t_{SU}	Start-up time with external ballastafter main supply (VDD_HV_A) stabilization	Cfp_reg = 3 µF	—	74	—	µs
t_{SU_int}	Start-up time with internal ballast after main supply (VDD_HV_A) stabilization	Cfp_reg = 3 µF	—	103	—	µs
t_{ramp}	Load current transient	Iload from 15% to 55% C_{fp_reg} = 3 µF		1.0		µs

1. Split capacitance on each pair VDD_LV pin should sum up to a total value of C_{fp_reg}
2. Typical values will vary over temperature, voltage, tolerance, drift, but total variation must not exceed minimum and maximum values.
3. Ceramic X7R or X5R type with capacitance-temperature characteristics +/-15% of -55 degC to +125degC is recommended. The tolerance +/-20% is acceptable.
4. It is required to minimize the board parasitic inductance from decoupling capacitor to VDD_HV_FLA pin and the routing inductance should be less than 1nH.

5. 1. For VDD_HV_x, 1µf on each side of the chip
      a. 0.1 µf close to each VDD/VSS pin pair.
      b. 10 µf near for each power supply source
      c. For VDD_LV, 0.1uf close to each VDD/VSS pin pair is required. Depending on the the selected regulation mode, this amount of capacitance will need to be subtracted from the total capacitance required by the regulator for e.g., as specified by CFP_REG parameter.
   2. For VDD_LV, 0.1uf close to each VDD/VSS pin pair is required. Depending on the the selected regulation mode, this amount of capacitance will need to be subtracted from the total capacitance required by the regulator for e.g., as specified by CFP_REG parameter
6. Only applicable to ADC1
7. In external ballast configuration the following must be ensured during power-up and power-down (Note: If $V_{DD\_HV\_BALLAST}$ is supplied from the same source as VDD_HV_A this condition is implicitly met):
   - During power-up, $V_{DD\_HV\_BALLAST}$ must have met the min spec of 2.25V before VDD_HV_A reaches the POR_HV_RISE min of 2.75V.
   - During power-down, $V_{DD\_HV\_BALLAST}$ must not drop below the min spec of 2.25V until VDD_HV_A is below POR_HV_FALL min of 2.7V.

NOTE

For a typical configuration using an external ballast transistor with separate supply for VDD_HV_A and the ballast collector, a bulk storage capacitor (as defined in Table 9) is required on VDD_HV_A close to the device pins to ensure a stable supply voltage.

Extra care must be taken if the VDD_HV_A supply is also being used to power the external ballast transistor or the device is running in internal regulation mode. In these modes, the inrush current on device Power Up or on exit from Low Power Modes is significant and may cause the VDD_HV_A voltage to drop resulting in an LVD reset event. To avoid this, the board layout should be optimized to reduce common trace resistance or additional capacitance at the ballast transistor collector (or VDD_HV_A pins in the case of internal regulation mode) is required. NXP recommends that customers simulate the external voltage supply circuitry.

In all circumstances, the voltage on VDD_HV_A must be maintained within the specified operating range (see Recommended operating conditions) to prevent LVD events.

4.4 Voltage monitor electrical characteristics

Table 10. Voltage monitor electrical characteristics

Symbol	Parameter	State	Conditions	Configuration			Threshold			Unit
				Power Up [1]	Mask Opt[2]	Reset Type	Min	Typ	Max	V
V_{POR_LV}	LV supply power on reset detector	Fall	Untrimmed	Yes	No	POR	0.930	0.979	1.028	V
			Trimmed				-	-	-	V
		Rise	Untrimmed				0.980	1.029	1.078	V
			Trimmed				-	-	-	V
$V_{HVD\_LV\_cold}$	LV supply high voltage monitoring, detecting at device pin	Fall	Untrimmed	No	Yes	Functional	Disabled at Start			
			Trimmed				1.325	1.345	1.375	V
		Rise	Untrimmed				Disabled at Start			
			Trimmed				1.345	1.365	1.395	V
$V_{LVD\_LV\_PD2\_hot}$	LV supply low voltage monitoring, detecting on the PD2 core (hot) area	Fall	Untrimmed	Yes	No	POR	1.0800	1.1200	1.1600	V
			Trimmed				1.1250	1.1425	1.1600	V
		Rise	Untrimmed				1.1000	1.1400	1.1800	V
			Trimmed				1.1450	1.1625	1.1800	V
$V_{LVD\_LV\_PD1\_hot\ (BGFP)}$	LV supply low voltage monitoring, detecting on the PD1 core (hot) area	Fall	Untrimmed	Yes	No	POR	1.0800	1.1200	1.1600	V
			Trimmed				1.1140	1.1370	1.1600	V
		Rise	Untrimmed				1.1000	1.140	1.1800	V
			Trimmed				1.1340	1.1570	1.1800	V
$V_{LVD\_LV\_PD0\_hot\ (BGFP)}$	LV supply low voltage monitoring, detecting on the PD0 core (hot) area	Fall	Untrimmed	Yes	No	POR	1.0800	1.1200	1.1600	V
			Trimmed				1.1140	1.1370	1.1600	V
		Rise	Untrimmed				1.1000	1.1400	1.1800	V
			Trimmed				1.1340	1.1570	1.1800	V
V_{POR_HV}	HV supply power on reset detector	Fall	Untrimmed	Yes	No	POR	2.7000	2.8500	3.0000	V
			Trimmed				-	-	-	V
		Rise	Untrimmed				2.7500	2.9000	3.0500	V
			Trimmed				-	-	-	V
$V_{LVD\_IO\_A\_LO}$ [3]	HV IO_A supply low voltage monitoring - low range	Fall	Untrimmed	Yes	No	POR	2.7500	2.9230	3.0950	V
			Trimmed				2.9780	3.0390	3.1000	V
		Rise	Untrimmed				2.7800	2.9530	3.1250	V
			Trimmed				3.0080	3.0690	3.1300	V
$V_{LVD\_IO\_A\_HI}$[3]	HV IO_A supply low voltage monitoring - high range	Fall	Trimmed	No	Yes	Functional	Disabled at Start			
							4.0600	4.151	4.2400	V
		Rise	Trimmed				Disabled at Start			
							4.1150	4.2010	4.3000	V

Table continues on the next page...

Table 10. Voltage monitor electrical characteristics (continued)

Symbol	Parameter	State	Conditions	Configuration			Threshold			Unit
				Power Up [1]	Mask Opt[2]	Reset Type	Min	Typ	Max	V
$V_{LVD\_LV\_PD2\_cold}$	LV supply low voltage monitoring, detecting at the device pin	Fall	Untrimmed	No	Yes	Functional	Disabled at Start			
			Trimmed				1.1400	1.1550	1.1750	V
		Rise	Untrimmed				Disabled at Start			
			Trimmed				1.1600	1.1750	1.1950	V

1. All monitors that are active at power-up will gate the power up recovery and prevent exit from POWERUP phase until the minimum level is crossed. These monitors can in some cases be masked during normal device operation, but when active will always generate a POR reset.
2. Voltage monitors marked as non maskable are essential for device operation and hence cannot be masked.
3. There is no voltage monitoring on the $V_{DD\_HV\_ADC0}$, $V_{DD\_HV\_ADC1}$, $V_{DD\_HV\_B}$ and $V_{DD\_HV\_C}$ I/O segments. For applications requiring monitoring of these segments, either connect these to $V_{DD\_HV\_A}$ at the PCB level or monitor externally.

4.5 Supply current characteristics

Current consumption data is given in the following table. These specifications are design targets and are subject to change per device characterization.

NOTE

The ballast must be chosen in accordance with the ballast transistor supplier operating conditions and recommendations.

Table 11. Current consumption characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
$I_{DD\_BODY\_1}$ 2, 3	RUN Body Mode Profile Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies[4] T_a = 125°C [5] V_{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 80MHz	—	—	147	mA
		T_a = 105°C	—	—	142	mA
		T_a = 85 °C	—	—	137	mA
$I_{DD\_BODY\_2}$ 6	RUN Body Mode Profile Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies[4] T_a = 125°C[5] V_{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 160MHz	—	—	246	mA

Table continues on the next page...

Table 11. Current consumption characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
		T_a = 105°C	—	—	235	mA
		T_a = 85°C	—	—	210	mA
$I_{DD\_BODY\_3}$ [7]	RUN Body Mode Profile Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies[4] T_a = 125 °C [5] V_{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 120MHz	—	—	181	mA
		T_a = 105 °C	—	—	176	mA
		T_a = 85°C	—	—	171	mA
$I_{DD\_BODY\_4}$[8]	RUN Body Mode Profile Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies[4] T_a = 125 °C [5] V_{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 120MHz	—	—	264	mA
		T_a = 105 °C	—	—	176	mA
		T_a = 85 °C	—	—	171	mA
I_{DD_STOP}	STOP mode Operating current	T_a = 125 °C[9] V_{DD_LV} = 1.25 V	—	—	49	mA
		T_a = 105 °C V_{DD_LV} = 1.25 V	—	10.6	—	
		T_a = 85 °C V_{DD_LV} = 1.25 V	—	8.1	—	
		T_a = 25 °C V_{DD_LV} = 1.25 V	—	4.6	—	
$I_{DD\_HV\_ADC\_REF}$[10, 11]	ADC REF Operating current	T_a = 125 °C[5] 2 ADCs operating at 80 MHz $V_{DD\_HV\_ADC\_REF}$ = 5.5 V	—	200	400	µA
		T_a = 105 °C 2 ADCs operating at 80 MHz $V_{DD\_HV\_ADC\_REF}$ = 5.5 V	—	200	—	
		T_a = 85 °C 2 ADCs operating at 80 MHz $V_{DD\_HV\_ADC\_REF}$ = 5.5 V	—	200	—	
		T_a = 25 °C 2 ADCs operating at 80 MHz	—	200	—	

Table continues on the next page...

Table 11. Current consumption characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
		$V_{DD\_HV\_ADC\_REF}$ = 3.6 V				
$I_{DD\_HV\_ADCx}$[11]	ADC HV Operating current	T_a = 125 °C[5] ADC operating at 80 MHz $V_{DD\_HV\_ADC}$ = 5.5 V	—	1.2	2	mA
		T_a = 25 °C ADC operating at 80 MHz $V_{DD\_HV\_ADC}$ = 3.6 V	—	1	2	
$I_{DD\_HV\_FLASH}$[12]	Flash Operating current during read access	T_a = 125 °C[5] 3.3 V supplies 160 MHz frequency	—	40	45	mA
		T_a = 105 °C 3.3 V supplies 160 MHz frequency	—	40	45	
		T_a = 85 °C 3.3 V supplies 160 MHz frequency	—	40	45	

1. The content of the Conditions column identifies the components that draw the specific current.
2. Single e200Z4 core cache disabled @80 MHz, no FlexRay, no ENET, 2 x CAN, 8 LINFlexD, 2 SPI, ADC0 and 1 used constantly, no HSM, Memory: 2M flash, 128K RAM RUN mode, Clocks: FIRC on, XOSC, PLL on, SIRC on for TOD, no 32KHz crystal (TOD runs off SIRC).
3. Recommended Transistors:MJD31 @ 85°C, 105°C and 125°C. In case of internal ballast mode, it is expected that the external ballast is not mounted and BAL_SELECT_INT pin is tied to VDD_HV_A supply on board. Internal ballast can be used for all use cases with current consumption upto 150mA. For internal ballast configuration the VRC_CTL pin should be left floating.
4. The power consumption does not consider the dynamic current of I/Os
5. Tj=150°C. Assumes Ta=125°C
   - Assumes maximum θJA of 2s2p board. SeeThermal attributes
6. e200Z4 core, 160MHz, cache enabled; e200Z2 core , 80MHz, no FlexRay, no ENET, 7 CAN, 16 LINFlexD, 4 SPI, 1x ADC used constantly, includes HSM at start-up / periodic use, Memory: 3M flash, 256K RAM, Clocks: FIRC on, XOSC on, PLL on, SIRC on, no 32KHz crystal
7. e200Z4 core, 120MHz, cache enabled; e200Z2 core, 60MHz; no FlexRay, no ENET, 7 CAN, 16 LINFlexD, 4 SPI, 1x ADC used constantly, includes HSM at start-up / periodic use, Memory: 3M flash, 128K RAM, Clocks: FIRC on, XOSC on, PLL on, SIRC on, no 32KHz crystal
8. e200Z4 core, 160MHz, cache enabled; e200Z4 core, 80MHz; HSM fully operational (Z0 core @80MHz) FlexRay, 5x CAN, 5x LINFlexD, 2x SPI, 1x ADC used constantly, 1xeMIOS (5 ch), Memory: 3M flash, 384K RAM, Clocks: FIRC on, XOSC on, PLL on, SIRC on, no 32KHz crystal
9. Assuming Ta=Tj, as the device is in Stop mode. Assumes maximum θJA of 2s2p board. SeeThermal attributes.
10. Internal structures hold the input voltage less than $V_{DD\_HV\_ADC\_REF}$ + 1.0 V on all pads powered by V_{DDA} supplies, if the maximum injection current specification is met (3 mA for all pins) and V_{DDA} is within the operating voltage specifications.
11. This value is the total current for two ADCs.Each ADC might consume upto 2mA at max.
12. This assumes the default configuration of flash controller register. For more details, refer to Flash memory program and erase specifications

Table 12. Low Power Unit (LPU) Current consumption characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
LPU_RUN	with 256K RAM	T_a = 25 °C SYS_CLK = 16MHz ADC0 = OFF, SPI0 = OFF, LIN0 = OFF, CAN0 = OFF	—	10	—	mA
		T_a = 85 °C SYS_CLK = 16MHz ADC0 = ON, SPI0 = ON, LIN0 = ON, CAN0 = ON	—	10.5	—	
		T_a = 105 °C SYS_CLK = 16MHz ADC0 = ON, SPI0 = ON, LIN0 = ON, CAN0 = ON	—	11	—	
		T_a = 125 °C[2] SYS_CLK = 16MHz ADC0 = ON, SPI0 = ON, LIN0 = ON, CAN0 = ON	—	—	26	
LPU_STOP	with 256K RAM	T_a = 25 °C	—	0.18	—	mA
		T_a = 85 °C	—	0.60	—	
		T_a = 105 °C	—	1.00	—	
		T_a = 125 °C [2]	—	—	10.6	

1. The content of the Conditions column identifies the components that draw the specific current.
2. Assuming Ta=Tj, as the device is in static (fully clock gated) mode. Assumes maximum θJA of 2s2p board. SeeThermal attributes

Table 13. STANDBY Current consumption characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
STANDBY0	STANDBY with 8K RAM	T_a = 25 °C	—	71	—	µA
		T_a = 85 °C	—	125	700	
		T_a = 105 °C	—	195	1225	
		T_a = 125 °C [2]	—	314	2100	
STANDBY1	STANDBY with 64K RAM	T_a = 25 °C	—	72	—	µA
		T_a = 85 °C	—	140	715	
		T_a = 105 °C	—	225	1275	
		T_a = 125 °C [2]	—	358	2250	
STANDBY2	STANDBY with 128K RAM	T_a = 25 °C	—	75	—	µA
		T_a = 85 °C	—	155	730	
		T_a = 105 °C	—	255	1350	
		T_a = 125 °C [2]	—	396	2600	
STANDBY3	STANDBY with 256K RAM	T_a = 25 °C	—	80	—	µA
		T_a = 85 °C	—	180	800	
		T_a = 105 °C	—	290	1425	
		T_a = 125 °C [2]	—	465	2900	
STANDBY3	FIRC ON	T_a = 25 °C	—	500	—	µA

1. The content of the Conditions column identifies the components that draw the specific current.
2. Assuming Ta=Tj, as the device is in static (fully clock gated) mode. Assumes maximum θJA of 2s2p board. SeeThermal attributes

NOTE

For the Precision channel Analog inputs, SIUL2_MSCRn[PUS] must be configured to 0 before entering STANDBY. An increase in current would be observed when SIUL2_MSCRn[PUS] is configured to be 1, irrespective of the state of IBE or PUE. The current numbers would increase irrespective of whether the pad is pulled low/high externally.

4.6 Electrostatic discharge (ESD) characteristics

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

NOTE

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 14. ESD ratings

Symbol	Parameter	Conditions[1]	Class	Max value[2]	Unit
$V_{ESD(HBM)}$	Electrostatic discharge (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500 750 (corners)	V

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. Data based on characterization results, not tested in production.

4.7 Electromagnetic Compatibility (EMC) specifications

EMC measurements to IC-level IEC standards are available from NXP on request.

5 I/O parameters

5.1 AC specifications @ 3.3 V Range

Table 15. Functional Pad AC Specifications @ 3.3 V Range

Symbol	Prop. Delay (ns)[1] L>H/H>L		Rise/Fall Edge (ns)		Drive Load (pF)	SIUL2_MSCRn[SRC 1:0]
	Min	Max	Min	Max		MSB,LSB
pad_sr_hv (output)		6/6		1.9/1.5	25	11
	2.5/2.5	8.25/7.5	0.8/0.6	3.25/3	50	
	6.4/5	19.5/19.5	3.5/2.5	12/12	200	
	2.2/2.5	8/8	0.55/0.5	3.9/3.5	25	10
	0.090	1.1	0.035	1.1	asymmetry[2]	
	2.9/3.5	12.5/11	1/1	7/6	50	
	11/8	35/31	7.7/5	25/21	200	
	8.3/9.6	45/45	4/3.5	25/25	50	01
	13.5/15	65/65	6.3/6.2	30/30	200	
	13/13	75/75	6.8/6	40/40	50	00[3]
	21/22	100/100	11/11	51/51	200	
pad_i_hv/ pad_sr_hv (input)[4]		2/2		0.5/0.5	0.5	NA

1. As measured from 50% of core side input to Voh/Vol of the output
2. This row specifies the min and max asymmetry between both the prop delay and the edge rates for a given PVT and 25pF load. Required for the Flexray spec.
3. Slew rate control modes
4. Input slope = 2ns

NOTE

The specification given above is based on simulation data into an ideal lumped capacitor. Customer should use IBIS models for their specific board/loading conditions to simulate the expected signal integrity and edge rates of their system.

NOTE

The specification given above is measured between 20% / 80%.

5.2 DC electrical specifications @ 3.3V Range

Table 16. DC electrical specifications @ 3.3V Range

Symbol	Parameter	Value		Unit
		Min	Max	
Vih (pad_i_hv)	Pad_I_HV Input Buffer High Voltage	0.72*VDD_HV_x	VDD_HV_x + 0.3	V
Vil (pad_i_hv)	Pad_I_HV Input Buffer Low Voltage	VDD_HV_x - 0.3	0.45*VDD_HV_x	V
Vhys (pad_i_hv)	Pad_I_HV Input Buffer Hysteresis	0.11*VDD_HV_x		V
Vih_hys	CMOS Input Buffer High Voltage (with hysteresis enabled)	0.67*VDD_HV_x	VDD_HV_x + 0.3	V
Vil_hys	CMOS Input Buffer Low Voltage (with hysteresis enabled)	VDD_HV_x - 0.3	0.35*VDD_HV_x	V
Vih	CMOS Input Buffer High Voltage (with hysteresis disabled)	0.57 * VDD_HV_x[1]	VDD_HV_x[1] + 0.3	V
Vil	CMOS Input Buffer Low Voltage (with hysteresis disabled)	VDD_HV_x - 0.3	0.4 * VDD_HV_x[1]	V
Vhys	CMOS Input Buffer Hysteresis	0.09 * VDD_HV_x[1]		V
Pull_IIH (pad_i_hv)	Weak Pullup Current[2] Low	15		µA
Pull_IIH (pad_i_hv)	Weak Pullup Current[3] High		55	µA
Pull_IIL (pad_i_hv)	Weak Pulldown Current[3] Low	28		µA
Pull_IIL (pad_i_hv)	Weak Pulldown Current[2] High		85	µA
Pull_Ioh	Weak Pullup Current[4]	15	50	µA
Pull_Iol	Weak Pulldown Current[5]	15	50	µA
Iinact_d	Digital Pad Input Leakage Current (weak pull inactive)	-2.5	2.5	µA
Voh	Output High Voltage[6]	0.8 *VDD_HV_x[1]	—	V
Vol	Output Low Voltage[7] Output Low Voltage[8]	—	0.2 *VDD_HV_x[1] 0.1 *VDD_HV_x	V
Ioh_f	Full drive Ioh[9] (SIUL2_MSCRn.SRC[1:0] = 11)	18	70	mA
Iol_f	Full drive Iol[9] (SIUL2_MSCRn.SRC[1:0] = 11)	21	120	mA
Ioh_h	Half drive Ioh[9] (SIUL2_MSCRn.SRC[1:0] = 10)	9	35	mA
Iol_h	Half drive Iol[9] (SIUL2_MSCRn.SRC[1:0] = 10)	10.5	60	mA

1. VDD_HV_x = VDD_HV_A, VDD_HV_B, VDD_HV_C
2. Measured when pad=0.69*VDD_HV_x
3. Measured when pad=0.49*VDD_HV_x
4. Measured when pad = 0 V
5. Measured when pad = VDD_HV_x
6. Measured when pad is sourcing 2 mA
7. Measured when pad is sinking 2 mA
8. Measured when pad is sinking 1.5 mA
9. Ioh/Iol is derived from spice simulations. These values are NOT guaranteed by test.

5.3 AC specifications @ 5 V Range

Table 17. Functional Pad AC Specifications @ 5 V Range

Symbol	Prop. Delay (ns)[1] L>H/H>L		Rise/Fall Edge (ns)		Drive Load (pF)	SIUL2_MSCRn[SRC 1:0]
	Min	Max	Min	Max		MSB,LSB
pad_sr_hv (output)		4.5/4.5		1.3/1.2	25	11
		6/6		2.5/2	50	
		13/13		9/9	200	
		5.25/5.25		3/2	25	10
		9/8		5/4	50	
		22/22		18/16	200	
		27/27		13/13	50	01[2]
		40/40		24/24	200	
		40/40		24/24	50	00[2]
		65/65		40/40	200	
pad_i_hv/ pad_sr_hv (input)		1.5/1.5		0.5/0.5	0.5	NA

1. As measured from 50% of core side input to Voh/Vol of the output
2. Slew rate control modes

NOTE

The above specification is based on simulation data into an ideal lumped capacitor. Customer should use IBIS models for their specific board/loading conditions to simulate the expected signal integrity and edge rates of their system.

NOTE

The above specification is measured between 20% / 80%.

5.4 DC electrical specifications @ 5 V Range

Table 18. DC electrical specifications @ 5 V Range

Symbol	Parameter	Value		Unit
		Min	Max	
Vih (pad_i_hv)	pad_i_hv Input Buffer High Voltage	0.7*VDD_HV_x	VDD_HV_x + 0.3	V

Table continues on the next page...

Table 18. DC electrical specifications @ 5 V Range (continued)

Symbol	Parameter	Value		Unit
		Min	Max	
Vil (pad_i_hv)	pad_i_hv Input Buffer Low Voltage	VDD_HV_x - 0.3	0.45*VDD_HV_x	V
Vhys (pad_i_hv)	pad_i_hv Input Buffer Hysteresis	0.09*VDD_HV_x		V
Vih_hys	CMOS Input Buffer High Voltage (with hysteresis enabled)	0.65* VDD_HV_x	VDD_HV_x + 0.3	V
Vil_hys	CMOS Input Buffer Low Voltage (with hysteresis enabled)	VDD_HV_x - 0.3	0.35*VDD_HV_x	V
Vih	CMOS Input Buffer High Voltage (with hysteresis disabled)	0.55 * VDD_HV_x[1]	VDD_HV_x[1] + 0.3	V
Vil	CMOS Input Buffer Low Voltage (with hysteresis disabled)	VDD_HV_x - 0.3	0.40 * VDD_HV_x[1]	V
Vhys	CMOS Input Buffer Hysteresis	0.09 * VDD_HV_x[1]		V
Pull_IIH (pad_i_hv)	Weak Pullup Current[2] Low	23		µA
Pull_IIH (pad_i_hv)	Weak Pullup Current[3] High		82	µA
Pull_IIL (pad_i_hv)	Weak Pulldown Current[3] Low	40		µA
Pull_IIL (pad_i_hv)	Weak Pulldown Current[2] High		130	µA
Pull_Ioh	Weak Pullup Current[4]	30	80	µA
Pull_Iol	Weak Pulldown Current[5]	30	80	µA
Iinact_d	Digital Pad Input Leakage Current (weak pull inactive)	-2.5	2.5	µA
Voh	Output High Voltage[6]	0.8 * VDD_HV_x[1]	—	V
Vol	Output Low Voltage[7] Output Low Voltage[8]	—	0.2*VDD_HV_x 0.1*VDD_HV_x	V
Ioh_f	Full drive Ioh[9] (SIUL2_MSCRn.SRC[1:0] = 11)	18	70	mA
Iol_f	Full drive Iol[9] (SIUL2_MSCRn.SRC[1:0] = 11)	21	120	mA
Ioh_h	Half drive Ioh[9] (SIUL2_MSCRn.SRC[1:0] = 10)	9	35	mA
Iol_h	Half drive Iol[9] (SIUL2_MSCRn.SRC[1:0] = 10)	10.5	60	mA

1. VDD_HV_x = VDD_HV_A, VDD_HV_B, VDD_HV_C
2. Measured when pad=0.69*VDD_HV_x
3. Measured when pad=0.49*VDD_HV_x
4. Measured when pad = 0 V
5. Measured when pad = VDD_HV_x
6. Measured when pad is sourcing 2 mA
7. Measured when pad is sinking 2 mA
8. Measured when pad is sinking 1.5 mA
9. Ioh/Iol is derived from spice simulations. These values are NOT guaranteed by test.

5.5 Reset pad electrical characteristics

The device implements a dedicated bidirectional RESET pin.

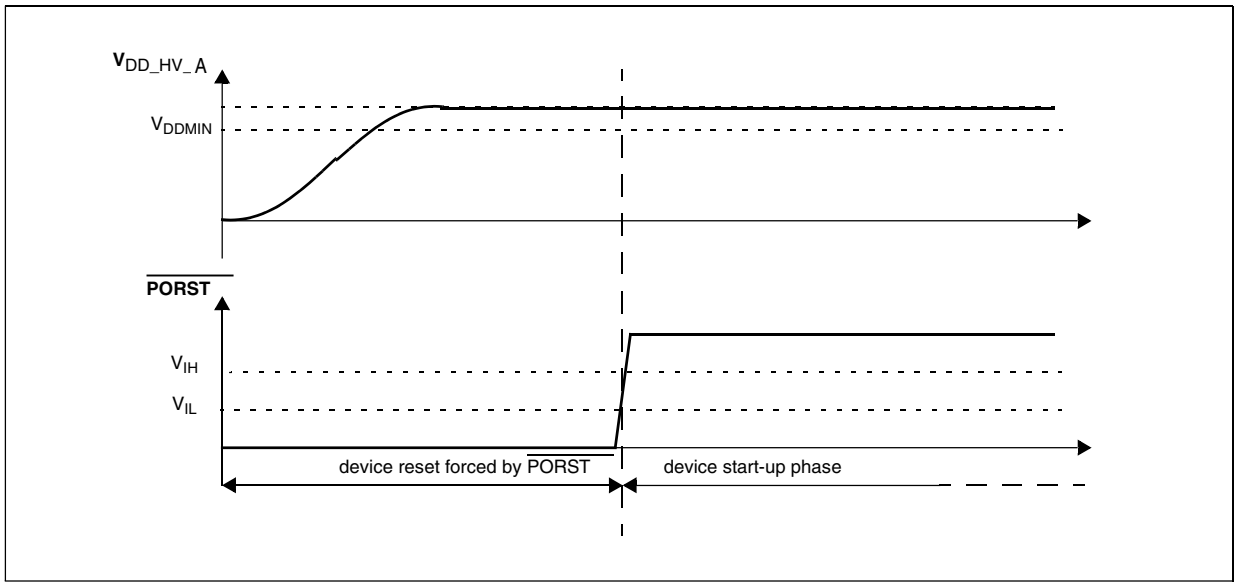


Figure 3. Start-up reset requirements

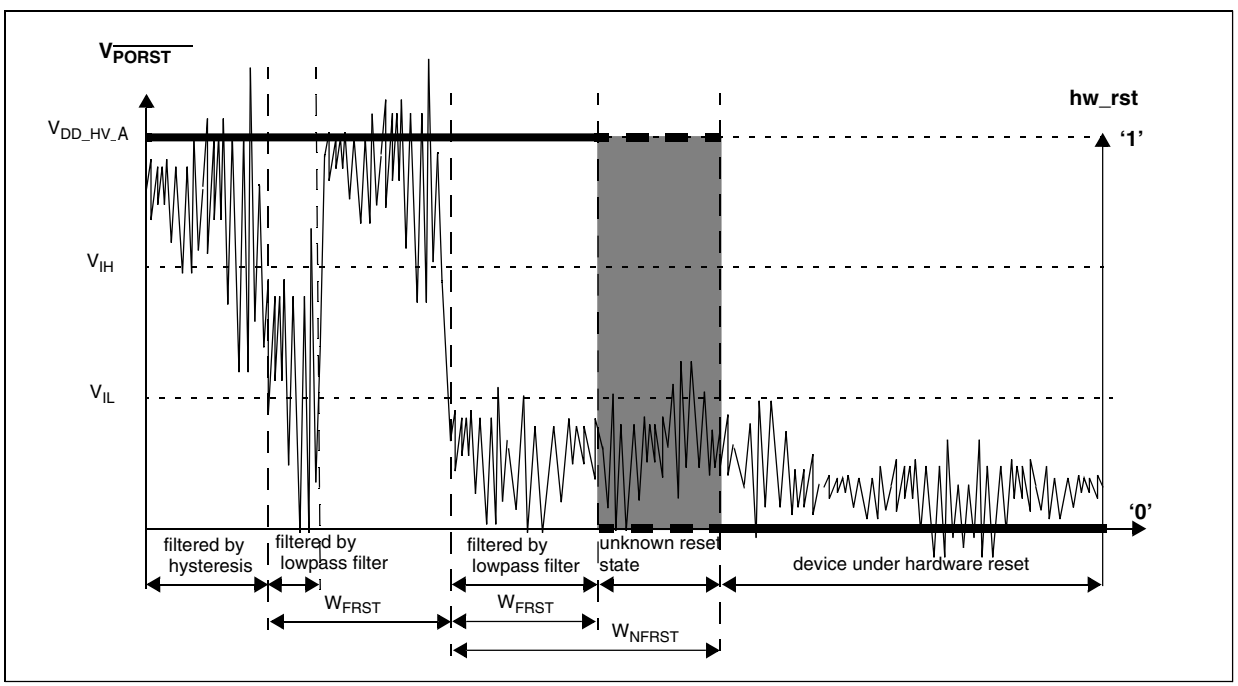


Figure 4. Noise filtering on reset signal

Table 19. Functional reset pad electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{IH}	CMOS Input Buffer High Voltage	—	$0.65*V_{DD\_HV\_x}$	—	$V_{DD\_HV\_x}+0.3$	V
V_{IL}	CMOS Input Buffer Low Voltage	—	$V_{DD\_HV\_x}-0.3$	—	$0.35*V_{DD\_HV\_x}$	V

Table continues on the next page...

Table 19. Functional reset pad electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{HYS}	CMOS Input Buffer hysterisis	—	300	—	—	mV
V_{DD_POR}	Minimum supply for strong pull-down activation	—	—	—	1.2	V
I_{OL_R}	Strong pull-down current [1]	Device under power-on reset $V_{DD\_HV\_IO}$= V_{DD_POR} V_{OL} = 0.35*$V_{DD\_HV\_IO}$	0.2	—	—	mA
		Device under power-on reset 3.0 V < $V_{DD\_HV\_IO}$ < 5.5 V V_{OL} = 0.35*$V_{DD\_HV\_IO}$	11	—	—	mA
W_{FRST}	$\overline{\text{RESET}}$ input filtered pulse	—	—	—	500	ns
W_{NFRST}	$\overline{\text{RESET}}$ input not filtered pulse	—	2000	—	—	ns
$\|I_{WPU}\|$	Weak pull-up current absolute value	RESET pin V_{IN} = V_{DD}	23	—	82	µA

1. Strong pull-down is active on PHASE0, PHASE1, PHASE2, and the beginning of PHASE3 for RESET.

5.6 PORST electrical specifications

Table 20. PORST electrical specifications

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
W_{FPORST}	$\overline{\text{PORST}}$ input filtered pulse	—	—	200	ns
$W_{NFPORST}$	$\overline{\text{PORST}}$ input not filtered pulse	1000	—	—	ns
V_{IH}	Input high level	0.65 x $V_{DD\_HV\_A}$	—	—	V
V_{IL}	Input low level	—	—	0.35 x $V_{DD\_HV\_A}$	V

6 Peripheral operating requirements and behaviours

6.1 Analog

6.1.1 ADC electrical specifications

The device provides a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

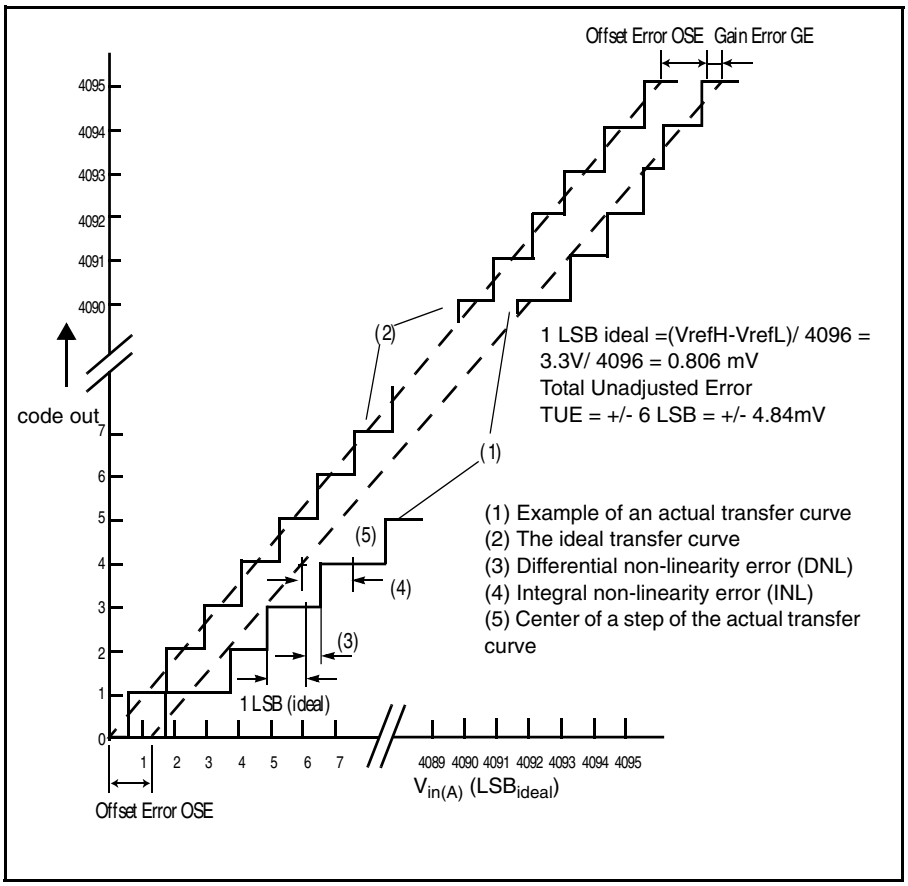


Figure 5. ADC characteristics and error definitions

6.1.1.1 Input equivalent circuit and ADC conversion characteristics

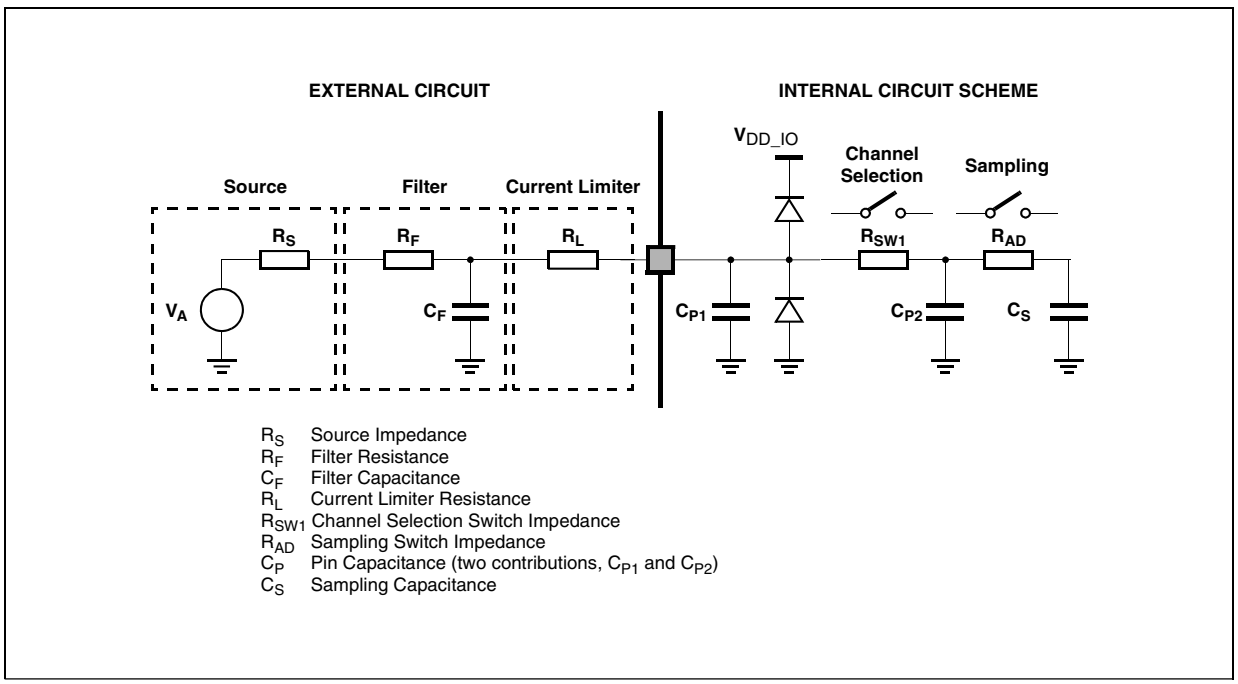


Figure 6. Input equivalent circuit

NOTE

The ADC performance specifications are not guaranteed if two ADCs simultaneously sample the same shared channel.

Table 21. ADC conversion characteristics (for 12-bit)

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
f_{CK}	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK[2] frequency)	—	15.2	80	80	MHz
f_s	Sampling frequency	80 MHz	—	—	1.00	MHz
t_{sample}	Sample time[3]	80 MHz@ 100 ohm source impedance	250	—	—	ns
t_{conv}	Conversion time[4]	80 MHz	700	—	—	ns
t_{total_conv}	Total Conversion time t_{sample} + t_{conv} (for standard and extended channels)	80 MHz	1.5[5]	—	—	µs
	Total Conversion time t_{sample} + t_{conv} (for precision channels)		1	—	—	
C_S,[6]	ADC input sampling capacitance	—	—	3	5	pF
C_{P1}[6]	ADC input pin capacitance 1	—	—	—	5	pF
C_{P2}[6]	ADC input pin capacitance 2	—	—	—	0.8	pF
R_{SW1}[6]	Internal resistance of analog source	V_{REF} range = 4.5 to 5.5 V	—	—	0.3	kΩ
		V_{REF} range = 3.15 to 3.6 V	—	—	875	Ω

Table continues on the next page...

Table 21. ADC conversion characteristics (for 12-bit) (continued)

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
R_{AD}[6]	Internal resistance of analog source	—	—	—	825	Ω
INL	Integral non-linearity (precise channel)	—	–2	—	2	LSB
INL	Integral non-linearity (standard channel)	—	–3	—	3	LSB
DNL	Differential non-linearity	—	–1	—	1	LSB
OFS	Offset error	—	–6	—	6	LSB
GNE	Gain error	—	–4	—	4	LSB
ADC Analog Pad (pad going to one ADC)	Max leakage (precision channel)	150 °C	—	—	250	nA
	Max leakage (standard channel)	150 °C	—	—	2500	nA
	Max leakage (standard channel)	105 °C $_{TA}$	—	5	250	nA
	Max positive/negative injection		–5	—	5	mA
$TUE_{precision\ channels}$	Total unadjusted error for precision channels	Without current injection	–6	+/-4	6	LSB
		With current injection[7]		+/-5		LSB
$TUE_{standard/extended\ channels}$	Total unadjusted error for standard/ extended channels	Without current injection	–8	+/-6	8	LSB
		With current injection[7]		+/-8		LSB
$t_{recovery}$	STOP mode to Run mode recovery time				< 1	µs

1. Active ADC input, VinA < [min(ADC_VrefH, ADC_ADV, VDD_HV_IOx)]. VDD_HV_IOx refers to I/O segment supply voltage. Violation of this condition would lead to degradation of ADC performance. Please refer to Table: 'Absolute maximum ratings' to avoid damage. Refer to Table: 'Recommended operating conditions (VDD_HV_x = 3.3 V)' for required relation between IO_supply_A,B,C and ADC_Supply.
2. The internally generated clock (known as AD_clk or ADCK) could be same as the peripheral clock or half of the peripheral clock based on register configuration in the ADC.
3. During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample}. After the end of the sample time t_{sample}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming.
4. This parameter does not include the sample time t_{sample}, but only the time for determining the digital result and the time to load the result register with the conversion result.
5. Apart from tsample and tconv, few cycles are used up in ADC digital interface and hence the overall throughput from the ADC is lower.
6. See Figure 2.
7. Current injection condition for ADC channels is defined for an inactive ADC channel (on which conversion is NOT being performed), and this occurs when voltage on the ADC pin exceeds the I/O supply or ground. However, absolute maximum voltage spec on pad input (VINA, see Table: Absolute maximum ratings) must be honored to meet TUE spec quoted here

Table 22. ADC conversion characteristics (for 10-bit)

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
f_{CK}	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK[2] frequency.)	—	15.2	80	80	MHz
f_s	Sampling frequency	—	—	—	1.00	MHz
t_{sample}	Sample time[3]	80 MHz@ 100 ohm source impedance	275	—	—	ns

Table continues on the next page...

Table 22. ADC conversion characteristics (for 10-bit) (continued)

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
t_{conv}	Conversion time[4]	80 MHz	550	—	—	ns
t_{total_conv}	Total Conversion time tsample + tconv (for standard channels)	80 MHz	1	—	—	µs
	Total Conversion time tsample + tconv (for extended channels)		1.5	—	—	
C_S	ADC input sampling capacitance	—	—	3	5	pF
C_{P1}[5]	ADC input pin capacitance 1	—	—	—	5	pF
C_{P2}[5]	ADC input pin capacitance 2	—	—	—	0.8	pF
R_{SW1}[5]	Internal resistance of analog source	V_{REF} range = 4.5 to 5.5 V	—	—	0.3	kΩ
		V_{REF} range = 3.15 to 3.6 V	—	—	875	Ω
R_{AD}[5]	Internal resistance of analog source	—	—	—	825	Ω
INL	Integral non-linearity	—	–2	—	2	LSB
DNL	Differential non-linearity	—	–1	—	1	LSB
OFS	Offset error	—	–4	—	4	LSB
GNE	Gain error	—	–4	—	4	LSB
ADC Analog Pad (pad going to one ADC)	Max leakage (standard channel)	150 °C	—	—	2500	nA
	Max positive/negative injection		–5	—	5	mA
	Max leakage (standard channel)	105 °C T_A	—	5	250	nA
$TUE_{standard/extended}$ channels	Total unadjusted error for standard channels	Without current injection	–4	+/-3	4	LSB
		With current injection[6]		+/-4		LSB
$t_{recovery}$	STOP mode to Run mode recovery time				< 1	µs

1. Active ADC Input, VinA < [min(ADC_ADV, IO_Supply_A,B,C)]. Violation of this condition would lead to degradation of ADC performance. Please refer to Table: 'Absolute maximum ratings' to avoid damage. Refer to Table: 'Recommended operating conditions' for required relation between IO_supply_A, B, C and ADC_Supply.
2. The internally generated clock (known as AD_clk or ADCK) could be same as the peripheral clock or half of the peripheral clock based on register configuration in the ADC.
3. During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample}. After the end of the sample time t_{sample}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming.
4. This parameter does not include the sample time t_{sample}, but only the time for determining the digital result and the time to load the result register with the conversion result.
5. See Figure 2-1
6. Current injection condition for ADC channels is defined for an inactive ADC channel (on which conversion is NOT being performed), and this occurs when voltage on the ADC pin exceeds the I/O supply or ground. However, absolute maximum voltage spec on pad input (VINA, see Table: Absolute maximum ratings) must be honored to meet TUE spec quoted here

6.1.2 Analog Comparator (CMP) electrical specifications

Table 23. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	250	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	5	11	µA
V_{AIN}	Analog input voltage	V_{SS}	—	$V_{IN1\_CMP\_REF}$	V
V_{AIO}	Analog input offset voltage [1]	-47	—	47	mV
V_H	Analog comparator hysteresis [2]	—	1	25	mV
	• CR0[HYSTCTR] = 00	—	20	50	mV
	• CR0[HYSTCTR] = 01	—	40	70	mV
	• CR0[HYSTCTR] = 10	—	60	105	mV
	• CR0[HYSTCTR] = 11				
t_{DHS}	Propagation Delay, High Speed Mode (Full Swing) [1, 3]	—	—	250	ns
t_{DLS}	Propagation Delay, Low power Mode (Full Swing) [1, 3]	—	5	21	µs
	Analog comparator initialization delay, High speed mode[4]	—	4		µs
	Analog comparator initialization delay, Low speed mode [4]	—	100		µs
I_{DAC6b}	6-bit DAC current adder (when enabled)				
	3.3V Reference Voltage	—	6	9	µA
	5V Reference Voltage	—	10	16	µA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[5]
DNL	6-bit DAC differential non-linearity	–0.8	—	0.8	LSB

1. Measured with hysteresis mode of 00
2. Typical hysteresis is measured with input voltage range limited to 0.6 to $V_{DD\_HV\_A}$-0.6V
3. Full swing = VIH, VIL
4. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
5. 1 LSB = $V_{reference}/64$

6.2 Clocks and PLL interfaces modules

6.2.1 Main oscillator electrical characteristics

This device provides a driver for oscillator in pierce configuration with amplitude control. Controlling the amplitude allows a more sinusoidal oscillation, reducing in this way the EMI. Other benefits arises by reducing the power consumption. This Loop Controlled Pierce (LCP mode) requires good practices to reduce the stray capacitance of traces between crystal and MCU.

An operation in Full Swing Pierce (FSP mode), implemented by an inverter is also available in case of parasitic capacitances and cannot be reduced by using crystal with high equivalent series resistance. For this mode, a special care needs to be taken regarding the serial resistance used to avoid the crystal overdrive.

Other two modes called External (EXT Wave) and disable (OFF mode) are provided. For EXT Wave, the drive is disabled and an external source of clock within CMOS level based in analog oscillator supply can be used. When OFF, EXTAL is pulled down by 240 Kohms resistor and the feedback resistor remains active connecting XTAL through EXTAL by 1M resistor.

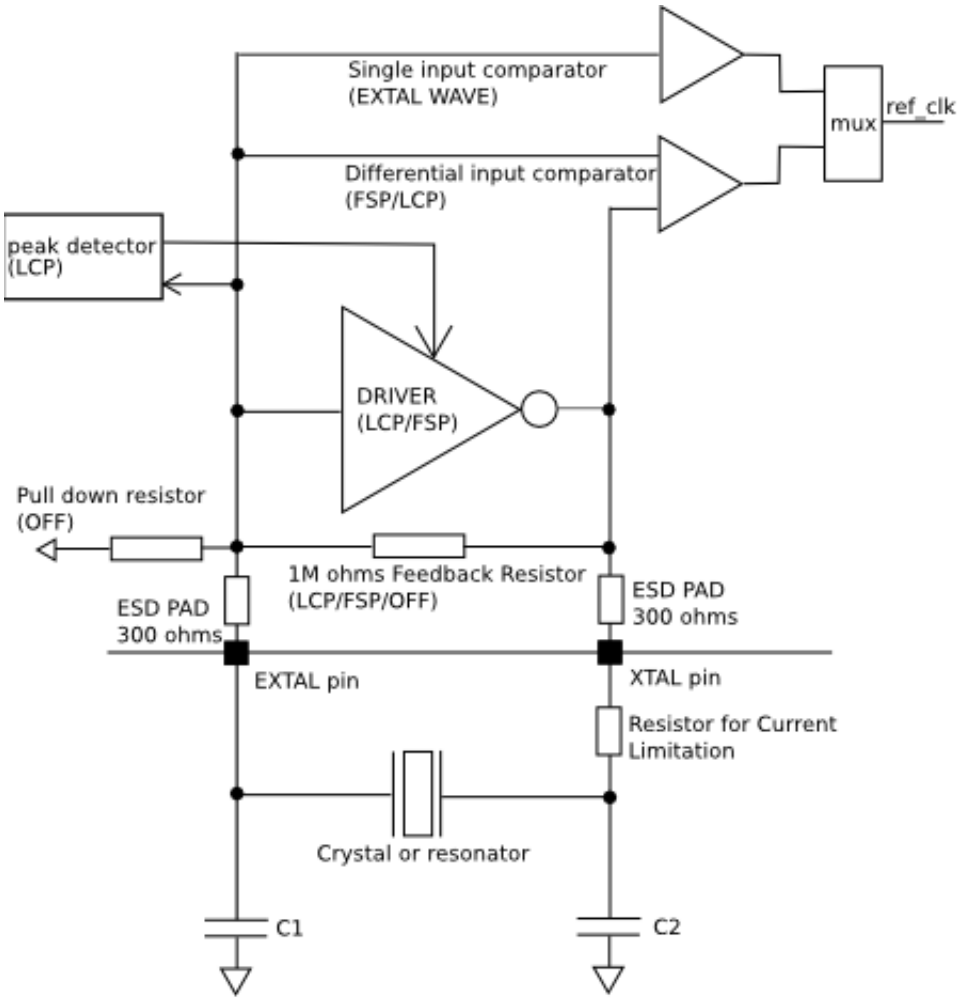


Figure 7. Oscillator connections scheme

Table 24. Main oscillator electrical characteristics

Symbol	Parameter	Mode	Conditions	Min	Typ	Max	Unit
f_{XOSCHS}	Oscillator frequency	FSP/LCP		8		40	MHz
$g_{mXOSCHS}$	Driver Transconductance	LCP			23		mA/V
		FSP			33		
V_{XOSCHS}	Oscillation Amplitude	LCP[1, 2]	8 MHz		1.0		V_{PP}
			16 MHz		1.0		
			40 MHz		0.8		
$T_{XOSCHSSU}$	Startup time	FSP/LCP[1]	8 MHz		2		ms
			16 MHz		1		
			40 MHz		0.5		
	Oscillator Analog Circuit supply current	FSP	8 MHz		2.2		mA
			16 MHz		2.2		

Table continues on the next page...

Table 24. Main oscillator electrical characteristics (continued)

Symbol	Parameter	Mode	Conditions	Min	Typ	Max	Unit
			40 MHz		3.2		
		LCP	8 MHz		141		uA
			16 MHz		252		
			40 MHz		518		
V_{IH}	Input High level CMOS Schmitt trigger	EXT Wave	Oscillator supply=3.3	1.95			V
V_{IL}	Input low level CMOS Schmitt trigger	EXT Wave	Oscillator supply=3.3			1.25	V

1. Values are very dependent on crystal or resonator used and parasitic capacitance observed in the board.
2. Typ value for oscillator supply 3.3 V@27 °C

6.2.2 32 kHz Oscillator electrical specifications

Table 25. 32 kHz oscillator electrical specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{osc_lo}	Oscillator crystal or resonator frequency		32		40	KHz
t_{cst}	Crystal Start-up Time[1, 2]				2	s

1. This parameter is characterized before qualification rather than 100% tested.
2. Proper PC board layout procedures must be followed to achieve specifications.

6.2.3 16 MHz RC Oscillator electrical specifications

Table 26. 16 MHz RC Oscillator electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
F_{Target}	IRC target frequency	—	—	16	—	MHz
PTA	IRC frequency variation after trimming	—	-5	—	5	%
$T_{startup}$	Startup time	—		—	1.5	us
T_{STJIT}	Cycle to cycle jitter		—	—	1.5	%
T_{LTJIT}	Long term jitter		—	—	0.2	%

NOTE

The above start up time of 1 us is equivalent to 16 cycles of 16 MHz.

6.2.4 128 KHz Internal RC oscillator Electrical specifications

Table 27. 128 KHz Internal RC oscillator electrical specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F_{oscu}[1]	Oscillator frequency	Calibrated	119	128	136.5	KHz
	Temperature dependence				600	ppm/C
	Supply dependence				18	%/V
	Supply current	Clock running			2.75	µA
		Clock stopped			200	nA

1. Vdd=1.2 V, 1.32V, T_a=-40 C, 125 C

6.2.5 PLL electrical specifications

Table 28. PLL electrical specifications

Parameter	Min	Typ	Max	Unit	Comments
Input Frequency	8		40	MHz	
VCO Frequency Range	600		1280	MHz	
Duty Cycle at pllclkout	48%		52%		This specification is guaranteed at PLL IP boundary
Period Jitter			See Table 29	ps	NON SSCG mode
TIE			See Table 29		at 960 M Integrated over 1MHz offset not valid in SSCG mode
Modulation Depth (Center Spread)	+/- 0.25%		+/- 3.0%		
Modulation Frequency			32	KHz	
Lock Time			60	µs	Calibration mode

Table 29. Jitter calculation

Type of jitter	Jitter due to Supply Noise (ps) J_{SN}[1]	Jitter due to Fractional Mode (ps) J_{SDM}[2]	Jitter due to Fractional Mode J_{SSCG} (ps) [3]	1 Sigma Random Jitter J_{RJ} (ps) [4]	Total Period Jitter (ps)
Period Jitter	60 ps	3% of pllclkout1,2	Modulation depth	0.1% of pllclkout1,2	+/-(J_{SN}+J_{SDM}+J_{SSCG}+$N^{[4]}$ ×J_{RJ})
Long Term Jitter (Integer Mode)				40	+/-(N x J_{RJ})
Long Term jitter (Fractional Mode)				100	+/-(N x J_{RJ})

1. This jitter component is due to self noise generated due to bond wire inductances on different PLL supplies. The jitter value is valid for inductor value of 5nH or less each on VDD_LV and VSS_LV.

2. This jitter component is added when the PLL is working in the fractional mode.
3. This jitter component is added when the PLL is working in the Spread Spectrum Mode. Else it is 0.
4. The value of N is dependent on the accuracy requirement of the application. See Percentage of sample exceeding specified value of jitter table

Table 30. Percentage of sample exceeding specified value of jitter

N	Percentage of samples exceeding specified value of jitter (%)
1	31.73
2	4.55
3	0.27
4	6.30 × 1e-03
5	5.63 × 1e-05
6	2.00 × 1e-07
7	2.82 × 1e-10

6.3 Memory interfaces

6.3.1 Flash memory program and erase specifications

NOTE

All timing, voltage, and current numbers specified in this section are defined for a single embedded flash memory within an SoC, and represent average currents for given supplies and operations.

Table 31 shows the estimated Program/Erase times.

Table 31. Flash memory program and erase specifications

Symbol	Characteristic[1]	Typ[2]	Factory Programming[3, 4]		Field Update			Unit
			Initial Max	Initial Max, Full Temp	Typical End of Life[5]	Lifetime Max[6]		
			$20°C \le T_A \le 30°C$	$-40°C \le T_J \le 150°C$	$-40°C \le T_J \le 150°C$	≤ 1,000 cycles	≤ 250,000 cycles	
t_{dwpgm}	Doubleword (64 bits) program time	43	100	150	55	500		µs
t_{ppgm}	Page (256 bits) program time	73	200	300	108	500		µs
t_{qppgm}	Quad-page (1024 bits) program time	268	800	1,200	396	2,000		µs
t_{16kers}	16 KB Block erase time	168	290	320	250	1,000		ms
t_{16kpgm}	16 KB Block program time	34	45	50	40	1,000		ms

Table continues on the next page...

Table 31. Flash memory program and erase specifications (continued)

Symbol	Characteristic[1]	Typ[2]	Factory Programming[3, 4]		Field Update			Unit
			Initial Max	Initial Max, Full Temp	Typical End of Life[5]	Lifetime Max[6]		
			20°C ≤T_A ≤30°C	-40°C ≤T_J ≤150°C	-40°C ≤T_J ≤150°C	≤ 1,000 cycles	≤ 250,000 cycles	
t_{32kers}	32 KB Block erase time	217	360	390	310	1,200		ms
t_{32kpgm}	32 KB Block program time	69	100	110	90	1,200		ms
t_{64kers}	64 KB Block erase time	315	490	590	420	1,600		ms
t_{64kpgm}	64 KB Block program time	138	180	210	170	1,600		ms
$t_{256kers}$	256 KB Block erase time	884	1,520	2,030	1,080	4,000	—	ms
$t_{256kpgm}$	256 KB Block program time	552	720	880	650	4,000	—	ms

1. Program times are actual hardware programming times and do not include software overhead. Block program times assume quad-page programming.
2. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.
3. Conditions: ≤ 150 cycles, nominal voltage.
4. Plant Programing times provide guidance for timeout limits used in the factory.
5. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.
6. Conditions: -40°C ≤ T_J ≤ 150°C, full spec voltage.

6.3.2 Flash memory Array Integrity and Margin Read specifications

Table 32. Flash memory Array Integrity and Margin Read specifications

Symbol	Characteristic	Min	Typical	Max[1]	Units[2]
$t_{ai16kseq}$	Array Integrity time for sequential sequence on 16 KB block.	—	—	512 x Tperiod x Nread	—
$t_{ai32kseq}$	Array Integrity time for sequential sequence on 32 KB block.	—	—	1024 x Tperiod x Nread	—
$t_{ai64kseq}$	Array Integrity time for sequential sequence on 64 KB block.	—	—	2048 x Tperiod x Nread	—
tai256kseq	Array Integrity time for sequential sequence on 256 KB block.	—	—	8192 x Tperiod x Nread	—
$t_{mr16kseq}$	Margin Read time for sequential sequence on 16 KB block.	73.81	—	110.7	µs
$t_{mr32kseq}$	Margin Read time for sequential sequence on 32 KB block.	128.43	—	192.6	µs
$t_{mr64kseq}$	Margin Read time for sequential sequence on 64 KB block.	237.65	—	356.5	µs
$t_{mr256kseq}$	Margin Read time for sequential sequence on 256 KB block.	893.01	—	1,339.5	µs

1. Array Integrity times need to be calculated and is dependent on system frequency and number of clocks per read. The equation presented require Tperiod (which is the unit accurate period, thus for 200 MHz, Tperiod would equal 5e-9) and Nread (which is the number of clocks required for read, including pipeline contribution. Thus for a read setup that requires 6 clocks to read with no pipeline, Nread would equal 6. For a read setup that requires 6 clocks to read, and has the address pipeline set to 2, Nread would equal 4 (or 6 - 2).)
2. The units for Array Integrity are determined by the period of the system clock. If unit accurate period is used in the equation, the results of the equation are also unit accurate.

6.3.3 Flash memory module life specifications

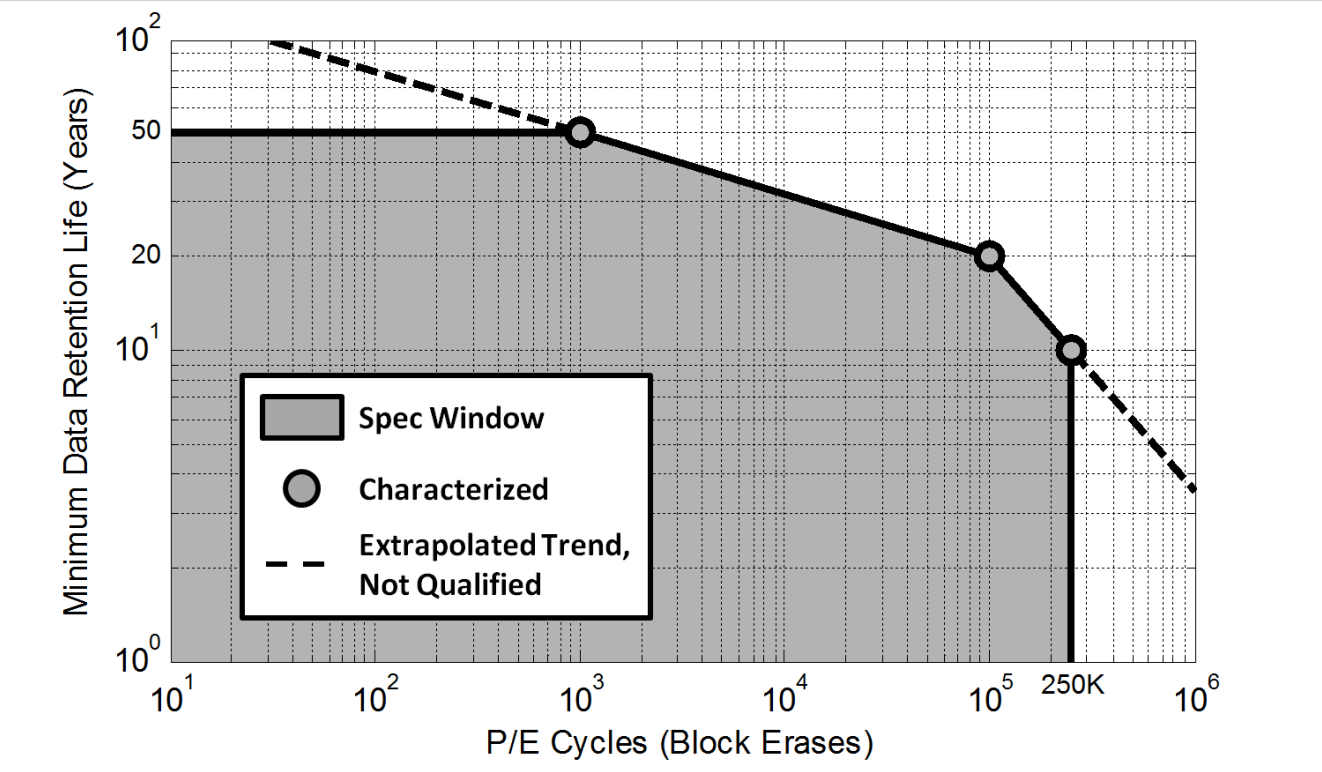
Table 33. Flash memory module life specifications

Symbol	Characteristic	Conditions	Min	Typical	Units
Array P/E cycles	Number of program/erase cycles per block for 16 KB, 32 KB and 64 KB blocks.[1]	—	250,000	—	P/E cycles
	Number of program/erase cycles per block for 256 KB blocks.[2]	—	1,000	250,000	P/E cycles
Data retention	Minimum data retention.	Blocks with 0 - 1,000 P/E cycles.	50	—	Years
		Blocks with 100,000 P/E cycles.	20	—	Years
		Blocks with 250,000 P/E cycles.	10	—	Years

1. Program and erase supported across standard temperature specs.
2. Program and erase supported across standard temperature specs.

6.3.4 Data retention vs program/erase cycles

Graphically, Data Retention versus Program/Erase Cycles can be represented by the following figure. The spec window represents qualified limits. The extrapolated dotted line demonstrates technology capability, however is beyond the qualification limits.



6.3.5 Flash memory AC timing specifications

Table 34. Flash memory AC timing specifications

Symbol	Characteristic	Min	Typical	Max	Units
t_{psus}	Time from setting the MCR-PSUS bit until MCR-DONE bit is set to a 1.	—	9.4 plus four system clock periods	11.5 plus four system clock periods	µs
t_{esus}	Time from setting the MCR-ESUS bit until MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	µs
t_{res}	Time from clearing the MCR-ESUS or PSUS bit with EHV = 1 until DONE goes low.	—	—	100	ns
t_{done}	Time from 0 to 1 transition on the MCR-EHV bit initiating a program/erase until the MCR-DONE bit is cleared.	—	—	5	ns
t_{dones}	Time from 1 to 0 transition on the MCR-EHV bit aborting a program/erase until the MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	µs
t_{drcv}	Time to recover once exiting low power mode.	16	—	45	µs

Table continues on the next page...

Table 34. Flash memory AC timing specifications (continued)

Symbol	Characteristic	Min	Typical	Max	Units
		plus seven system clock periods.		plus seven system clock periods	
$t_{aistart}$	Time from 0 to 1 transition of UT0-AIE initiating a Margin Read or Array Integrity until the UT0-AID bit is cleared. This time also applies to the resuming from a suspend or breakpoint by clearing AISUS or clearing NAIBP	—	—	5	ns
t_{aistop}	Time from 1 to 0 transition of UT0-AIE initiating an Array Integrity abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Array Integrity suspend request.	—	—	80 plus fifteen system clock periods	ns
t_{mrstop}	Time from 1 to 0 transition of UT0-AIE initiating a Margin Read abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Margin Read suspend request.	10.36 plus four system clock periods	—	20.42 plus four system clock periods	µs

6.3.6 Flash read wait state and address pipeline control settings

The following table describes the recommended RWSC and APC settings at various operating frequencies based on specified intrinsic flash access times of the flash module controller array at 125 °C.

Table 35. Flash Read Wait State and Address Pipeline Control Combinations

Flash frequency	RWSC setting	APC setting
0 MHz < fFlash <= 33 MHz	0	0
33 MHz < fFlash <= 100 MHz	2	1
100 MHz < fFlash <= 133 MHz	3	1
133 MHz < fFlash <= 160 MHz	4	1

6.4 Communication interfaces

6.4.1 DSPI timing

Table 36. DSPI electrical specifications

No	Symbol	Parameter	Conditions	High Speed Mode[1]		low Speed mode		Unit
				Min	Max	Min	Max	
1	t_{SCK}	DSPI cycle time	Master	25	—	50	—	ns
			Slave (MTFE = 0)	40	—	60	—	
2	t_{CSC}	PCS to SCK delay	—	16	—	—	—	ns
3	t_{ASC}	After SCK delay	—	16	—	—	—	ns
4	t_{SDC}	SCK duty cycle	—	$t_{SCK}/2$ - 10	$t_{SCK}/2$ + 10	—	—	ns
5	t_A	Slave access time	$\overline{SS}$ active to SOUT valid	—	40	—	—	ns
6	t_{DIS}	Slave SOUT disable time	$_{SS}$ inactive to SOUT High-Z or invalid	—	10	—	—	ns
7	t_{PCSC}	PCSx to $\overline{PCSS}$ time	—	13	—	—	—	ns
8	t_{PASC}	$\overline{PCSS}$ to PCSx time	—	13	—	—	—	ns
9	t_{SUI}	Data setup time for inputs	Master (MTFE = 0)	NA	—	20	—	ns
			Slave	2	—	2	—	
			Master (MTFE = 1, CPHA = 0)	15	—	8[2]	—	
			Master (MTFE = 1, CPHA = 1)	15	—	20	—	
10	t_{HI}	Data hold time for inputs	Master (MTFE = 0)	NA	—	–5	—	ns
			Slave	4	—	4	—	
			Master (MTFE = 1, CPHA = 0)	0	—	11[2]	—	
			Master (MTFE = 1, CPHA = 1)	0	—	-5	—	
11	t_{SUO}	Data valid (after SCK edge)	Master (MTFE = 0)	—	NA	—	4	ns
			Slave	—	15	—	23	
			Master (MTFE = 1, CPHA = 0)	—	4	—	16[2]	
			Master (MTFE = 1, CPHA = 1)	—	4	—	4	
12	t_{HO}	Data hold time for outputs	Master (MTFE = 0)	NA	—	–2	—	ns

Table continues on the next page...

Table 36. DSPI electrical specifications (continued)

No	Symbol	Parameter	Conditions	High Speed Mode[1]		low Speed mode		Unit
				Min	Max	Min	Max	
			Slave	4	—	6	—	
			Master (MTFE = 1, CPHA = 0)	-2	—	10[2]	—	
			Master (MTFE = 1, CPHA = 1)	–2	—	–2	—	

1. Only one {SIN,SOUT and SCK} group per DSPI/SPI will support high frequency mode. See Table 3.
2. SMPL_PTR should be set to 1

NOTE

Restriction For High Speed modes

- DSPI2, DSPI3, SPI1 and SPI2 will support 40MHz Master mode SCK
- DSPI2, DSPI3, SPI1 and SPI2 will support 25MHz Slave SCK frequency
- Only one {SIN,SOUT and SCK} group per DSPI/SPI will support high frequency mode. See Table 38.
- For Master mode MTFE will be 1 for high speed mode
- For high speed slaves, their master have to be in MTFE=1 mode or should be able to support 15ns tSUO delay

NOTE

For numbers shown in the following figures, see Table 36

Table 37. Continuous SCK timing

Spec	Characteristics	Pad Drive/Load	Value	
			Min	Max
tSCK	SCK cycle timing	strong/50 pF	100 ns	-
-	PCS valid after SCK	strong/50 pF	-	15 ns
-	PCS valid after SCK	strong/50 pF	-4 ns	-

Table 38. DSPI high speed mode I/Os

DSPI	High speed SCK	High speed SIN	High speed SOUT
DSPI2	GPIO[78]	GPIO[76]	GPIO[77]
DSPI3	GPIO[100]	GPIO[101]	GPIO[98]
SPI1	GPIO[173]	GPIO[175]	GPIO[176]
SPI2	GPIO[79]	GPIO[110]	GPIO[111]

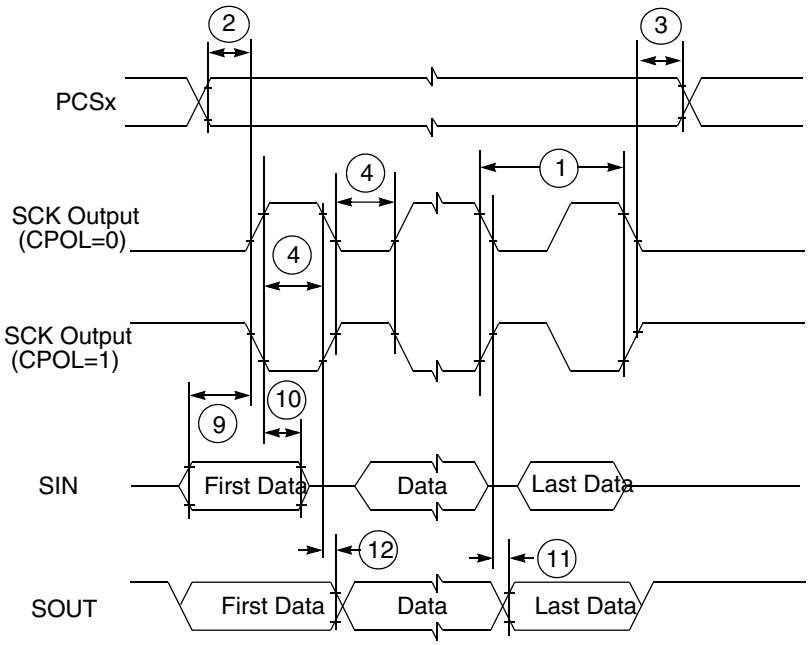


Figure 8. DSPI classic SPI timing — master, CPHA = 0

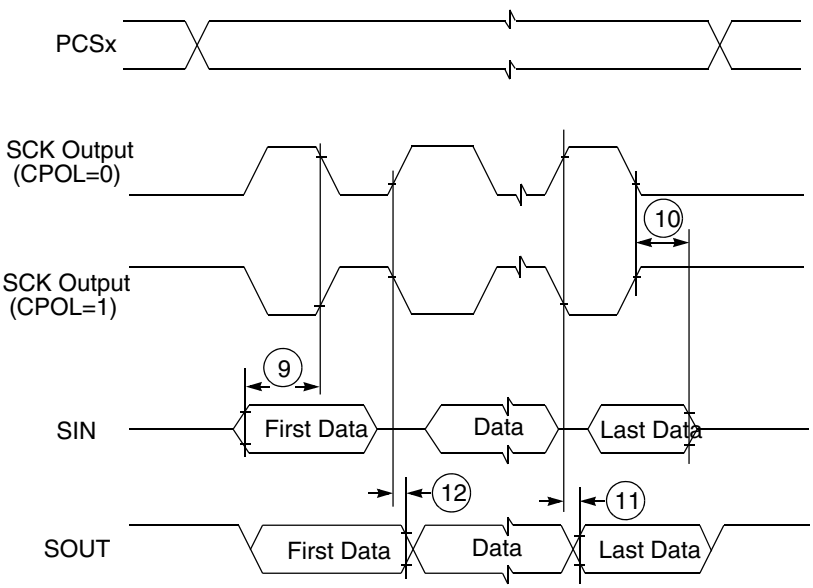


Figure 9. DSPI classic SPI timing — master, CPHA = 1

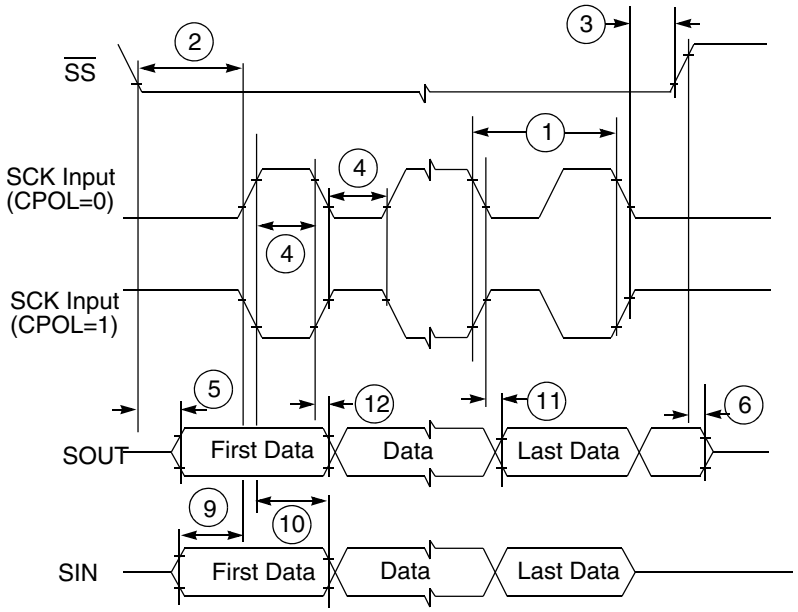


Figure 10. DSPI classic SPI timing — slave, CPHA = 0

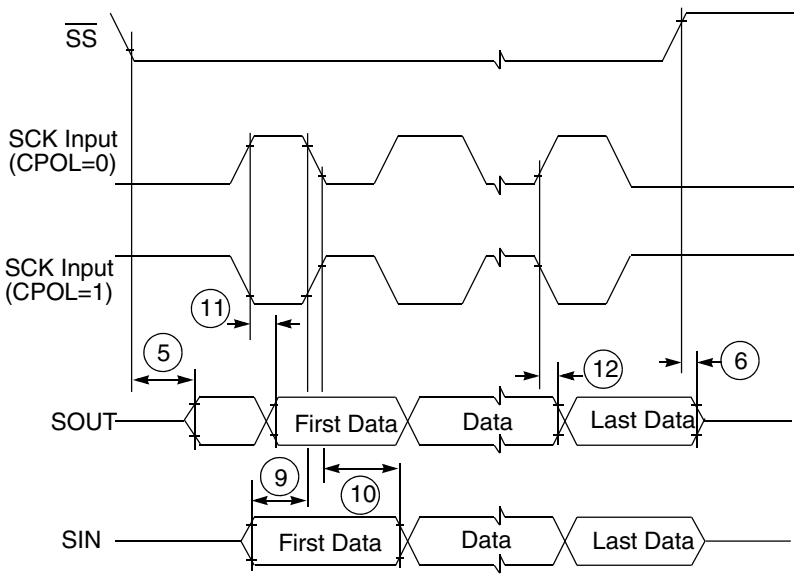


Figure 11. DSPI classic SPI timing — slave, CPHA = 1

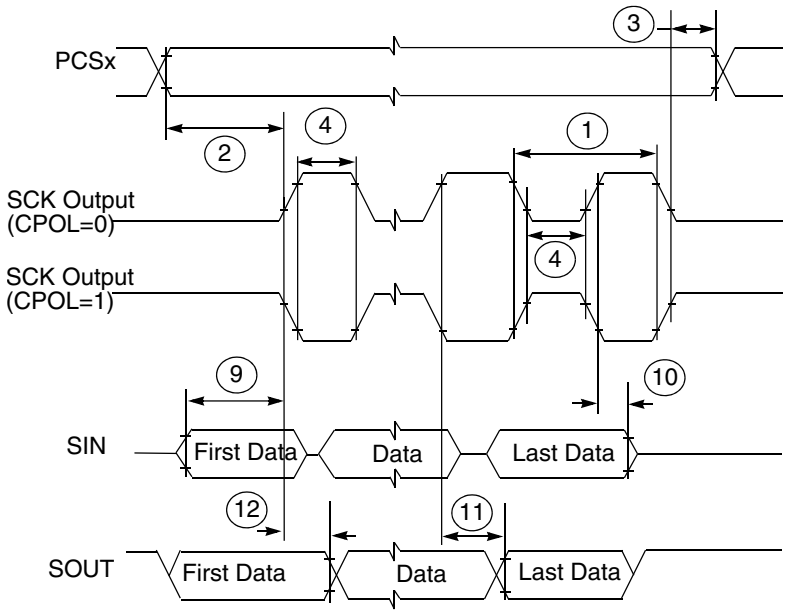


Figure 12. DSPI modified transfer format timing — master, CPHA = 0

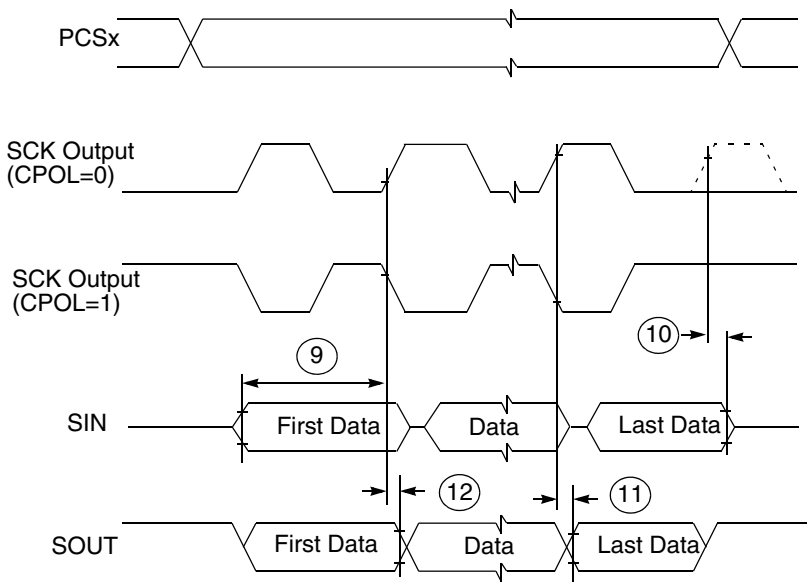


Figure 13. DSPI modified transfer format timing — master, CPHA = 1

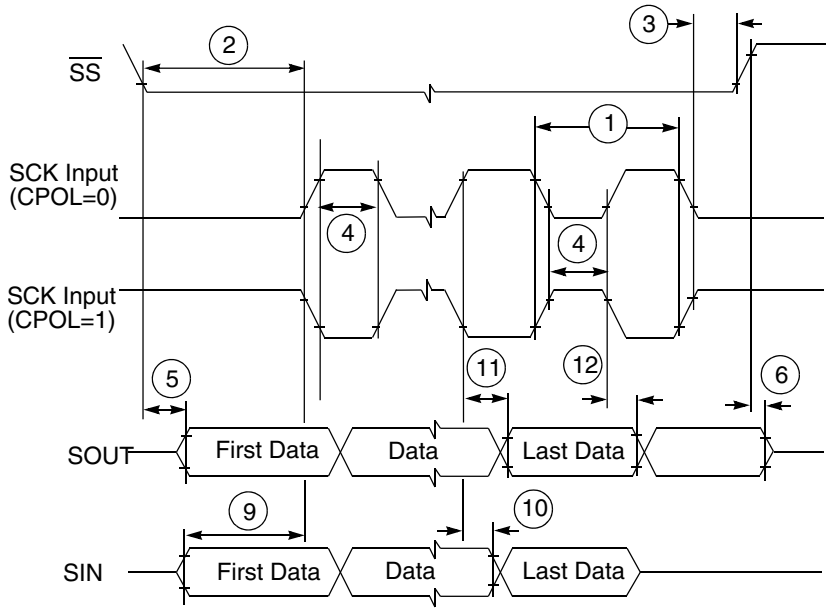


Figure 14. DSPI modified transfer format timing – slave, CPHA = 0

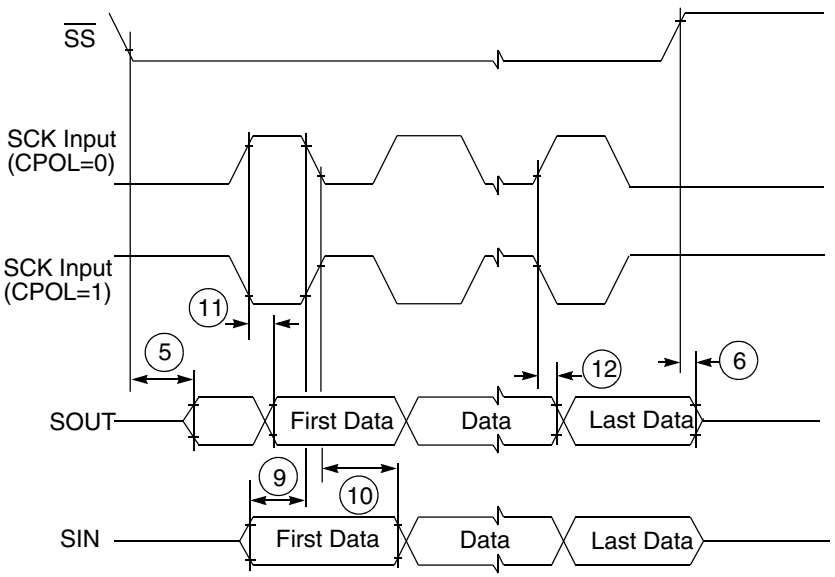


Figure 15. DSPI modified transfer format timing — slave, CPHA = 1

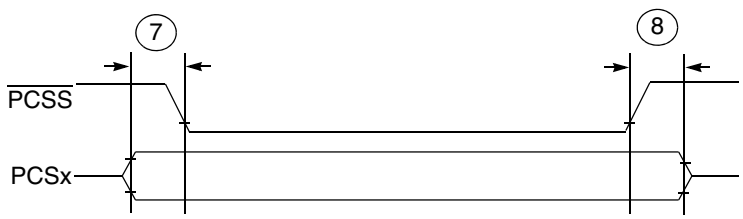


Figure 16. DSPI PCS strobe (PCSS) timing

6.4.2 FlexRay electrical specifications

6.4.2.1 FlexRay timing

This section provides the FlexRay Interface timing characteristics for the input and output signals. It should be noted that these are recommended numbers as per the FlexRay EPL v3.0 specification, and subject to change per the final timing analysis of the device.

6.4.2.2 TxEN

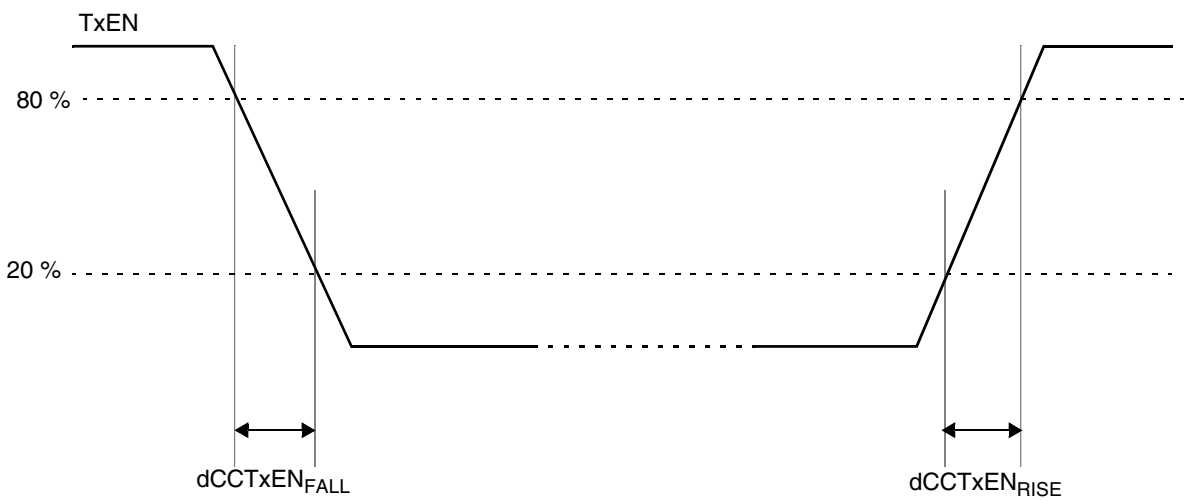


Figure 17. TxEN signal

Table 39. TxEN output characteristics[1]

Name	Description	Min	Max	Unit
$dCCTxEN_{RISE25}$	Rise time of TxEN signal at CC	—	9	ns
$dCCTxEN_{FALL25}$	Fall time of TxEN signal at CC	—	9	ns
$dCCTxEN_{01}$	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
$dCCTxEN_{10}$	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

1. All parameters specified for $V_{DD\_HV\_IOx}$ = 3.3 V -5%, +±10%, TJ = –40 °C / 150 °C, TxEN pin load maximum 25 pF

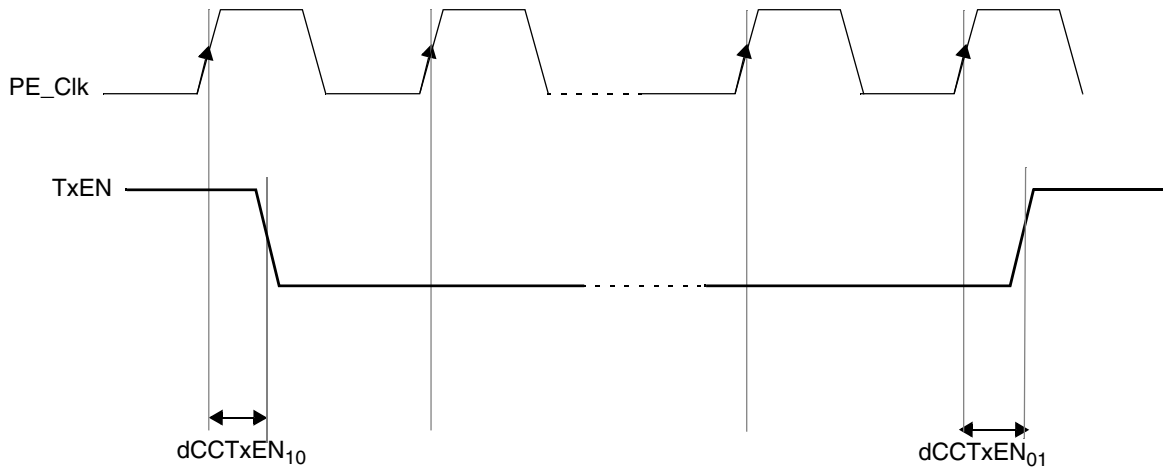


Figure 18. TxEN signal propagation delays

6.4.2.3 TxD

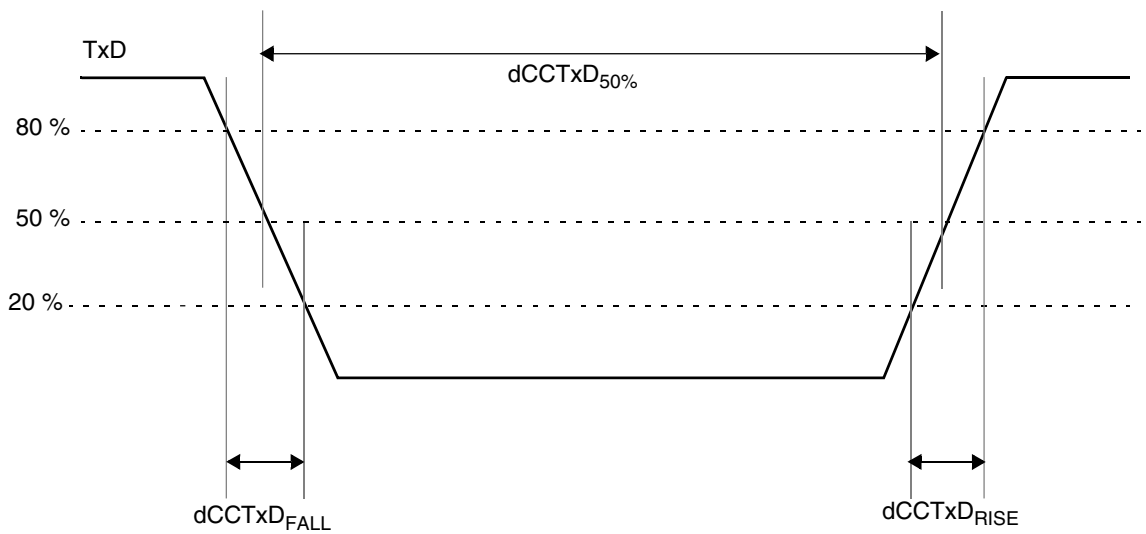


Figure 19. TxD Signal

Table 40. TxD output characteristics

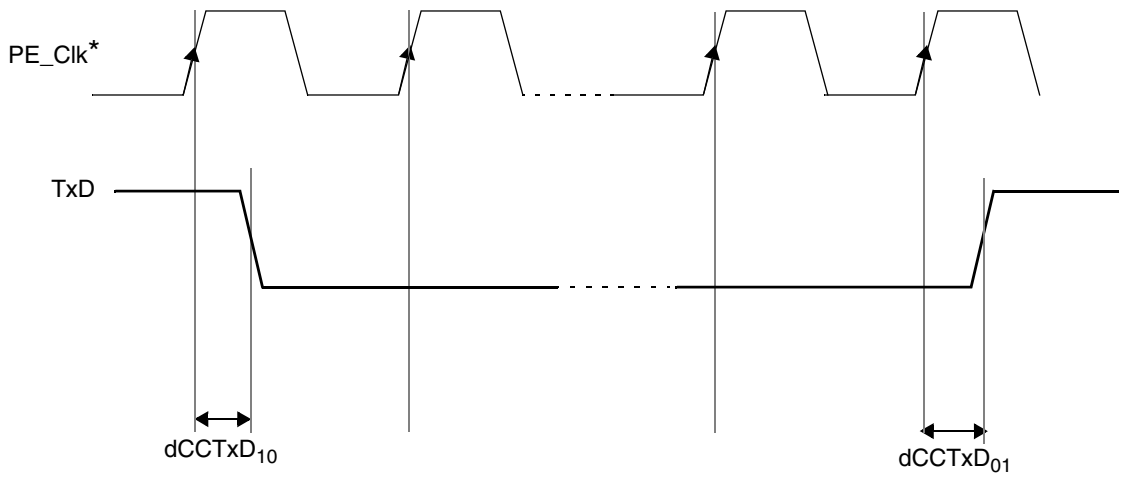
Name	Description[1]	Min	Max	Unit
$dCCT_{xAsym}$	Asymmetry of sending CC @ 25 pF load (=dCCTxD50% - 100 ns)	–2.45	2.45	ns
$dCCTxD_{RISE25}$+$dCCTxD_{FALL25}$	Sum of Rise and Fall time of TxD signal at the output	—	9[2]	ns

Table continues on the next page...

Table 40. TxD output characteristics (continued)

Name	Description[1]	Min	Max	Unit
$dCCTxD_{01}$	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge	—	25	ns
$dCCTxD_{10}$	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge	—	25	ns

1. All parameters specified for $V_{DD\_HV\_IOx}$ = 3.3 V -5%, +±10%, TJ = –40 °C / 150 °C, TxD pin load maximum 25 pF.
2. For 3.3 V ± 10% operation, this specification is 10 ns.



*FlexRay Protocol Engine Clock

Figure 20. TxD Signal propagation delays

6.4.2.4 RxD

Table 41. RxD input characteristic

Name	Description[1]	Min	Max	Unit
C_CCRxD	Input capacitance on RxD pin	—	7	pF
uCCLogic_1	Threshold for detecting logic high	35	70	%
uCCLogic_0	Threshold for detecting logic low	30	65	%
$dCCRxD_{01}$	Sum of delay from actual input to the D input of the first FF, rising edge	—	10	ns
$dCCRxD_{10}$	Sum of delay from actual input to the D input of the first FF, falling edge	—	10	ns

1. All parameters specified for VDD_HV_IOx = 3.3 V -5%, +±10%, TJ = –40 oC / 150 oC.

6.4.3 Ethernet switching specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

6.4.3.1 MII signal switching specifications

The following timing specs meet the requirements for MII style interfaces for a range of transceiver devices.

Table 42. MII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RXCLK frequency	—	25	MHz
MII1	RXCLK pulse width high	35%	65%	RXCLK period
MII2	RXCLK pulse width low	35%	65%	RXCLK period
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
—	TXCLK frequency	—	25	MHz
MII5	TXCLK pulse width high	35%	65%	TXCLK period
MII6	TXCLK pulse width low	35%	65%	TXCLK period
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	ns
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns

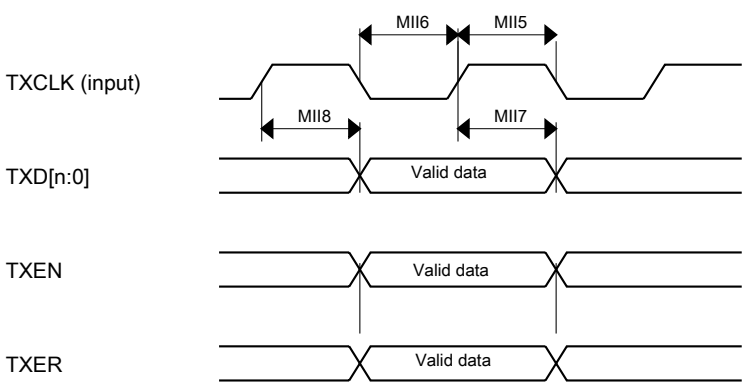


Figure 21. RMII/MII transmit signal timing diagram

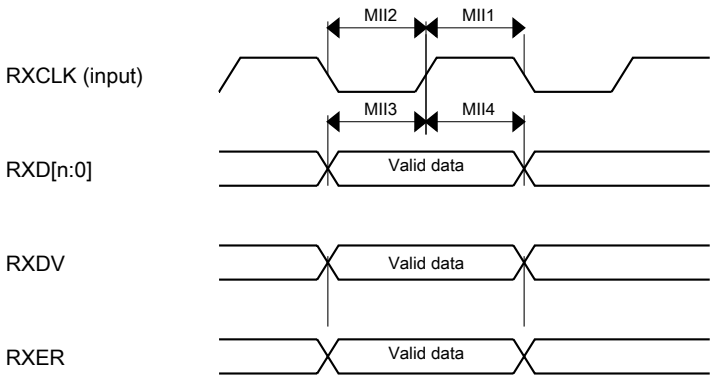


Figure 22. RMII/MII receive signal timing diagram

6.4.3.2 RMII signal switching specifications

The following timing specs meet the requirements for RMII style interfaces for a range of transceiver devices.

Table 43. RMII signal switching specifications

Num	Description	Min.	Max.	Unit
—	EXTAL frequency (RMII input clock RMII_CLK)	—	50	MHz
RMII1	RMII_CLK pulse width high	35%	65%	RMII_CLK period
RMII2	RMII_CLK pulse width low	35%	65%	RMII_CLK period
RMII3	RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	—	ns
RMII4	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns
RMII7	RMII_CLK to TXD[1:0], TXEN invalid	4	—	ns
RMII8	RMII_CLK to TXD[1:0], TXEN valid	—	15	ns

6.4.4 SAI electrical specifications

All timing requirements are specified relative to the clock period or to the minimum allowed clock period of a device

Table 44. Master mode SAI Timing

no	Parameter	Value		Unit
		Min	Max	
	Operating Voltage	2.7	3.6	V
S1	SAI_MCLK cycle time	40	-	ns

Table continues on the next page...

Table 44. Master mode SAI Timing (continued)

no	Parameter	Value		Unit
		Min	Max	
S2	SAI_MCLK pulse width high/low	45%	55%	MCLK period
S3	SAI_BCLK cycle time	80	-	BCLK period
S4	SAI_BCLK pulse width high/low	45%	55%	ns
S5	SAI_BCLK to SAI_FS output valid	-	15	ns
S6	SAI_BCLK to SAI_FS output invalid	0	-	ns
S7	SAI_BCLK to SAI_TXD valid	-	15	ns
S8	SAI_BCLK to SAI_TXD invalid	0	-	ns
S9	SAI_RXD/SAI_FS input setup before SAI_BCLK	28	-	ns
S10	SAI_RXD/SAI_FS input hold after SAI_BCLK	0	-	ns

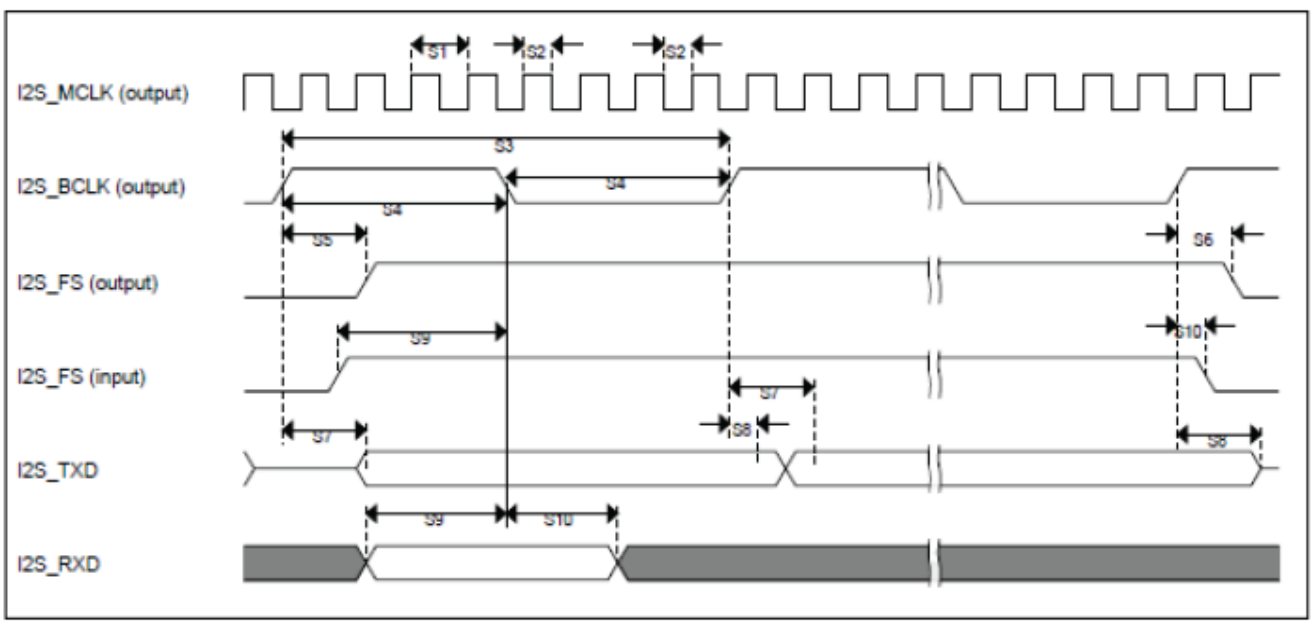


Figure 23. Master mode SAI Timing

Table 45. Slave mode SAI Timing

No	Parameter	Value		Unit
		Min	Max	
	Operating Voltage	2.7	3.6	V
S11	SAI_BCLK cycle time (input)	80	-	ns
S12	SAI_BCLK pulse width high/low (input)	45%	55%	BCLK period
S13	SAI_FS input setup before SAI_BCLK	10	-	ns
S14	SAI_FS input hold after SAI_BCLK	2	-	ns

Table continues on the next page...

Table 45. Slave mode SAI Timing (continued)

No	Parameter	Value		Unit
		Min	Max	
S15	SAI_BCLK to SAI_TXD/SAI_FS output valid	-	28	ns
S16	SAI_BCLK to SAI_TXD/SAI_FS output invalid	0	-	ns
S17	SAI_RXD setup before SAI_BCLK	10	-	ns
S18	SAI_RXD hold after SAI_BCLK	2	-	ns

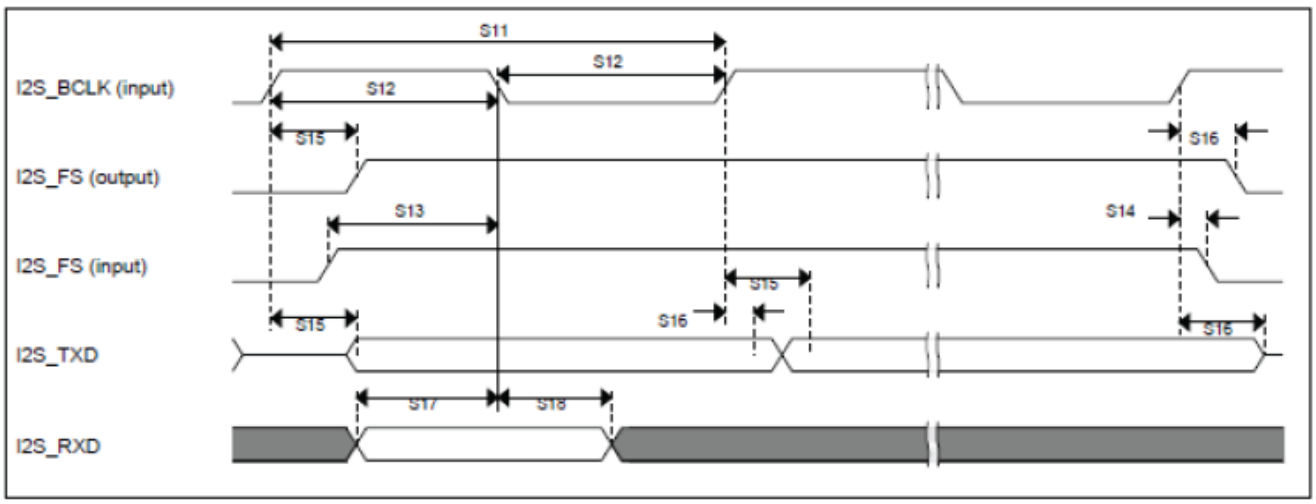


Figure 24. Slave mode SAI Timing

6.5 Debug specifications

6.5.1 JTAG interface timing

Table 46. JTAG pin AC electrical characteristics [1]

#	Symbol	Characteristic	Min	Max	Unit
1	t_{JCYC}	TCK Cycle Time [2]	62.5	—	ns
2	t_{JDC}	TCK Clock Pulse Width	40	60	%
3	$t_{TCKRISE}$	TCK Rise and Fall Times (40% - 70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	TMS, TDI Data Setup Time	5	—	ns
5	t_{TMSH}, t_{TDIH}	TMS, TDI Data Hold Time	5	—	ns
6	t_{TDOV}	TCK Low to TDO Data Valid	—	20[3]	ns
7	t_{TDOI}	TCK Low to TDO Data Invalid	0	—	ns
8	t_{TDOHZ}	TCK Low to TDO High Impedance	—	15	ns
11	t_{BSDV}	TCK Falling Edge to Output Valid	—	600[4]	ns

Table continues on the next page...

Table 46. JTAG pin AC electrical characteristics [1] (continued)

#	Symbol	Characteristic	Min	Max	Unit
12	t_{BSDVZ}	TCK Falling Edge to Output Valid out of High Impedance	—	600	ns
13	t_{BSDHZ}	TCK Falling Edge to Output High Impedance	—	600	ns
14	t_{BSDST}	Boundary Scan Input Valid to TCK Rising Edge	15	—	ns
15	t_{BSDHT}	TCK Rising Edge to Boundary Scan Input Invalid	15	—	ns

1. These specifications apply to JTAG boundary scan only.
2. This timing applies to TDI, TDO, TMS pins, however, actual frequency is limited by pad type for EXTEST instructions. Refer to pad specification for allowed transition frequency
3. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
4. Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

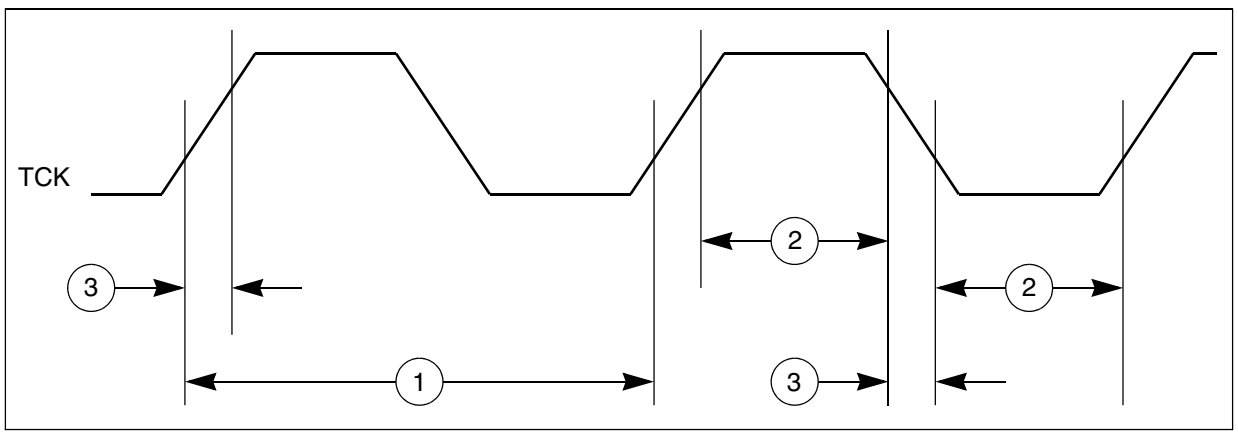


Figure 25. JTAG test clock input timing

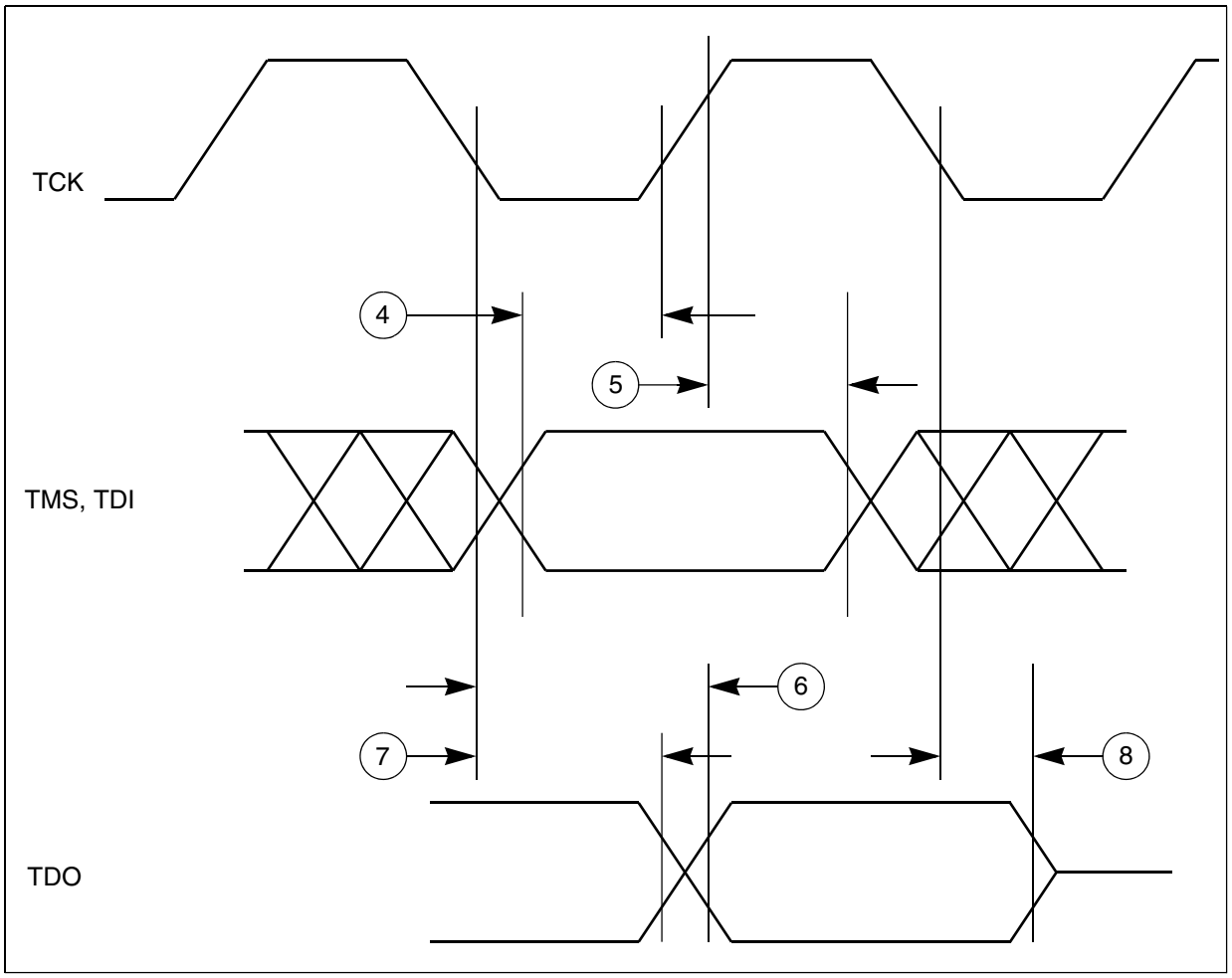


Figure 26. JTAG test access port timing

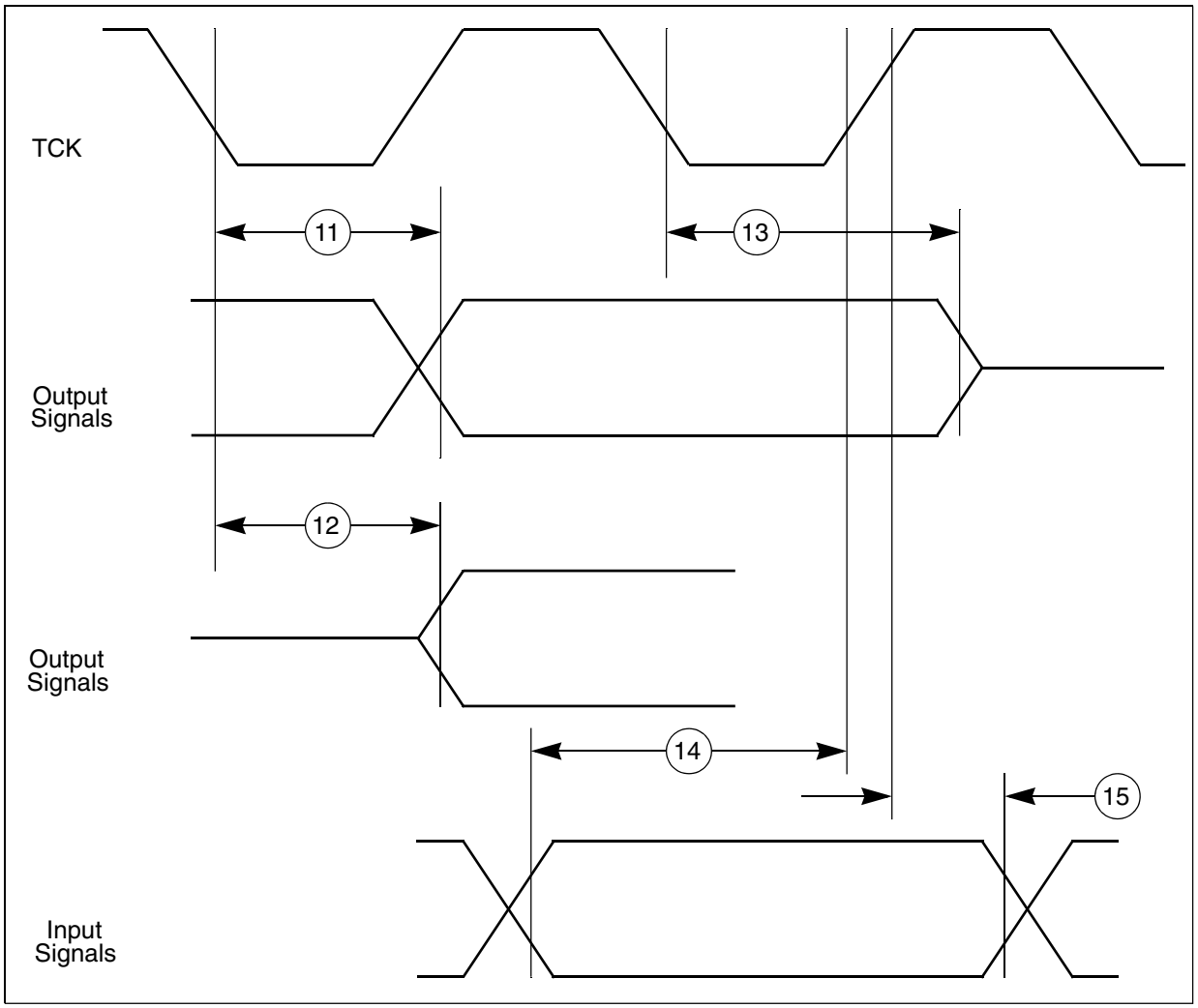


Figure 27. JTAG boundary scan timing

6.5.2 Nexus timing

Table 47. Nexus debug port timing [1]

No.	Symbol	Parameter	Conditions	Min	Max	Unit
1	t_{MCYC}	MCKO Cycle Time	—	15.6	—	ns
2	t_{MDC}	MCKO Duty Cycle	—	40	60	%
3	t_{MDOV}	MCKO Low to MDO, $\overline{\text{MSEO}}$, $\overline{\text{EVTO}}$ Data Valid[2]	—	–0.1	0.25	tMCYC
4	t_{EVTIPW}	$\overline{\text{EVTI}}$ Pulse Width	—	4	—	tTCYC
5	t_{EVTOPW}	$\overline{\text{EVTO}}$ Pulse Width	—	1	—	tMCYC
6	t_{TCYC}	TCK Cycle Time[3]	—	62.5	—	ns
7	t_{TDC}	TCK Duty Cycle	—	40	60	%
8	t_{NTDIS}, t_{NTMSS}	TDI, TMS Data Setup Time	—	8	—	ns

Table continues on the next page...

Table 47. Nexus debug port timing [1] (continued)

No.	Symbol	Parameter	Conditions	Min	Max	Unit
9	t_{NTDIH}, t_{NTMSH}	TDI, TMS Data Hold Time	—	5	—	ns
10	t_{JOV}	TCK Low to TDO/RDY Data Valid	—	0	25	ns

1. JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal.
2. For all Nexus modes except DDR mode, MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.
3. The system clock frequency needs to be four times faster than the TCK frequency.

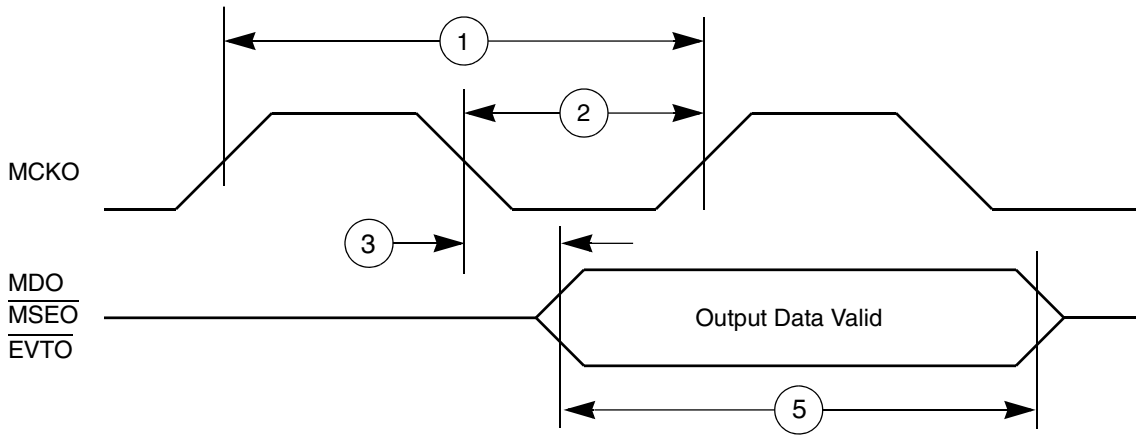


Figure 28. Nexus output timing

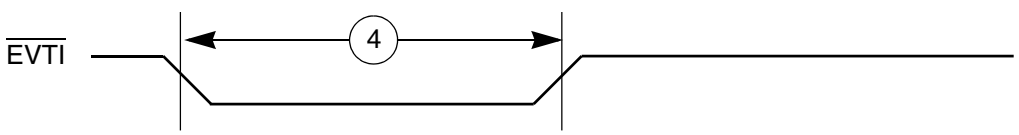


Figure 29. Nexus EVTI Input Pulse Width

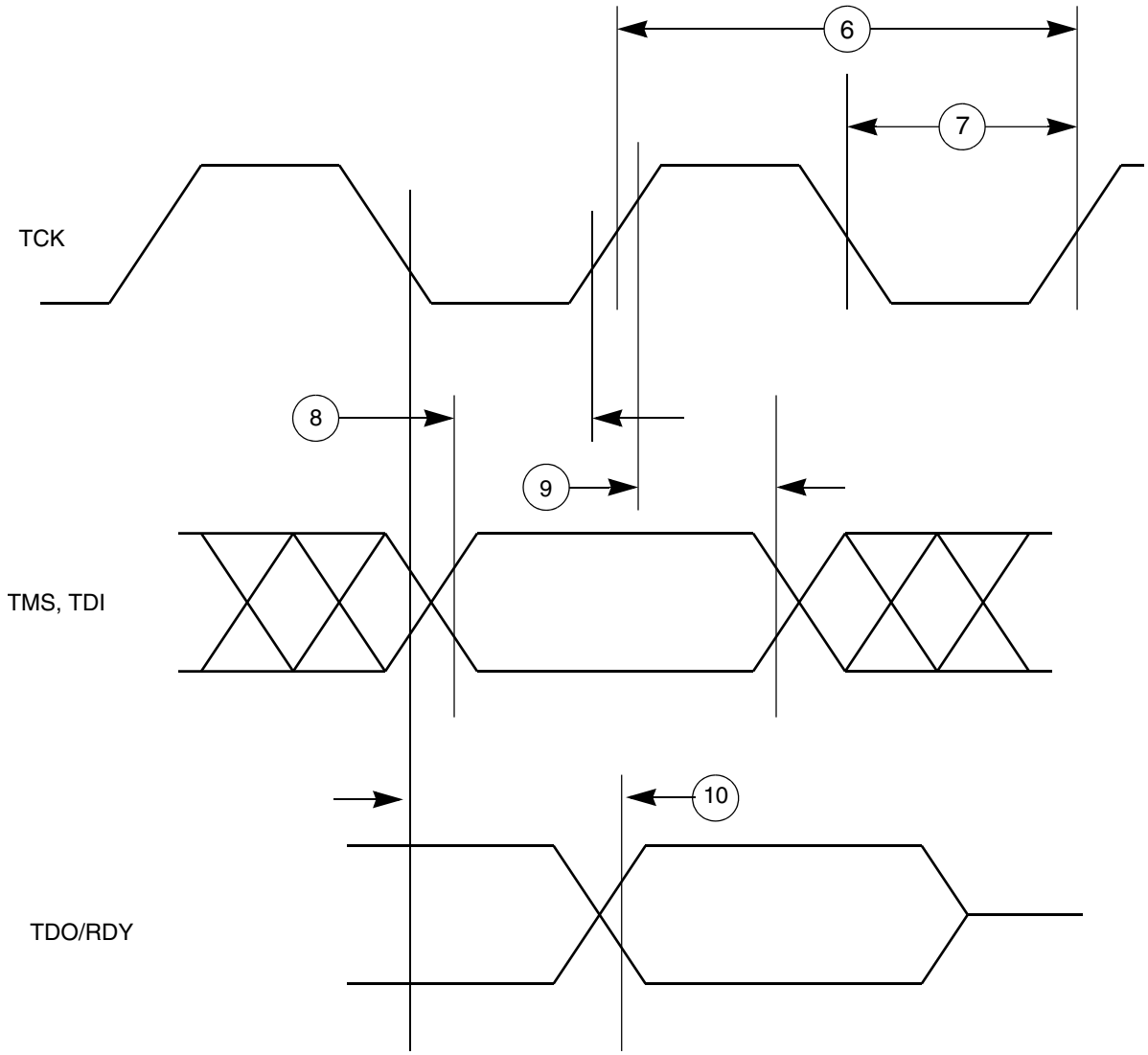


Figure 30. Nexus TDI, TMS, TDO timing

6.5.3 WKPU/NMI timing

Table 48. WKPU/NMI glitch filter

No.	Symbol	Parameter	Min	Typ	Max	Unit
1	W_{FNMI}	NMI pulse width that is rejected	—	—	20	ns
2	$W_{NFNMI}D$	NMI pulse width that is passed	400	—	—	ns

6.5.4 External interrupt timing (IRQ pin)

Table 49. External interrupt timing specifications

No.	Symbol	Parameter	Conditions	Min	Max	Unit
1	t_{IPWL}	IRQ pulse width low	—	3	—	t_{CYC}
2	t_{IPWH}	IRQ pulse width high	—	3	—	t_{CYC}
3	t_{ICYC}	IRQ edge to edge time	—	6	—	t_{CYC}

These values applies when IRQ pins are configured for rising edge or falling edge events, but not both.

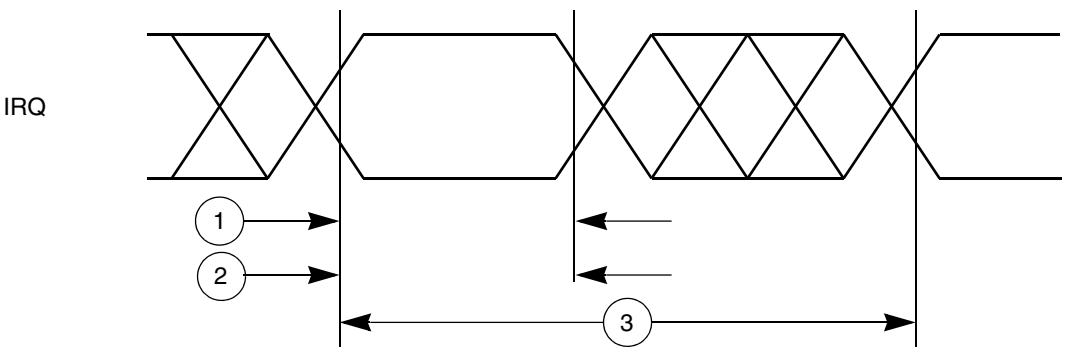


Figure 31. External interrupt timing

7 Thermal attributes

7.1 Thermal attributes

Board type	Symbol	Description	176LQFP	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	50.7	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	24.2	°C/W	1, 2, 3
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	38.1	°C/W	1, 3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction	17.8	°C/W	1, 3

Table continues on the next page...

Thermal attributes

Board type	Symbol	Description	176LQFP	Unit	Notes
		to ambient (200 ft./ min. air speed)			
—	$R_{\theta JB}$	Thermal resistance, junction to board	10.9	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	8.4	°C/W	5
—	Ψ_{JT}	Thermal resistance, junction to package top	0.5	°C/W	6
—	Ψ_{JB}	Thermal characterization parameter, junction to package bottom	0.3	°C/W	7

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal resistance between the die and the solder pad on the bottom of the package based on simulation without any interface resistance. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
7. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

Board type	Symbol	Description	324 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	31.0	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	24.3	°C/W	1,2,3
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	23.5	°C/W	1, 3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	20.1	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	16.8	°C/W	4

Table continues on the next page...

Board type	Symbol	Description	324 MAPBGA	Unit	Notes
—	$R_{\theta JC}$	Thermal resistance, junction to case	7.4	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top natural convection	0.2	°C/W	6
—	Ψ_{JB}	Thermal characterization parameter, junction to package bottom natural convection	7.3	°C/W	7

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

Board type	Symbol	Description	256 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	42.6	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	26.0	°C/W	1,2,3
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	31.0	°C/W	1,3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	21.3	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	12.8	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	7.9	°C/W	5

Table continues on the next page...

Thermal attributes

Board type	Symbol	Description	256 MAPBGA	Unit	Notes
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	0.2	°C/W	6
—	$R_{\theta JB\_CSB}$	Thermal characterization parameter, junction to package bottom outside center (natural convection)	9.0	°C/W	7

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

Board type	Symbol	Description	100 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	50.9	°C/W	1,2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	27.0	°C/W	1,2,3
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	38.0	°C/W	1,3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	22.2	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	10.8	°C/W	4

Table continues on the next page...

Board type	Symbol	Description	100 MAPBGA	Unit	Notes
—	$R_{\theta JC}$	Thermal resistance, junction to case	8.2	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	0.2	°C/W	6
—	Ψ_{JB}	Thermal characterization parameter, junction to package bottom outside center (natural convection)	7.8	°C/W	7

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

8 Dimensions

8.1 Obtaining package dimensions

Package dimensions are provided in package drawing.

To find a package drawing, go to www.nxp.com and perform a keyword search for the drawing's document number:

Package	NXP Document Number
100 MAPBGA	98ASA00802D
176-pin LQFP-EP	98ASA00698D
256 MAPBGA	98ASA00346D
324 MAPBGA	98ASA10582D

9 Pinouts

9.1 Package pinouts and signal descriptions

For package pinouts and signal descriptions, refer to the Reference Manual.

10 Reset sequence

10.1 Reset sequence

This section describes different reset sequences and details the duration for which the device remains in reset condition in each of those conditions.

10.1.1 Reset sequence duration

Table 50 specifies the reset sequence duration for the five different reset sequences described in Reset sequence description.

Table 50. RESET sequences

No.	Symbol	Parameter	T_{Reset}			Unit
			Min	Typ [1]	Max	
1	T_{DRB}	Destructive Reset Sequence, BIST enabled	6.2	7.3	-	ms
2	T_{DR}	Destructive Reset Sequence, BIST disabled	110	182	-	us
3	T_{ERLB}	External Reset Sequence Long, Unsecure Boot	6.2	7.3	-	ms
4	T_{FRL}	Functional Reset Sequence Long, Unsecure Boot	110	182	-	us
5	T_{FRS}	Functional Reset Sequence Short, Unsecure Boot	7	9	-	us

1. The Typ value is applicable only if the reset sequence duration is not prolonged by an extended assertion of RESET_B by an external reset generator.

10.1.2 BAF execution duration

Following table specifies the typical BAF execution time in case BAF boot header is present at first location (Typical) and last location (worst case). Total Boot time is the sum of reset sequence duration and BAF execution time.

Table 51. BAF execution duration

BAF execution duration	Min	Typ	Max	Unit
BAF execution time (boot header at first location)	—	200	—	µs
BAF execution time (boot header at last location)	—	—	320	µs

10.1.3 Reset sequence description

The figures in this section show the internal states of the device during the five different reset sequences. The dotted lines in the figures indicate the starting point and the end point for which the duration is specified in .

With the beginning of DRUN mode, the first instruction is fetched and executed. At this point, application execution starts and the internal reset sequence is finished.

The following figures show the internal states of the device during the execution of the reset sequence and the possible states of the RESET_B signal pin.

NOTE

RESET_B is a bidirectional pin. The voltage level on this pin can either be driven low by an external reset generator or by the device internal reset circuitry. A high level on this pin can only be generated by an external pullup resistor which is strong enough to overdrive the weak internal pulldown resistor. The rising edge on RESET_B in the following figures indicates the time when the device stops driving it low. The reset sequence durations given in are applicable only if the internal reset sequence is not prolonged by an external reset generator keeping RESET_B asserted low beyond the last Phase3.

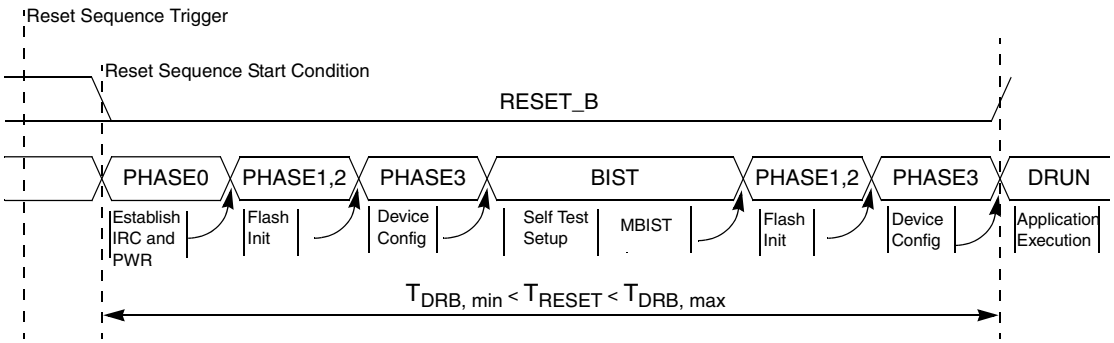


Figure 32. Destructive reset sequence, BIST enabled

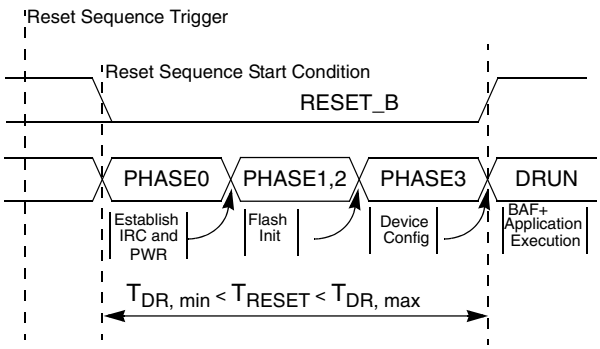


Figure 33. Destructive reset sequence, BIST disabled

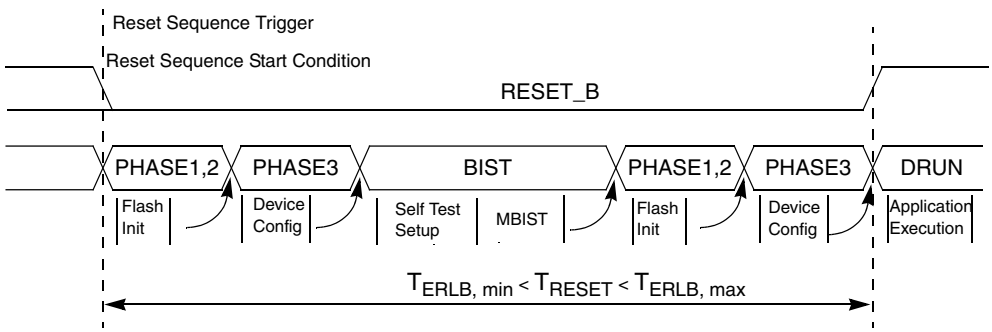


Figure 34. External reset sequence long, BIST enabled

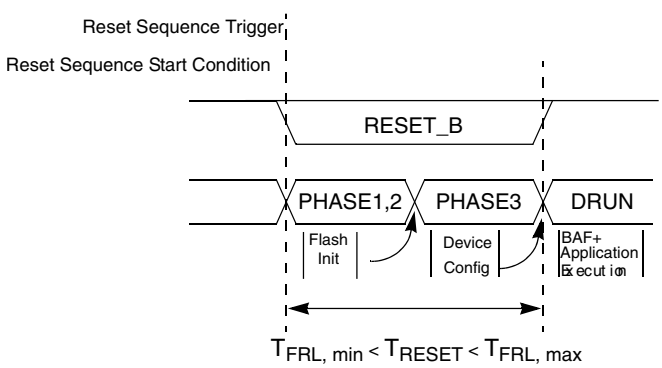


Figure 35. Functional reset sequence long

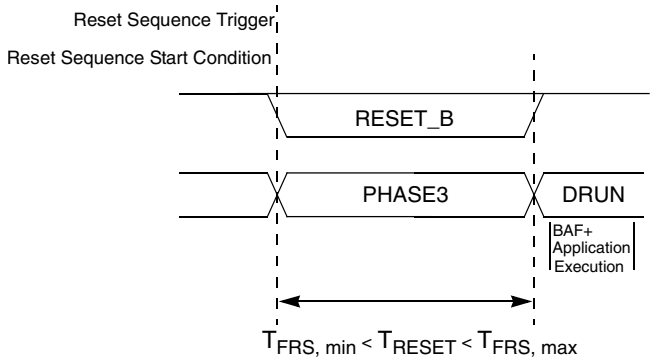


Figure 36. Functional reset sequence short

The reset sequences shown in Figure 35 and Figure 36 are triggered by functional reset events. RESET_B is driven low during these two reset sequences only if the corresponding functional reset source (which triggered the reset sequence) was enabled to drive RESET_B low for the duration of the internal reset sequence. See the RGM_FBRE register in the device reference manual for more information.

11 Revision History

11.1 Revision History

The following table provides a revision history for this document.

Table 52. Revision History

Rev. No.	Date	Substantial Changes
Rev 1	14 March 2013	Initial Release

Rev 2	7 August 2015	• In features:
		  • Updated BAF feature with sentence, Boot Assist Flash (BAF) supports internal flash programming via a serial link (SCI)
		  • Updated FlexCAN3 with FD support
		  • Updated number of STMs to two.
		• In Block diagram:
		  • Updated SRAM size from 128 KB to 256 KB.
		• In Family Comparison:
		  • Added note: All optional features (Flash memory, RAM, Peripherals) start with lowest number or address (e.g. FlexCAN0) and end at highest available number or address (e.g. MPC574xB/D have 6 CAN, ending with FlexCAN5).
		  • Revised MPC5746C Family Comparison table.
		• In Ordering parts:
		  • Updated ordering parts diagram to include 100 MAPBGA information and optional fields.
		• In table: Absolute maximum ratings
		  • Removed entry: 'V_{SS_HV}'
		  • Added spec for 'V_{DD12}'
		  • Updated 'Max' column for 'V_{INA}'

Table continues on the next page...

Table 52. Revision History (continued)

Rev. No.	Date	Substantial Changes
		• Updated footnote for $V_{DD\_HV\_ADC1\_REF}$. • Added footnote to 'Conditions', All voltages are referred to V_{SS_HV} unless otherwise specified • Removed footnote from 'Max', Absolute maximum voltages are currently maximum burn-in voltages. Absolute maximum specifications for device stress have not yet been determined. • In section: Recommended operating conditions • Added opening text: "The following table describes the operating conditions ... " • Added note: "$V_{DD\_HV\_A}$, $V_{DD\_HV\_B}$ and $V_{DD\_HV\_C}$ are all ... " • In table: Recommended operating conditions (VDD_HV_x = 3.3 V) and (VDD_HV_x = 5 V) • Added footnote to 'Conditions' cloumn, (All voltages are referred to V_{SS_HV} unless otherwise specified). • Updated footnote for 'Min' column to Device will be functional down (and electrical specifications as per various datasheet parameters will be guaranteed) to the point where one of the LVD/HVD resets the device. When voltage drops outside range for an LVD/HVD, device is reset. • Removed footnote for '$V_{DD\_HV\_A}$', '$V_{DD\_HV\_B}$', and '$V_{DD\_HV\_C}$' entry and updated the parameter column. • Removed entry : 'V_{SS_HV}' • Updated 'Parameter' column for '$V_{DD\_HV\_FLA}$', '$V_{DD\_HV\_ADC1\_REF}$', 'V_{DD_LV}' • Updated 'Min' column for '$V_{DD\_HV\_ADC0}$' '$V_{DD\_HV\_ADC1}$' • Updated 'Parameter' 'Min' 'Max' columns for '$V_{SS\_HV\_ADC0}$' and '$V_{SS\_HV\_ADC1}$' • Updated footnote for 'V_{DD_LV} ' to V_{DD_LV} supply pins should never be grounded (through a small impedance). If these are not driven, they should only be left floating. • Removed row for symbol 'V_{SS_LV}' • Removed footnote from 'Max' column of '$V_{DD\_HV\_ADC0}$' and '$V_{DD\_HV\_ADC1}$', (PA3, PA7, PA10, PA11 and PE12 ADC_1 channels are coming from $V_{DD\_HV\_B}$ domain hence $V_{DD\_HV\_ADC1}$ should be within ±100 mV of $V_{DD\_HV\_B}$ when these channels are used for ADC_1). • In table: Recommended operating conditions ($V_{DD\_HV\_x}$ = 3.3 V) • Removed footnote from '$V_{IN1\_CMP\_REF}$', (Only applicable when supplying from external source). • In table: Recommended operating conditions ($V_{DD\_HV\_x}$ = 5 V) • Added spec for '$V_{IN1\_CMP\_REF}$' and corresponding footnotes.
		• In section: Voltage monitor electrical characteristics • Updated description for Low Voltage detector block. • Added note, BCP56, MCP68 and MJD31 are guaranteed ballasts. • In table: Voltage regulator electrical specifications • Added footnote, Ceramic X7R or X5R type with capacitance-temperature characteristics +/-15% of -55 degC to +125degC is recommended. The tolerance +/-20% is acceptable. • Revised table, Voltage monitor electrical characteristics
		• In section: Supply current characteristics • In table: Current consumption characteristics • $I_{DD\_BODY\_4}$: Updated SYS_CLK to 120 MHz. • $I_{DD\_BODY\_4}$: Updated Max for T_a= 105 °C fand 85 °C) • I_{dd_STOP}: Added condition for T_a= 105 °C and removed Max value for T_a= 85 °C. • $I_{DD\_HV\_ADC\_REF}$: Added condition for T_a= 105 °C and 85 °C and removed Max value for T_a= 25 °C. • $I_{DD\_HV\_FLASH}$: Added condition for T_a= 105 °C and 85 °C • In table: Low Power Unit (LPU) Current consumption characteristics • LPU_RUN and LPU_STOP: Added condition for T_a= 105 °C and 85 °C

Table continues on the next page...

Table 52. Revision History (continued)

Rev. No.	Date	Substantial Changes

		• In table: STANDBY Current consumption characteristics
		  • Added condition for T_a= 105 °C and 85 °C for all entries.
		
		• In section: I/O parameters
		  • In table: Functional Pad AC Specifications @ 3.3 V Range
		  • Updated values for 'pad_sr_hv (output)'
		  • In table: DC electrical specifications @ 3.3V Range
		  • Updateded Min and Max values for Vih and Vil respectively.
		  • In table: Functional Pad AC Specifications @ 5 V Range
		  • Updated values for 'pad_sr_hv (output)'
		  • In table DC electrical specifications @ 5 V Range
		  • Updated Min value for Vhys

		• In section: Reset pad electrical characteristics
		  • Revised table, Reset electrical characteristics
		  • Deleted note, There are some specific ports that supports TTL functionality. These ports are, PB[4], PB[5], PB[6], PB[7], PB[8], PB[9], PD[0], PD[1], PD[2], PD[3], PD[4], PD[5], PD[6], PD[7], PD[8], PD[9], PD[10], and PD[11].
		• In section: PORST electrical specifications
		  • In table: PORST electrical specifications
		  • Updated 'Min' value for $W_{NFPORST}$
		
		• In section: Peripheral operating requirements and behaviours
		  • Changed section title from Input impedance and ADC accuracy to Input equivalent circuit and ADC conversion characteristics.
		  • Revised table: ADC conversion characteristics (for 12-bit) and ADC conversion characteristics (for 10-bit)
		  • Removed table, ADC supply configurations.
		
		• In section: Analogue Comparator (CMP) electrical specifications
		  • In table: Comparator and 6-bit DAC electrical specifications
		  • Updated 'Max' value of I_{DDLS}
		  • Updated 'Min' and 'Max' for V_{AIO} and DNL
		  • Updated 'Descripton' 'Min' 'Max' od V_H
		  • Updated row for t_{DHS}
		  • Added row for t_{DLS}
		  • Removed row for V_{CMPOh} and V_{CMPOl}
		
		• In section: Clocks and PLL interfaces modules
		  • In table: Main oscillator electrical characteristics
		  • V_{XOSCHS}: Removed values for 4 MHz.
		  • $T_{XOSCHSSU}$: Updated range to 8-40 MHz.
		  • In table: 16 MHz RC Oscillator electrical specifications
		  • Updated 'Max' for $T_{startup}$ and T_{LTJIT}
		  • Removed $F_{Untrimmed}$ row
		  • In table: 128 KHz Internal RC oscillator electrical specifications
		  • Fosc: Removed Uncaliberated 'Condition' and updated 'Min', 'Typ', and 'Max' for Caliberated condition
		  • Fosc: Updated 'Temperature dependence' and 'Supply dependence' Max values
		  • In table: PLL electrical specifications
		  • Removed entries for Input Clock Low Level, Input Clock High Level, Power consumption, Regulator Maximum Output Current, Analog Supply, Digital Supply (V_{DD_LV}), Modulation Depth (Down Spread), PLL reset assertion time, and Power Consumption

Table continues on the next page...

Table 52. Revision History (continued)

Rev. No.	Date	Substantial Changes
		• Removed 'Typ' value for Duty Cycle at pllclkout • Removed 'Min' value for Lock Time in calibration mode. • In table: Jitter calculation • Added 1 Sigma Random Jitter and Total Period Jitter values for Long Term Jitter (Interger and Fractional Mode) rows.
		• In section Flash read wait state and address pipeline control settings • In Flash Read Wait State and Address Pipeline Control: Updated APC for 40 MHz. • Removed section: On-chip peripherals
		• In section, Thermal attributes • Added table for 100 MAPBGA • In section Obtaining package dimensions • Updated package details for 100 MAPBGA
		• Editoral updates throughtout including correction of various module names.
Rev 3	2 March 2016	• In section, Recommended operating conditions • Added a new Note • In section, Voltage regulator electrical characteristics • In table, Voltage regulator electrical specifications: • Added a new row for $C_{HV\_VDD\_B}$ • Added a footnote on $V_{DD\_HV\_BALLAST}$ • Added a new Note at the end of this section • In section, Voltage monitor electrical characteristics • In table, Voltage monitor electrical characteristics: • Removed "V_{LVD_FLASH}" and "V_{LVD_FLASH} during low power mode using LPBG as reference" rows • Updated Fall and Rise trimmed Minimum values for $V_{HVD\_LV\_cold}$ • In section, Supply current characteristics • In table, Current consumption characteristics: • Updated the footnote mentioned in the Condition column of I_{DD_STOP} row • Updated all TBD values • In table, Low Power Unit (LPU) Current consumption characteristics: • Updated the typical value of LPU_STOP to 0.18 mA • Updated all TBD values • In table, STANDBY Current consumption characteristics: • Updated all TBD values • In section, AC specifications @ 3.3 V Range • In table, Functional Pad AC Specifications @ 3.3 V Range: • Updated Rise/Fall Edge values • In section, DC electrical specifications @ 3.3V Range • In table, DC electrical specifications @ 3.3V Range: • Updated Max value for Vol to 0.1 * VDD_HV_x • In section, AC specifications @ 5 V Range • In table, Functional Pad AC Specifications @ 5 V Range: • Updated Rise/Fall Edge values • In section, DC electrical specifications @ 5 V Range • In table, DC electrical specifications @ 5 V Range:

Table continues on the next page...

Table 52. Revision History (continued)

Rev. No.	Date	Substantial Changes
		• Updated Min and Max values for Pull_Ioh and Pull_Iol rows • Updated Max value for Vol to 0.1 * VDD_HV_x • In section, Reset pad electrical characteristics • In table, Functional reset pad electrical specifications: • Updated parameter column for V_{IH}, V_{IL} and V_{HYS} rows • Updated Min and Max values for V_{IH} and V_{IL} rows • In section, PORST electrical specifications • In table, PORST electrical specifications: • Updated Unit and Min/Max values for V_{IH} and V_{IL} rows • In section, Input equivalent circuit and ADC conversion characteristics • In table, ADC conversion characteristics (for 12-bit): • Updated "ADC Analog Pad (pad going to one ADC)" row • In table, ADC conversion characteristics (for 10-bit): • Updated "ADC Analog Pad (pad going to one ADC)" row • In section, Analog Comparator (CMP) electrical specifications • In table, Comparator and 6-bit DAC electrical specifications: • Updated Min and Max values for V_{AIO} to ±47 mV • Updated Max value for t_{DLS} to 21 µs • In section, Main oscillator electrical characteristics • In table, Main oscillator electrical characteristics: • Updated V_{IH} Min value to 1.95V • Updated V_{IL} Max value to 1.25V • Removed V_{IH} Typ value • In section, PLL electrical specifications • In table, PLL electrical specifications: • Updated Max value for Modulation Depth (Center Spread) to +/- 3.0%
Rev 4	9 March 2016	• In section, Voltage regulator electrical characteristics • In table, Voltage regulator electrical specifications: • Updated the footnote on $V_{DD\_HV\_BALLAST}$
Rev 5	27 February 2017	• In Family Comparison section: • Updated the "MPC5746C Family Comparison" table. • added "NVM Memory Map 1", "NVM Memory Map 2", and "RAM Memory Map" tables. • Updated the product version, flash memory size and optional fields information in Ordering Information section. • In Recommended Operating Conditions section, removed the note related to additional crossover current. • VDD_HV_C row added in "Voltage regulator electrical specifications" table in Voltage regulator electrical characteristics section. • In Voltage Monitor Electrical Characteristics section, updated the "Trimmed" Fall and Rise specs of VHVD_LV_cold parameter in "Voltage Monitor Electrical Characteristics" table. • In AC Electrical Specifications: 3.3 V Range section, changed the occurrences of “ipp_sre[1:0]” to “SIUL2_MSCRn.SRC[1:0]” in the table.

Table continues on the next page...

Table 52. Revision History (continued)

Rev. No.	Date	Substantial Changes

		• In DC Electrical Specifications: 3.3 V Range section, changed the occurrences of “ipp_sre[1:0]” to “SIUL2_MSCRn.SRC[1:0]” and updated "Vol min and max" values in the table.
		• In AC Electrical Specifications: 5 V Range section, changed the occurrences of “ipp_sre[1:0]” to “SIUL2_MSCRn.SRC[1:0]” in the table.
		• In DC Electrical Specifications: 5 V Range section, changed the occurrences of “ipp_sre[1:0]” to “SIUL2_MSCRn.SRC[1:0]” and updated "Vol min and max" values in the table.
		• In "Flash memory AC timing specifications" table in Flash memory AC timing specifications section:
		  • Updated the "t_{psus}" typ value from 7 us to 9.4 us.
		  • Updated the "t_{psus}" max value from 9.1 us to 11.5 us.
		• Added "Continuous SCK Timing" table in DSPI timing section.
		• Added "ADC pad leakage" at 105°C TA conditions in "ADC conversion characteristics (for 12-bit)" table in ADC electrical specifications section.
		• In "STANDBY Current consumption characteristics" table in Supply current characteristics section:
		  • Updated the Typ and max values of IDD Standby current.
		  • Added IDD Standby3 current spec for FIRC ON.
		• Removed IVDDHV and IVDDLV specs in 16 MHz RC Oscillator electrical specifications section.
		• Added Reset Sequence section, with Reset Sequence Duration, BAF execution duration section, and Reset Sequence Distribution as its sub-sections.

Rev 5.1	22 May 2017	• Removed the Introduction section from Section 4 "General". • In AC Specifications@3.3V section, removed note related to Cz results and added two notes. • In AC Specifications@5V section, added two notes. • In ADC Electrical Specifications section, added spec value of "ADC Analog Pad" at Max leakage (standard channel)@ 105 C T_A in "ADC conversion characteristics (for 10-bit)" table. • In PLL Electrical Specifications section, updated the first footnote of "Jitter calculation" table. • In Analog Comparator Electrical Specifications section, updated the TDLS (propagation delay, low power mode) max value in "Comparator and 6-bit DAC electrical specifications" table to 21 us. • In Recommended Operating Conditions section, updated the footnote link to T_A in "Recommended operating conditions (V DD_HV_x = 5V)" table.
Rev 6	21 Nov 2018	• In Table 2 changed the Code Flash Block 9 (0x01240000 - 0x0127FFFF) from 'not available' to 'available' for MPC5746. • In Table 3 added 32 and 64 KB flash blocks and footnote "Flexible patitions for boot and EEPROM". • Added Table 4.

Table 52. Revision History

Rev. No.	Date	Substantial Changes

		• Updated GPIO and added GPI row in Table 1.
		• Changed the EEPROM support for MPC574xC devices from Emulated up to"64K" to "Emulated up to 128K" in Table 1.
		• Changed "$V_{DD\_HV\_A}$" to "$V_{DD\_HV\_IO}$" and changed the condition from "$V_{DD\_HV\_A}$ = V_{DD_POR}" to "3.0 V < $V_{DD\_HV\_IO}$ < 5.5 V" in Table 19.
		• Added the text "For internal ballast configuration the VRC_CTL pin should be left floating" in existing foot note "Recommended Transistors:MJD31 @ 85°C....." in Table 11.
		• Added note "For the Precision channel Analog inputs...pulled low/high externally" after the table "STANDBY Current consumption characteristics" in Supply current characteristics.
		• In Table 36 :
		  • Added footnote in "High Speed Mode" column.
		  • For Parameter "DSPI cycle time" changed the Condition from "Master (MTFE=0)" to "Master".
		• In Voltage monitor electrical characteristics
		  • Under the column "Reset Type" changed "Destructive" to "POR" throughout the table "Voltage monitor electrical characteristics".
		  • Changed the Reset type of "$V_{LVD\_IO\_A\_HI}$" to "Functional"