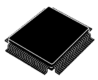
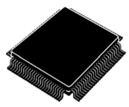
SPC582Bx

SPC58 2B Line - 32 bit Power Architecture automotive MCU Single core 80Mhz, 1MByte Flash, ASIL-B

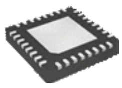
Datasheet - production data



eTQFP64 (10 x 10 x 1.0 mm)



eTQFP100 (14 x 14 x 1.0 mm)



QFN48 (7 x 7 x 0.9 mm)

Features

- AEC-Q100 qualified
- High performance e200z2 single core
  - 32-bit Power Architecture technology CPU
  - Core frequency as high as 80 MHz
  - Variable Length Encoding (VLE)
  - Floating Point, End-to-End Error Correction
- 1088 KB (1024 KB code flash + 64 KB data flash) on-chip flash memory: supports read during program and erase operations, and multiple blocks allowing EEPROM emulation
- 96 KB on-chip general-purpose SRAM
- Multi-channel direct memory access controller (eDMA) with 16 channels
- 1 interrupt controller (INTC)
- Comprehensive new generation ASIL-B safety concept
  - ASIL-B of ISO 26262
  - FCCU for collection and reaction to failure notifications
  - Memory Error Management Unit (MEMU) for collection and reporting of error events in memories
  - Cyclic redundancy check (CRC) unit
  - End-to-end Error Correction Code (e2eECC) logic
- Crossbar switch architecture for concurrent access to peripherals, Flash, or RAM from multiple bus masters with end-to-end ECC
- Body cross triggering unit (BCTU)
  - Triggers ADC conversions from any eMIOS channel
  - Triggers ADC conversions from up to 2 dedicated PIT_RTIs
  - 1 event configuration register dedicated to each timer event allows to define the corresponding ADC channel
  - Synchronization with ADC to avoid collision
- 1 enhanced 12-bit SAR analog-to-digital converters
  - Up to 27 channels
  - enhanced diagnosis feature
- Communication interfaces
  - 6 LINFlexD modules
  - 4 deserial serial peripheral interface (DSPI) modules
  - 7 MCAN interfaces with advanced shared memory scheme and ISO CAN FD support
- Dual phase-locked loops with stable clock domain for peripherals and FM modulation domain for computational shell
- Nexus Class 3 debug and trace interface
- Boot assist Flash (BAF) supports factory programming using a serial bootload through the asynchronous CAN or LIN/UART.
- Enhanced modular IO subsystem (eMIOS): up to 32 timed I/O channels with 16-bit counter resolution
- Advanced and flexible supply scheme
  - On-chip voltage regulator for 1.2 V core logic supply.
- Junction temperature range -40 °C to 150 °C

Table 1. Device summary

Package	Part number		
	1 MB	**768 kB**	**512 kB**
eTQFP64	SPC582B60E1	SPC582B54E1	SPC582B50E1
eTQFP100	SPC582B60E3	SPC582B54E3	SPC582B50E3
QFN48	SPC582B60Q3	SPC582B54Q3	SPC582B50Q3

Contents

1 Introduction

This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the device. To ensure a complete understanding of the device functionality, refer also to the device reference manual and errata sheet.

2 Description

The SPC582Bx microcontroller is the entry member of a new family of devices superseding the SPC560Bx family.

SPC582Bx is built on the legacy of the SPC5x products, while introducing new features to answer the future requirements like the ASIL-B classification, high number of ISO CAN-FD channels, and provide significant power and performance improvement (MIPS per mW).

2.1 Device feature summary

Table 2 lists a summary of major features for the SPC582Bx device. The feature column represents a combination of module names and capabilities of certain modules. A detailed description of the functionality provided by each on-chip module is given later in this document.

Table 2. SPC582Bx device feature summary

Feature	Description
SPC58 family	40 nm
Number of Cores	1
Single Precision Floating Point	Yes
SIMD	No
VLE	Yes
MPU	Yes
CRC Channels	2 x 4
Software Watchdog Timer (SWT)	1
Core Nexus Class	3+
Event Processor	4 x SCU
	4 x PMC
Run control Module	Yes
System SRAM	96 KB (including 64 KB of standby RAM)
Flash	1088 KB (1024 code flash + 64 KB data flash)
Flash fetch accelerator	2 x 4 x 256-bit
DMA channels	16
DMA Nexus Class	3
LINFlexD	6
MCAN (ISO CAN-FD)	7
DSPI	4
I2C	1

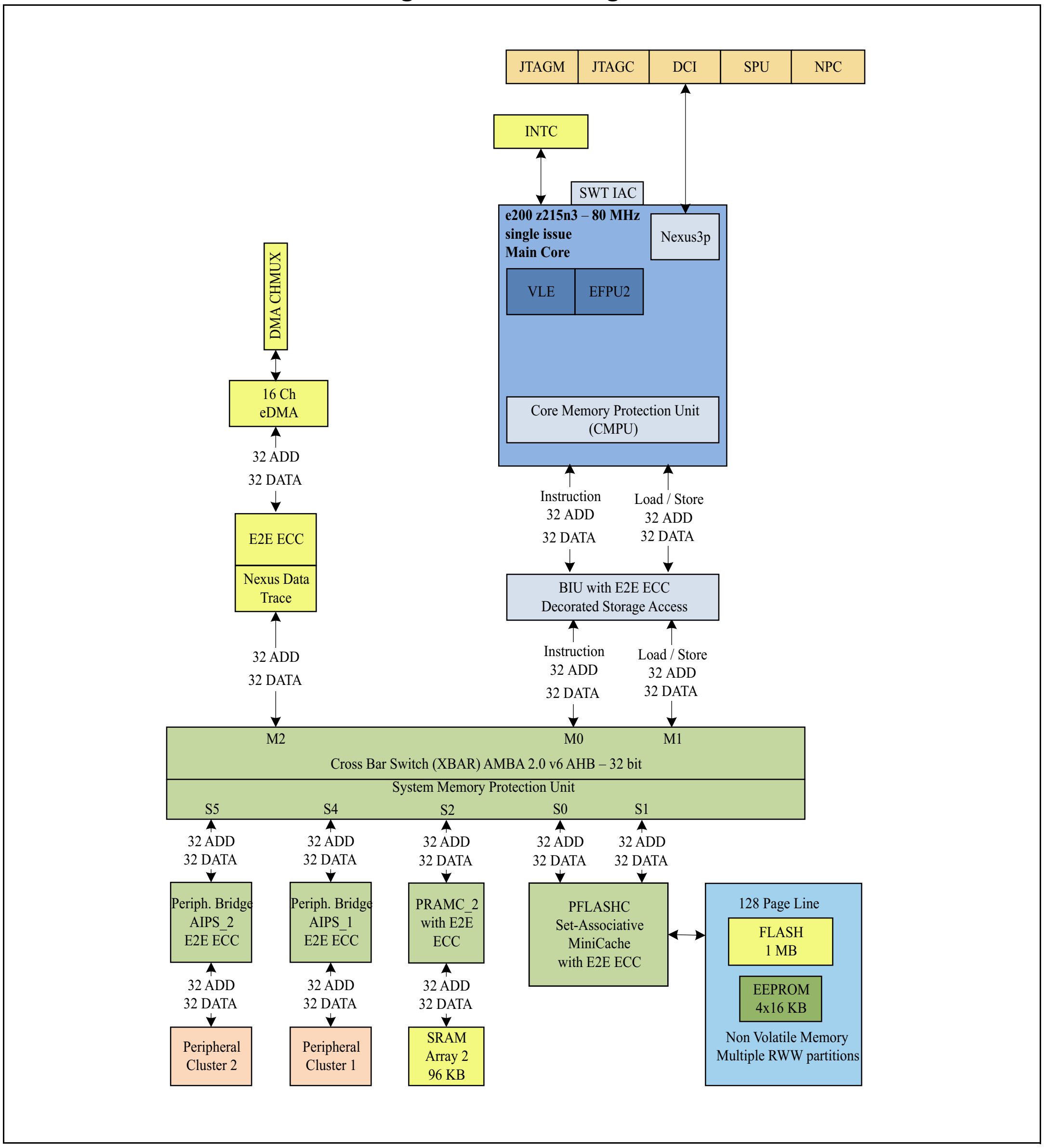
Table 2. SPC582Bx device feature summary (continued)

Feature	Description
System Timers	8 PIT channels
	4 AUTOSAR® (STM)
	RTC/API
eMIOS	32 channels
BCTU	32 channels
Interrupt controller	1 x 151 sources
ADC (SAR)	One 12-bit, up to 27 channels
Self Test Controller	Yes
PLL	Dual PLL with FM
Integrated linear voltage regulator	Yes
External Power Supplies	5 V, 3.3 V
Low Power Modes	STOP Mode
	HALT Mode
	Standby Mode

2.2 Block diagram

The figures below show the top-level block diagrams.

Figure 1. Block diagram



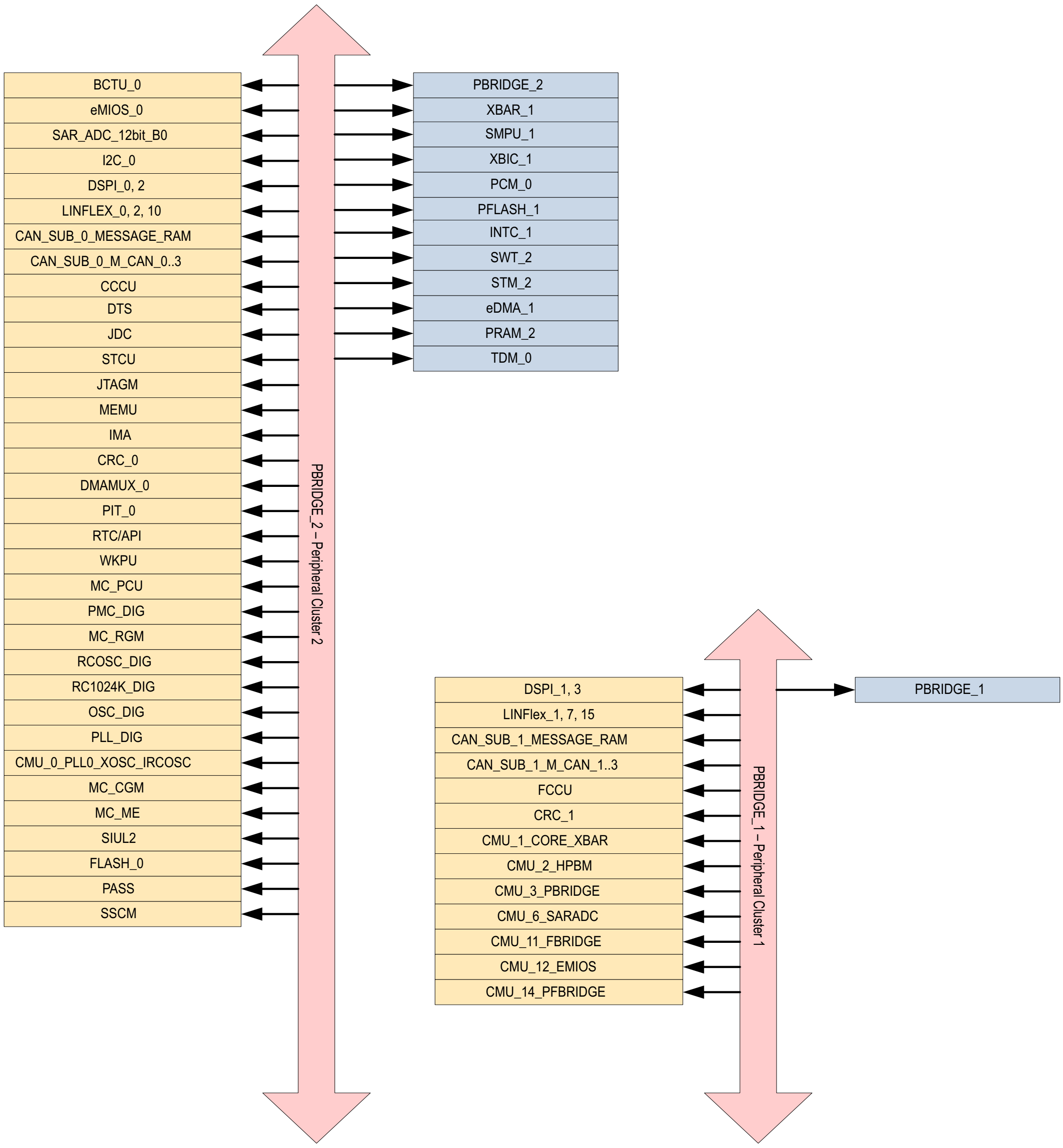


Figure 2. Periphery allocation

Note: In this diagram, ON-platform modules are shown in orange color and OFF-platform modules are shown in blue color.

2.3 Feature overview

On-chip modules within SPC582Bx include the following features:

- One main CPU, single issue, 32-bit CPU core complexes (e200z2).
  - Power Architecture embedded specification compliance
  - Instruction set enhancement allowing variable length encoding (VLE), encoding a mix of 16-bit and 32-bit instructions, for code size footprint reduction
  - Single-precision floating point operations
- 1088 KB (1024 KB code flash + 64 KB data flash) on-chip Flash memory
  - Supports read during program and erase operations, and multiple blocks allowing EEPROM emulation
- 96 KB on-chip general-purpose SRAM
- Multi channel direct memory access controllers
  - 16 eDMA channels
- One interrupt controller (INTC)
- Dual phase-locked loops with stable clock domain for peripherals and FM modulation domain for computational shell
- Crossbar switch architecture for concurrent access to peripherals, Flash, or RAM from multiple bus masters with end-to-end ECC
- System integration unit lite (SIUL)
- Boot assist Flash (BAF) supports factory programming using a serial bootload through the asynchronous CAN or LIN/UART.
- Hardware support for safety ASIL-B level related applications
- Enhanced modular IO subsystem (eMIOS): up to 32 timed I/O channels with 16-bit counter resolution
  - Buffered updates
  - Support for shifted PWM outputs to minimize occurrence of concurrent edges
  - Supports configurable trigger outputs for ADC conversion for synchronization to channel output waveforms
  - Shared or independent time bases
  - DMA transfer support available
- Body cross triggering unit (BCTU)
  - Triggers ADC conversions from any eMIOS channel
  - Triggers ADC conversions from up to 2 dedicated PIT_RTIs
  - One event configuration register dedicated to each timer event allows to define the corresponding ADC channel
  - Synchronization with ADC to avoid collision
- One 12-bit SAR analog-to-digital converter
  - up to 27 channels
  - enhanced diagnosis features
- Four deserial serial peripheral interface (DSPI) modules
- Six LIN and UART communication interface (LINFlexD) modules
  - LINFlexD_0 is a Master/Slave
  - All others are Masters

- Seven modular controller area network (MCAN) modules, all supporting flexible data rate (ISO CAN-FD)
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 standard, with some support for 2010 standard
- Device and board test support per Joint Test Action Group (JTAG) (IEEE 1149.1 and IEEE 1149.7), 2-pin JTAG interface
- On-chip voltage regulator controller manages the supply voltage down to 1.2 V for core logic
- Self-test capability

3 Package pinouts and signal descriptions

Refer to the SPC582Bx IO_ Definition document.

It includes the following sections:

1. Package pinouts
2. Pin descriptions
    a) Power supply and reference voltage pins
    b) System pins
    c) Generic pins

4 Electrical characteristics

4.1 Introduction

The present document contains the target Electrical Specification for the 40 nm family 32-bit MCU SPC582Bx products.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” (Controller Characteristics) is included in the “Symbol” column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” (System Requirement) is included in the “Symbol” column.

The electrical parameters shown in this document are guaranteed by various methods. To give the customer a better understanding, the classifications listed in *Table 3* are used and the parameters are tagged accordingly in the tables where appropriate.

Table 3. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design validation on a small sample size from typical devices.
D	Those parameters are derived mainly from simulations.

4.2 Absolute maximum ratings

Table 4 describes the maximum ratings for the device. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Stress beyond the listed maxima, even momentarily, may affect device reliability or cause permanent damage to the device.

Table 4. Absolute maximum ratings

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{DD_LV}	SR	D	Core voltage operating life range(1)	—	–0.3	—	1.4	V
$V_{DD\_HV\_IO\_MAIN}$ $V_{DD\_HV\_OSC}$ $V_{DD\_HV\_FLA}$	SR	D	I/O supply voltage(2)	—	–0.3	—	6.0	V
$V_{SS\_HV\_ADV}$	SR	D	ADC ground voltage	Reference to digital ground	–0.3	—	0.3	V
$V_{DD\_HV\_ADV}$	SR	D	ADC Supply voltage(2)	Reference to $V_{SS\_HV\_ADV}$	–0.3	—	6.0	V
$V_{SS\_HV\_ADR\_S}$	SR	D	SAR ADC ground reference	—	–0.3	—	0.3	V
$V_{DD\_HV\_ADR\_S}$	SR	D	SAR ADC voltage reference(2)	Reference to $V_{SS\_HV\_ADR\_S}$	–0.3	—	6.0	V
V_{SS}-$V_{SS\_HV\_ADR\_S}$	SR	D	$V_{SS\_HV\_ADR\_S}$ differential voltage	—	–0.3	—	0.3	V
V_{SS}-$V_{SS\_HV\_ADV}$	SR	D	$V_{SS\_HV\_ADV}$ differential voltage	—	–0.3	—	0.3	V
V_{IN}	SR	D	I/O input voltage range(2)(3) (4)	—	–0.3	—	6.0	V
				Relative to V_{ss}	–0.3	—	—	
				Relative to $V_{DD\_HV\_IO}$ and $V_{DD\_HV\_ADV}$	—	—	0.3	
T_{TRIN}	SR	D	Digital Input pad transition time(5)	—	—	—	1	ms
I_{INJ}	SR	T	Maximum DC injection current for each analog/digital PAD(6)	—	–5	—	5	mA

Table 4. Absolute maximum ratings (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
T_{STG}	SR	T	Maximum non-operating Storage temperature range	—	–55	—	125	°C
T_{PAS}	SR	C	Maximum non-operating temperature during passive lifetime	—	–55	—	150(7)	°C
$T_{STORAGE}$	SR	—	Maximum storage time, assembled part programmed in ECU	No supply; storage temperature in range –40 °C to 60 °C	—	—	20	years
T_{SDR}	SR	T	Maximum solder temperature Pb-free packaged(8)	—	—	—	260	°C
MSL	SR	T	Moisture sensitivity level(9)	—	—	—	3	—
T_{XRAY} dose	SR	T	Maximum cumulated XRAY dose	Typical range for X-rays source during inspection:80 ÷ 130 KV; 20 ÷ 50 µA	—	—	1	grey

1. V_{DD_LV}: allowed 1.335 V - 1.400 V for 60 seconds cumulative time at the given temperature profile. Remaining time allowed 1.260 V - 1.335 V for 10 hours cumulative time at the given temperature profile. Remaining time as defined in *Section 4.3: Operating conditions*.
2. V_{DD_HV}: allowed 5.5 V – 6.0 V for 60 seconds cumulative time at the given temperature profile, for 10 hours cumulative time with the device in reset at the given temperature profile. Remaining time as defined in *Section 4.3: Operating conditions*.
3. The maximum input voltage on an I/O pin tracks with the associated I/O supply maximum. For the injection current condition on a pin, the voltage will be equal to the supply plus the voltage drop across the internal ESD diode from I/O pin to supply. The diode voltage varies greatly across process and temperature, but a value of 0.3 V can be used for nominal calculations.
4. Relative value can be exceeded if design measures are taken to ensure injection current limitation (parameter IINJ).
5. This limitation applies to pads with digital input buffer enabled. If the digital input buffer is disabled, there are no maximum limits to the transition time.
6. The limits for the sum of all normal and injected currents on all pads within the same supply segment can be found in *Section 4.8.3: I/O pad current specifications*.
7. 175°C are allowed for limited time. Mission profile with passive lifetime temperature >150°C have to be evaluated by ST to confirm that are granted by product qualification.
8. Solder profile per IPC/JEDEC J-STD-020D.
9. Moisture sensitivity per JDEC test method A112.

4.3 Operating conditions

Table 5 describes the operating conditions for the device, and for which all the specifications in the data sheet are valid, except where explicitly noted. The device operating conditions must not be exceeded or the functionality of the device is not guaranteed.

Table 5. Operating conditions

Symbol		C	Parameter	Conditions	Value(1)			Unit
					Min	Typ	Max	
F_{SYS}	SR	P	Operating system clock frequency(4)	—	—	—	80	MHz
T_J	SR	C	Operating Junction temperature	—	–40	—	150	°C
T_A	SR	P	Operating Ambient temperature	—	–40	—	125	°C
V_{DD_LV}	SR	P	Core supply voltage(2)	—	1.14	1.20	1.26(3) (4)	V
$V_{DD\_HV\_IO\_MAIN}$ $V_{DD\_HV\_FLA}$ $V_{DD\_HV\_OSC}$	SR	P	IO supply voltage	—	3.0	—	5.5	V
$V_{DD\_HV\_ADV}$	SR	P	ADC supply voltage	—	3.0	—	5.5	V
$V_{SS\_HV\_ADV}$- V_{SS}	SR	D	ADC ground differential voltage	—	–25	—	25	mV
$V_{DD\_HV\_ADR\_S}$	SR	P	SAR ADC reference voltage	—	3.0	—	5.5	V
$V_{DD\_HV\_ADR\_S}$- $V_{DD\_HV\_ADV}$	SR	D	SAR ADC reference differential voltage	—	—	—	25	mV
$V_{SS\_HV\_ADR\_S}$	SR	P	SAR ADC ground reference voltage	—	$V_{SS\_HV\_ADV}$			V
$V_{SS\_HV\_ADR\_S}$- $V_{SS\_HV\_ADV}$	SR	D	$V_{SS\_HV\_ADR\_S}$ differential voltage	—	–25	—	25	mV
V_{RAMP_HV}	SR	D	Slew rate on HV power supply	—	—	—	100	V/ms

Table 5. Operating conditions (continued)

Symbol		C	Parameter	Conditions	Value[1]			Unit
					Min	Typ	Max	
V_{IN}	SR	P	I/O input voltage range	—	0	—	5.5	V
I_{INJ1}	SR	T	Injection current (per pin) without performance degradation[5] [6] [7]	Digital pins and analog pins	–3.0	—	3.0	mA
I_{INJ2}	SR	D	Dynamic Injection current (per pin) with performance degradation[7] [8]	Digital pins and analog pins	–10	—	10	mA

1. The ranges in this table are design targets and actual data may vary in the given range.
2. Core voltage as measured on device pin to guarantee published silicon performance.
3. Core voltage can exceed 1.26 V with the limitations provided in *Section 4.2: Absolute maximum ratings*, provided that HVD134_C monitor reset is disabled.
4. 1.260 V - 1.290 V range allowed periodically for supply with sinusoidal shape and average supply value below or equal to 1.236 V at the given temperature profile.
5. Full device lifetime. I/O and analog input specifications are only valid if the injection current on adjacent pins is within these limits. See *Section 4.2: Absolute maximum ratings* for maximum input current for reliability requirements.
6. The I/O pins on the device are clamped to the I/O supply rails for ESD protection. When the voltage of the input pins is above the supply rail, current will be injected through the clamp diode to the supply rails. For external RC network calculation, assume typical 0.3 V drop across the active diode. The diode voltage drop varies with temperature.
7. The limits for the sum of all normal and injected currents on all pads within the same supply segment can be found in *Section 4.8.3: I/O pad current specifications*.
8. Positive and negative Dynamic current injection pulses are allowed up to this limit. I/O and ADC specifications are not granted. See the dedicated chapters for the different specification limits. See the Absolute Maximum Ratings table for maximum input current for reliability requirements. Refer to the following pulses definitions: Pulse1 (ISO 7637-2:2011), Pulse 2a(ISO 7637-2:2011 5.6.2), Pulse 3a (ISO 7637-2:2011 5.6.3), Pulse 3b (ISO 7637-2:2011 5.6.3).

4.3.1 Power domains and power up/down sequencing

The following table shows the constraints and relationships for the different power domains. Supply1 (on rows) can exceed Supply2 (on columns), only if the cell at the given row and column is reporting ‘ok’. This limitation is valid during power-up and power-down phases, as well as during normal device operation.

Table 6. Device supply relation during power-up/power-down sequence

		Supply2			
		V_{DD_LV}	$V_{DD\_HV\_IO\_MAIN}$ $V_{DD\_HV\_FLA}$ $V_{DD\_HV\_OSC}$	$V_{DD\_HV\_ADV}$	$V_{DD\_HV\_ADR}$
Supply1	$V_{DD\_HV\_IO\_MAIN}$ $V_{DD\_HV\_FLA}$ $V_{DD\_HV\_OSC}$(1)	ok		ok	ok
	$V_{DD\_HV\_ADV}$	ok	not allowed		ok
	$V_{DD\_HV\_ADR}$	ok	not allowed	not allowed	

1. The application shall grant that these supplies are always at the same voltage level.

During power-up, all functional terminals are maintained in a known state as described in the device pinout Microsoft Excel file attached to the IO_Definition document.

4.4 Electrostatic discharge (ESD)

The following table describes the ESD ratings of the device:

- All ESD testing are in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits,
- Device failure is defined as: “If after exposure to ESD pulses, the device does not meet the device specification requirements, which include the complete DC parametric and functional testing at room temperature and hot temperature, maximum DC parametric variation within 10% of maximum specification”.

Table 7. ESD ratings

Parameter	C	Conditions	Value	Unit
ESD for Human Body Model (HBM)(1)	T	All pins	2000	V
ESD for field induced Charged Device Model (CDM)(2)	T	All pins	500	V
	T	Corner Pins	750	V

1. This parameter tested in conformity with ANSI/ESD STM5.1-2007 Electrostatic Discharge Sensitivity Testing.
2. This parameter tested in conformity with ANSI/ESD STM5.3-1990 Charged Device Model - Component Level.

4.5 Electromagnetic compatibility characteristics

EMC measurements at IC-level IEC standards are available from STMicroelectronics on request.

4.6 Temperature profile

The device is qualified in accordance to AEC-Q100 Grade1 requirements, such as HTOL 1,000 h and HTDR 1,000 hrs, T_J = 150 °C.

4.7 Device consumption

Table 8. Device consumption

Symbol		C	Parameter	Conditions	Value[1]			Unit
					Min	Typ	Max	
I_{DD_LKG}[2],[3]	CC	C	Leakage current on the V_{DD_LV} supply	T_J = 40 °C	—	—	2	mA
		D		T_J = 25 °C	—	0.65	1	
		D		T_J = 55 °C	—	—	2.5	
		D		T_J = 95 °C	—	—	6	
		D		T_J = 120 °C	—	—	14	
		P		T_J = 150 °C	—	—	35	
I_{DD_LV}[3]	CC	P	Dynamic current on the V_{DD_LV} supply, very high consumption profile[4]	—	—	—	50	mA
I_{DD_HV}	CC	P	Total current on the V_{DD_HV} supply[4]	f_{MAX}	—	—	37	mA
$I_{DD\_LV\_GW}$	CC	T	Dynamic current on the V_{DD_LV} supply, gateway profile[5]	—	—	—	48	mA
$I_{DD\_HV\_GW}$	CC	T	Dynamic current on the V_{DD_HV} supply, gateway profile[5]	—	—	—	17	mA
I_{DDHALT}[6]	CC	T	Dynamic current on the V_{DD_LV} supply +Total current on the V_{DD_HV} supply	—	—	26	37	mA
I_{DDSTOP}[7]	CC	T	Dynamic current on the V_{DD_LV} supply +Total current on the V_{DD_HV} supply	—	—	6.5	9	mA
$I_{DDSTBY8}$	CC	D	Total standby mode current on V_{DD_LV} and V_{DD_HV} supply, 8 KB RAM[8]	T_J = 25 °C	—	40	90	µA
		C		T_J = 40 °C	—	—	135	
		D		T_J = 55 °C	—	—	210	
		D		T_J = 120 °C	—	—	1.2	mA
		P		T_J = 150 °C	—	—	2.5	
$I_{DDSTBY64}$	CC	D	Total standby mode current on V_{DD_LV} and V_{DD_HV} supply, 64 KB RAM[8]	T_J = 25 °C	—	55	125	µA
		C		T_J = 40 °C	—	—	190	
		D		T_J = 55 °C	—	—	290	
		D		T_J = 120 °C	—	—	1.6	mA
		P		T_J = 150 °C	—	—	3.5	

1. The ranges in this table are design targets and actual data may vary in the given range.

2. The leakage considered is the sum of core logic and RAM memories. The contribution of analog modules is not considered, and they are computed in the dynamic I_{DD_LV} and I_{DD_HV} parameters.
3. I_{DD_LKG} (leakage current) and I_{DD_LV} (dynamic current) are reported as separate parameters, to give an indication of the consumption contributors. The tests used in validation, characterization and production are verifying that the total consumption (leakage+dynamic) is lower or equal to the sum of the maximum values provided (I_{DD_LKG} + I_{DD_LV}). The two parameters, measured separately, may exceed the maximum reported for each, depending on the operative conditions and the software profile used.
4. Use case: 1 x e200Z2 @80 MHz, all IPs clock enabled, Flash access with prefetch disabled, Flash consumption includes parallel read and program/erase, 1xSARADC in continuous conversion, DMA continuously triggered by ADC conversion, 4 DSPI / 3 CAN / 2 LINFlex transmitting, RTC and STM running, 1xEMIOS running (12 channels in OPWMT mode), FIRC, SIRC, FXOSC, PLL0-1 running. The switching activity estimated for dynamic consumption does not include I/O toggling, which is highly dependent on the application. Details of the software configuration are separately. The total device consumption is I_{DD_LV} + I_{DD_HV} + I_{DD_LKG} for the selected temperature.
5. Gateway use case: One core running at 80 MHz, DMA, PLL, FLASH read only 25%, 7xCAN, 1xSARADC.
6. Flash in Low Power. Sysclk at 80 MHz, PLL0_PHI at 80 MHz, XTAL at 8 MHz, FIRC 16 MHz ON, RCOSC1M off. FlexCAN: instances: 0, 1, 2, 3, 4, 5, 6 ON (configured but no reception or transmission), ADC ON (continuously converting). All others IPs clock-gated.
7. Sysclk = RC16 MHz, RC16 MHz ON, RC1 MHz ON, PLL OFF. All possible peripherals off and clock gated. Flash in power down mode.
8. STANDBY mode: device configured for minimum consumption, RC16 MHz off, RC1 MHz on.

4.8 I/O pad specification

The following table describes the different pad type configurations.

Table 9. I/O pad specification descriptions

Pad type	Description
Weak configuration	Provides a good compromise between transition time and low electromagnetic emission.
Medium configuration	Provides transition fast enough for the serial communication channels with controlled current to reduce electromagnetic emission.
Strong configuration	Provides fast transition speed; used for fast interface.
Very strong configuration	Provides maximum speed and controlled symmetric behavior for rise and fall transition. Used for fast interface requiring fine control of rising/falling edge jitter.
Input only pads	These low input leakage pads are associated with the ADC channels.
Standby pads	Some pads are active during Standby. Low Power Pads input buffer can only be configured in TTL mode. When the pads are in Standby mode, the Pad-Keeper feature is activated: if the pad status is high, the weak pull-up resistor is automatically enabled; if the pad status is low, the weak pull-down resistor is automatically enabled.

Note: Each I/O pin on the device supports specific drive configurations. See the signal description table in the device reference manual for the available drive configurations for each I/O pin. PMC_DIG_VSIO register has to be configured to select the voltage level (3.3 V or 5.0 V) for each IO segment.

Logic level is configurable in running mode while it is TTL not-configurable in STANDBY for LP (low power) pads, so if a LP pad is used to wakeup from STANDBY, it should be configured as TTL also in running mode in order to prevent device wrong behavior in STANDBY.

4.8.1 I/O input DC characteristics

The following table provides input DC electrical characteristics, as described in *Figure 3*.

Figure 3. I/O input electrical characteristics

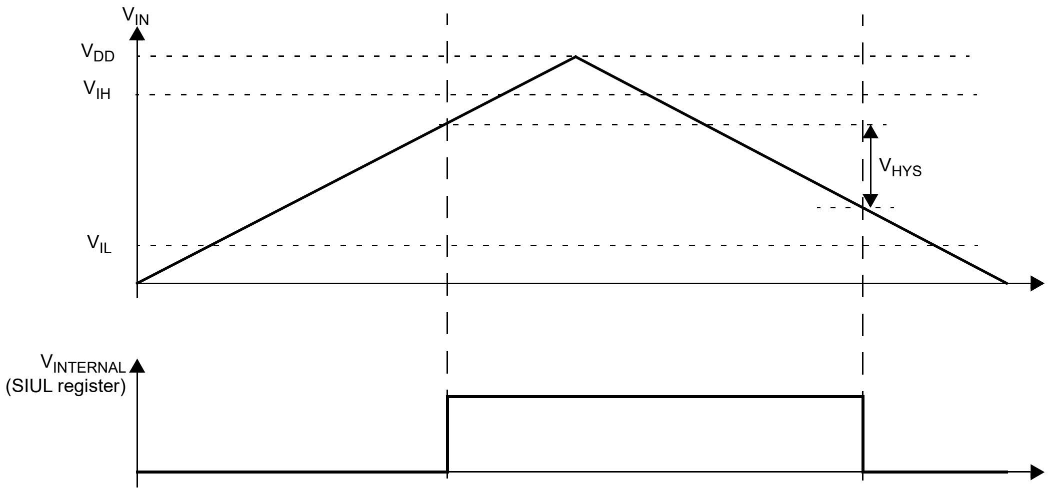


Table 10. I/O input electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
TTL								
V_{ihttl}	SR	P	Input high level TTL	—	2	—	$V_{DD\_HV\_IO}$ + 0.3	V
V_{ilttl}	SR	P	Input low level TTL	—	–0.3	—	0.8	V
V_{hysttl}	CC	C	Input hysteresis TTL	—	0.3	—	—	V
CMOS								
V_{ihcmos}	SR	P	Input high level CMOS	—	0.65 * V_{DD}	—	$V_{DD\_HV\_IO}$ + 0.3	V
V_{ilcmos}	SR	P	Input low level CMOS	—	–0.3	—	0.35 * V_{DD}	V
$V_{hyscmos}$	CC	C	Input hysteresis CMOS	—	0.10 * V_{DD}	—	—	V
COMMON								
I_{LKG}	CC	P	Pad input leakage	INPUT-ONLY pads T_J = 150 °C	—	—	200	nA
I_{LKG}	CC	P	Pad input leakage	STRONG pads T_J = 150 °C	—	—	1,000	nA
I_{LKG}	CC	P	Pad input leakage	VERY STRONG pads, T_J = 150 °C	—	—	1,000	nA

Table 10. I/O input electrical characteristics (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
C_{P1}	CC	D	Pad capacitance	—	—	—	10	pF
V_{drift}	CC	D	Input V_{il}/V_{ih} temperature drift	In a 1 ms period, with a temperature variation <30 °C	—	—	100	mV
W_{FI}	SR	C	Wakeup input filtered pulse(1)	—	—	—	20	ns
W_{NFI}	SR	C	Wakeup input not filtered pulse(1)	—	400	—	—	ns

1. In the range from W_{FI} (max) to W_{NFI} (min), pulses can be filtered or not filtered, according to operating temperature and voltage. Refer to the device pinout IO definition excel file for the list of pins supporting the wakeup filter feature.

Table 11. I/O pull-up/pull-down electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
I_{WPU}	CC	T	Weak pull-up current absolute value	V_{IN} = 1.1 V(1)	—	—	130	µA
		P		V_{IN} = 0.69 * $V_{DD\_HV\_IO}$(2)	15	—	—	
R_{WPU}	CC	D	Weak Pull-up resistance	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%	33	—	93	KΩ
R_{WPU}	CC	D	Weak Pull-up resistance	$V_{DD\_HV\_IO}$ = 3.3 V ± 10%	19	—	62	KΩ
I_{WPD}	CC	T	Weak pull-down current absolute value	V_{IN} = 0.69 * $V_{DD\_HV\_IO}$(1)	—	—	130	µA
		P		V_{IN} = 0.9 V(2)	15	—	—	
R_{WPD}	CC	D	Weak Pull-down resistance	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%	29	—	60	KΩ
R_{WPD}	CC	D	Weak Pull-down resistance	$V_{DD\_HV\_IO}$ = 3.3 V ± 10%	19	—	60	KΩ

1. Maximum current when forcing a change in the pin level opposite to the pull configuration.
2. Minimum current when keeping the same pin level state than the pull configuration.

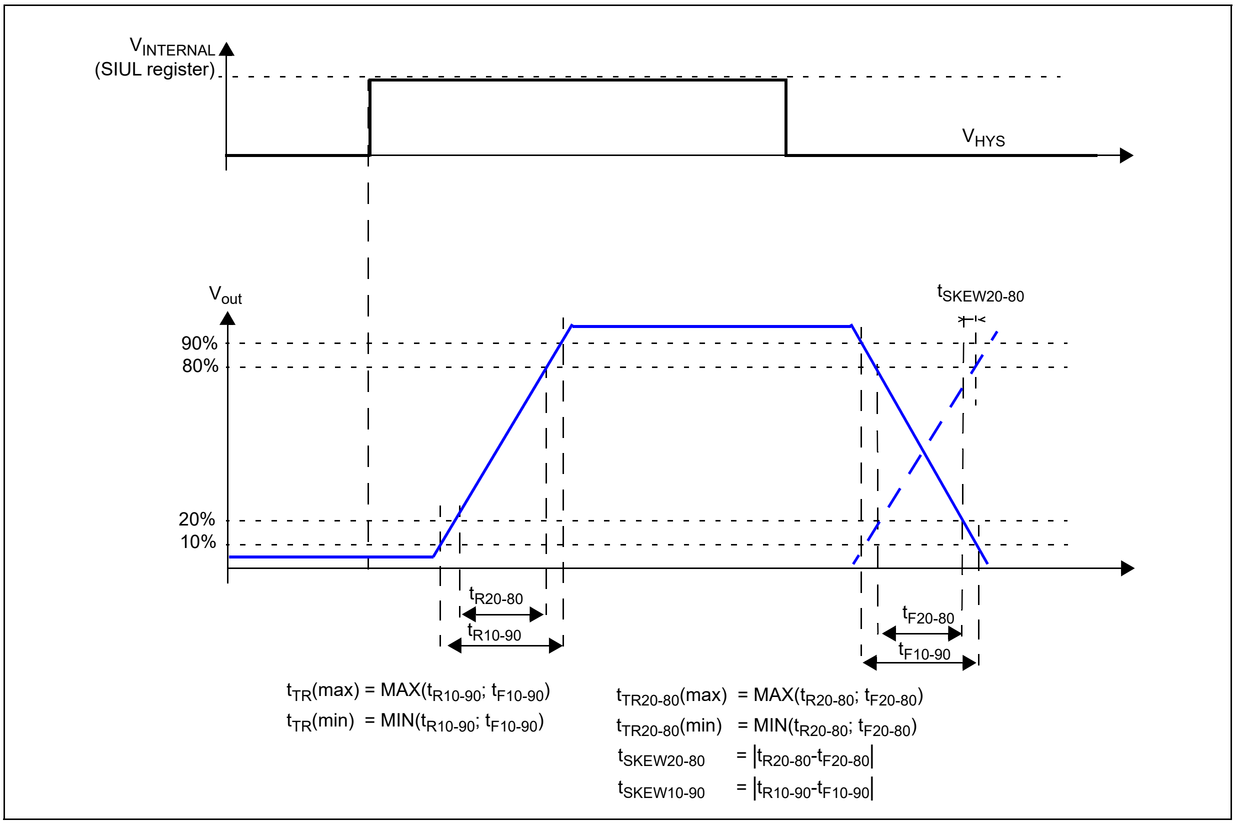
Note: When the device enters into standby mode, the LP pads have the input buffer switched-on. As a consequence, if the pad input voltage VIN is V_{SS}<V_{IN}<V_{DD_HV}, an additional consumption can be measured in the VDD_HV domain. The highest consumption can be seen around mid-range (VIN ~=VDD_HV/2), 2-3mA depending on process, voltage and

temperature.
This situation may occur if the PAD is used as a ADC input channel, and $V_{SS}<V_{IN}<V_{DD\_HV}$. The applications should ensure that LP pads are always set to VDD_HV or VSS, to avoid the extra consumption. Please refer to the device pinout IO definition excel file to identify the low-power pads which also have an ADC function.

4.8.2 I/O output DC characteristics

Figure 4 provides description of output DC electrical characteristics.

Figure 4. I/O output DC electrical characteristics definition



The following tables provide DC characteristics for bidirectional pads:

- *Table 12* provides output driver characteristics for I/O pads when in WEAK/SLOW configuration.
- *Table 13* provides output driver characteristics for I/O pads when in MEDIUM configuration.
- *Table 14* provides output driver characteristics for I/O pads when in STRONG/FAST configuration.
- *Table 15* provides output driver characteristics for I/O pads when in VERY STRONG/VERY FAST configuration.

Note: 10%/90% is the default condition for any parameter if not explicitly mentioned differently.

Table 12. WEAK/SLOW I/O output characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{ol_W}	CC	D	Output low voltage for Weak type PADs	I_{ol} = 0.5 mA V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	—	—	0.1*V_{DD}	V
V_{oh_W}	CC	D	Output high voltage for Weak type PADs	Ioh = 0.5 mA V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	0.9*V_{DD}	—	—	V
R_W	CC	P	Output impedance for Weak type PADs	V_{DD} = 5.0 V ± 10%	380	—	1040	Ω
				V_{DD} = 3.3 V ± 10%	250	—	700	
F_{max_W}	CC	T	Maximum output frequency for Weak type PADs	CL = 25 pF V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	—	—	2	MHz
				CL = 50 pF V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	—	—	1	MHz
t_{TR_W}	CC	T	Transition time output pin weak configuration, 10%-90%	CL = 25 pF V_{DD} = 5.0 V + 10% V_{DD} = 3.3 V + 10%	25	—	120	ns
				CL = 50 pF V_{DD} = 5.0 V ± 10 % V_{DD} = 3.3 V ± 10 %	50	—	240	ns
$\|t_{SKEW\_W}\|$	CC	T	Difference between rise and fall time, 90%-10%	—	—	—	25	%
I_{DCMAX_W}	CC	D	Maximum DC current	V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	—	—	0.5	mA

Table 13. MEDIUM I/O output characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{ol_M}	CC	D	Output low voltage for Medium type PADs	I_{ol} = 2.0 mA V_{DD} =5.0 V ± 10 % V_{DD} =3.3 V ± 10 %	—	—	0.1*V_{DD}	V
V_{oh_M}	CC	D	Output high voltage for Medium type PADs	I_{oh}=2.0 mA V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	0.9*V_{DD}	—	—	V

Table 13. MEDIUM I/O output characteristics (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
$R_{\_M}$	CC	P	Output impedance for Medium type PADs	V_{DD} = 5.0 V ± 10%	90	—	260	Ω
				V_{DD} = 3.3 V ± 10%	60	—	170	
F_{max_M}	CC	T	Maximum output frequency for Medium type PADs	CL = 25 pF V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	—	—	12	MHz
				CL = 50 pF V_{DD} = 5.0 V ± 10 % V_{DD} = 3.3 V ± 10 %	—	—	6	MHz
t_{TR_M}	CC	T	Transition time output pin MEDIUM configuration, 10%-90%	CL = 25 pF V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	8	—	30	ns
				CL = 50 pF V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	12	—	60	ns
$\|t_{SKEW\_M}\|$	CC	T	Difference between rise and fall time, 90%-10%	—	—	—	25	%
I_{DCMAX_M}	CC	D	Maximum DC current	V_{DD} = 5.0 V ± 10% V_{DD} = 3.3 V ± 10%	—	—	2	mA

Table 14. STRONG/FAST I/O output characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{ol_S}	CC	D	Output low voltage for Strong type PADs	I_{ol} = 8.0 mA V_{DD} = 5.0 V ± 10%	—	—	0.1*V_{DD}	V
				I_{ol} = 5.5 mA V_{DD} =3 .3 V ± 10%	—	—	0.15*V_{DD}	V
V_{oh_S}	CC	D	Output high voltage for Strong type PADs	I_{oh} = 8.0 mA V_{DD} = 5.0 V ± 10%	0.9*V_{DD}	—	—	V
				I_{oh} = 5.5 mA V_{DD} = 3.3 V ± 10%	0.85*V_{DD}	—	—	V
$R_{\_S}$	CC	P	Output impedance for Strong type PADs	V_{DD} = 5.0 V ± 10%	20	—	65	Ω
				V_{DD} = 3.3 V ± 10%	28	—	90	

Table 14. STRONG/FAST I/O output characteristics (continued)

Symbol		C	Parameter	Conditions	Value Min	Value Typ	Value Max	Unit
F_{max_S}	CC	T	Maximum output frequency for Strong type PADs	CL = 25 pF V_{DD}=5.0 V ± 10%	—	—	50	MHz
				CL = 50 pF V_{DD}=5.0 V ± 10%	—	—	25	MHz
				CL = 25 pF V_{DD} = 3.3 V ± 10%	—	—	25	MHz
				CL = 50 pF V_{DD} = 3.3 V ± 10%	—	—	12.5	MHz
t_{TR_S}	CC	T	Transition time output pin STRONG configuration, 10%-90%	CL = 25 pF V_{DD} = 5.0 V ± 10%	3	—	10	ns
				CL = 50 pF V_{DD} = 5.0 V ± 10%	5	—	16	
				CL = 25 pF V_{DD} = 3.3 V ± 10%	1.5	—	15	
				CL = 50 pF V_{DD} = 3.3 V ± 10%	2.5	—	26	
I_{DCMAX_S}	CC	D	Maximum DC current	V_{DD} = 5 V ± 10%	—	—	8	mA
				V_{DD} = 3.3 V ± 10%	—	—	5.5	
$\|t_{SKEW\_S}\|$	CC	T	Difference between rise and fall time, 90%-10%	—	—	—	25	%

Table 15. VERY STRONG/VERY FAST I/O output characteristics

Symbol		C	Parameter	Conditions	Value Min	Value Typ	Value Max	Unit
V_{ol_V}	CC	D	Output low voltage for Very Strong type PADs	I_{ol} = 9.0 mA V_{DD} =5.0 V ± 10%	—	—	0.1*V_{DD}	V
				I_{ol} = 9.0 mA V_{DD} =3.3 V ± 10%	—	—	0.15*V_{DD}	V
V_{oh_V}	CC	D	Output high voltage for Very Strong type PADs	I_{oh} = 9.0 mA V_{DD} = 5.0 V ± 10%	0.9*V_{DD}	—	—	V
				I_{oh} = 9.0 mA V_{DD} = 3.3 V ± 10%	0.85*V_{DD}	—	—	V
$R_{\_V}$	CC	P	Output impedance for Very Strong type PADs	V_{DD} = 5.0 V ± 10%	20	—	60	Ω
				V_{DD} = 3.3 V ± 10%	18	—	50	

Table 15. VERY STRONG/VERY FAST I/O output characteristics (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
F_{max_V}	CC	T	Maximum output frequency for Very Strong type PADs	CL = 25 pF V_{DD} = 5.0 V ± 10%	—	—	50	MHz
				CL = 50 pF V_{DD} = 5.0 V ± 10%	—	—	25	MHz
				CL = 25 pF V_{DD} = 3.3 V ± 10%	—	—	50	MHz
				CL = 50 pF V_{DD} = 3.3 V ± 10%	—	—	25	MHz
t_{TR_V}	CC	T	10–90% threshold transition time output pin VERY STRONG configuration	CL = 25 pF V_{DD} = 5.0 V ± 10%	1	—	6	ns
				CL = 50 pF V_{DD} = 5.0 V ± 10%	3	—	12	
				CL = 25 pF V_{DD} = 3.3 V ± 10%	1.5	—	6	
				CL = 50 pF V_{DD} = 3.3 V ± 10%	3	—	11	
$t_{TR20\text{-}80\_V}$	CC	T	20–80% threshold transition time output pin VERY STRONG configuration (Flexray Standard)	CL = 25 pF V_{DD} = 5.0 V ± 10%	0.8	—	4.5	ns
				CL = 15 pF V_{DD} = 3.3 V ± 10%	1	—	4.5	
t_{TRTTL_V}	CC	T	TTL threshold transition time for output pin in VERY STRONG configuration (Ethernet standard)	CL = 25 pF V_{DD} = 3.3 V ± 10%	0.88	—	5	ns
$\Sigma t_{TR20\text{-}80\_V}$	CC	T	Sum of transition time 20–80% output pin VERY STRONG configuration	CL = 25 pF V_{DD} = 5.0 V ± 10%	—	—	9	ns
				CL = 15 pF V_{DD} = 3.3 V ± 10%	—	—	9	
$\lvert t_{SKEW\_V}\rvert$	CC	T	Difference between rise and fall delay	CL = 25 pF V_{DD} = 5.0 V ± 10%	0	—	1.2	ns
I_{DCMAX_V}	CC	D	Maximum DC current	V_{DD} = 5.0 V±10% V_{DD} = 3.3 V ± 10%	—	—	9	mA

4.8.3 I/O pad current specifications

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a V_{DD}/V_{SS} supply pair as described in the device pinout Microsoft Excel file attached to the IO_Definition document.

Table 16 provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the I_{RMSSEG} maximum value.

In order to ensure device functionality, the sum of the dynamic and static current of the I/O on a single segment should remain below the I_{DYNSEG} maximum value.

Pad mapping on each segment can be optimized using the pad usage information provided on the I/O Signal Description table.

Table 16. I/O consumption

Symbol		C	Parameter	Conditions	Value(1) Min	Typ	Max	Unit
Average consumption(2)								
I_{RMSSEG}	SR	D	Sum of all the DC I/O current within a supply segment	—	—	—	80	mA
I_{RMS_W}	CC	D	RMS I/O current for WEAK configuration	C_L = 25 pF, 2 MHz, V_{DD} = 5.0 V ± 10 %	—	—	1.1	mA
				C_L = 50 pF, 1 MHz, V_{DD} = 5.0 V ± 10 %	—	—	1.1	
				C_L = 25 pF, 2 MHz, V_{DD} = 3.3 V ± 10 %	—	—	1.0	
				C_L = 25 pF, 1 MHz, V_{DD} = 3.3 V ± 10%	—	—	1.0	
I_{RMS_M}	CC	D	RMS I/O current for MEDIUM configuration	C_L = 25 pF, 12 MHz, V_{DD} = 5.0 V ± 10%	—	—	5.5	mA
				C_L = 50 pF, 6 MHz, V_{DD} = 5.0 V ± 10%	—	—	5.5	
				C_L = 25 pF, 12 MHz, V_{DD} = 3.3 V ± 10%	—	—	4.2	
				C_L = 25 pF, 6 MHz, V_{DD} = 3.3 V ± 10%	—	—	4.2	
I_{RMS_S}	CC	D	RMS I/O current for STRONG configuration	C_L = 25 pF, 50 MHz, V_{DD} = 5.0 V ± 10%	—	—	21	mA
				C_L = 50 pF, 25 MHz, V_{DD} = 5.0 V ± 10%	—	—	21	
				C_L = 25 pF, 25 MHz, V_{DD} = 3.3 V ± 10%	—	—	10	
				C_L = 25 pF, 12.5 MHz, V_{DD} = 3.3 V ± 10%	—	—	10	

Table 16. I/O consumption (continued)

Symbol		C	Parameter	Conditions	Value(1) Min	Typ	Max	Unit
I_{RMS_V}	CC	D	RMS I/O current for VERY STRONG configuration	C_L = 25 pF, 50 MHz, V_{DD} = 5.0 V ± 10%	—	—	23	mA
				C_L = 50 pF, 25 MHz, V_{DD} = 5.0 V ± 10%	—	—	23	
				C_L = 25 pF, 50 MHz, V_{DD} = 3.3 V ± 10%	—	—	16	
				C_L = 25 pF, 25 MHz, V_{DD} = 3.3 V ± 10%	—	—	16	
Dynamic consumption(3)								
I_{DYN_SEG}	SR	D	Sum of all the dynamic and DC I/O current within a supply segment	V_{DD} = 5.0 V ± 10%	—	—	195	mA
				V_{DD} = 3.3 V ± 10%	—	—	150	
I_{DYN_W}	CC	D	Dynamic I/O current for WEAK configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%	—	—	16.7	mA
				C_L = 50 pF, V_{DD} = 5.0 V ± 10%	—	—	16.8	
				C_L = 25 pF, V_{DD} = 3.3 V ± 10%	—	—	12.9	
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%	—	—	12.9	
I_{DYN_M}	CC	D	Dynamic I/O current for MEDIUM configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%	—	—	18.2	mA
				C_L = 50 pF, V_{DD} = 5.0 V ± 10%	—	—	18.4	
				C_L = 25 pF, V_{DD} = 3.3 V ± 10%	—	—	14.3	
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%	—	—	16.4	
I_{DYN_S}	CC	D	Dynamic I/O current for STRONG configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%	—	—	57	mA
				C_L = 50 pF, V_{DD} = 5.0 V ± 10%	—	—	63.5	
				C_L = 25 pF, V_{DD} = 3.3 V ± 10%	—	—	31	
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%	—	—	33.5	

Table 16. I/O consumption (continued)

Symbol		C	Parameter	Conditions	Value(1) Min	Typ	Max	Unit
I_{DYN_V}	CC	D	Dynamic I/O current for VERY STRONG configuration	C_L = 25 pF, V_{DD} = 5.0 V ± 10%	—	—	62	mA
				C_L = 50 pF, V_{DD} = 5.0 V ± 10%	—	—	70	
				C_L = 25 pF, V_{DD} = 3.3 V ± 10%	—	—	52	
				C_L = 50 pF, V_{DD} = 3.3 V ± 10%	—	—	55	

1. I/O current consumption specifications for the 4.5 V $\leq V_{DD\_HV\_IO} \leq$ 5.5 V range are valid for VSIO_[VSIO_xx] = 1, and VSIO[VSIO_xx] = 0 for 3.0 V $\leq V_{DD\_HV\_IO} \leq$ 3.6 V.
2. Average consumption in one pad toggling cycle.
3. Stated maximum values represent peak consumption that lasts only a few ns during I/O transition. When possible (timed output) it is recommended to delay transition between pads by few cycles to reduce noise and consumption.

4.9 Reset pad (PORST) electrical characteristics

The device implements dedicated bidirectional reset pins as below specified. PORST pin does not require active control. It is possible to implement an external pull-up to ensure correct reset exit sequence. Recommended value is 4.7 KΩ.

Figure 5. Startup Reset requirements

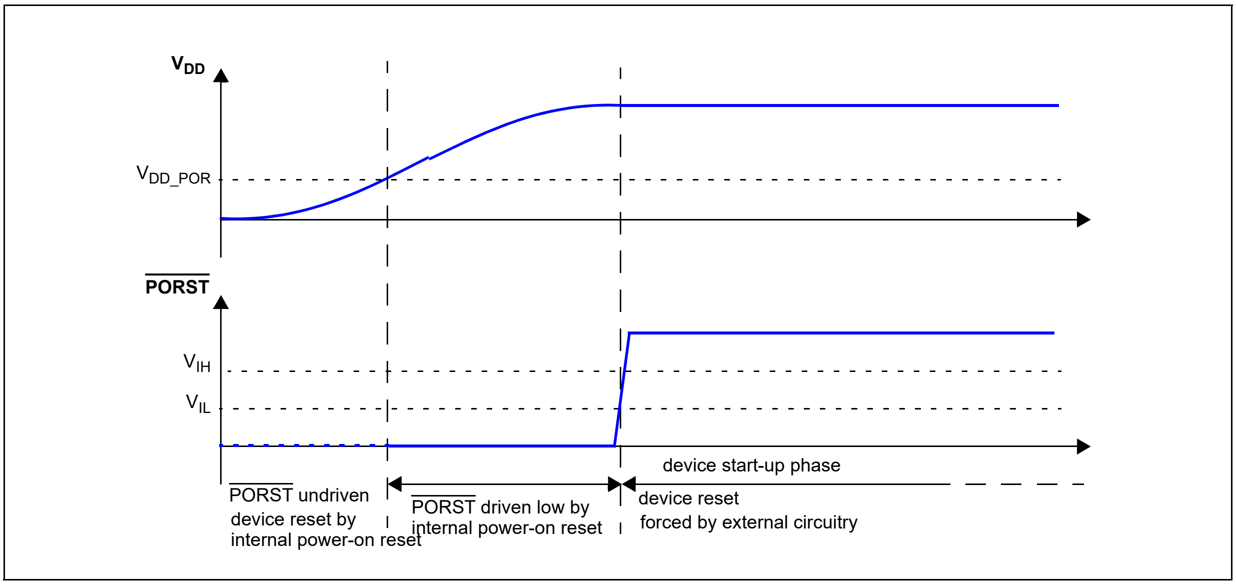


Figure 6 describes device behavior depending on supply signal on PORST:

1. PORST low pulse has too low amplitude: it is filtered by input buffer hysteresis. Device remains in current state.
2. PORST low pulse has too short duration: it is filtered by low pass filter. Device remains in current state.
3. PORST low pulse is generating a reset:
   a) PORST low but initially filtered during at least WFRST. Device remains initially in current state.
   b) PORST potentially filtered until WNFRST. Device state is unknown. It may either be reset or remains in current state depending on extra condition (temperature, voltage, device).
   c) PORST asserted for longer than WNFRST. Device is under reset.

Figure 6. Noise filtering on reset signal

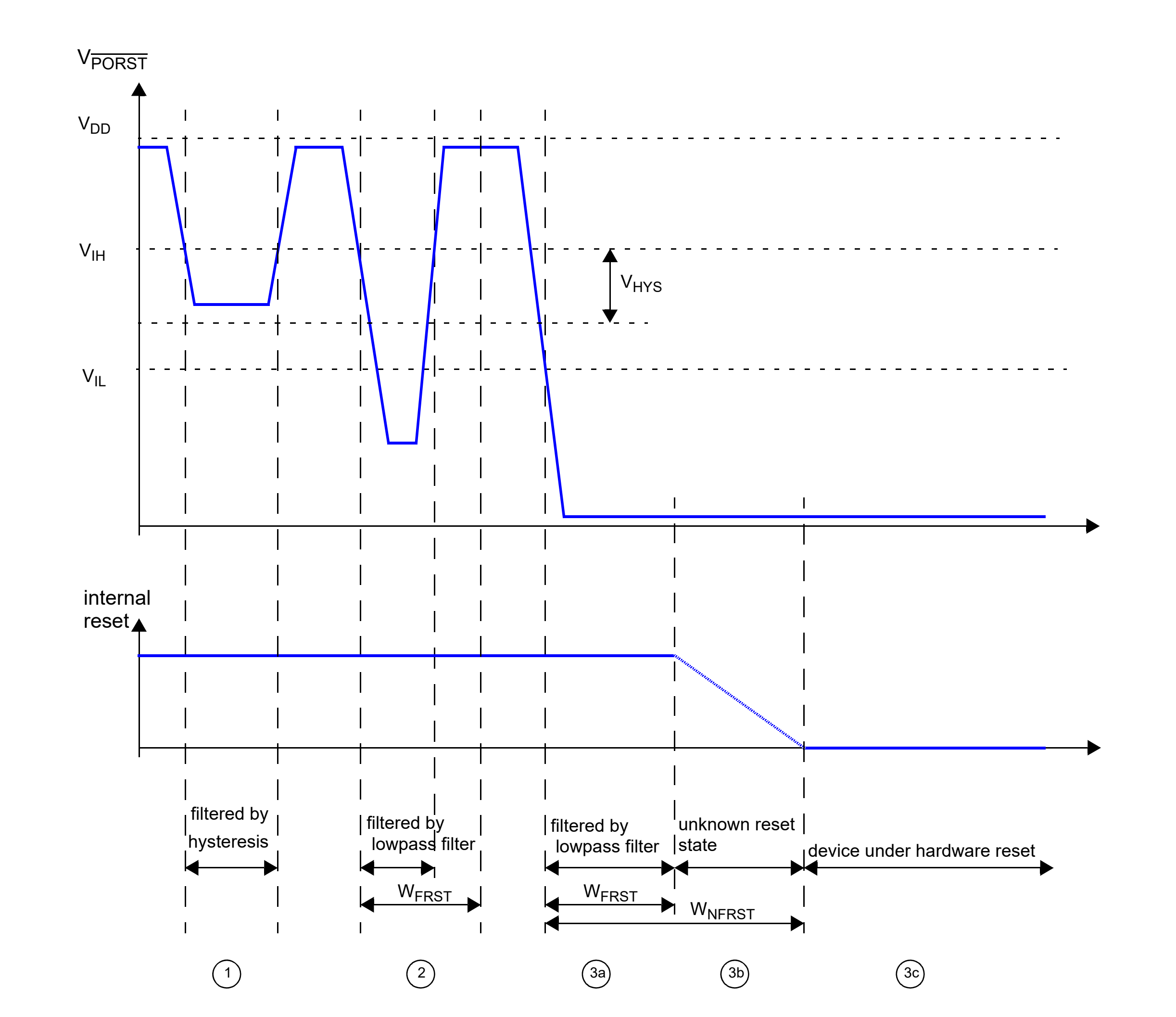


Table 17. Reset PAD electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{IHRES}	SR	P	Input high level TTL	V_{DD_HV} = 5.0 V ± 10% V_{DD_HV} = 3.3 V ± 10%	2	—	$V_{DD\_HV\_IO}$ +0.3	V
V_{ILRES}	SR	P	Input low level TTL	V_{DD_HV} = 5.0 V ± 10%	-0.3	—	0.8	V
				V_{DD_HV} = 3.3 V ± 10%	-0.3	—	0.6	
V_{HYSRES}	CC	C	Input hysteresis TTL	V_{DD_HV} = 5.0 V ± 10%	0.3	—	—	V
				V_{DD_HV} = 3.3 V ± 10%	0.2	—	—	
V_{DD_POR}	CC	D	Minimum supply for strong pull-down activation	V_{DD_HV} = 5.0 V ± 10%	—	—	1.6	V
				V_{DD_HV} = 3.3 V ± 10%	—	—	1.05	

Table 17. Reset PAD electrical characteristics (continued)

Symbol		C	Parameter	Conditions	Value Min	Value Typ	Value Max	Unit
I_{OL_R}	CC	P	Strong pull-down current [1]	V_{DD_HV} = 5.0 V ± 10%	12	—	—	mA
				V_{DD_HV} = 3.3 V ± 10%	8	—	—	
I_{WPU}	CC	P	Weak pull-up current absolute value	V_{IN} = 1.1 V[2] V_{DD_HV} = 5.0 V ± 10%	—	—	130	µA
		P		V_{IN} = 1.1 V V_{DD_HV} = 3.3 V ± 10%	—	—	70	
		P		V_{IN} = 0.69 * $V_{DD\_HV\_IO}$[3] V_{DD_HV} = 5.0 V ± 10%	15	—	—	
		P		V_{IN} = 0.69 * $V_{DD\_HV\_IO}$ V_{DD_HV} = 3.3 V ± 10%	15	—	—	
I_{WPD}	CC	P	Weak pull-down current absolute value	V_{IN} = 0.69 * $V_{DD\_HV\_IO}$[2] V_{DD_HV} = 5.0 V ± 10%	—	—	130	µA
		P		V_{IN} = 0.69 * $V_{DD\_HV\_IO}$[2] V_{DD_HV} = 3.3 V ± 10%	—	—	80	
		P		V_{IN} = 0.9 V V_{DD_HV} = 5.0 V ± 10%	15	—	—	
		P		V_{IN} = 0.9 V $V_{DD\_HVDD\_HV}$ = 3.3 V ± 10%	15	—	—	
W_{FRST}	CC	P	Input filtered pulse	V_{DD_HV} = 5.0 V ± 10%	—	—	500	ns
		P		V_{DD_HV} = 3.3 V ± 10%	—	—	600	
W_{NFRST}	CC	P	Input not filtered pulse	V_{DD_HV} = 5.0 V ± 10%	2000	—	—	ns
		P		V_{DD_HV} = 3.3 V ± 10%	3000	—	—	

1. I_{ol_r} applies to PORST: Strong Pull-down is active on PHASE0 for PORST. Refer to the device pinout IO definition excel file for details regarding pin usage.
2. Maximum current when forcing a change in the pin level opposite to the pull configuration.
3. Minimum current when keeping the same pin level state than the pull configuration.

Table 18. Reset Pad state during power-up and reset

PAD	POWER-UP State	RESET state	DEFAULT state[1]	STANDBY state
PORST	Strong pull-down	Weak pull-down	Weak pull-down	Weak pull-up

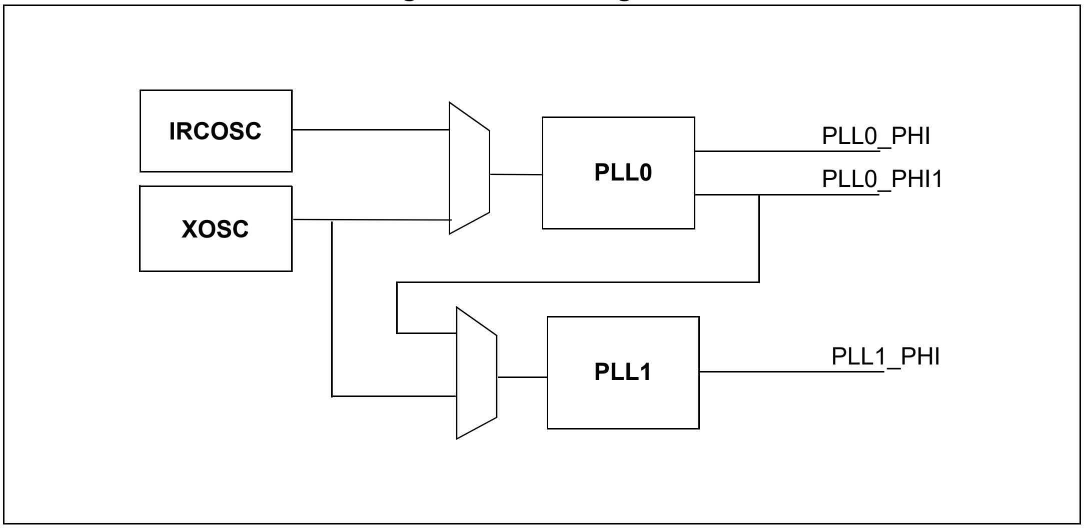
1. Before SW Configuration. Please refer to the Device Reference Manual, Reset Generation Module (MC_RGM) Functional Description chapter for the details of the power-up phases.

4.10 PLLs

Two phase-locked loop (PLL) modules are implemented to generate system and auxiliary clocks on the device.

Figure 7 depicts the integration of the two PLLs. Refer to device Reference Manual for more detailed schematic.

Figure 7. PLLs integration



4.10.1 PLL0

Table 19. PLL0 electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{PLL0IN}	SR	—	PLL0 input clock(1)	—	8	—	44	MHz
Δ_{PLL0IN}	SR	—	PLL0 input clock duty cycle(1)	—	40	—	60	%
f_{INFIN}	SR	—	PLL0 PFD (Phase Frequency Detector) input clock frequency	—	8	—	20	MHz
$f_{PLL0VCO}$	CC	P	PLL0 VCO frequency	—	600	—	1400	MHz
$f_{PLL0PHI0}$	CC	D	PLL0 output frequency	—	4.762	—	F_{SYS}(2)	MHz
$f_{PLL0PHI1}$	CC	D	PLL0 output clock PHI1	—	20	—	175(3)	MHz
$t_{PLL0LOCK}$	CC	P	PLL0 lock time	—	—	—	100	μs
$\|\Delta_{PLL0PHI0SPJ}\|$(4)	CC	T	PLL0_PHI0 single period jitter f_{PLL0IN} = 20 MHz (resonator)	$f_{PLL0PHI0}$ = 400 MHz, 6-sigma pk-pk	—	—	200	ps

Table 19. PLL0 electrical characteristics (continued)

Symbol		C	Parameter	Conditions	Value Min	Value Typ	Value Max	Unit
$\|\Delta_{PLL0PHI1SPJ}\|$(4)	CC	D	PLL0_PHI1 single period jitter f_{PLL0IN} = 20 MHz (resonator)	$f_{PLL0PHI1}$ = 40 MHz, 6-sigma pk-pk	—	—	300(5)	ps
$\Delta_{PLL0LTJ}$(4)	CC	D	PLL0 output long term jitter(5) f_{PLL0IN} = 20 MHz (resonator), VCO frequency = 800 MHz	10 periods accumulated jitter (80 MHz equivalent frequency), 6-sigma pk-pk	—	—	±250	ps
				16 periods accumulated jitter (50 MHz equivalent frequency), 6-sigma pk-pk	—	—	±300	ps
				long term jitter (< 1 MHz equivalent frequency), 6-sigma pk-pk)	—	—	±500	ps
I_{PLL0}	CC	D	PLL0 consumption	FINE LOCK state	—	—	6	mA

1. PLL0IN clock retrieved directly from either internal RCOSC or external FXOSC clock. Input characteristics are granted when using internal RCOSC or external oscillator is used in functional mode.
2. Refer to *Section 4.3: Operating conditions* for the maximum operating frequency.
3. If the PLL0_PHI1 is used as an input for PLL1, then the PLL0_PHI1 frequency shall obey the maximum input frequency limit set for PLL1 (87.5 MHz, according to *Table 20*).
4. Jitter values reported in this table refer to the internal jitter, and do not include the contribution of the divider and the path to the output CLKOUT pin.
5. V_{DD_LV} noise due to application in the range V_{DD_LV} = 1.20 V±5%, with frequency below PLL bandwidth (40 kHz) will be filtered.

4.10.2 PLL1

PLL1 is a frequency modulated PLL with Spread Spectrum Clock Generation (SSCG) support.

Table 20. PLL1 electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{PLL1IN}	SR	—	PLL1 input clock(1)	—	37.5	—	87.5	MHz
Δ_{PLL1IN}	SR	—	PLL1 input clock duty cycle(1)	—	35	—	65	%
f_{INFIN}	SR	—	PLL1 PFD (Phase Frequency Detector) input clock frequency	—	37.5		87.5	MHz
$f_{PLL1VCO}$	CC	P	PLL1 VCO frequency	—	600	—	1400	MHz
$f_{PLL1PHI0}$	CC	D	PLL1 output clock PHI0	—	4.762	—	F_{SYS}(2)	MHz
$t_{PLL1LOCK}$	CC	P	PLL1 lock time	—	—	—	50	μs
$f_{PLL1MOD}$	CC	T	PLL1 modulation frequency	—	—	—	250	kHz
$\|\delta_{PLL1MOD}\|$	CC	T	PLL1 modulation depth (when enabled)	Center spread(3)	0.25	—	2	%
				Down spread	0.5	—	4	%
$\|\Delta_{PLL1PHI0SPJ}\|$(4)	CC	T	PLL1_PHI0 single period peak to peak jitter	$f_{PLL1PHI0}$ = 200 MHz, 6-sigma	—	—	500(5)	ps
I_{PLL1}	CC	D	PLL1 consumption	FINE LOCK state	—	—	5	mA

1. PLL1IN clock retrieved directly from either internal PLL0 or external FXOSC clock. Input characteristics are granted when using internal PPL0 or external oscillator is used in functional mode.
2. Refer to *Section 4.3: Operating conditions* for the maximum operating frequency.
3. The device maximum operating frequency F_{SYS} (max) includes the frequency modulation. If center modulation is selected, the FSYS must be below the maximum by MD (Modulation Depth Percentage), such that FSYS(max)=FSYS(1+MD%). Refer to the Reference Manual for the PLL programming details.
4. Jitter values reported in this table refer to the internal jitter, and do not include the contribution of the divider and the path to the output CLKOUT pin.
5. 1.25 V±5%, application noise below 40 kHz at V_{DD_LV} pin - no frequency modulation.

4.11 Oscillators

4.11.1 Crystal oscillator 40 MHz

Table 21. External 40 MHz oscillator electrical specifications

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
f_{XTAL}	CC	D	Crystal Frequency Range[1]	—	4[2]	8	MHz
					>8	20	
					>20	40	
t_{cst}	CC	T	Crystal start-up time [3],[4]	T_J = 150 °C	—	5	ms
t_{rec}	CC	D	Crystal recovery time[5]	—	—	0.5	ms
V_{IHEXT}	CC	D	EXTAL input high voltage[6] (External Reference)	V_{REF} = 0.29 * $V_{DD\_HV\_OSC}$	V_{REF} + 0.75	—	V
V_{ILEXT}	CC	D	EXTAL input low voltage[6] (External Reference)	V_{REF} = 0.29 * $V_{DD\_HV\_OSC}$	—	V_{REF} - 0.75	V
C_{S_EXTAL}	CC	D	Total on-chip stray capacitance on EXTAL pin[7]	—	3	7	pF
C_{S_XTAL}	CC	D	Total on-chip stray capacitance on XTAL pin[7]	—	3	7	pF
g_m	CC	P	Oscillator Transconductance	f_{XTAL} = 4 – 8 MHz freq_sel[2:0] = 000	3.9	13.6	mA/V
		D		f_{XTAL} = 5 - 10 MHz freq_sel[2:0] = 001	5	17.5	
		D		f_{XTAL} = 10 – 15 MHz freq_sel[2:0] = 010	8.6	29.3	
		P		f_{XTAL} = 15 - 20 MHz freq_sel[2:0] = 011	14.4	48	
		D		f_{XTAL} = 20 - 25 MHz freq_sel[2:0] = 100	21.2	69	
		D		f_{XTAL} = 25 – 30 MHz freq_sel[2:0] = 101	27	86	
		D		f_{XTAL} = 30 - 35 MHz freq_sel[2:0] = 110	33.5	115	
		P		f_{XTAL} = 35 - 40 MHz freq_sel[2:0] = 111	33.5	115	
V_{EXTAL}	CC	D	Oscillation Amplitude on the EXTAL pin after startup[8]	T_J = –40 °C to 150 °C	0.5	1.8	V

Table 21. External 40 MHz oscillator electrical specifications (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
V_{HYS}	CC	D	Comparator Hysteresis	T_J = –40 °C to 150 °C	0.1	1.0	V
I_{XTAL}	CC	D	XTAL current(8),(9)	T_J = –40 °C to 150 °C	—	14	mA

1. The range is selectable by UTEST miscellaneous DCF client XOSC_FREQ_SEL.
2. The XTAL frequency, if used to feed the PPL0 (or PLL1), shall obey the minimum input frequency limit set for PLL0 (or PLL1).
3. This value is determined by the crystal manufacturer and board design, and it can potentially be higher than the maximum provided.
4. Proper PC board layout procedures must be followed to achieve specifications.
5. Crystal recovery time is the time for the oscillator to settle to the correct frequency after adjustment of the integrated load capacitor value.
6. Applies to an external clock input and not to crystal mode.
7. See crystal manufacturer's specification for recommended load capacitor (C_L) values. The external oscillator requires external load capacitors when operating from 8 MHz to 16 MHz. Account for on-chip stray capacitance (C_{S_EXTAL}/C_{S_XTAL}) and PCB capacitance when selecting a load capacitor value. When operating at 20 MHz/40 MHz, the integrated load capacitor value is selected via S/W to match the crystal manufacturer's specification, while accounting for on-chip and PCB capacitance.
8. Amplitude on the EXTAL pin after startup is determined by the ALC block, that is the Automatic Level Control Circuit. The function of the ALC is to provide high drive current during oscillator startup, but reduce current after oscillation in order to reduce power, distortion, and RFI, and to avoid over driving the crystal. The operating point of the ALC is dependent on the crystal value and loading conditions.
9. I_{XTAL} is the oscillator bias current out of the XTAL pin with both EXTAL and XTAL pins grounded. This is the maximum current during startup of the oscillator.

4.11.2 RC oscillator 16 MHz

Table 22. Internal RC oscillator electrical specifications

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
f_{Target}	CC	D	IRC target frequency	—	—	16	—	MHz
δf_{var_noT}	CC	P	IRC frequency variation without temperature compensation	T < 150 °C	–5	—	5	%
δf_{var_T}	CC	T	IRC frequency variation with temperature compensation	T < 150 °C	–3	—	3	%
δf_{var_SW}		T	IRC software trimming accuracy	Trimming temperature	–0.5	±0.3	0.5	%
T_{start_noT}	CC	T	Startup time to reach within f_{var_noT}	Factory trimming already applied	—	—	5	µs

Table 22. Internal RC oscillator electrical specifications (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
T_{start_T}	CC	T	Startup time to reach within f_{var_T}	Factory trimming already applied	—	—	120	µs
I_{FIRC}	CC	T	Current consumption on HV power supply (1)	After T_{start_T}	—	—	1200	µA

1. The actual consumption difference can be higher due to additional consumption of core logic clocked by RCOSC16M.

4.11.3 Low power RC oscillator

Table 23. 1024 kHz internal RC oscillator electrical characteristics

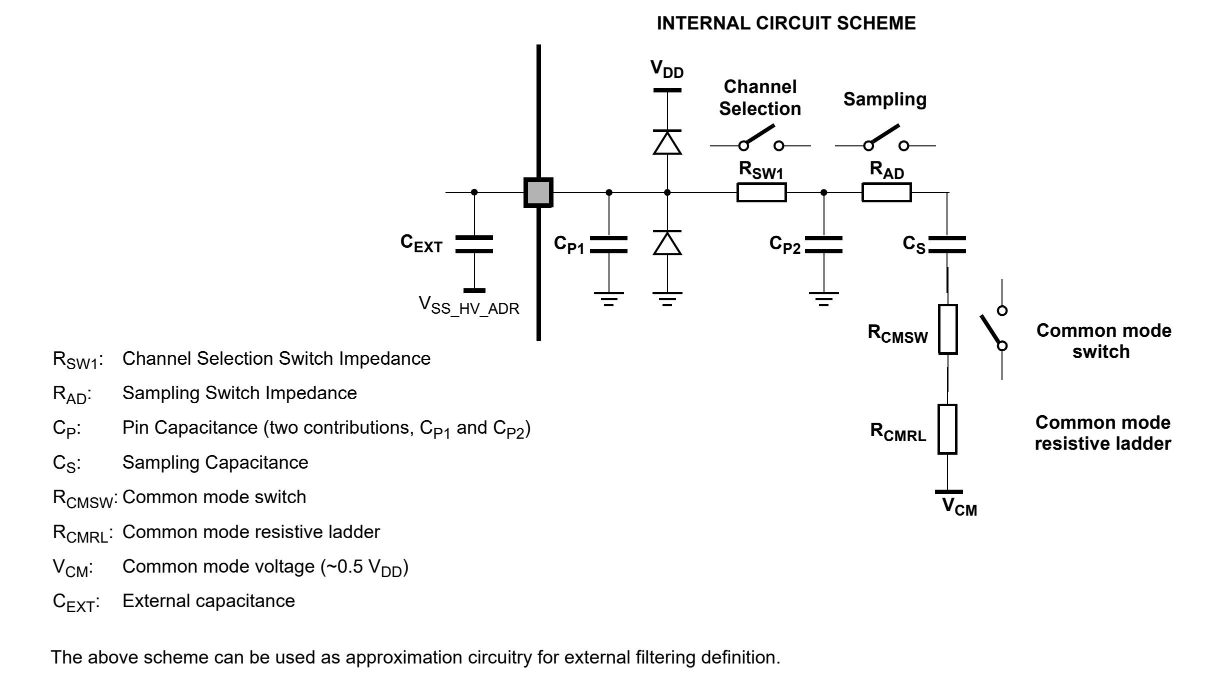
Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
F_{sirc}	CC	T	Slow Internal RC oscillator frequency	—	—	1024	—	kHz
δf_{var_T}	CC	P	Frequency variation across temperature	–40 °C < T < 150 °C	–9	—	+9	%
δf_{var_V}	CC	P	Frequency variation across voltage	–40 °C < T < 150 °C	–5	—	+5	%
I_{sirc}	CC	T	Slow Internal RC oscillator current	T = 55 °C	—	—	6	µA
T_{sirc}	CC	T	Start up time, after switching ON the internal regulator.	—	—	—	12	µS

4.12 ADC system

4.12.1 ADC input description

Figure 8 shows the input equivalent circuit for SARn and SARB channels.

Figure 8. Input equivalent circuit (Fast SARn and SARB channels)



All specifications in the following are table valid for the full input voltage range for the analog inputs.

Table 24. ADC pin specification

Symbol		C	Parameter	Conditions	Value Min	Value Max	Unit
$R_{20K\Omega}$	CC	D	Internal voltage reference source impedance.	—	16	30	KΩ
I_{LKG}	CC	—	Input leakage current, two ADC channels on input-only pin.	See IO chapter *Table 10: I/O input electrical characteristics*, parameter I_{LKG}.			
I_{INJ1}	SR	—	Injection current on analog input preserving functionality at full or degraded performances.	See Operating Conditions chapter *Table 5: Operating conditions*, I_{INJ1} parameter.			
C_{HV_ADC}	SR	D	$V_{DD\_HV\_ADV}$ external capacitance.	See Power Management chapter *Table 27: External components integration*, C_{ADC} parameter.			
C_{P1}	CC	D	Pad capacitance	See IO chapter *Table 10: I/O input electrical characteristics*, parameter C_{P1}.			
C_{P2}	CC	D	Internal routing capacitance	—	—	2	pF

Table 24. ADC pin specification (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
C_S	CC	D	SAR ADC sampling capacitance	—	—	5	pF
R_{SWn}	CC	D	Analog switches resistance	—	0	1.8	kΩ
R_{AD}	CC	D	ADC input analog switches resistance	SARn 12-bit	—	0.8	kΩ
R_{CMSW}	CC	D	Common mode switch resistance	Sum of the two resistances	—	9	kΩ
R_{CMRL}	CC	D	Common mode resistive ladder				kΩ
R_{SAFEPD}[1]	CC	D	Discharge resistance for ADC input-only pins (strong pull-down for safety)	$V_{DD\_HV\_IO}$ = 5.0 V ± 10%	—	300	W
				$V_{DD\_HV\_IO}$ = 3.3 V ± 10%	—	500	W
C_{EXT}	SR	—	External capacitance at the pad input pin	To preserve the accuracy of the ADC, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible. This capacitor contributes to attenuating the noise present on the input pin. The impedance relative to the signal source can limit the ADC's sample rate.			

1. It enables discharge of up to 100 nF from 5 V every 300 ms. Refer to the device pinout Microsoft Excel file attached to the IO_Definition document for the pads supporting it.

4.12.2 SAR ADC 12 bit electrical specification

The SARn ADCs are 12-bit Successive Approximation Register analog-to-digital converters with full capacitive DAC. The SARn architecture allows input channel multiplexing.

Note: The functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maximum may affect device reliability or cause permanent damage to the device.

Table 25. SARn ADC electrical specification

Symbol		C	Parameter	Conditions	Value		Unit
					Min	Max	
f_{ADCK}	SR	P	Clock frequency	Standard frequency mode	7.5	13.33	MHz
		T		High frequency mode	>13.33	16.0	
$t_{ADCINIT}$	SR	—	ADC initialization time	—	1.5	—	µs
$t_{ADCBIASINIT}$	SR	—	ADC BIAS initialization time	—	5	—	µs
$t_{ADCPRECH}$	SR	T	ADC decharge time	Fast channel	$1/f_{ADCK}$	—	µs
				Standard channel	$2/f_{ADCK}$	—	

Table 25. SARn ADC electrical specification (continued)

Symbol		C	Parameter	Conditions	Value Min	Value Max	Unit
ΔV_{PRECH}	SR	D	Decharge voltage precision	T_J < 150 °C	0	0.25	V
$R_{20K\Omega}$	CC	D	Internal voltage reference source impedance	—	16	30	KΩ
ΔV_{INTREF}	CC	P	Internal reference voltage precision	Applies to all internal reference points ($V_{SS\_HV\_ADR}$, 1/3 * $V_{DD\_HV\_ADR}$, 2/3 * $V_{DD\_HV\_ADR}$, $V_{DD\_HV\_ADR}$)	–0.20	0.20	V
$t_{ADCSAMPLE}$	SR	P	ADC sample time[1]	Fast channel – 12-bit configuration	$6/f_{ADCK}$	—	μs
		D		Fast channel – 10-bit configuration mode 1[2] (Standard frequency mode only)	$6/f_{ADCK}$		
				Fast channel – 10-bit configuration mode 2[3] (Standard frequency mode only)	$5/f_{ADCK}$		
				Fast channel – 10-bit configuration mode 3[4] (High frequency mode only)	$6/f_{ADCK}$		
				Standard channel– 12-bit configuration	$12/f_{ADCK}$		
				Standard channel– 10-bit configuration mode 1[2] (Standard frequency mode only)	$12/f_{ADCK}$		
				Standard channel – 10-bit configuration mode 2[3] (Standard frequency mode only)	$10/f_{ADCK}$		
				Standard channel – 10-bit configuration mode 3[4] (High frequency mode only)	$12/f_{ADCK}$		
				Conversion of BIAS test channels through 20 kΩ input.	$40/f_{ADCK}$		
$t_{ADCEVAL}$	SR	P	ADC evaluation time	12-bit configuration	$12/f_{ADCK}$	—	μs
		D		10-bit configuration	$10/f_{ADCK}$	—	

Table 25. SARn ADC electrical specification (continued)

Symbol		C	Parameter	Conditions	Value Min	Value Max	Unit
$I_{ADCREFH}$ (5),(6)	CC	T	ADC high reference current	Run mode (average across all codes)	—	7	µA
				Power Down mode	—	1	
$I_{ADCREFL}$ (6)	CC	D	ADC low reference current	Run mode $V_{DD\_HV\_ADR\_S} \leq 5.5$ V	—	15	µA
				Power Down mode $V_{DD\_HV\_ADR\_S} \leq 5.5$ V	—	1	
I_{ADV_S} (6)	CC	P	$V_{DD\_HV\_ADV}$ power supply current	Run mode	—	4.0	mA
		D		Power Down mode	—	0.04	
TUE_{12}	CC	T	Total unadjusted error in 12-bit configuration(7)	$T_J < 150$ °C, $V_{DD\_HV\_ADV} > 3$ V, $V_{DD\_HV\_ADR\_S} > 3$ V	–4	4	LSB (12b)
		P		$T_J < 150$ °C, $V_{DD\_HV\_ADV} > 3$ V, $V_{DD\_HV\_ADR\_S} > 3$ V	–6	6	
		T		$T_J < 150$ °C, $V_{DD\_HV\_ADV} > 3$ V, 3 V > $V_{DD\_HV\_ADR\_S} > 2$ V	–6	6	
		D		High frequency mode, $T_J < 150$ °C, $V_{DD\_HV\_ADV} > 3$ V, $V_{DD\_HV\_ADR\_S} > 3$ V	–12	12	
TUE_{10}	CC	D	Total unadjusted error in 10-bit configuration(7)	Mode 1, $T_J < 150$ °C, $V_{DD\_HV\_ADV} > 3$ V $V_{DD\_HV\_ADR\_S} > 3$ V	–1.5	1.5	LSB (10b)
		D		Mode 1, $T_J < 150$ °C, $V_{DD\_HV\_ADV} > 3$ V, 3 V > $V_{DD\_HV\_ADR\_S} > 2$ V	–2.0	2.0	
		C		Mode 2, $T_J < 150$ °C, $V_{DD\_HV\_ADV} > 3$ V $V_{DD\_HV\_ADR\_S} > 3$ V	–3.0	3.0	
		C		Mode 3, $T_J < 150$ °C, $V_{DD\_HV\_ADV} > 3$ V $V_{DD\_HV\_ADR\_S} > 3$ V	–4.0	4.0	

Table 25. SARn ADC electrical specification (continued)

Symbol		C	Parameter	Conditions	Value Min	Value Max	Unit
ΔTUE_{12}	CC	D	TUE degradation due to $V_{DD\_HV\_ADR}$ offset with respect to $V_{DD\_HV\_ADV}$	$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in [0:25\ mV]$	–1	1	LSB (12b)
				$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in [25:50\ mV]$	–2	2	
				$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in [50:75\ mV]$	–4	4	
				$V_{IN} < V_{DD\_HV\_ADV}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in [75:100\ mV]$	–6	6	
				$V_{DD\_HV\_ADV} < V_{IN} < V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in [0:25\ mV]$	–2.5	2.5	
				$V_{DD\_HV\_ADV} < V_{IN} < V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in [25:50\ mV]$	–4	4	
				$V_{DD\_HV\_ADV} < V_{IN} < V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in [50:75\ mV]$	–7	7	
				$V_{DD\_HV\_ADV} < V_{IN} < V_{DD\_HV\_ADR}$ $V_{DD\_HV\_ADR} - V_{DD\_HV\_ADV} \in [75:100\ mV]$	–12	12	
DNL(8)	CC	P	Differential non-linearity	Standard frequency mode, $V_{DD\_HV\_ADV} > 4$ V $V_{DD\_HV\_ADR\_S} > 4$ V	–1	2	LSB (12b)
		T		High frequency mode, $V_{DD\_HV\_ADV} > 4$ V $V_{DD\_HV\_ADR\_S} > 4$ V	–1	2	

1. Minimum ADC sample times are dependent on adequate charge transfer from the external driving circuit to the internal sample capacitor. The time constant of the entire circuit must allow the sampling capacitor to charge within 1/2 LSB within the sampling window. Refer to *Figure 8* for models of the internal ADC circuit, and the values to use in external RC sizing and calculating the sampling window duration.
2. Mode1: 6 sampling cycles + 10 conversion cycles at 13.33 MHz.
3. Mode2: 5 sampling cycles + 10 conversion cycles at 13.33 MHz.
4. Mode3: 6 sampling cycles + 10 conversion cycles at 16 MHz.
5. $I_{ADCREFH}$ and $I_{ADCREFL}$ are independent from ADC clock frequency. It depends on conversion rate: consumption is driven by the transfer of charge between internal capacitances during the conversion.
6. Current parameter values are for a single ADC.

7. TUE is granted with injection current within the range defined in *Table 24*, for parameters classified as T and D.
8. DNL is granted with injection current within the range defined in *Table 24*, for parameters classified as T and D.

4.13 Power management

The power management module monitors the different power supplies as well as it generates the required internal supplies. The device can operate in the following configurations:

Table 26. Power management regulators

Device	External regulator	Internal SMPS regulator	Internal linear regulator external ballast	Internal linear regulator internal ballast	Auxiliary regulator	Clamp regulator	Internal standby regulator(1)
SPC582Bx	—	—	—	X	—	—	X

1. Standby regulator is automatically activated when the device enters standby mode.

4.13.1 Power management integration

Use the integration schemes provided below to ensure the proper device function, according to the selected regulator configuration.

The internal regulators are supplied by $V_{DD\_HV\_IO\_MAIN}$ supply and are used to generate V_{DD_LV} supply.

Place capacitances on the board as near as possible to the associated pins and limit the serial inductance of the board to less than 5 nH.

It is recommended to use the internal regulators only to supply the device itself.

Figure 9. Internal regulator with internal ballast mode

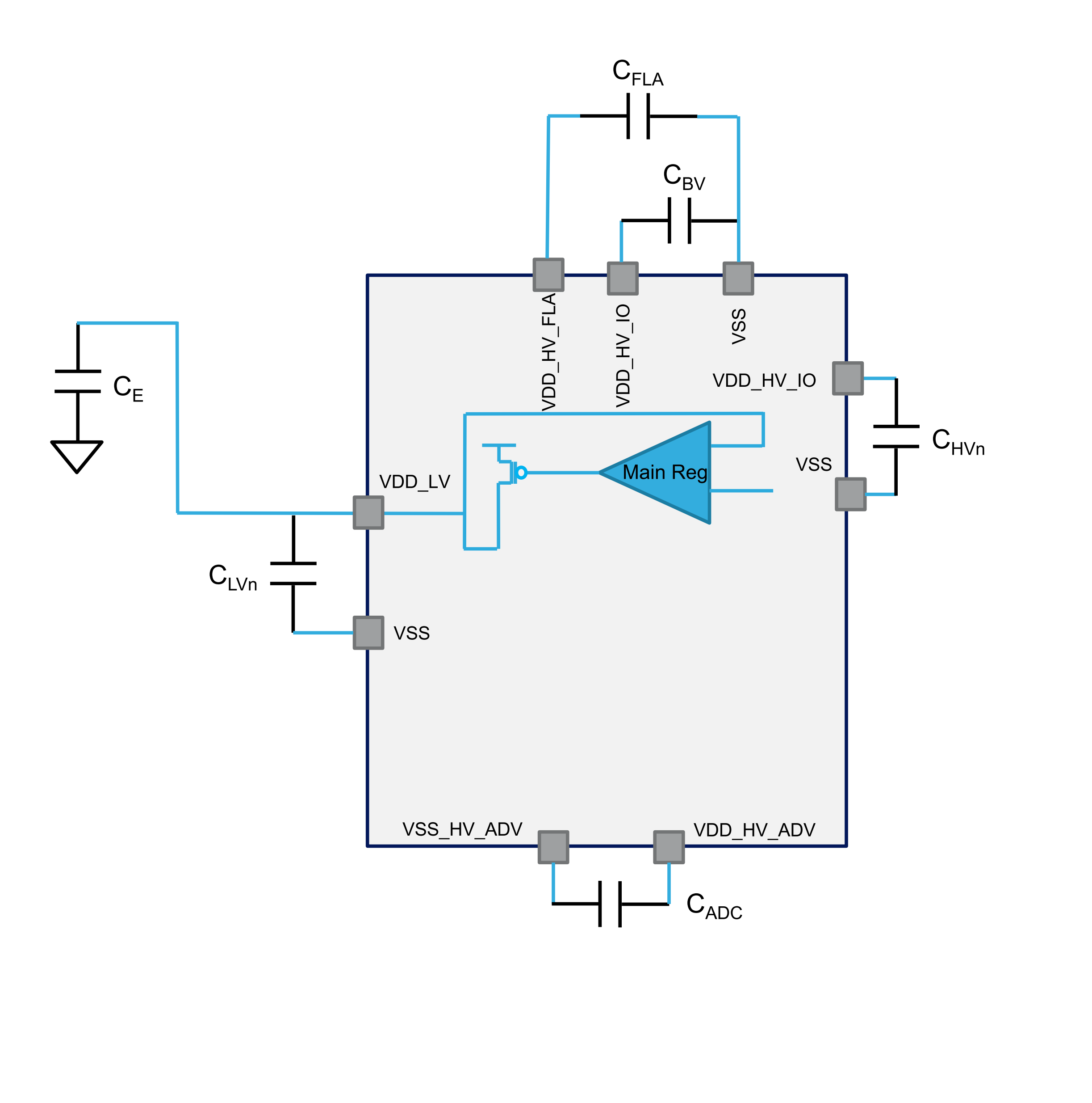


Figure 10. Standby regulator with internal ballast mode

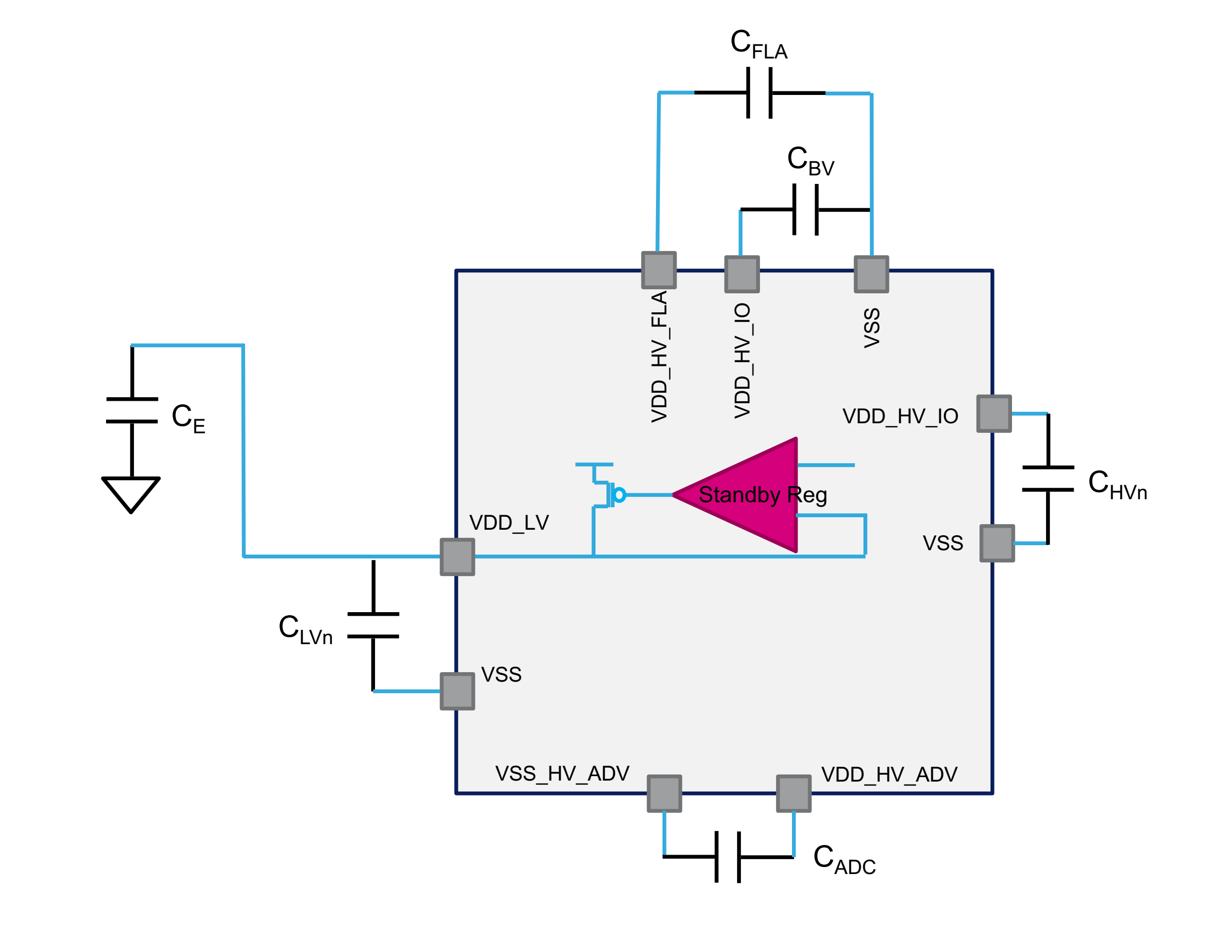


Table 27. External components integration

Symbol		C	Parameter	Conditions(1)	Value			Unit
					Min	Typ	Max	
Common Components								
C_E	SR	D	Internal voltage regulator stability external capacitance(2) (3)	—	—	1	—	μF
R_E	SR	D	Stability capacitor equivalent serial resistance	Total resistance including board track	5	—	50	mΩ
C_{LVn}	SR	D	Internal voltage regulator decoupling external capacitance (2) (4) (5)	Each V_{DD_LV}/V_{SS} pair	—	100	—	nF
R_{LVn}	SR	D	Stability capacitor equivalent serial resistance	—	—	—	50	mΩ
C_{BV}	SR	D	Bulk capacitance for HV supply (2)	on one $V_{DD\_HV\_IO\_MAIN}/V_{SS}$ pair	—	4.7	—	μF
C_{HVn}	SR	D	Decoupling capacitance for ballast and IOs (2)	on all $V_{DD\_HV\_IO}/V_{SS}$ and $V_{DD\_HV\_ADR}/V_{SS}$ pairs	—	100	—	nF

Table 27. External components integration (continued)

Symbol		C	Parameter	Conditions(1)	Value			Unit
					Min	Typ	Max	
C_{FLA}	SR	D	Decoupling capacitance for Flash supply (2) (6)	—	—	10	—	nF
C_{ADC}	SR	D	ADC supply external capacitance(2) (6)	$V_{DD\_HV\_ADV}/V_{SS\_HV\_ADV}$ pair	—	0.5	—	µF

1. V_{DD} = 3.3 V ± 10% / 5.0 V ± 10%, T_J = –40 / 150 °C, unless otherwise specified.
2. Recommended X7R or X5R ceramic –50% / +35% variation across process, temperature, voltage and after aging.
3. CE capacitance is required both in internal and external regulator mode.
4. For noise filtering, add a high frequency bypass capacitance of 10 nF.
5. For applications it is recommended to implement at least 5 C_{LV} capacitances.
6. Recommended X7R capacitors. For noise filtering, add a high frequency bypass capacitance of 100 nF.

4.13.2 Voltage regulators

Table 28. Linear regulator specifications

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{MREG}	CC	P	Main regulator output voltage	Power-up, before trimming, no load	1.13	1.21	1.29	V
	CC	P		After trimming, maximum load	1.09	1.19	1.26	
IDD_{MREG}	CC	T	Main regulator current provided to V_{DD_LV} domain The maximum current required by the device (I_{DD_LV}) may exceed the maximum current which can be provided by the internal linear regulator. In this case, the internal regulator mode cannot be used.	—	—	—	85	mA
IDD_{CLAMP}	CC	D	Main regulator rush current sinked from $V_{DD\_HV\_IO\_MAIN}$ domain during V_{DD_LV} domain loading	Power-up condition	—	—	40	mA
ΔIDD_{MREG}	CC	T	Main regulator output current variation	20 µs observation window	-50	—	50	mA
$I_{MREGINT}$	CC	D	Main regulator current consumption	I_{MREG} = max	—	—	1.1	mA
		D		I_{MREG} = 0 mA	—	—	1.1	

Table 29. Standby regulator specifications

Symbol		C	Parameter	Conditions	Value			Unit
					Min	Typ	Max	
V_{SBY}	CC	P	Standby regulator output voltage	After trimming, maximum load	0.92	0.98	1.19	V
IDD_{SBY}	CC	T	Standby regulator current provided to V_{DD_LV} domain	—	—	0.984	5	mA

4.13.3 Voltage monitors

The monitors and their associated levels for the device are given in *Table 30*. *Figure 11* illustrates the workings of voltage monitoring threshold.

Figure 11. Voltage monitor threshold definition

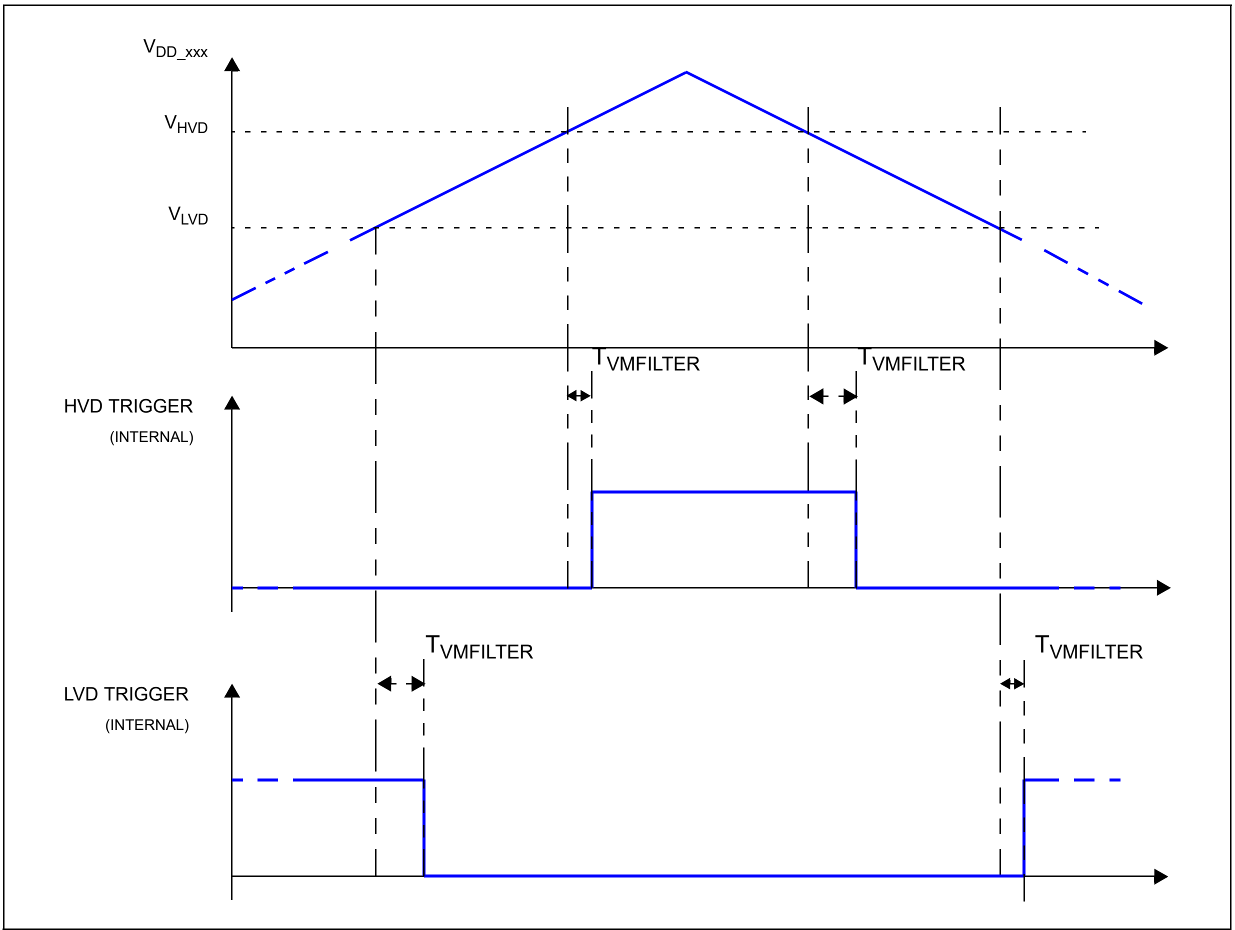


Table 30. Voltage monitor electrical characteristics

Symbol		C	Supply/Parameter[1]	Conditions	Value[2] Min	Typ	Max	Unit
PowerOn Reset HV								
V_{POR200_C}	CC	P	$V_{DD\_HV\_IO\_MAIN}$	—	1.80	2.02	2.40	V
Minimum Voltage Detectors HV								
V_{MVD270_C}	CC	P	$V_{DD\_HV\_IO\_MAIN}$	—	2.71	2.76	2.80	V
V_{MVD270_F}	CC	P	$V_{DD\_HV\_FLA}$	—	2.71	2.76	2.80	V
V_{MVD270_SBY}	CC	P	$V_{DD\_HV\_IO\_MAIN}$ (in Standby)	—	2.68	2.76	2.84	V
Low Voltage Detectors HV								
V_{LVD290_C}	CC	P	$V_{DD\_HV\_IO\_MAIN}$	—	2.89	2.94	2.99	V
V_{LVD290_F}	CC	P	$V_{DD\_HV\_FLA}$	—	2.89	2.94	2.99	V
V_{LVD290_AS}	CC	P	$V_{DD\_HV\_ADV}$ (ADCSAR pad)	—	2.89	2.94	2.99	V
V_{LVD400_AS}	CC	P	$V_{DD\_HV\_ADV}$ (ADCSAR pad)	—	4.15	4.23	4.31	V
V_{LVD400_IM}	CC	P	$V_{DD\_HV\_IO\_MAIN}$	—	4.15	4.23	4.31	V

Table 30. Voltage monitor electrical characteristics (continued)

Symbol		C	Supply/Parameter(1)	Conditions	Value(2)			Unit
					Min	Typ	Max	
Minimum Voltage Detectors LV								
V_{MVD082_C}	CC	P	V_{DD_LV}	—	0.85	0.88	0.91	V
V_{MVD094_C}	CC	P	V_{DD_LV}	—	0.98	1.00	1.02	V
V_{MVD094_FA}	CC	P	V_{DD_LV} (Flash)	—	1.00	1.02	1.04	V
V_{MVD094_FB}	CC	P	V_{DD_LV} (Flash)	—	1.00	1.02	1.04	V
Low Voltage Detectors LV								
V_{LVD100_C}	CC	P	V_{DD_LV}	—	1.06	1.08	1.11	V
V_{LVD100_SB}	CC	P	V_{DD_LV} (In Standby)	—	0.91	0.93	0.95	V
V_{LVD100_F}	CC	P	V_{DD_LV} (Flash)	—	1.08	1.10	1.12	V
High Voltage Detectors LV								
V_{HVD134_C}	CC	P	V_{DD_LV}	—	1.28	1.31	1.33	V
Upper Voltage Detectors LV								
V_{UVD140_C}	CC	P	V_{DD_LV}	—	1.34	1.37	1.39	V
Common								
$T_{VMFILTER}$	CC	D	Voltage monitor filter(3)	—	5	—	25	µs

1. Even if LVD/HVD monitor reaction is configurable, the application ensures that the device remains in the operative condition range, and the internal LVDx monitors are disabled by the application. Then an external voltage monitor with minimum threshold of VDD_LV(min) = 1.08 V measured at the device pad, has to be implemented.
For HVDx, if the application disables them, then they need to grant that VDD_LV and VDD_HV voltage levels stay withing the limitations provided in *Section 4.2: Absolute maximum ratings*.
2. The values reported are Trimmed values, where applicable.
3. See *Figure 11*. Transitions shorter than minimum are filtered. Transitions longer than maximum are not filtered, and will be delayed by $T_{VMFILTER}$ time. Transitions between minimum and maximum can be filtered or not filtered, according to temperature, process and voltage variations.

4.14 Flash

The following table shows the Wait State configuration.

Table 31. Wait State configuration

RWSC	CORE FREQUENCY (MHZ)
2	f ≤ 80
1	f ≤ 54
0	f ≤ 27

The following table shows the Program/Erase Characteristics.

Table 32. Flash memory program and erase specifications

Symbol	Characteristics[1][2]	Value									Unit
		Typ[3]	C	Initial max			Typical end of life[4]	Lifetime max[5]		C	
				25 °C [6]	All temp [7]	C		< 1 K cycles	≤ 250 K cycles		
$t_{dwprogram}$	Double Word (64 bits) program time [Packaged part]	51	C	156	—	—	168	500		C	µs
$t_{pprogram}$	Page (256 bits) program time	86	C	288	—	—	288	1000		C	µs
$t_{pprogrameep}$	Page (256 bits) program time Data Flash - EEPROM (partition 1) [Packaged part]	100	C	316	—	—	331	1000		C	µs
$t_{qprogram}$	Quad Page (1024 bits) program time	264	C	1248	1440	P	1020	2000		C	µs
$t_{qprogrameep}$	Quad Page (1024 bits) program time Data Flash - EEPROM (partition 1) [Packaged part]	294	C	1368	1584	P	1173	2000		C	µs
$t_{16kpperase}$	16 KB block pre-program and erase time	230	C	500	550	P	265	1000	—	C	ms
$t_{32kpperase}$	32 KB block pre-program and erase time	320	C	584	670	P	370	1200	—	C	ms
$t_{64kpperase}$	64 KB block pre-program and erase time	500	C	800	850	P	575	1600	—	C	ms
$t_{128kpperase}$	128 KB block pre-program and erase time	850	C	1520	1870	P	930	4000	—	C	ms
—	—	—	C	—	—	P	—	—	—	C	ms
$t_{16kprogram}$	16 KB block program time	40	C	54	60	P	48	1000	—	C	ms
$t_{32kprogram}$	32 KB block program time	80	C	108	120	P	90	1200	—	C	ms
$t_{64kprogram}$	64 KB block program time	162	C	210	240	P	180	1600	—	C	ms

Table 32. Flash memory program and erase specifications (continued)

Symbol	Characteristics(1)(2)	Value									Unit
		Typ(3)	C	Initial max			Typical end of life(4)	Lifetime max(5)		C	
				25 °C (6)	All temp (7)	C		< 1 K cycles	≤ 250 K cycles		
$t_{128kprogram}$	128 KB block program time	324	C	420	516	P	360	2000	—	C	ms
—	—	—	C	—	—	P	—	—	—	C	ms
$t_{16kprogrameep}$	Program 16 KB Data Flash - EEPROM (partition 1) [Packaged part]	47	C	62	70	P	77	1750		C	ms
$t_{16keraseeep}$	Erase 16 KB Data Flash - EEPROM (partition 1) [Packaged part]	250	C	584	864	P	475	3600		C	ms
t_{prr}	Program rate(8)	2.59	C	3.36	4.12	C	2.88	—		C	s/MB
t_{err}	Erase rate(8)	6.8	C	12.1	14.9	C	7.44	—		C	s/MB
t_{prfm}	Program rate Factory Mode(8)	1.76	C	2.25	2.75	C	—	—		C	s/MB
t_{erfm}	Erase rate Factory Mode(8)	5.0	C	8.2	9.8	C	—	—		C	s/MB
$t_{ffprogram}$	Full flash programming time(9)	2.59	C	3.37	4.12	P	2.89	—	—	C	s
$t_{fferase}$	Full flash erasing time(9)	5.16	C	13.8	16.4	P	7.81	—	—	C	s
t_{ESRT}	Erase suspend request rate(10)	200	T	—	—	—	—	—		—	µs
t_{PSRT}	Program suspend request rate(10)	30	T	—	—	—	—	—		—	µs
t_{AMRT}	Array Integrity Check - Margin Read suspend request rate	15	T	—	—	—	—	—		—	µs
t_{PSUS}	Program suspend latency(11)	—	—	—	—	—	—	12		T	µs
t_{ESUS}	Erase suspend latency(11)	—	—	—	—	—	—	22		T	µs
t_{AIC0S}	Array Integrity Check (1.0 MB, sequential)(12)	60	T	—	—	—	—	—	—	—	ms
$t_{AIC256KS}$	Array Integrity Check (128 KB, sequential)(12)	2.5	T	—	—	—	—	—	—	—	ms
t_{AIC0P}	Array Integrity Check (1.0 MB, proprietary)(12)	7.2	T	—	—	—	—	—	—	—	s
t_{MR0S}	Margin Read (1.0 MB, sequential)(12)	300	T	—	—	—	—	—	—	—	ms
$t_{MR256KS}$	Margin Read (128 KB, sequential)(12)	12.5	T	—	—	—	—	—	—	—	ms

1. Characteristics are valid both for Data Flash and Code Flash, unless specified in the characteristics column.
2. Actual hardware operation times; this does not include software overhead.
3. Typical program and erase times assume nominal supply values and operation at 25 °C.
4. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations. These values are characteristic, but not tested.
5. Lifetime maximum program & erase times apply across the voltages and temperatures and occur after the specified number of program/erase cycles. These maximum values are characterized but not tested or guaranteed.
6. Initial factory condition: < 100 program/erase cycles, 25 °C typical junction temperature and nominal (± 5%) supply voltages.
7. Initial maximum "All temp" program and erase times provide guidance for time-out limits used in the factory and apply for less than or equal to 100 program or erase cycles, –40 °C < TJ < 150 °C junction temperature and nominal (± 5%) supply voltages.
8. Rate computed based on 128 KB sectors.
9. Only code sectors, not including EEPROM.
10. Time between suspend resume and next suspend. Value stated actually represents Min value specification.
11. Timings guaranteed by design.
12. AIC is done using system clock, thus all timing is dependent on system frequency and number of wait states. Timing in the table is calculated at max frequency.

All the Flash operations require the presence of the system clock for internal synchronization. About 50 synchronization cycles are needed: this means that the timings of the previous table can be longer if a low frequency system clock is used.

Table 33. Flash memory Life Specification

Symbol	Characteristics(1) (2)	Value				Unit
		Min	C	Typ	C	
N_{CER16K}	16 KB CODE Flash endurance	10	—	100	—	Kcycles
N_{CER32K}	32 KB CODE Flash endurance	10	—	100	—	Kcycles
N_{CER64K}	64 KB CODE Flash endurance	10	—	100	—	Kcycles
$N_{CER128K}$	128 KB CODE Flash endurance	1	—	100	—	Kcycles
$N_{CER256K}$	128 KB CODE Flash endurance	1	—	100	—	Kcycles
	128 KB CODE Flash endurance(3)	10	—	100	—	Kcycles
N_{DER16K}	16 KB DATA EEPROM Flash endurance	250	—	—	—	Kcycles
t_{DR1k}	Minimum data retention Blocks with 0 - 1,000 P/E cycles	25	—	—	—	Years
t_{DR10k}	Minimum data retention Blocks with 1,001 - 10,000 P/E cycles	20	—	—	—	Years
t_{DR100k}	Minimum data retention Blocks with 10,001 - 100,000 P/E cycles	15	—	—	—	Years
t_{DR250k}	Minimum data retention Blocks with 100,001 - 250,000 P/E cycles	10	—	—	—	Years

1. Program and erase cycles supported across specified temperature specifications.
2. It is recommended that the application enables the core cache memory.
3. 10K cycles on 4-128 KB blocks is not intended for production. Reduced reliability and degraded erase time are possible.

4.15 AC Specifications

All AC timing specifications are valid up to 150 °C, except where explicitly noted.

4.15.1 Debug and calibration interface timing

4.15.1.1 JTAG interface timing

Table 34. JTAG pin AC electrical characteristics

#	Symbol		C	Characteristic	Value(1),(2)		Unit
					Min	Max	
1	t_{JCYC}	CC	D	TCK cycle time	100	—	ns
2	t_{JDC}	CC	T	TCK clock pulse width	40	60	%
3	$t_{TCKRISE}$	CC	D	TCK rise and fall times (40%–70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	CC	D	TMS, TDI data setup time	5	—	ns
5	t_{TMSH}, t_{TDIH}	CC	D	TMS, TDI data hold time	5	—	ns
6	t_{TDOV}	CC	D	TCK low to TDO data valid	—	15(3)	ns
7	t_{TDOI}	CC	D	TCK low to TDO data invalid	0	—	ns
8	t_{TDOHZ}	CC	D	TCK low to TDO high impedance	—	15	ns
9	t_{JCMPPW}	CC	D	JCOMP assertion time	100	—	ns
10	t_{JCMPS}	CC	D	JCOMP setup time to TCK low	40	—	ns
11	t_{BSDV}	CC	D	TCK falling edge to output valid	—	600(4)	ns
12	t_{BSDVZ}	CC	D	TCK falling edge to output valid out of high impedance	—	600	ns
13	t_{BSDHZ}	CC	D	TCK falling edge to output high impedance	—	600	ns
14	t_{BSDST}	CC	D	Boundary scan input valid to TCK rising edge	15	—	ns
15	t_{BSDHT}	CC	D	TCK rising edge to boundary scan input invalid	15	—	ns

1. These specifications apply to JTAG boundary scan only. See *Table 35* for functional specifications.
2. JTAG timing specified at $V_{DD\_HV\_IO\_JTAG}$ = 4.0 to 5.5 V and max. loading per pad type as specified in the I/O section of the datasheet.
3. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
4. Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

Figure 12. JTAG test clock input timing

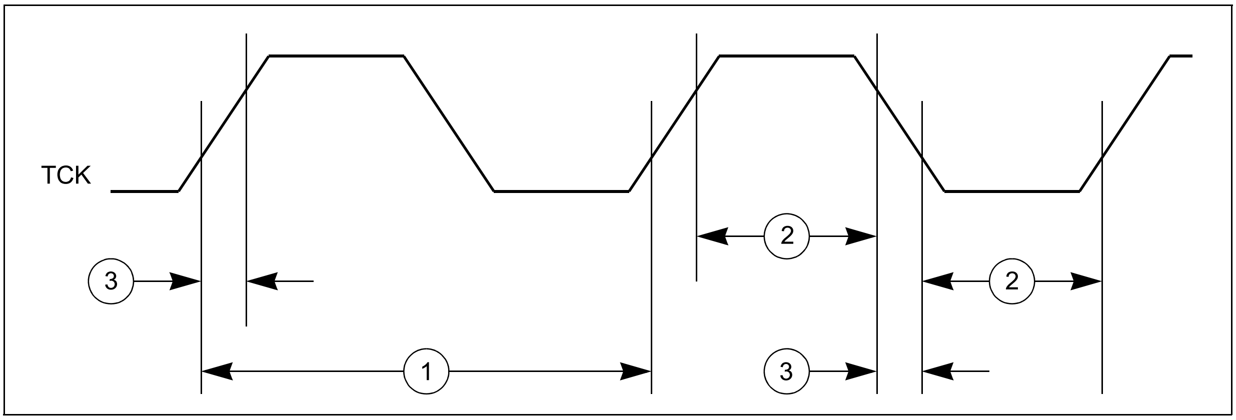


Figure 13. JTAG test access port timing

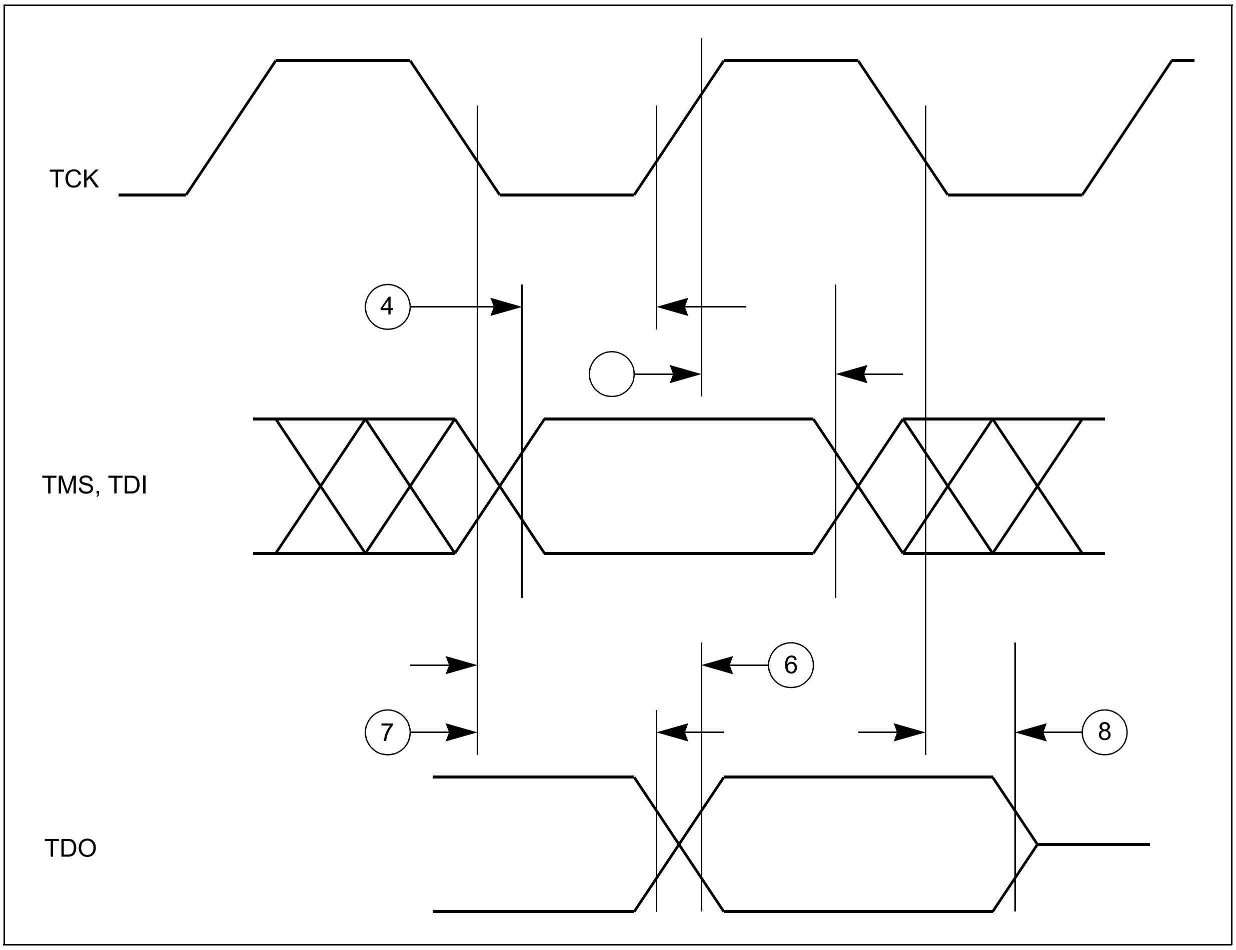


Figure 14. JTAG JCOMP timing

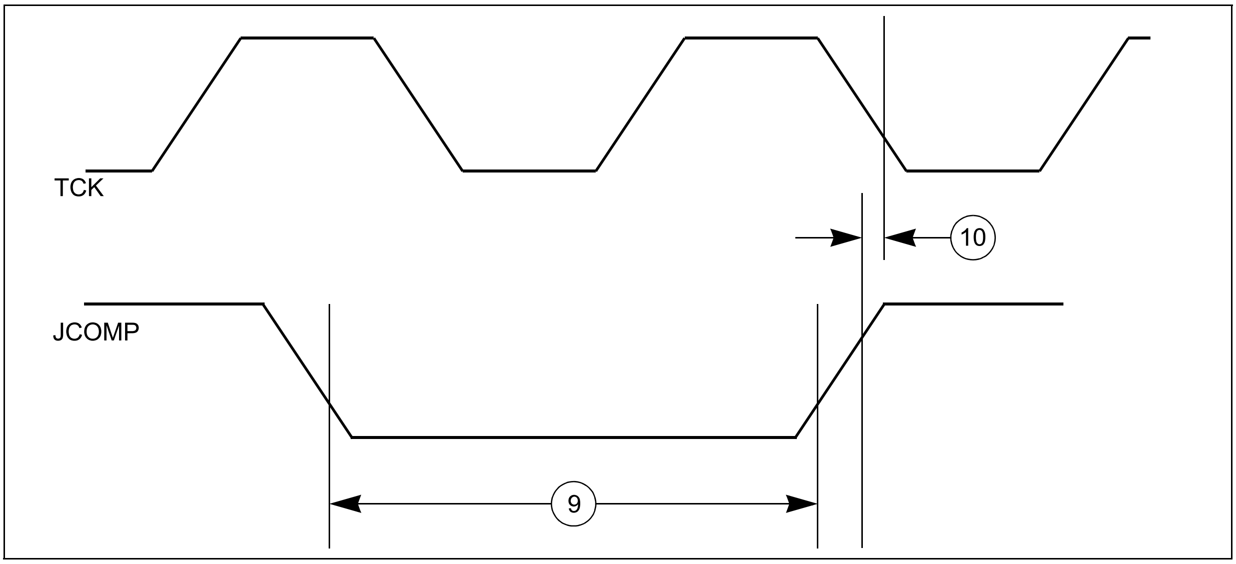
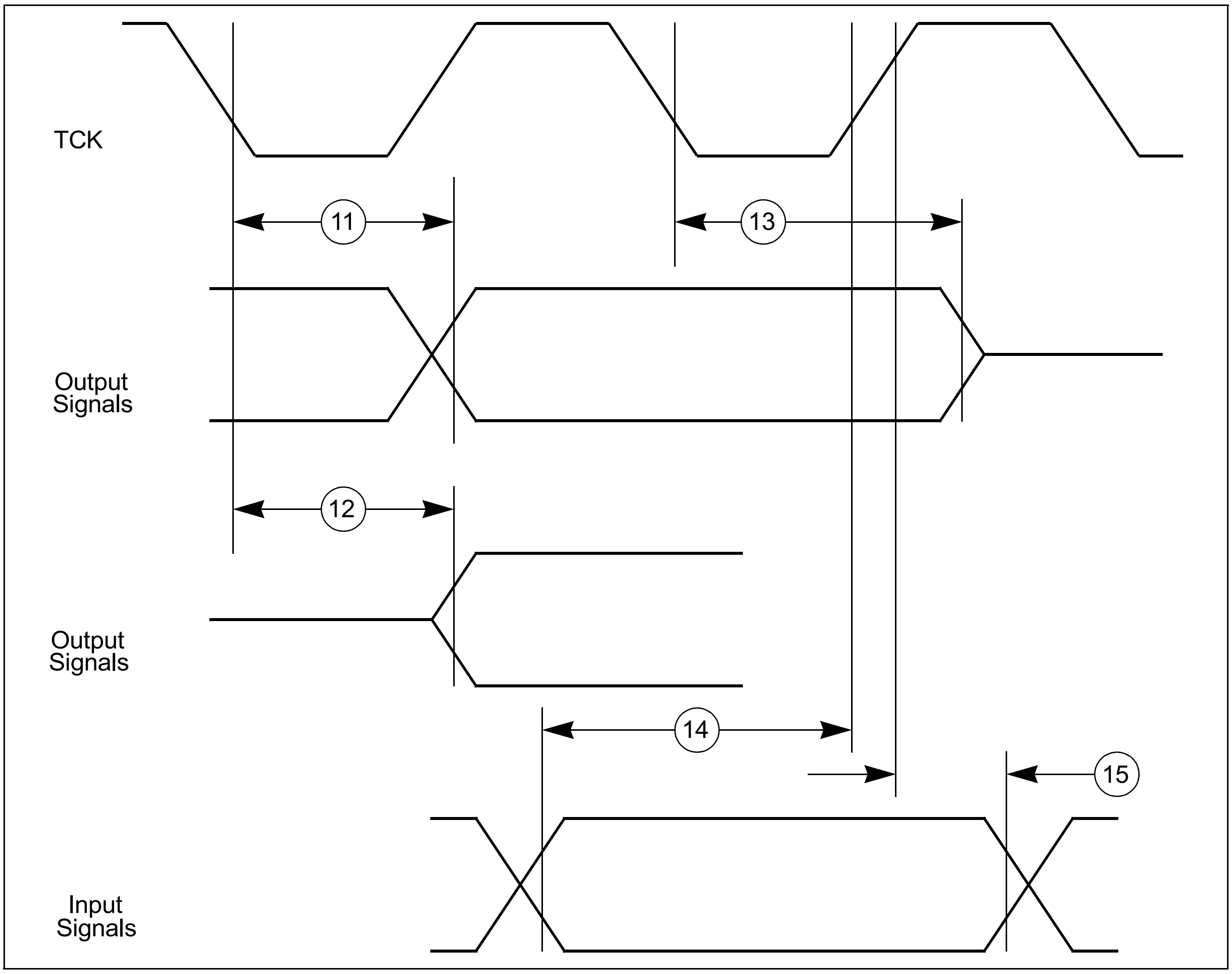


Figure 15. JTAG boundary scan timing



4.15.1.2 Nexus interface timing

Table 35. Nexus debug port timing

#	Symbol		C	Characteristic	Value(1)		Unit
					Min	Max	
7	t_{EVTIPW}	CC	D	$\overline{\text{EVTI}}$ pulse width	4	—	t_{CYC}(2)
8	t_{EVTOPW}	CC	D	$\overline{\text{EVTO}}$ pulse width	40	—	ns
9	t_{TCYC}	CC	D	TCK cycle time	2(3),(4)	—	t_{CYC}(2)
				Absolute minimum TCK cycle time(5) (TDO sampled on posedge of TCK)	40(6)	—	ns
				Absolute minimum TCK cycle time(7) (TDO sampled on negedge of TCK)	20(6)	—	
11	t_{NTDIS}	CC	D	TDI data setup time	5	—	ns
12	t_{NTDIH}	CC	D	TDI data hold time	5	—	ns
13	t_{NTMSS}	CC	D	TMS data setup time	5	—	ns
14	t_{NTMSH}	CC	D	TMS data hold time	5	—	ns
15	—	CC	D	TDO propagation delay from falling edge of TCK(8)	—	16	ns
16	—	CC	D	TDO hold time with respect to TCK falling edge (minimum TDO propagation delay)	2.25	—	ns

1. Nexus timing specified at $V_{DD\_HV\_IO\_JTAG}$ = 3.0 V to 5.5 V, and maximum loading per pad type as specified in the I/O section of the data sheet.
2. t_{CYC} is system clock period.
3. Achieving the absolute minimum TCK cycle time may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual peripheral frequency being used. To ensure proper operation TCK frequency should be set to the peripheral frequency divided by a number greater than or equal to that specified here.
4. This is a functionally allowable feature. However, it may be limited by the maximum frequency specified by the Absolute minimum TCK period specification.
5. This value is TDO propagation time 36 ns + 4 ns setup time to sampling edge.
6. This may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual system frequency being used.
7. This value is TDO propagation time 16 ns + 4 ns setup time to sampling edge.
8. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.

Figure 16. Nexus output timing

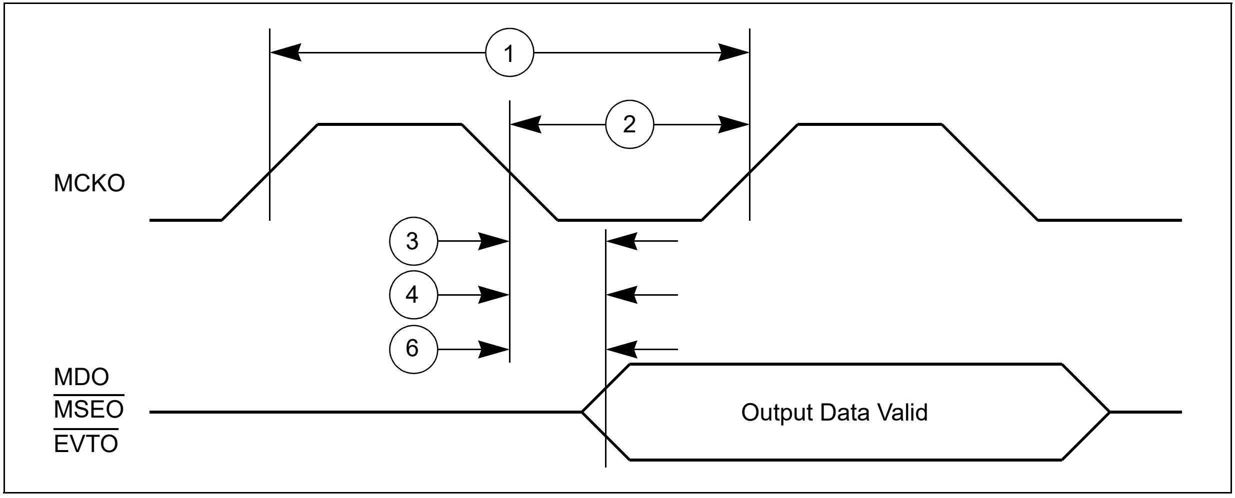


Figure 17. Nexus event trigger and test clock timings

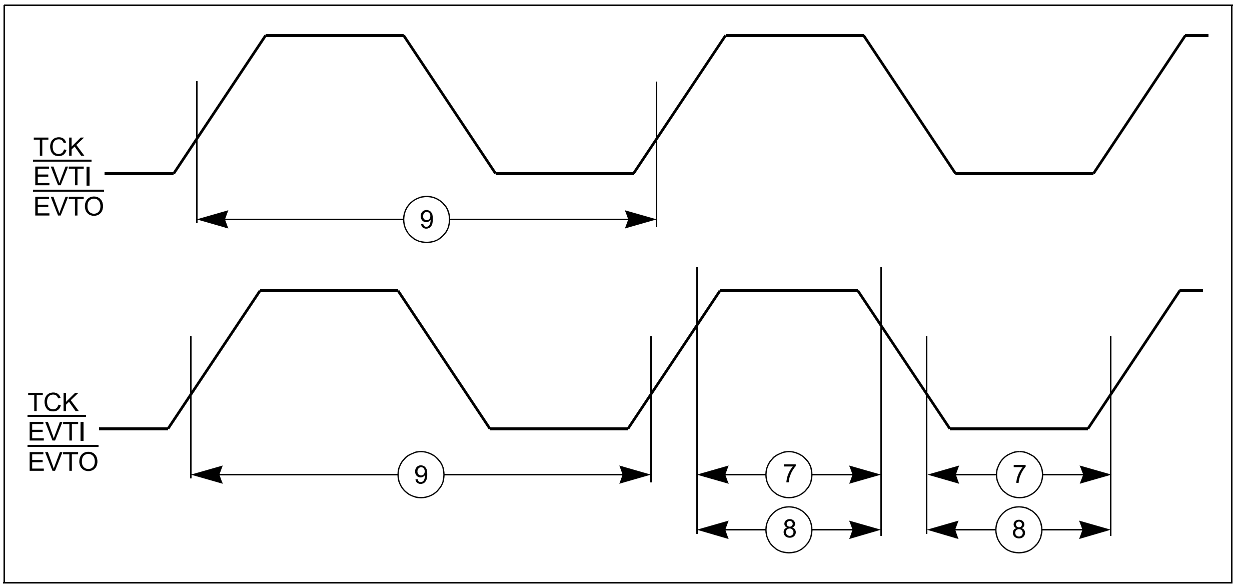
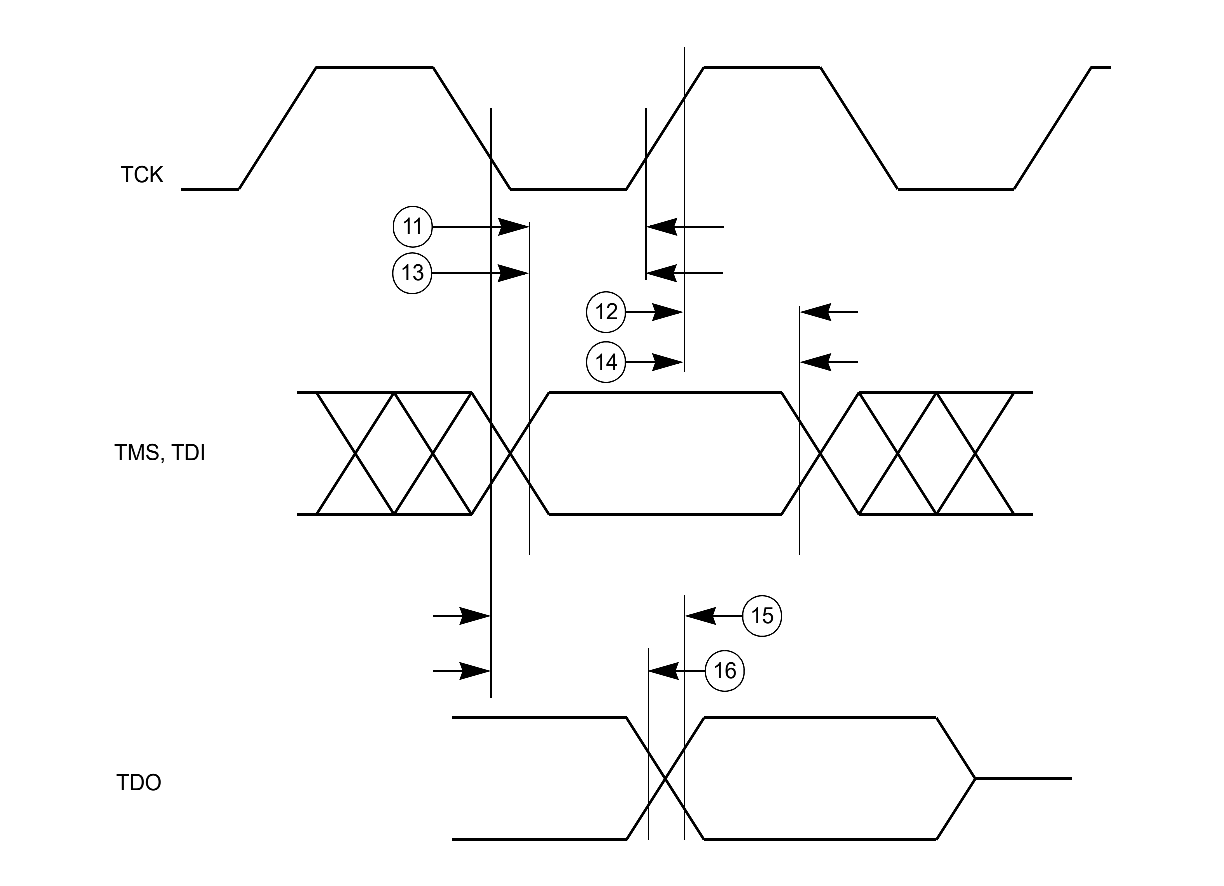


Figure 18. Nexus TDI, TMS, TDO timing



4.15.1.3 External interrupt timing (IRQ pin)

Table 36. External interrupt timing

Characteristic	Symbol	Min	Max	Unit
IRQ Pulse Width Low	t_{IPWL}	3	—	t_{cyc}
IRQ Pulse Width High	t_{IPWH}	3	—	t_{cyc}
IRQ Edge to Edge Time(1)	t_{ICYC}	6	—	t_{cyc}

1. Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

Figure 19. External interrupt timing

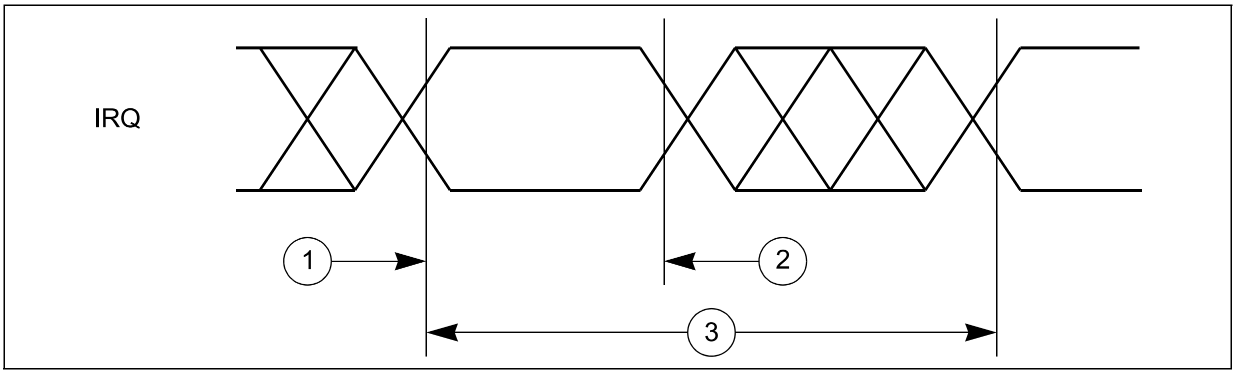
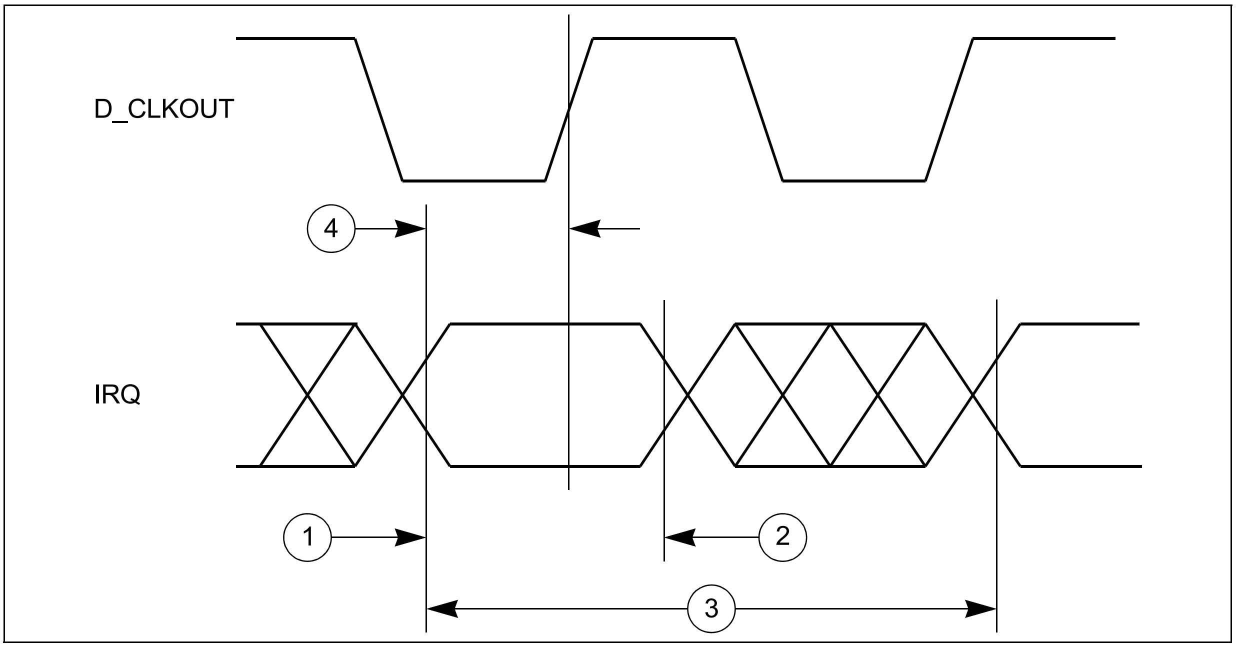


Figure 20. External interrupt timing



4.15.2 DSPI timing with CMOS pads

DSPI channel frequency support is shown in *Table 37*.

Timing specifications are shown in the tables below.

Table 37. DSPI channel frequency support

DSPI use mode(1)			Max usable frequency (MHz)(2),(3)
CMOS (Master mode)	Full duplex – Classic timing (Table 38)	DSPI_0, DSPI_1, DSPI_2, DSPI_3,	10
	Full duplex – Modified timing (Table 39)	DSPI_0, DSPI_1, DSPI_2, DSPI_3,	10
	Output only mode (SCK/SOUT/PCS) (Table 38 and Table 39)	DSPI_0, DSPI_1, DSPI_2, DSPI_3,	10
	Output only mode TSB mode (SCK/SOUT/PCS)	DSPI_0, DSPI_1, DSPI_2, DSPI_3,	10
CMOS (Slave mode Full duplex) (Table 40)		—	10

1. Each DSPI module can be configured to use different pins for the interface. Refer to the device pinout Microsoft Excel file attached to the IO_Definition document for the available combinations. It is not possible to reach the maximum performance with every possible combination of pins.
2. Maximum usable frequency can be achieved if used with fastest configuration of the highest drive pads.
3. Maximum usable frequency does not take into account external device propagation delay.

4.15.2.1 DSPI master mode full duplex timing with CMOS pads

4.15.2.1.1 DSPI CMOS master mode – classic timing

Note: In the following table, all output timing is worst case and includes the mismatching of rise and fall times of the output pads.

Table 38. DSPI CMOS master classic timing (full duplex and output only) MTFE = 0, CPHA = 0 or 1

#	Symbol		C	Characteristic	Condition		Value(1)		Unit
					Pad drive(2)	Load (C_L)	Min	Max	
1	t_{SCK}	CC	D	SCK cycle time	SCK drive strength				
					Very strong	25 pF	59.0	—	ns
					Strong	50 pF	80.0	—	ns
					Medium	50 pF	200.0	—	ns
2	t_{CSC}	CC	D	PCS to SCK delay	SCK and PCS drive strength				
					Very strong	25 pF	$(N^{(3)} \times t_{SYS}{}^{(4)}) - 16$	—	ns
					Strong	50 pF	$(N^{(3)} \times t_{SYS}{}^{(4)}) - 16$	—	ns
					Medium	50 pF	$(N^{(3)} \times t_{SYS}{}^{(4)}) - 16$	—	ns
					PCS medium and SCK strong	PCS = 50 pF SCK = 50 pF	$(N^{(3)} \times t_{SYS}{}^{(4)}) - 29$	—	ns

Table 38. DSPI CMOS master classic timing (full duplex and output only) MTFE = 0, CPHA = 0 or 1 (continued)

#	Symbol		C	Characteristic	Condition		Value[(1)]		Unit
					Pad drive[(2)]	Load (C_L)	Min	Max	
3	t_{ASC}	CC	D	After SCK delay	SCK and PCS drive strength				
					Very strong	PCS = 0 pF SCK = 50 pF	$(M^{(5)} \times t_{SYS}{}^{(4)}) - 35$	—	ns
					Strong	PCS = 0 pF SCK = 50 pF	$(M^{(5)} \times t_{SYS}{}^{(4)}) - 35$	—	ns
					Medium	PCS = 0 pF SCK = 50 pF	$(M^{(5)} \times t_{SYS}{}^{(4)}) - 35$	—	ns
					PCS medium and SCK strong	PCS = 0 pF SCK = 50 pF	$(M^{(5)} \times t_{SYS}{}^{(4)}) - 35$	—	ns
4	t_{SDC}	CC	D	SCK duty cycle[(6)]	SCK drive strength				
					Very strong	0 pF	$^1/_2 t_{SCK} - 2$	$^1/_2 t_{SCK} + 2$	ns
					Strong	0 pF	$^1/_2 t_{SCK} - 2$	$^1/_2 t_{SCK} + 2$	ns
					Medium	0 pF	$^1/_2 t_{SCK} - 5$	$^1/_2 t_{SCK} + 5$	ns
PCS strobe timing									
5	t_{PCSC}	CC	D	PCSx to $\overline{PCSS}$ time[(7)]	PCS and PCSS drive strength				
					Strong	25 pF	16.0	—	ns
6	t_{PASC}	CC	D	$\overline{PCSS}$ to PCSx time[(7)]	PCS and PCSS drive strength				
					Strong	25 pF	16.0	—	ns
SIN setup time									
7	t_{SUI}	CC	D	SIN setup time to SCK[(8)]	SCK drive strength				
					Very strong	25 pF	25.0	—	ns
					Strong	50 pF	31.0	—	ns
					Medium	50 pF	52.0	—	ns
SIN hold time									
8	t_{HI}	CC	D	SIN hold time from SCK[(8)]	SCK drive strength				
					Very strong	0 pF	–1.0	—	ns
					Strong	0 pF	–1.0	—	ns
					Medium	0 pF	–1.0	—	ns
SOUT data valid time (after SCK edge)									
9	t_{SUO}	CC	D	SOUT data valid time from SCK[(9)]	SOUT and SCK drive strength				
					Very strong	25 pF	—	7.0	ns
					Strong	50 pF	—	8.0	ns
					Medium	50 pF	—	16.0	ns

Table 38. DSPI CMOS master classic timing (full duplex and output only) MTFE = 0, CPHA = 0 or 1 (continued)

#	Symbol		C	Characteristic	Condition		Value[1]		Unit
					Pad drive[2]	Load (C_L)	Min	Max	
SOUT data hold time (after SCK edge)									
10	t_{HO}	CC	D	SOUT data hold time after SCK[9]	SOUT and SCK drive strength				
					Very strong	25 pF	–7.7	—	ns
					Strong	50 pF	–11.0	—	ns
					Medium	50 pF	–15.0	—	ns

1. All timing values for output signals in this table are measured to 50% of the output voltage.
2. Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.
3. N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
4. t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min t_{SYS} = 10 ns).
5. M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
6. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
7. PCSx and PCSS using same pad configuration.
8. Input timing assumes an input slew rate of 1 ns (10% – 90%) and uses TTL voltage thresholds.
9. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

Figure 21. DSPI CMOS master mode — classic timing, CPHA = 0

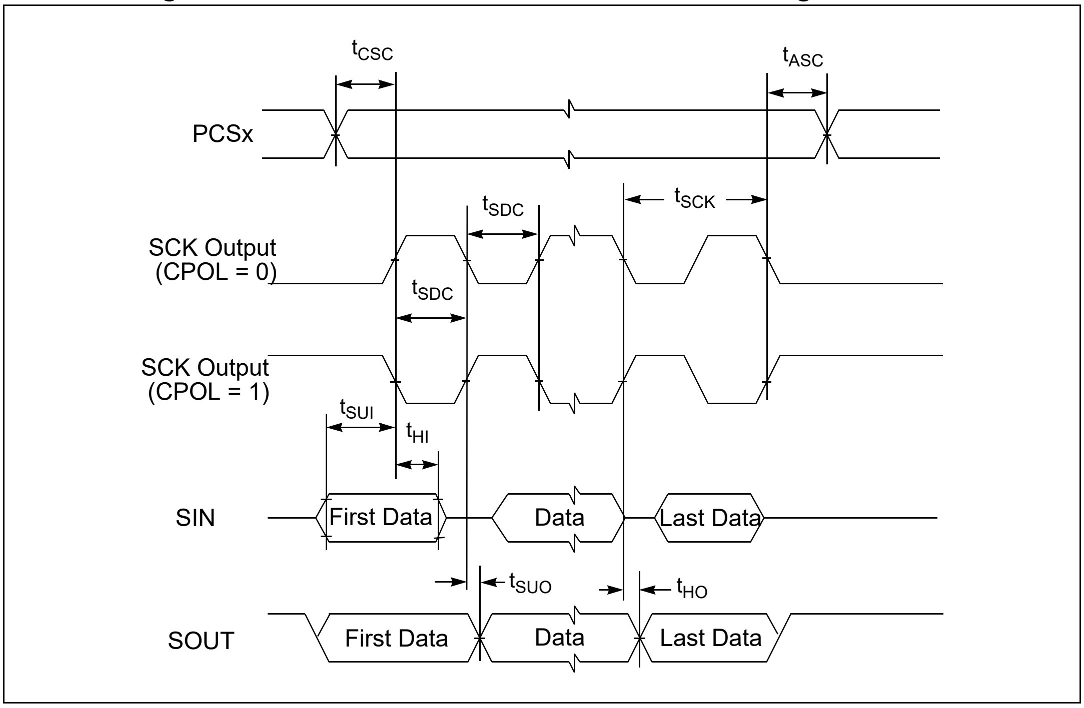


Figure 22. DSPI CMOS master mode — classic timing, CPHA = 1

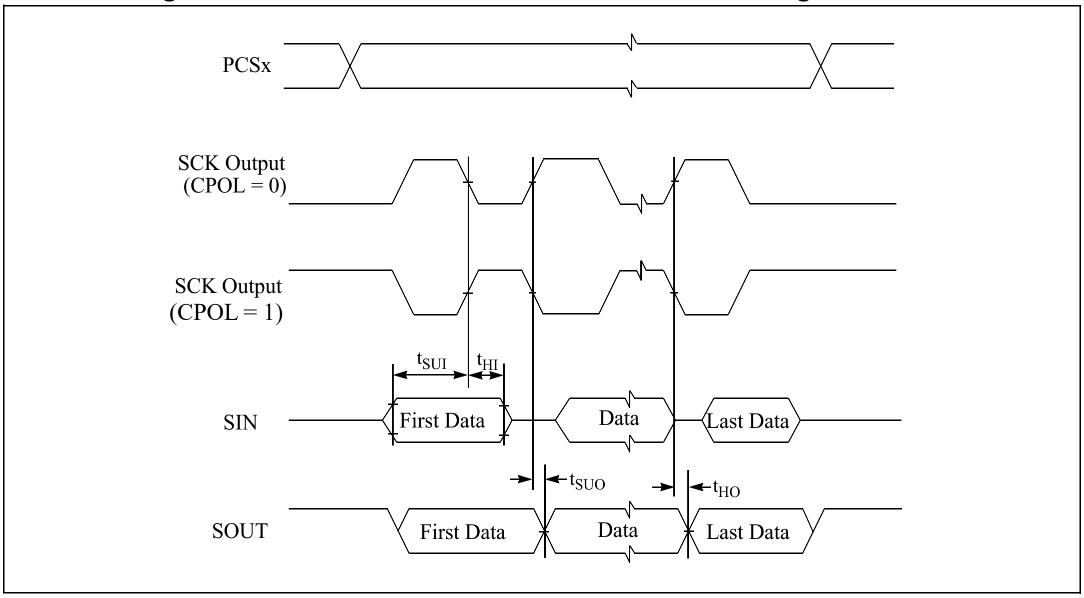
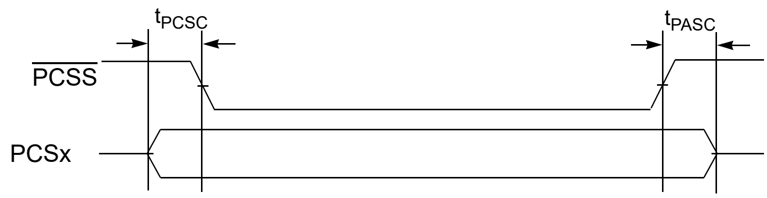


Figure 23. DSPI PCS strobe ($\overline{PCSS}$) timing (master mode)



4.15.2.1.2 DSPI CMOS master mode — modified timing

Note: In the following table, all output timing is worst case and includes the mismatching of rise and fall times of the output pads.

Table 39. DSPI CMOS master modified timing (full duplex and output only) MTFE = 1, CPHA = 0 or 1

#	Symbol		C	Characteristic	Condition		Value(1)		Unit
					Pad drive(2)	Load (C_L)	Min	Max	
1	t_{SCK}	CC	D	SCK cycle time	SCK drive strength				
					Very strong	25 pF	33.0	—	ns
					Strong	50 pF	80.0	—	ns
					Medium	50 pF	200.0	—	ns
2	t_{CSC}	CC	D	PCS to SCK delay	SCK and PCS drive strength				
					Very strong	25 pF	$(N^{(3)} \times t_{SYS}^{(4)}) - 16$	—	ns
					Strong	50 pF	$(N^{(3)} \times t_{SYS}^{(4)}) - 16$	—	ns
					Medium	50 pF	$(N^{(3)} \times t_{SYS}^{(4)}) - 16$	—	ns
					PCS medium and SCK strong	PCS = 50 pF SCK = 50 pF	$(N^{(3)} \times t_{SYS}^{(4)}) - 29$	—	ns
3	t_{ASC}	CC	D	After SCK delay	SCK and PCS drive strength				
					Very strong	PCS = 0 pF SCK = 50 pF	$(M^{(5)} \times t_{SYS}^{(4)}) - 35$	—	ns
					Strong	PCS = 0 pF SCK = 50 pF	$(M^{(5)} \times t_{SYS}^{(4)}) - 35$	—	ns
					Medium	PCS = 0 pF SCK = 50 pF	$(M^{(5)} \times t_{SYS}^{(4)}) - 35$	—	ns
					PCS medium and SCK strong	PCS = 0 pF SCK = 50 pF	$(M^{(5)} \times t_{SYS}^{(4)}) - 35$	—	ns

Table 39. DSPI CMOS master modified timing (full duplex and output only) MTFE = 1, CPHA = 0 or 1 (continued)

#	Symbol		C	Characteristic	Condition		Value[1]		Unit
					Pad drive[2]	Load (C_L)	Min	Max	
4	t_{SDC}	CC	D	SCK duty cycle[6]	SCK drive strength				
					Very strong	0 pF	$^1/_2 t_{SCK} - 2$	$^1/_2 t_{SCK} + 2$	ns
					Strong	0 pF	$^1/_2 t_{SCK} - 2$	$^1/_2 t_{SCK} + 2$	
					Medium	0 pF	$^1/_2 t_{SCK} - 5$	$^1/_2 t_{SCK} + 5$	
PCS strobe timing									
5	t_{PCSC}	CC	D	PCSx to $\overline{PCSS}$ time[7]	PCS and PCSS drive strength				
					Strong	25 pF	16.0	—	ns
6	t_{PASC}	CC	D	$\overline{PCSS}$ to PCSx time[7]	PCS and PCSS drive strength				
					Strong	25 pF	16.0	—	ns
SIN setup time									
7	t_{SUI}	CC	D	SIN setup time to SCK CPHA = 0[8]	SCK drive strength				
					Very strong	25 pF	$25 - (P^{(9)} \times t_{SYS}{}^{(4)})$	—	ns
					Strong	50 pF	$31 - (P^{(9)} \times t_{SYS}{}^{(4)})$	—	
					Medium	50 pF	$52 - (P^{(9)} \times t_{SYS}{}^{(4)})$	—	
				SIN setup time to SCK CPHA = 1[8]	SCK drive strength				
					Very strong	25 pF	25.0	—	ns
					Strong	50 pF	31.0	—	
					Medium	50 pF	52.0	—	
SIN hold time									
8	t_{HI}	CC	D	SIN hold time from SCK CPHA = 0[8]	SCK drive strength				
					Very strong	0 pF	$-1 + (P^{(9)} \times t_{SYS}{}^{(3)})$	—	ns
					Strong	0 pF	$-1 + (P^{(9)} \times t_{SYS}{}^{(3)})$	—	
					Medium	0 pF	$-1 + (P^{(9)} \times t_{SYS}{}^{(3)})$	—	
				SIN hold time from SCK CPHA = 1[8]	SCK drive strength				
					Very strong	0 pF	–1.0	—	ns
					Strong	0 pF	–1.0	—	
					Medium	0 pF	–1.0	—	

Table 39. DSPI CMOS master modified timing (full duplex and output only) MTFE = 1, CPHA = 0 or 1 (continued)

#	Symbol	C		Characteristic	Condition		Value[1]		Unit
					Pad drive[2]	Load (C_L)	Min	Max	
SOUT data valid time (after SCK edge)									
9	t_{SUO}	CC	D	SOUT data valid time from SCK CPHA = 0, [10]	SOUT and SCK drive strength				
					Very strong	25 pF	—	$7.0 + t_{SYS}$[4]	ns
					Strong	50 pF	—	$8.0 + t_{SYS}$[4]	
					Medium	50 pF	—	$16.0 + t_{SYS}$[4]	
				SOUT data valid time from SCK CPHA = 1[10]	SOUT and SCK drive strength				
					Very strong	25 pF	—	7.0	ns
					Strong	50 pF	—	8.0	
					Medium	50 pF	—	16.0	
SOUT data hold time (after SCK edge)									
10	t_{HO}	CC	D	SOUT data hold time after SCK CPHA = 0[10]	SOUT and SCK drive strength				
					Very strong	25 pF	$-7.7 + t_{SYS}$[4]	—	ns
					Strong	50 pF	$-11.0 + t_{SYS}$[4]	—	
					Medium	50 pF	$-15.0 + t_{SYS}$[4]	—	
				SOUT data hold time after SCK CPHA = 1[10]	SOUT and SCK drive strength				
					Very strong	25 pF	–7.7	—	ns
					Strong	50 pF	–11.0	—	
					Medium	50 pF	–15.0	—	

1. All timing values for output signals in this table are measured to 50% of the output voltage.
2. Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.
3. N is the number of clock cycles added to time between PCS assertion and SCK assertion and is software programmable using DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, N is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
4. t_{SYS} is the period of DSPI_CLKn clock, the input clock to the DSPI module. Maximum frequency is 100 MHz (min t_{SYS} = 10 ns).
5. M is the number of clock cycles added to time between SCK negation and PCS negation and is software programmable using DSPI_CTARx[PASC] and DSPI_CTARx[ASC]. The minimum value is 2 cycles unless TSB mode or Continuous SCK clock mode is selected, in which case, M is automatically set to 0 clock cycles (PCS and SCK are driven by the same edge of DSPI_CLKn).
6. t_{SDC} is only valid for even divide ratios. For odd divide ratios the fundamental duty cycle is not 50:50. For these odd divide ratios cases, the absolute spec number is applied as jitter/uncertainty to the nominal high time and low time.
7. PCSx and PCSS using same pad configuration.
8. Input timing assumes an input slew rate of 1 ns (10% – 90%) and uses TTL voltage thresholds.
9. P is the number of clock cycles added to delay the DSPI input sample point and is software programmable using DSPI_ MCR[SMPL_PT]. The value must be 0, 1 or 2. If the baud rate divide ratio is /2 or /3, this value is automatically set to 1.

10. SOUT Data Valid and Data hold are independent of load capacitance if SCK and SOUT load capacitances are the same value.

Figure 24. DSPI CMOS master mode — modified timing, CPHA = 0

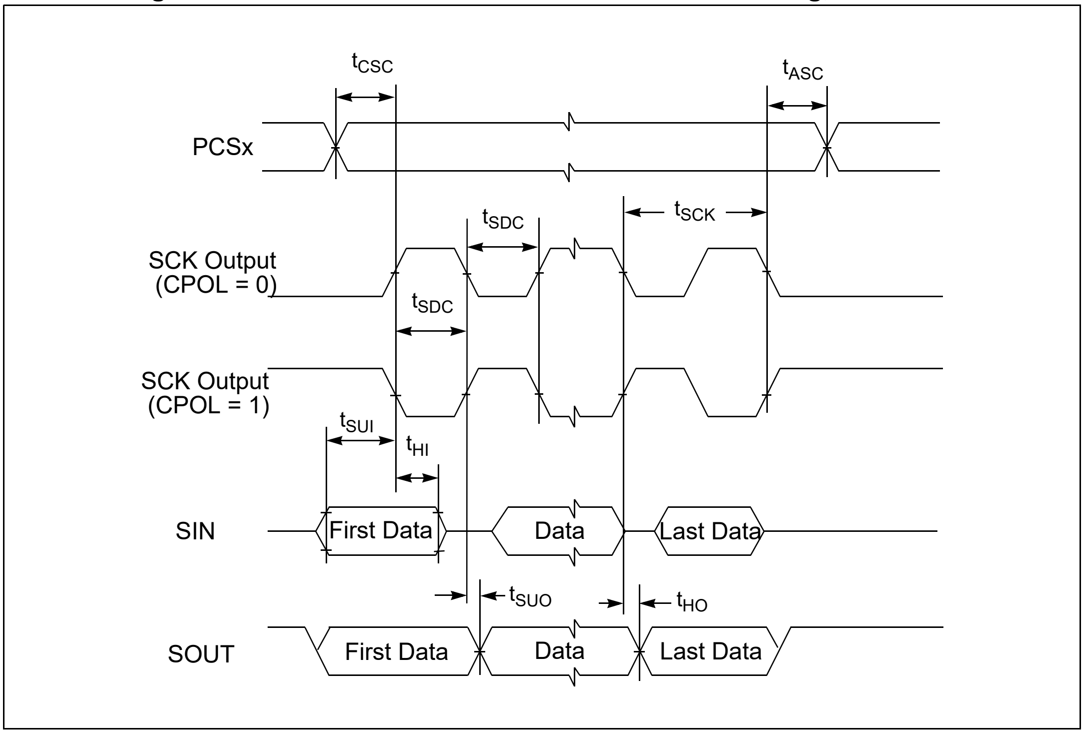


Figure 25. DSPI CMOS master mode — modified timing, CPHA = 1

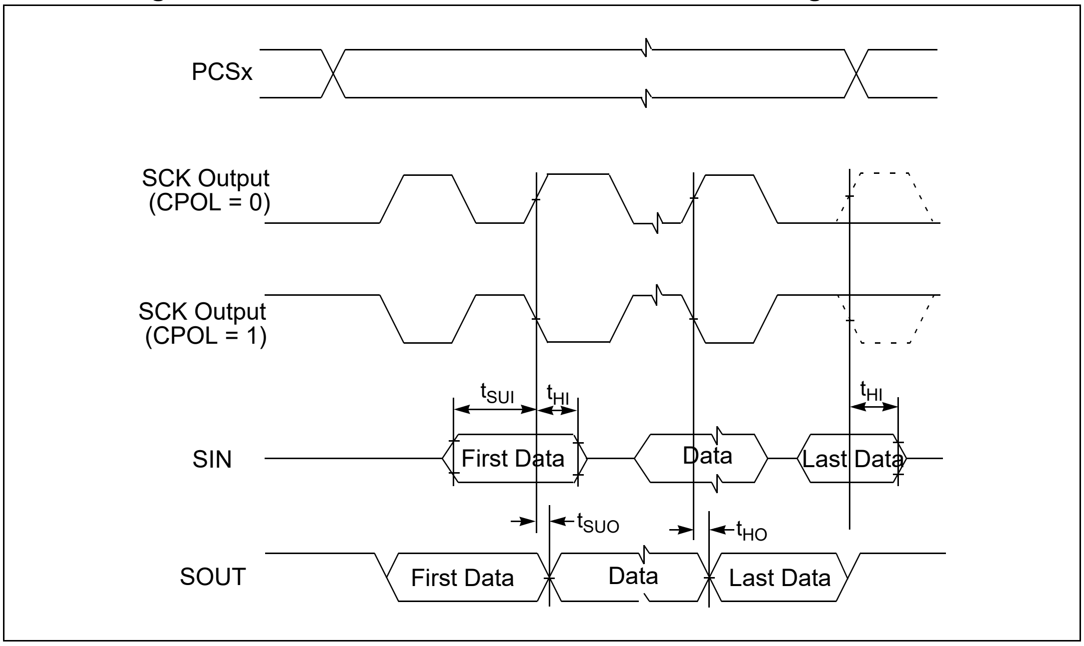
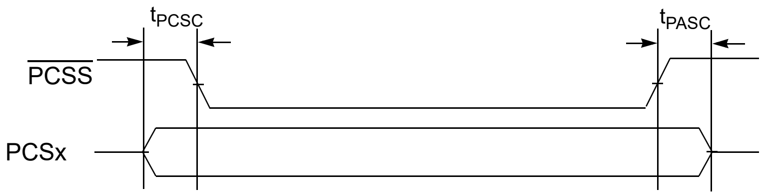


Figure 26. DSPI PCS strobe (PCSS) timing (master mode)



4.15.2.2 Slave mode timing

Table 40. DSPI CMOS slave timing — full duplex — normal and modified transfer formats (MTFE = 0/1)

#	Symbol		C	Characteristic	Condition		Min	Max	Unit
					Pad Drive	Load			
1	t_{SCK}	CC	D	SCK Cycle Time(1)	—	—	62	—	ns
2	t_{CSC}	SR	D	SS to SCK Delay(1)	—	—	16	—	ns
3	t_{ASC}	SR	D	SCK to SS Delay(1)	—	—	16	—	ns
4	t_{SDC}	CC	D	SCK Duty Cycle(1)	—	—	30	—	ns
5	t_A	CC	D	Slave Access Time(1) (2) (3) (SS active to SOUT driven)	Very strong	25 pF	—	50	ns
					Strong	50 pF	—	50	ns
					Medium	50 pF	—	60	ns
6	t_{DIS}	CC	D	Slave SOUT Disable Time(1) (2) (3) (SS inactive to SOUT High-Z or invalid)	Very strong	25 pF	—	5	ns
					Strong	50 pF	—	5	ns
					Medium	50 pF	—	10	ns
9	t_{SUI}	CC	D	Data Setup Time for Inputs(1)	—	—	10	—	ns
10	t_{HI}	CC	D	Data Hold Time for Inputs(1)	—	—	10	—	ns
11	t_{SUO}	CC	D	SOUT Valid Time(1) (2) (3) (after SCK edge)	Very strong	25 pF	—	30	ns
					Strong	50 pF	—	30	ns
					Medium	50 pF	—	50	ns
12	t_{HO}	CC	D	SOUT Hold Time(1) (2) (3) (after SCK edge)	Very strong	25 pF	2.5	—	ns
					Strong	50 pF	2.5	—	ns
					Medium	50 pF	2.5	—	ns

1. Input timing assumes an input slew rate of 1 ns (10% - 90%) and uses TTL voltage thresholds.
2. All timing values for output signals in this table, are measured to 50% of the output voltage.
3. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.

Figure 27. DSPI slave mode — modified transfer format timing (MFTE = 0/1) CPHA = 0

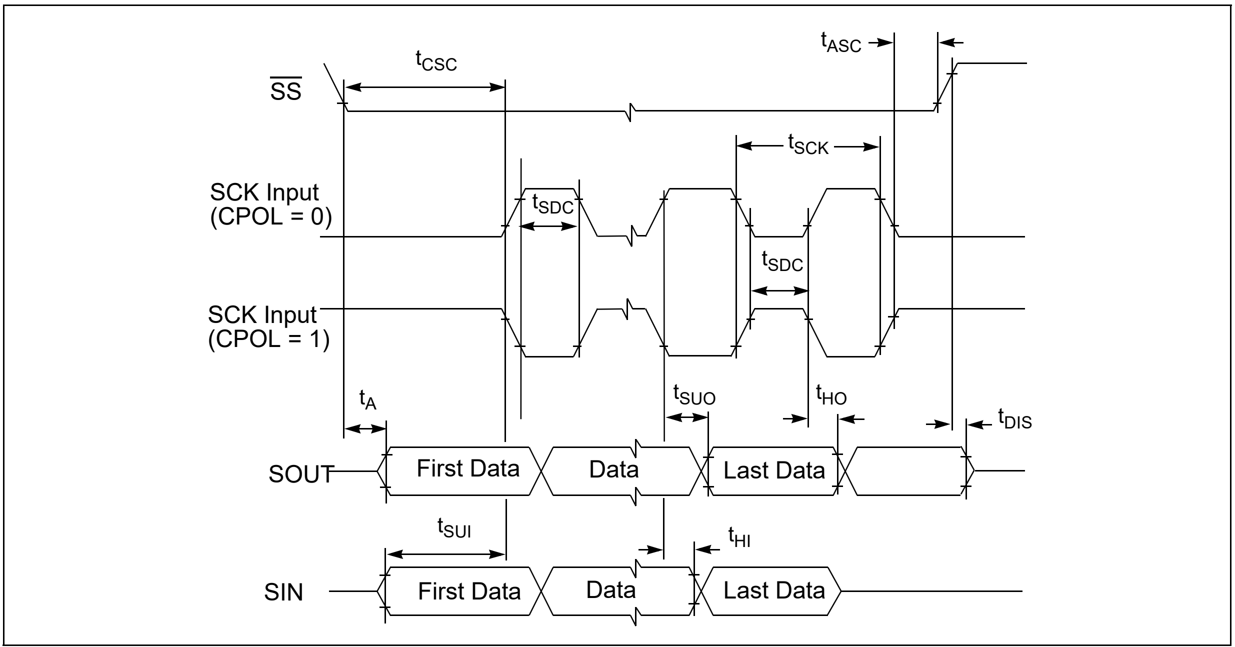
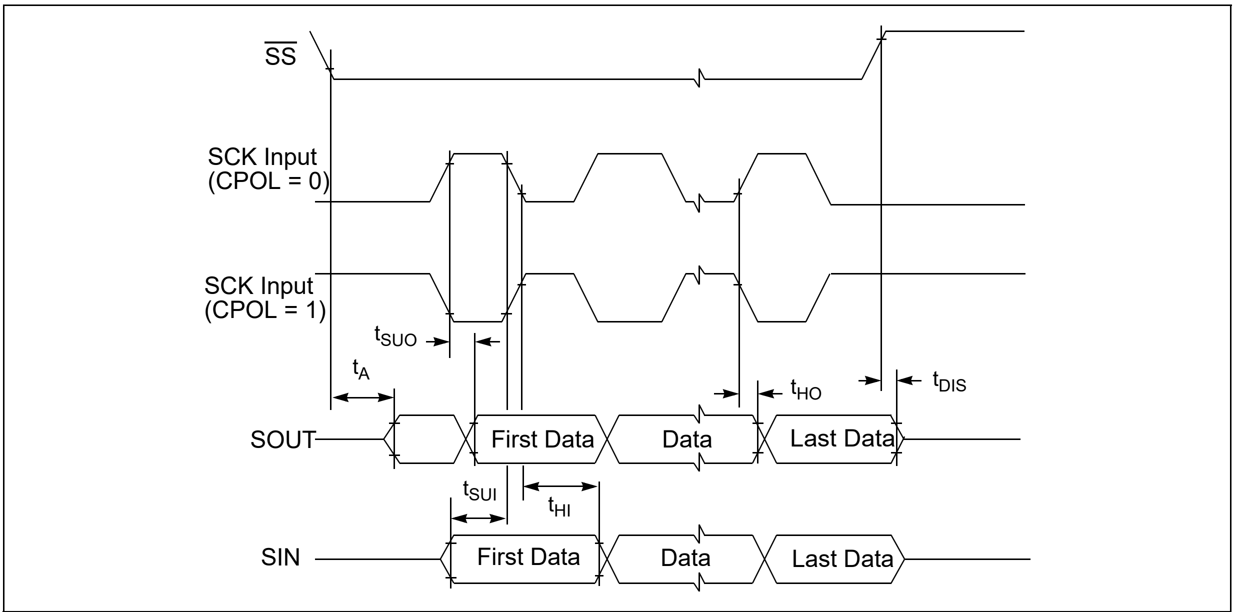


Figure 28. DSPI slave mode — modified transfer format timing (MFTE = 0/1) CPHA = 1



4.15.3 CAN timing

The following table describes the CAN timing.

Table 41. CAN timing

Symbol		C	Parameter	Condition	Value Min	Value Typ	Value Max	Unit
$t_{P(RX:TX)}$	CC	D	CAN controller propagation delay time standard pads	Medium type pads 25pF load	—	—	70	ns
	CC	D		Medium type pads 50pF load	—	—	80	
	CC	D		STRONG, VERY STRONG type pads 25pF load	—	—	60	
	CC	D		STRONG, VERY STRONG type pads 50pF load	—	—	65	
$t_{PLP(RX:TX)}$	CC	D	CAN controller propagation delay time low power pads	Medium type pads 25pF load	—	—	90	ns
	CC	D		Medium type pads 50pF load	—	—	100	
	CC	D		STRONG, VERY STRONG type pads 25pF load	—	—	80	
	CC	D		STRONG, VERY STRONG type pads 50pF load	—	—	85	

4.15.4 UART timing

UART channel frequency support is shown in the following table.

Table 42. UART frequency support

LINFlexD clock frequency LIN_CLK (MHz)	Oversampling rate	Voting scheme	Max usable frequency (Mbaud)
80	16	3:1 majority voting	5
	8		10
	6	Limited voting on one sample with configurable sampling point	13.33
	5		16
	4		20
100	16	3:1 majority voting	6.25
	8		12.5
	6	Limited voting on one sample with configurable sampling point	16.67
	5		20
	4		25

4.15.5 I2C timing

The I^2C AC timing specifications are provided in the following tables.

Note: In the following table, I2C input timing is valid for Automotive and TTL inputs levels, hysteresis enabled, and an input edge rate no slower than 1 ns (10% – 90%).

Table 43. I2C input timing specifications – SCL and SDA

No.	Symbol		C	Parameter	Value		Unit
					Min	Max	
1	—	CC	D	Start condition hold time	2	—	PER_CLK Cycle(1)
2	—	CC	D	Clock low time	8	—	PER_CLK Cycle
3	—	CC	D	Bus free time between Start and Stop condition	4.7	—	µs
4	—	CC	D	Data hold time	0.0	—	ns
5	—	CC	D	Clock high time	4	—	PER_CLK Cycle
6	—	CC	D	Data setup time	0.0	—	ns
7	—	CC	D	Start condition setup time (for repeated start condition only)	2	—	PER_CLK Cycle
8	—	CC	D	Stop condition setup time	2	—	PER_CLK Cycle

1. PER_CLK is the SoC peripheral clock, which drives the I^2C BIU and module clock inputs. See the Clocking chapter in the device reference manual for more detail.

Note: In the following table:

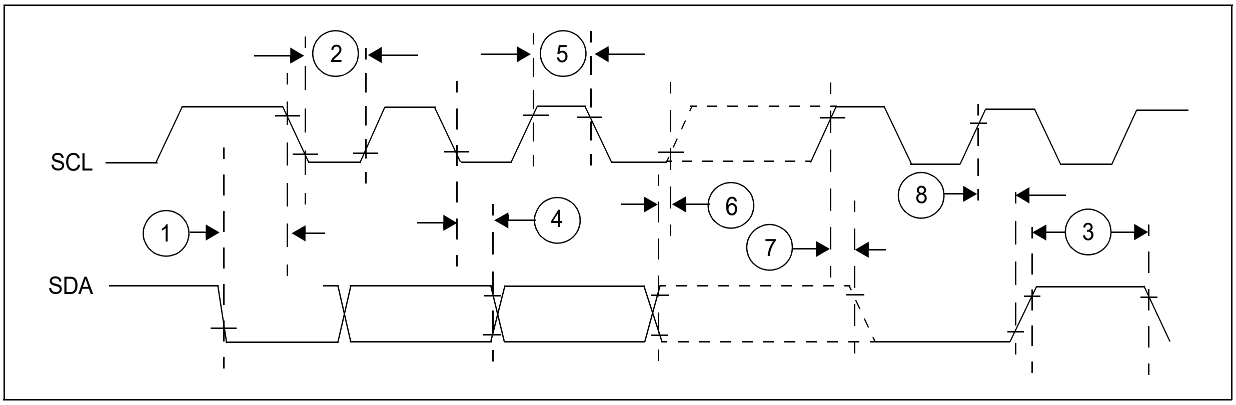
- *All output timing is worst case and includes the mismatching of rise and fall times of the output pads.*
- *Output parameters are valid for CL = 25 pF, where CL is the external load to the device (lumped). The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value.*
- *Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speeds and may cause incorrect operation.*
- *Programming the IBFD register (I2C bus Frequency Divider) with the maximum frequency results in the minimum output timings listed. The I2C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the pre-scale and division values programmed in the IBC field of the IBFD register.*

Table 44. I2C output timing specifications — SCL and SDA

No.	Symbol		C	Parameter	Value		Unit
					Min	Max	
1	—	CC	D	Start condition hold time	6	—	PER_CLK Cycle(1)
2	—	CC	D	Clock low time	10	—	PER_CLK Cycle
3	—	CC	D	Bus free time between Start and Stop condition	4.7	—	µs
4	—	CC	D	Data hold time	7	—	PER_CLK Cycle
5	—	CC	D	Clock high time	10	—	PER_CLK Cycle
6	—	CC	D	Data setup time	2	—	PER_CLK Cycle
7	—	CC	D	Start condition setup time (for repeated start condition only)	20	—	PER_CLK Cycle
8	—	CC	D	Stop condition setup time	10	—	PER_CLK Cycle

1. PER_CLK is the SoC peripheral clock, which drives the I²C BIU and module clock inputs. See the Clocking chapter in the device reference manual for more detail.

Figure 29. I²C input/output timing



5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

The following table lists the case numbers for SPC582Bx.

Table 45. Package case numbers

Package type	Device type
eTQFP64	Production
eTQFP100	Production
eTQFP144(1)	Emulation
QFN48	Production

1. eTQFP144 package is for emulation purpose only and not suitable for production. This package is not AEC-Q100 qualified.

5.1 eTQFP64 package information

Refer to *Section 5.1.1: Package mechanical drawings and data information* for full description of below figures and table notes.

Figure 30. eTQFP64 package outline

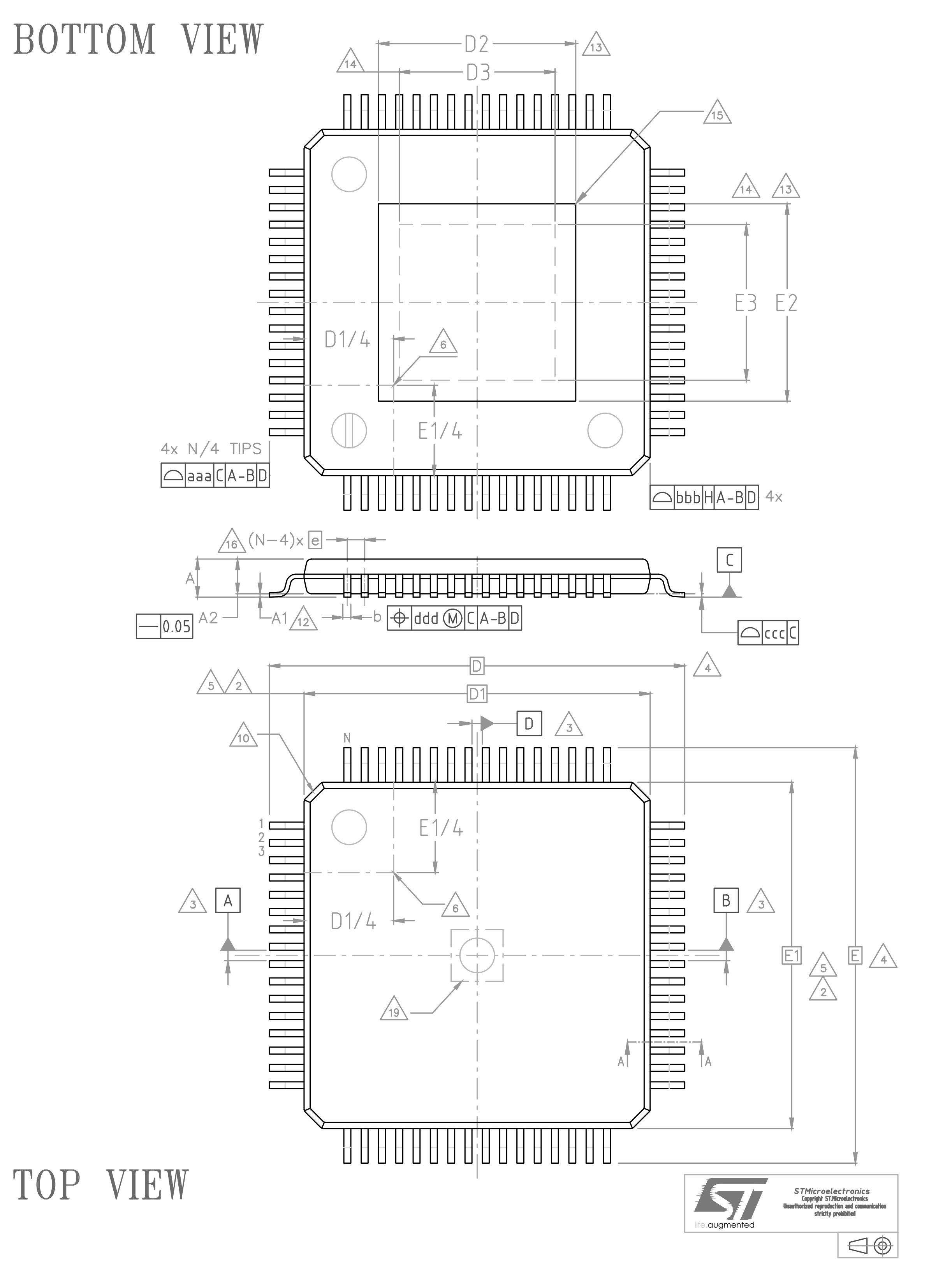


Figure 31. eTQFP64 section A-A

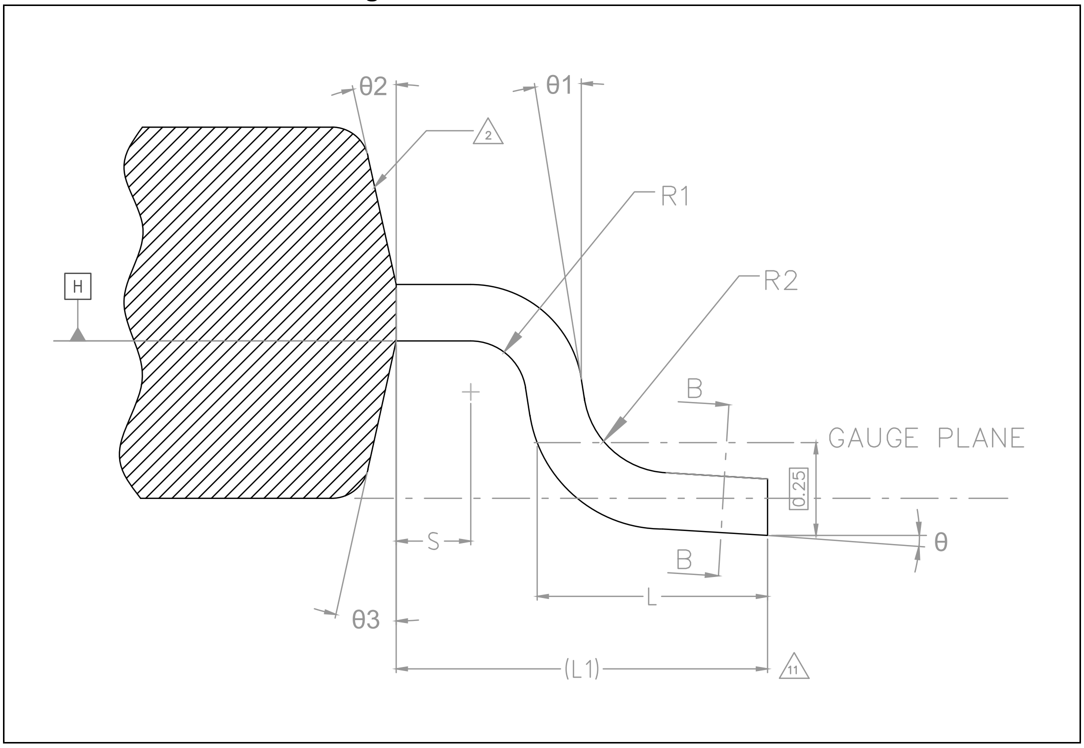


Figure 32. eTQFP64 section B-B

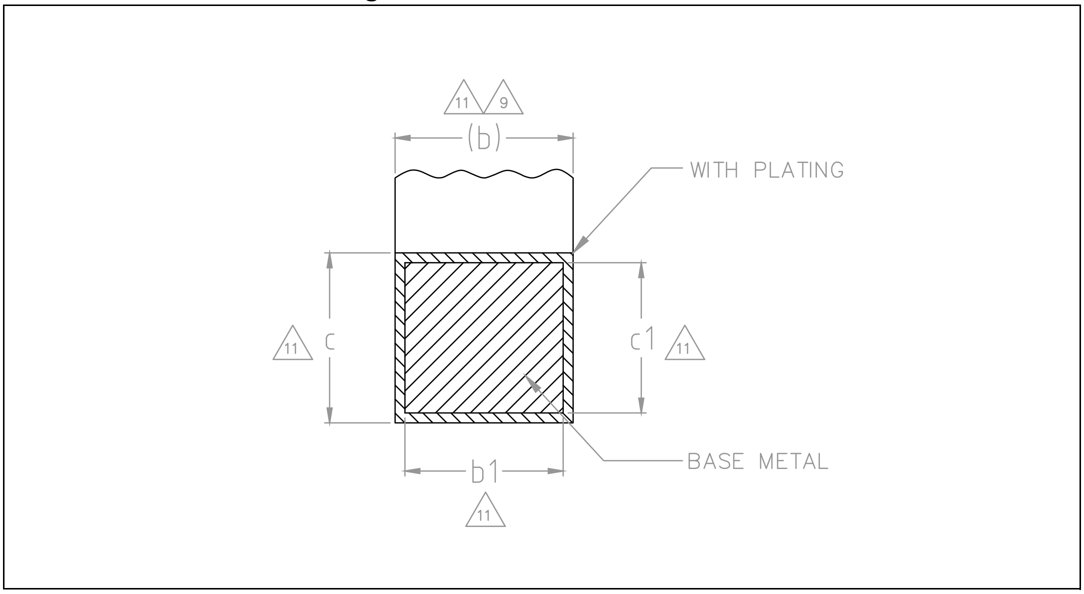


Table 46. eTQFP64 package mechanical data

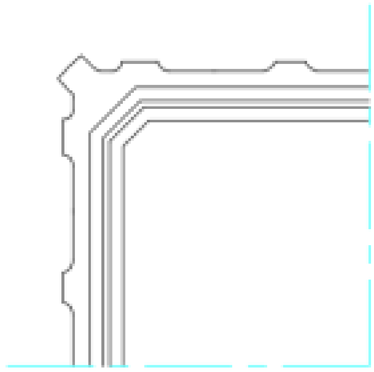
Symbol	Dimensions[7],[17]		
	Min.	Typ.	Max.
Θ	0°	3.5°	7°
Θ1	0°	—	—
Θ2	10°	12°	14°
Θ3	10°	12°	14°
A[15]	—	—	1.20
A1[12]	0.05	—	0.15
A2[15]	0.95	1.00	1.05
b[8],[9],[11]	0.17	0.22	0.27
b1[11]	0.17	0.20	0.23
c[11]	0.09	—	0.20
c1[11]	0.09	—	0.16
D[4]	12 BSC		
D1[2],[5]	10 BSC		
D2[13]	—	—	4.65
D3[14]	2.90	—	—
e	0.50 BSC		
E[4]	12 BSC		
E1[2],[5]	10 BSC		
E2[13]	—	—	4.65
E3[14]	2.90	—	—
L	0.45	0.60	0.75
L1	1 REF		
N[16]	64		
R1	0.08	—	—
R2	0.08	—	0.20
S	0.20	—	—
aaa[1],[18]	0.20		
bbb[1],[18]	0.20		
ccc[1],[18]	0.08		
ddd[1],[18]	0.08		

5.1.1 Package mechanical drawings and data information

The following notes are related to *Figure 30*, *Figure 31*, *Figure 32* and *Table 46*:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All dimensions are in millimeter except where explicitly noted.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located (if present). It includes all metal protrusions from exposed pad itself. Type of exposed pad on SPC582Bx is as *Figure 33*. End user should verify D2 and E2 dimensions according to the specific device application.
14. Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.
15. The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.
16. “N” is the max number of terminal positions for the specified body size.
17. Critical dimensions:
    a) Stand-Off
    b) Overall Width
    c) Lead Coplanarity
18. For symbols, recommended values and tolerances, see *Table 47*.
19. Notch may be present in this area (MAX 1.5mm square) if center top gate molding technology is applied. Resin gate residual not protruding out of package top surface.

Figure 33. eTQFP64 leadframe pad design



Note: number,

Table 47. eTQFP64 symbol definitions

Symbol	Definition	Notes
aaa	The tolerance that controls the position of the terminal pattern with respect to Datum A and B. The center of the tolerance zone for each terminal is defined by basic dimension e as related to Datum A and B.	For flange-molded packages, this tolerance also applies for basic dimensions D1 and E1. For packages tooled with intentional terminal tip protrusions, aaa does not apply to those protrusions.
bbb	The bilateral profile tolerance that controls the position of the plastic body sides. The centers of the profile zones are defined by the basic dimensions D and E.	—
ccc	The unilateral tolerance located above the seating plane where in the bottom surface of all terminals must be located.	This tolerance is commonly know as the “coplanarity” of the package terminals.
ddd	The tolerance that controls the position of the terminals to each other. The centers of the profile zones are defined by basic dimension e.	This tolerance is normally compounded with tolerance zone defined by “b”.

5.2 eTQFP100 package information

Refer to *Section 5.2.1: Package mechanical drawings and data information* for full description of below figures and table notes.

Figure 34. eTQFP100 package outline

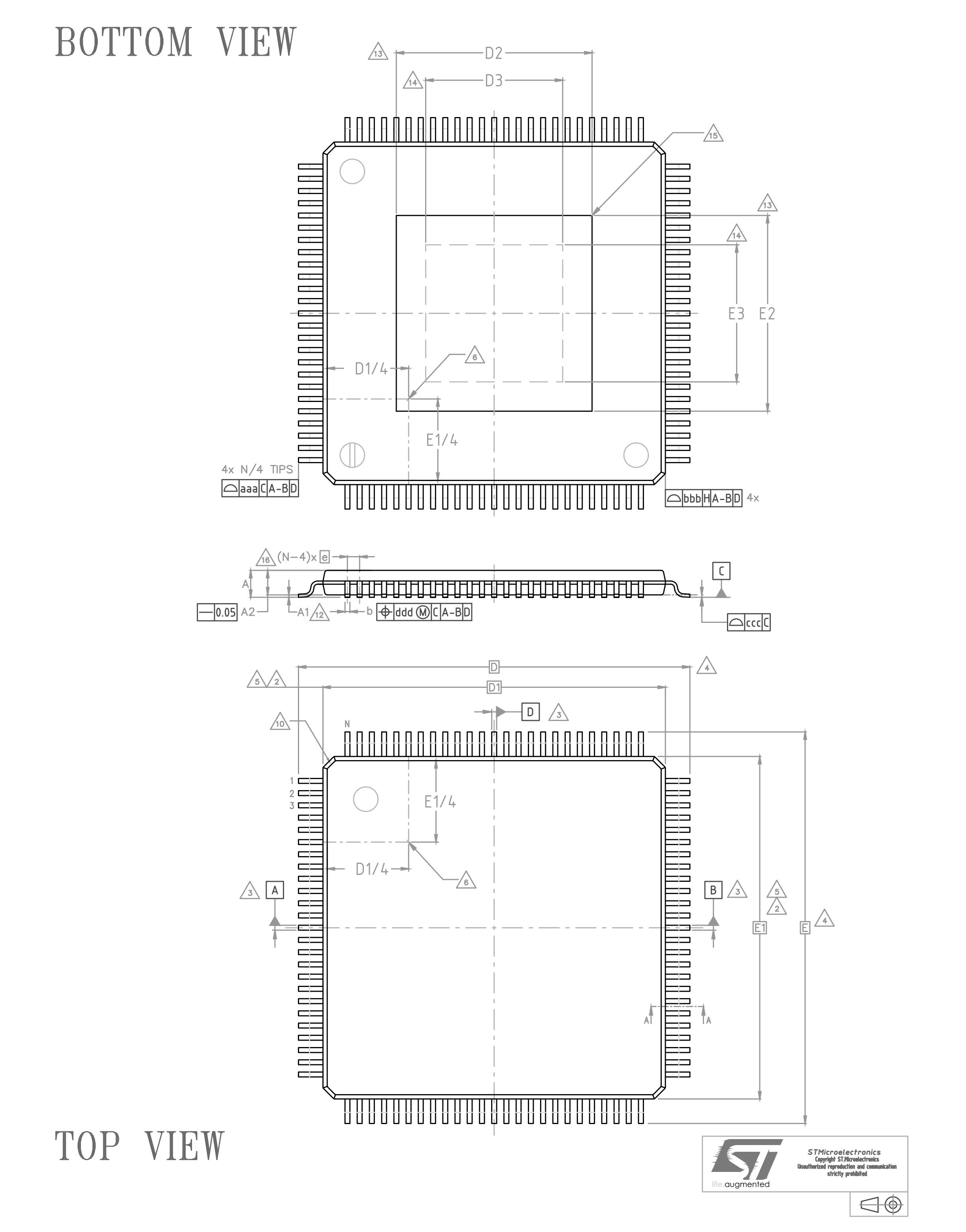


Figure 35. eTQFP100 section A-A

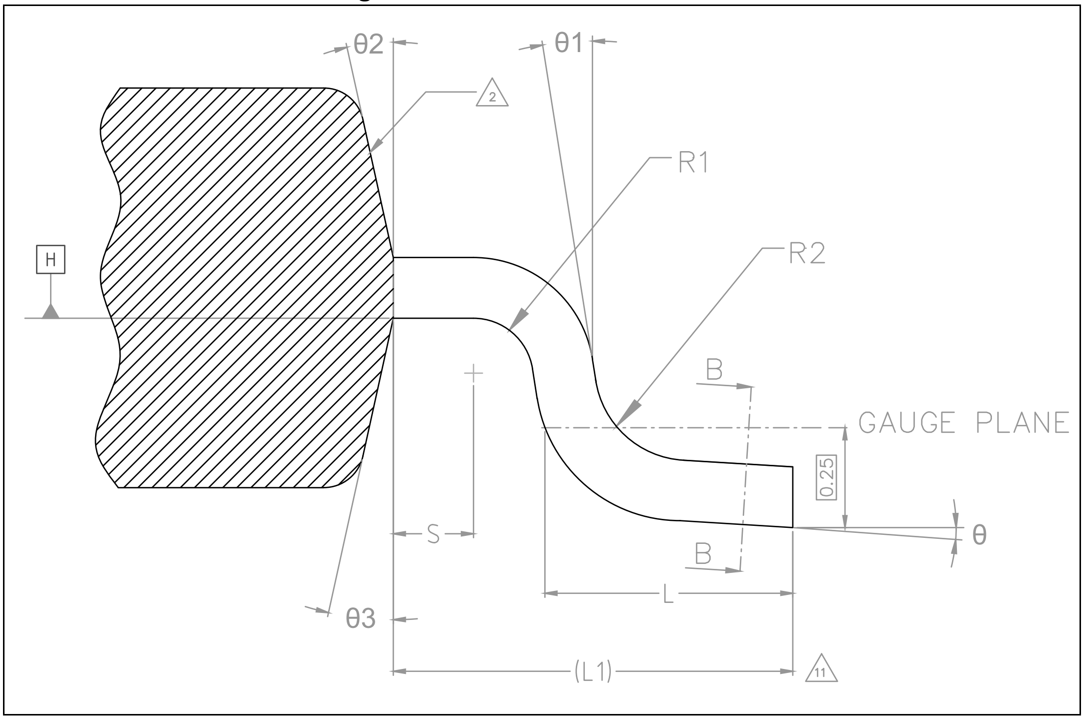


Figure 36. eTQFP100 section B-B

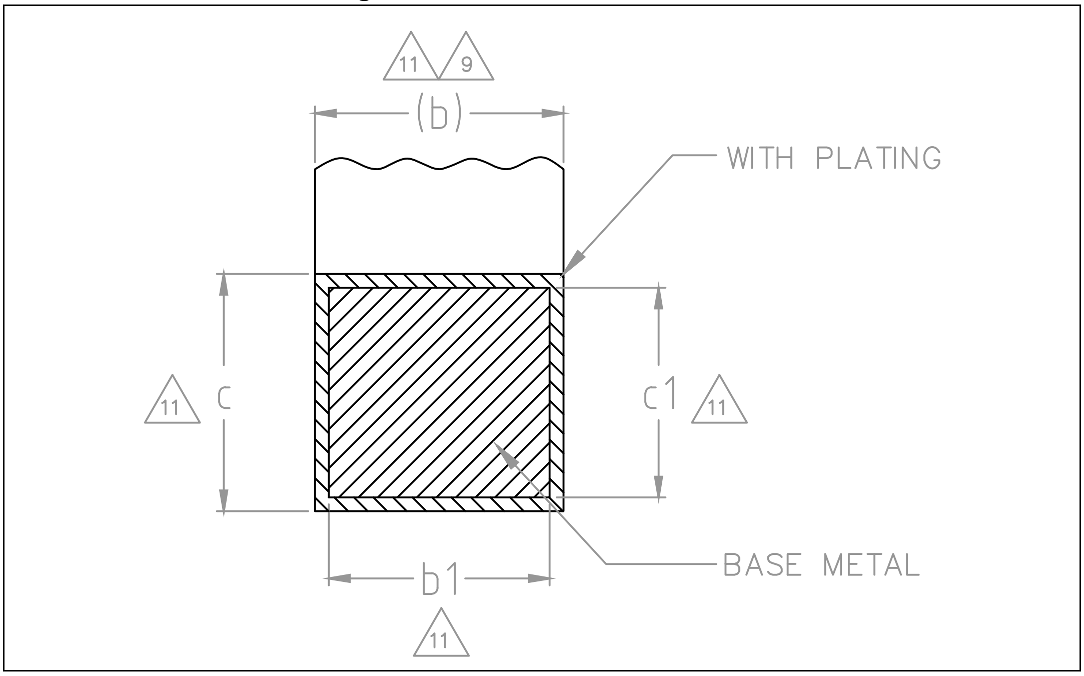


Table 48. eTQFP100 package mechanical data

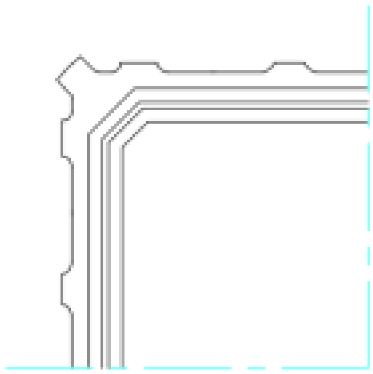
Symbol	Dimensions[7],[17]		
	Min.	Typ.	Max.
θ	0°	3.5°	7°
θ1	0°	—	—
θ2	10°	12°	14°
θ3	10°	12°	14°
A[15]	—	—	1.20
A1[12]	0.05	—	0.15
A2[15]	0.95	1.00	1.05
b[8],[9],[11]	0.17	0.22	0.27
b1[11]	0.17	0.20	0.23
c[11]	0.09	—	0.20
c1[11]	0.09	—	0.16
D[4]	16.00 BSC		
D1[2],[5]	14.00 BSC		
D2[13]	—	—	5.35
D3[14]	3.60	—	—
e	0.50 BSC		
E[4]	16.00 BSC		
E1[2],[5]	14.00 BSC		
E2[13]	—	—	5.35
E3[14]	3.60	—	—
L	0.45	0.60	0.75
L1	1.00 REF		
N[16]	100		
R1	0.08	—	—
R2	0.08	—	0.20
S	0.20	—	—
aaa[1],[18]	0.20		
bbb[1],[18]	0.20		
ccc[1],[18]	0.08		
ddd[1],[18]	0.08		

5.2.1 Package mechanical drawings and data information

The following notes are related to *Figure 34*, *Figure 35*, *Figure 36* and *Table 48*:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All dimensions are in millimeter except where explicitly noted.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located (if present). It includes all metal protrusions from exposed pad itself. Type of exposed pad on SPC582Bx is as *Figure 37*. End user should verify D2 and E2 dimensions according to the specific device application.
14. Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.
15. The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.
16. “N” is the max number of terminal positions for the specified body size.
17. Critical dimensions:
    a) Stand-Off
    b) Overall Width
    c) Lead Coplanarity
18. For symbols, recommended values and tolerances, see *Table 49*.

Figure 37. eTQFP100 leadframe pad design



Note: number, dimensions and positions of grooves are for reference only.

Table 49. eTQFP100 symbol definitions

Symbol	Definition	Notes
aaa	The tolerance that controls the position of the terminal pattern with respect to Datum A and B. The center of the tolerance zone for each terminal is defined by basic dimension e as related to Datum A and B.	For flange-molded packages, this tolerance also applies for basic dimensions D1 and E1. For packages tooled with intentional terminal tip protrusions, aaa does not apply to those protrusions.
bbb	The bilateral profile tolerance that controls the position of the plastic body sides. The centers of the profile zones are defined by the basic dimensions D and E.	—
ccc	The unilateral tolerance located above the seating plane where in the bottom surface of all terminals must be located.	This tolerance is commonly know as the “coplanarity” of the package terminals.
ddd	The tolerance that controls the position of the terminals to each other. The centers of the profile zones are defined by basic dimension e.	This tolerance is normally compounded with tolerance zone defined by “b”.

5.3 eTQFP144 package information

Refer to *Section 5.3.1: Package mechanical drawings and data information* for full description of below figures and table notes.

Figure 38. eTQFP144 package outline

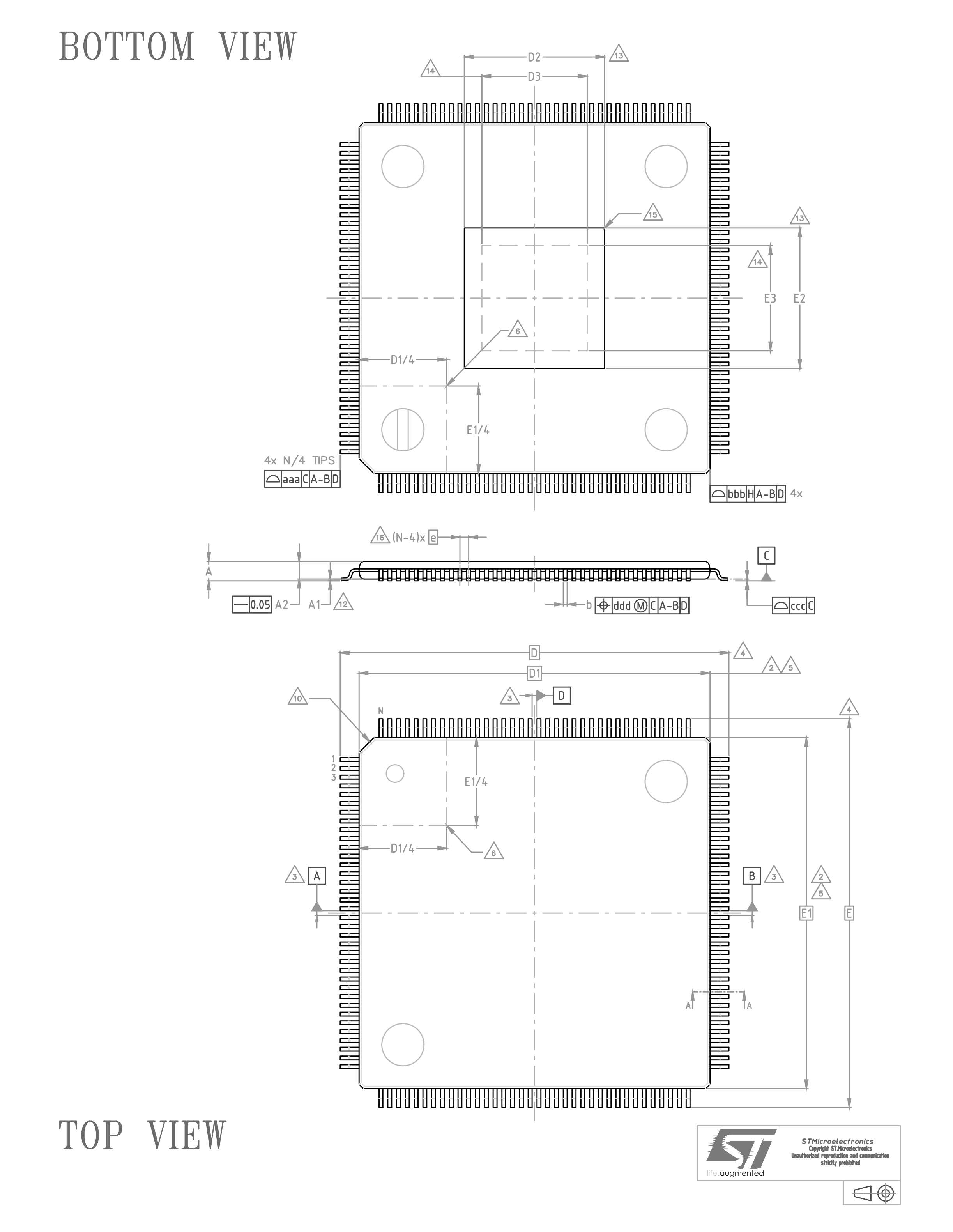


Figure 39. eTQFP144 section A-A

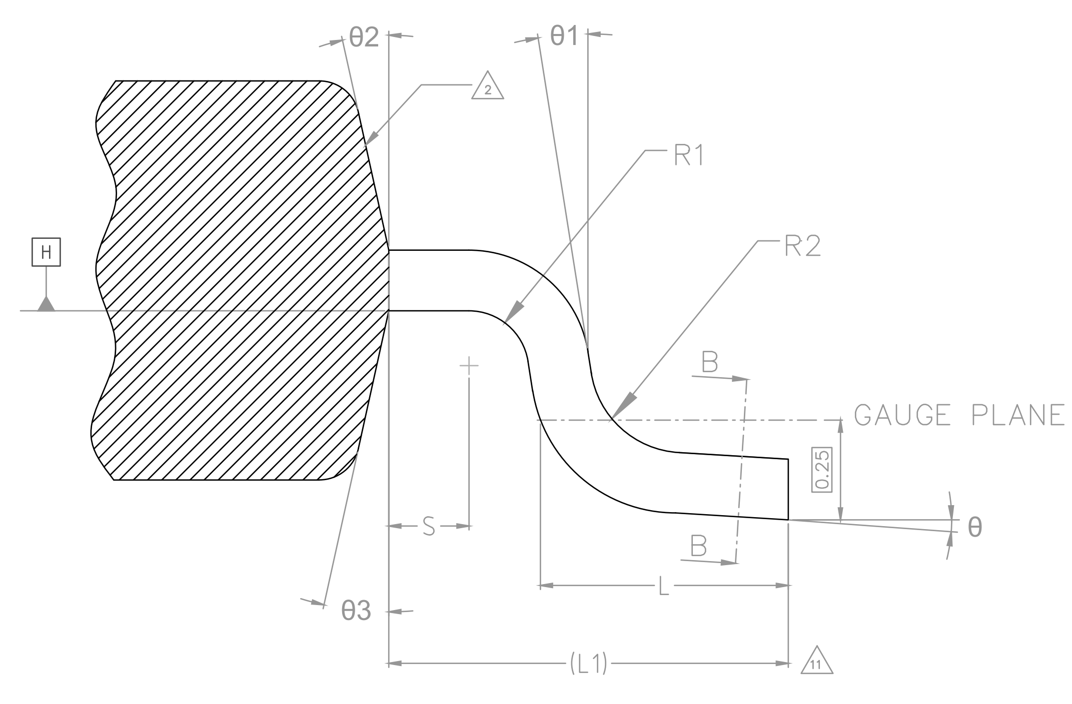


Figure 40. eTQFP144 section B-B

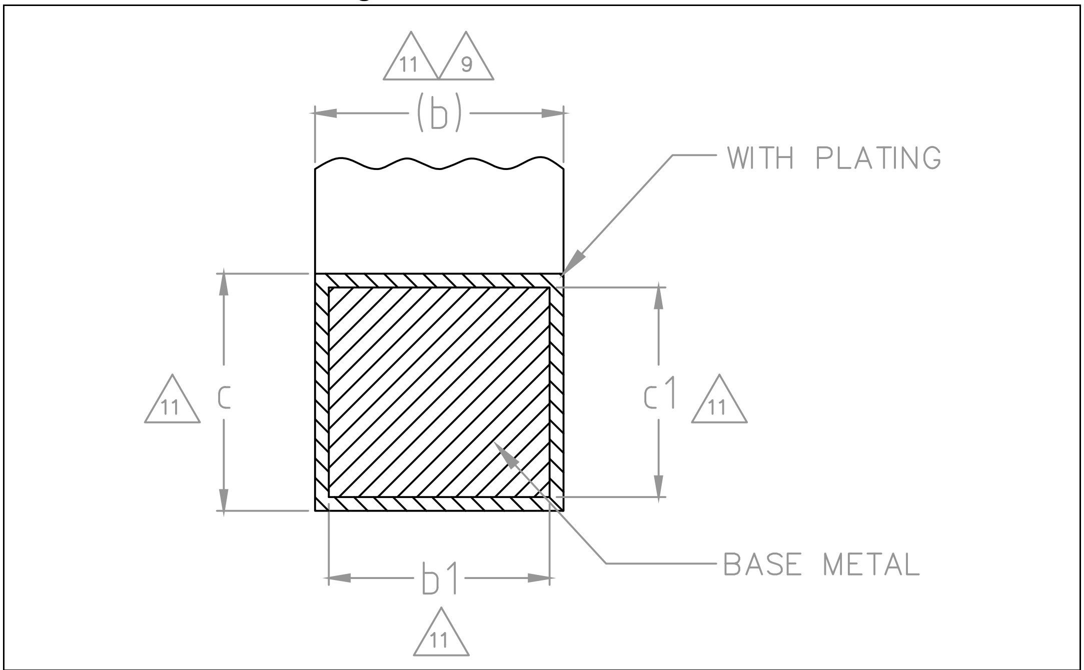


Table 50. eTQFP144 package mechanical data

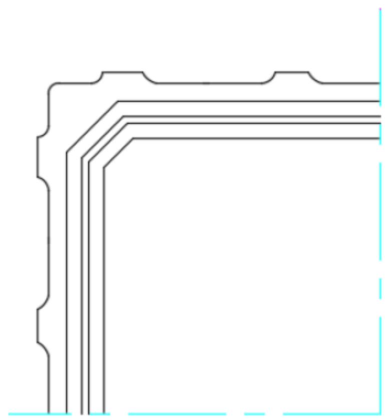
Symbol	Dimensions[7],[17]		
	Min.	Typ.	Max.
θ	0.0°	3.5°	7.0°
θ1	0.0°	—	—
θ2	10.0°	12.0°	14.0°
θ3	10.0°	12.0°	14.0°
A[15]	—	—	1.20
A1[12]	0.05	—	0.15
A2[15]	0.95	1.00	1.05
b[8],[9],[11]	0.17	0.22	0.27
b1[11]	0.17	0.20	0.23
c[11]	0.09	—	0.20
c1[11]	0.09	—	0.16
D[4]	—	22.00 BSC	—
D1[2],[5]	—	20.00 BSC	—
D2[13]	—	—	6.77
D3[14]	5.10	—	—
E[4]	—	22.00 BSC	—
E1[2],[5]	—	20.00 BSC	—
E2[13]	—	—	6.77
E3[14]	5.10	—	—
e	0.50 BSC		
L	0.45	0.60	0.75
L1	—	1.00 REF	—
N[16]	144		
R1	0.08	—	—
R2	0.08	—	0.20
S	0.20	—	—
aaa[1],[18]	0.20		
bbb[1],[18]	0.20		
ccc[1],[18]	0.08		
ddd[1],[18]	0.08		

5.3.1 Package mechanical drawings and data information

The following notes are related to *Figure 38*, *Figure 39*, *Figure 40* and *Table 50*:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All dimensions are in millimeter except where explicitly noted.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located (if present). It includes all metal protrusions from exposed pad itself. Type of exposed pad on SPC582Bx is as *Figure 41*. End user should verify D2 and E2 dimensions according to the specific device application.
14. Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.
15. The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.
16. “N” is the max number of terminal positions for the specified body size.
17. Critical dimensions:
    a) Stand-Off
    b) Overall Width
    c) Lead Coplanarity
18. For symbols, recommended values and tolerances, see *Table 51*.

Figure 41. eTQFP144 leadframe pad design



Note: number, dimensions and positions of grooves are for reference only.

Table 51. eTQFP144 symbol definitions

Symbol	Definition	Notes
aaa	The tolerance that controls the position of the terminal pattern with respect to Datum A and B. The center of the tolerance zone for each terminal is defined by basic dimension e as related to Datum A and B.	For flange-molded packages, this tolerance also applies for basic dimensions D1 and E1. For packages tooled with intentional terminal tip protrusions, aaa does not apply to those protrusions.
bbb	The bilateral profile tolerance that controls the position of the plastic body sides. The centers of the profile zones are defined by the basic dimensions D and E.	—
ccc	The unilateral tolerance located above the seating plane where in the bottom surface of all terminals must be located.	This tolerance is commonly know as the “coplanarity” of the package terminals.
ddd	The tolerance that controls the position of the terminals to each other. The centers of the profile zones are defined by basic dimension e.	This tolerance is normally compounded with tolerance zone defined by “b”.

5.4 QFN48 package information

Refer to *Section 5.4.1: Package mechanical drawings and data information* for full description of below figures and table notes.

Figure 42. QFN48 package outline

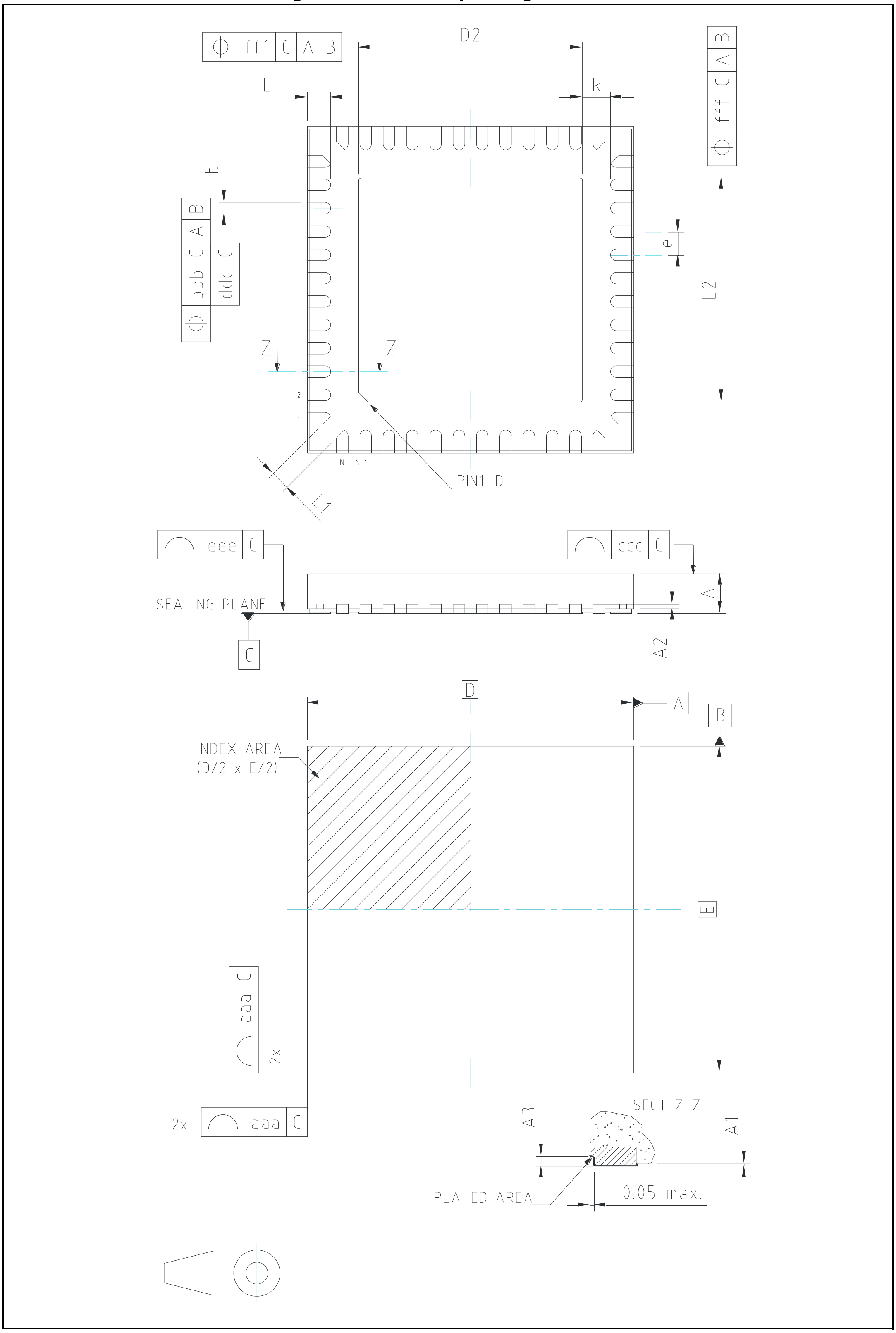


Table 52. QFN48 package mechanical data

Symbol	Dimensions		
	Min.	Typ.	Max.
A(4)	0.80	0.90	1.00
A1(11)	0.00	0.02	0.05
A2	0.2 REF		
A3(11)	0.10	—	—
b(4),(9)	0.20	0.25	0.30
D(4)	—	7.00	—
D2	4.70	4.80	4.90
e(4)	—	0.5	—
E(4)	—	7.00	—
E2	4.70	4.80	4.90
L(4)	0.45	0.50	0.55
L1(4)	0.35	—	—
N(4)	48		
k	0.25	—	—
aaa(1),(4)	0.15		
bbb(1),(4)	0.10		
ccc(1),(4)	0.08		
ddd(1),(4)	0.05		
eee(1),(4)	0.10		

5.4.1 Package mechanical drawings and data information

The following notes are related to *Figure 42* and *Table 52*:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size by much as 0.15 mm.
3. Datum A-B and D to be determined at datum plane H.
4. To be determined at setting datum plane C.
5. Detail of pin 1 identifier are optional but must be located within the zone indicated.
6. All Dimensions are in millimeters.
7. No intrusion allowed inwards the leads.
8. Exact shape of each corner is optional.
9. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
10. A1 is defined as the distance from the seating plane to the lowest point on the package body.
11. The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.
12. “N” is the max number of terminal positions for the specified body size.
13. For Tolerance of Form and Position see Table.
14. Critical dimensions:
    a) A
    b) A1
    c) A3
    d) D & E
    e) b & L
    f) D2 & E2
15. For Symbols, recommended values and tolerances see table below: (ACCORDING TO PACKAGE OR JEDEC SPEC IF REGISTERED)

Table 53. QFN48 symbol definitions

Symbol	Definition	Notes
aaa	The tolerance that controls the position of the terminal pattern with respect to Datum A and B. The center of the tolerance zone for each terminal is defined by basic dimension e as related to Datum A and B.	For flange-molded packages, this tolerance also applies for basic dimensions D1 and E1. For packages tooled with intentional terminal tip protrusions, aaa does not apply to those protrusions.
bbb	The bilateral profile tolerance that controls the position of the plastic body sides. The centers of the profile zones are defined by the basic dimensions D and E.	—
ccc	The unilateral tolerance located above the seating plane where in the bottom surface of all terminals must be located.	This tolerance is commonly known as the “coplanarity” of the package terminals.
ddd	The tolerance that controls the position of the terminals to each other. The centers of the profile zones are defined by basic dimension e.	This tolerance is normally compounded with tolerance zone defined by “b”.

5.5 Package thermal characteristics

The following tables describe the thermal characteristics of the device. The parameters in this chapter have been evaluated by considering the device consumption configuration reported in the *Section 4.7: Device consumption*.

5.5.1 eTQFP64

Table 54. Thermal characteristics for 64 exposed pad eTQFP package

Symbol		C	Parameter[1]	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2]	Four layer board (2s2p)	43.9	°C/W
$R_{\theta JB}$	CC	D	Junction-to-board[3]	—	23.8	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-case top[4]	—	28.9	°C/W
$R_{\theta JCbottom}$	CC	D	Junction-to-case bottom[5]	—	12.8	°C/W
Ψ_{JT}	CC	D	Junction-to-package top[6]	Natural convection	11.5	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
3. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
5. Thermal resistance between the die and the exposed pad ground on the bottom of the package based on simulation without any interface resistance.
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

5.5.2 eTQFP100

Table 55. Thermal characteristics for 100 exposed pad eTQFP package

Symbol		C	Parameter[1]	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2]	Four layer board (2s2p)	43.3	°C/W
$R_{\theta JB}$	CC	D	Junction-to-board[3]	—	26.1	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-case top[4]	—	27	°C/W
$R_{\theta JCbottom}$	CC	D	Junction-to-case bottom[5]	—	12.6	°C/W
Ψ_{JT}	CC	D	Junction-to-package top[6]	Natural convection	11.4	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
3. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
5. Thermal resistance between the die and the exposed pad ground on the bottom of the package based on simulation without any interface resistance.

6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

5.5.3 QFN48

Table 56. Thermal characteristics for QFN48 package

Symbol		C	Parameter[1]	Conditions	Value[2]	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[3]	Four layer board (2s2p)	43.9	°C/W
$R_{\theta JB}$	CC	D	Junction-to-board[4]	—	28.8	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-case top[5]	—	28.9	°C/W
$R_{\theta JCbottom}$	CC	D	Junction-to-case bottom[6]	—	22.5	°C/W
Ψ_{JT}	CC	D	Junction-to-package top[7]	Natural convection	11.5	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. These values are preliminary, therefore they are subject to change.
3. Per JEDEC JESD51 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the top case surface in ideal contact and measured by cold plate as per JEDEC best practice guidelines (JESD51-12).
6. Thermal resistance between the die and the bottom case surface in ideal contact and measured by cold plate as per JEDEC best practice guidelines (JESD51-12).
7. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

5.5.4 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

Equation 1

$$T_J = T_A + (R_{\theta JA} * P_D)$$

where:

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The thermal resistance values used are based on the JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The differences between the values determined for the single-layer (1s) board compared to a four-layer board that has two signal layers, a power and a ground plane (2s2p), demonstrate that the effective thermal resistance is not a constant. The thermal resistance depends on the:

- Construction of the application board (number of planes)
- Effective size of the board which cools the component
- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leaves the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single-layer board is within the normal range for the tightly packed printed circuit board. The value obtained on a board with the internal planes is usually within the normal range if the application board has:

- One oz. (35 micron nominal thickness) internal planes
- Components are well separated
- Overall power dissipation on the board is less than 0.02 W/cm^2

The thermal performance of any component depends on the power dissipation of the surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

Equation 2

$$T_J = T_B + (R_{\theta JB} * P_D)$$

where:

T_B = board temperature for the package perimeter (°C)

$R_{\theta JB}$ = junction-to-board thermal resistance (°C/W) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, the junction temperature is predictable if the application board is similar to the thermal test condition, with the component soldered to a board with internal planes.

The thermal resistance is expressed as the sum of a junction-to-case thermal resistance plus a case-to-ambient thermal resistance:

Equation 3

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and is not affected by other factors. The thermal environment can be controlled to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where 90% of the heat flow is through the case to heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case thermal resistance describes when using a heat sink or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models. More accurate compact Flotherm models can be generated upon request.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature by measuring the temperature at the top center of the package case using the following equation:

Equation 4

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_T = thermocouple temperature on top of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and approximately 1 mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

When board temperature is perfectly defined below the device, it is possible to use the thermal characterization parameter (Ψ_{JPB}) to determine the junction temperature by measuring the temperature at the bottom center of the package case (exposed pad) using the following equation:

Equation 5

$$T_J = T_B + (\Psi_{JPB} \times P_D)$$

where:

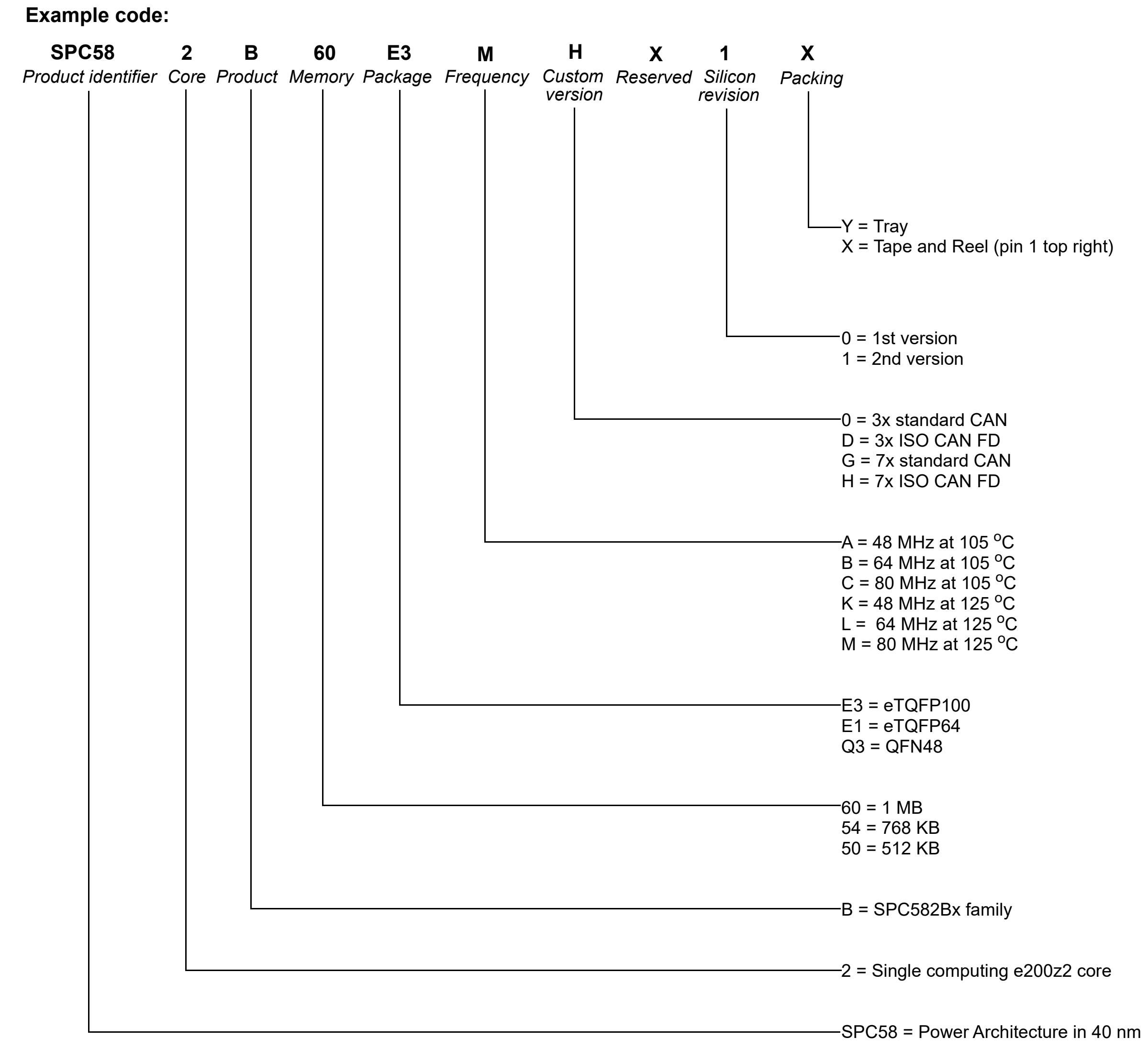
T_T = thermocouple temperature on bottom of the package (°C)

Ψ_{JT} = thermal characterization parameter (°C/W)

P_D = power dissipation in the package (W)

6 Ordering information

Figure 43. Ordering information scheme



Note: eTQFP144 package (SPC582B60E5-ENG) is available for emulation purpose only (with NEXUS port I/O).

Note: For the number of CAN Interfaces available by package, refer to the IO_Definition file.

Note: Please contact your ST sales office to ask for the availability of a particular commercial product.

Features (for instance, flash, RAM or peripherals) not included in the commercial product cannot be used.
ST cannot be called to take any liability for features used outside the commercial product.

Table 57. Code Flash options

SPC582B60 (1M)	SPC582B54 (768K)	SPC582B50 (512K)	Partition	Start address	End address
16	16	16	0	0x00FC0000	0x00FC3FFF
16	16	16	0	0x00FC4000	0x00FC7FFF
16	16	16	0	0x00FC8000	0x00FCBFFF
16	16	16	0	0x00FCC000	0x00FCFFFF
32	32	32	0	0x00FD0000	0x00FD7FFF
32	32	32	0	0x00FD8000	0x00FDFFFF
64	64	64	0	0x00FE0000	0x00FEFFFF
64	64	64	0	0x00FF0000	0x00FFFFFF
128	128	128	0	0x01000000	0x0101FFFF
128	128	128	0	0x01020000	0x0103FFFF
128	128	NA	0	0x01040000	0x0105FFFF
128	128	NA	0	0x01060000	0x0107FFFF
128	NA	NA	0	0x01080000	0x0109FFFF
128	NA	NA	0	0x010A0000	0x010BFFFF

Table 58. RAM options

SPC582B60	SPC582B54	SPC582B50	Type	Start address	End address
96(1)	80(1)	64(1)			
8	8	8	PRAMC_2 (STBY)	0x400A8000	0x400A9FFF
24	24	24	PRAMC_2 (STBY)	0x400AA000	0x400AFFFF
32	32	32	PRAMC_2 (STBY)	0x400B0000	0x400B7FFF
16	16	NA	PRAMC_2	0x400B8000	0x400BBFFF
16	NA	NA	PRAMC_2	0x400BC000	0x400BFFFF

1. Total KRAM (SRAM).

7 Revision history

Table 59. Document revision history

Date	Revision	Changes
07-April-2016	1	Initial version.
29-Jun-2017	2	The following are the changes in this version of the Datasheet. – Removed QFN32 package from the document. – Replaced RPNs SPC582B60E1, SPC582B60E3, and SPC582B60Q2 with “SPC582B60x, SPC582B54x, and SPC582B50x” *Table 1: Device summary*: – Updated the table. *Section 3.1: Introduction*: – Removed text “The IPs and...for the details”. – Removed the two notes. *Table 3: Parameter classifications*: – Updated the description of classification tag “T”. *Table 4: Absolute maximum ratings*: – For parameter “I_{INJ}”, text “DC” removed from description. – Added text “Exposure to absolute ... reliability” – Added text “even momentarily” – Updated values in conditions column. – Added parameter T_{TRIN}. – For parameter “T_{STG}”, maximum value updated from “175” to “125” – Added new parameter “T_{PAS}” – For parameter “I_{INJ}”, description updated from “maximum...PAD” to “maximum DC...pad” *Table 5: Operating Conditions*: – Footnote “1.260 V - 1.290 V range .. temperature profile” updated to Text “... average supply value below or equal to 1.236 V ...” – For parameter “I_{INJ1}” description, text “DC” removed. – For parameter “V_{DD_LV}”, changed the classification from “D” to “P” – Removed note “Core voltage as ....” – Added parameter I_{INJ2}. – Removed parameter “V_{RAMP_LV}”. – Updated the table footnote “Positive and negative Dynamic current....” *Table 6: Device supply relation during power-up/power-down sequence*: – “$V_{DD\_HV\_PMC}$” updated to “$V_{DD\_HV\_OSC}$”. – Parameter “V_{DD_LV}” removed *Section 3.4: Electromagnetic emission characteristics*: – Updated this section.

Table 59. Document revision history (continued)

Date	Revision	Changes
29-Jun-2017	2 (cont')	*Table 8: Device consumption*: – Updated the table and its values. *Section 3.8.2: I/O output DC characteristics*: – "WEAK" to "WEAK/SLOW" – "STRONG" to "STRONG/FAST" – "VERY STRONG" to "VERY STRONG / VERY FAST" – Added note "10%/90% is the...." *Table 14: I/O input electrical characteristics*: – Parameter "I_{LKG}" (Medium Pads (P), TJ=150°C/360 mA) removed. *Table 11: I/O pull-up/pull-down electrical characteristics*: – Added note "When the device enters into standby mode... an ADC function." *Table 12: WEAK/SLOW I/O output characteristics*: – Added "10%-90% in description of parameter "t_{TR_W}". – For parameter "F_{max_W}", updated condition "25 pF load" to "CL=25pF" – For parameter "t_{TR_S}", changed min value (25 pF load) from "4" to "3" – Changed min value (50 pF load) from "6" to "5" – For parameter "$\|t_{SKEW\_W}\|$", changed max value from "30" to "25". *Table 13: MEDIUM I/O output characteristics*: – Added "10%-90% in description of parameter "t_{TR_M}". – For parameter "$\|t_{SKEW\_W}\|$", changed max value from "30" to "25". *Table 14: STRONG/FAST I/O output characteristics*: – Added "10%-90% in description of parameter "t_{TR_S}". – Parameter "I_{DCMAX_S}" updated: – Condition added "V_{DD}=5V±10% – Condition added "V_{DD}=3.3V±10%, Max value updated to 5.5mA – For parameter "$\|t_{SKEW\_W}\|$", changed max value from "30" to "25". *Table 16: I/O consumption*: – Updated all the max values of parameters I_{DYN_W} and I_{DYN_M} *Section 3.8.3: I/O pad current specifications*: – Replaced all occurences of "50 pF load" with "CL=50pF". – Removed note "The external ballast...." *Table 19: PLL0 electrical characteristics*: – For parameter "I_{PLL0}", classification changed from "C" to "T". – Footnote "Jitter values...measurement" added for parameters: – $\|\Delta_{PLL0PHI0SPJ}\|$ – $\|\Delta_{PLL0PHI1SPJ}\|$ – $\Delta_{PLL0LTJ}$ *Table 20: PLL1 electrical characteristics*: – For parameter "I_{PLL1}", classification changed from "C" to "T". – Footnote "Jitter values...measurement" added for parameter "$\|\Delta_{PLL1PHI0SPJ}\|$" – Removed figure "Test circuit"

Table 59. Document revision history (continued)

Date	Revision	Changes
29-Jun-2017	2 (cont')	*Table 21: External 40 MHz oscillator electrical specifications*: – Footnote "I_{xatl} is the oscillator...Test circuit is shown in Figure 8" modified to "I_{xatl} is the oscillator...startup of the oscillator". – Minimum value of parameter "V_{IHEXT}" updated from "V_{REF}+0.6" to "V_{REF}+0.75" – Maximum value of parameter "V_{ILEXT}" updated from "V_{REF}-0.6" to "V_{REF}-0.75" – Parameter "g_m", value "D" updated to "P" for "$f_{XTAL} \leq$ 8 MHz", and "D" for others. – Footnote "This parameter is...100% tested" updated to "Applies to an...to crystal mode". Also added to parameter "V_I – For parameters "V_{IHEXT}" and "V_{ILEXT}", Condition "–" updated to "V_{REF} = 0.29 * $V_{DD\_HV\_OSC}$" – Classification for parameters "C_{S_EXTAL}" and "C_{S_EXTAL}" changed from "T" to "D". – Updated classification, conditions, min and max values for parameter "g_m". – Min and Max value of parameters C_{S_EXTAL} and C_{S_XTAL} updated to "3" (min) and "7" (max). Renamed the section "RC oscillator 1024 kHz" to *Section 3.11.3: Low power RC oscillator* *Table 22: Internal RC oscillator electrical specifications*: – For parameter "I_{FIRC}", replaced max value of 300 with 600. – Added footnote to the description. – For parameter $I_{FIRC,}$ changed the max value to 600 and added footnote. – Min, Typ and Max value of "δf_{var_SW}" updated from "-1", "-", "1" to "-0.5", "$\pm$0.3" and "0.5" respectively. *Table 23: 1024 kHz internal RC oscillator electrical characteristics*: – For parameter "δf_{var_V}", minimum and maximum value updated from "-0.05" and "+0.05" to "-5" and "+5". – For parameter "δf_{var_T}", and "δf_{var_V} " changed the cassification to "P". *Table 24: ADC pin specification*: – For I_{LKG}, changed condition "C" to "—". – For parameter C_{P2}, updated the max value to "1". *Table 25: SARn ADC electrical specification*: – Classification for parameter "$I_{ADCREFH}$" changed from "C" to "T". – For parameter f_{ADCK} (High frequency mode), changed min value from "7.5" to "> 13.33". – Deleted footnote "Values are subject to change (possibly improved to ±2 LSB) after characterization" *Table 28: Linear regulator specifications*: – Updated the min and typ values of parameter V_{MREG} (After trimming, maximum load).

Table 59. Document revision history (continued)

Date	Revision	Changes
29-Jun-2017	2 (cont')	*Table 29: Standby regulator specifications*: – Updated the min and max values for parameter V_{SBY}. – For parameter $IDD_{SBY,}$ added "0.984" to typ column. *Table 30: Voltage monitor electrical characteristics*: – Updated the Typ value of parameter V_{POR200_C} – Updated the min, typ, and max values of parameter $V_{LVD100\_SB,}$. – Updated the min and max values for parameter $V_{MVD270\_SBY.}$ – Removed "PowerOn Reset LV" Updated *Section 3.14: Flash* Updated *Figure 8: Input equivalent circuit (Fast SARn and SARB channels)* Updated *Figure 22: DSPI CMOS master mode — classic timing, CPHA = 1* *Table 35: Nexus debug port timing*: – Classification of parameters "t_{EVTIPW}" and "t_{EVTOPW}" changed from "P" to "D". *Table 38: DSPI CMOS master classic timing (full duplex and output only) — MTFE = 0, CPHA = 0 or 1*: – Changed the Min value of t_{SCK} (very strong) from 33 to 59. Added *Section 3.15.3: CAN timing* *Table 46: eTQFP64 package mechanical data*: – Updated the values. *Table 47: eTQFP100 package mechanical data*: – Updated the values. *Table 48: eTQFP144 package mechanical data*: – Updated the values. *Table 37: DSPI channel frequency support*: – Added column to show slower and faster frequencies.. *Table 49: Thermal characteristics for 64 exposed pad eTQFP package*: – Removed parameter $R_{\theta JMA}$. *Table 50: Thermal characteristics for 100 exposed pad eTQFP package*: – Removed parameter $R_{\theta JMA}$. – Updated the values of all the parameters. *Table 51: Thermal characteristics for 144 exposed pad eTQFP package*: – Removed parameter $R_{\theta JMA}$.

Table 59. Document revision history (continued)

Date	Revision	Changes
04-Jun-2018	3	The following are the changes in this version of the Datasheet. Replaced reference to IO_definition excel file by “the device pin out IO definition excel file”, throughout the document. Minor formatting changes throughout the document. *Section 2: Package pinouts and signal descriptions*: Changed introduction sentence since the pinout excel file will no longer be attached to the Datasheet. *Table 6: Device supply relation during power-up/power-down sequence*: Added a note “The application.....” to parameter $V_{DD\_HV\_OSC}$ *Table 8: Device consumption*: – “I_{DD_LKG}”: added footnote “I_{DD_LKG} and I_{DD_LV} are reported as...” – “I_{DD_LV}”: added Footnote “I_{DD_LKG} and I_{DD_LV} are reported as...” – Updated table footnote 4. – Updated all the typical and maximum values for I_{DD_LKG}, $I_{DDSTBY8}$, and $I_{DDSTBY64}$ parameters. *Table 9: I/O pad specification descriptions*: Removed latest sentence at Standby pads description. *Table 14: STRONG/FAST I/O output characteristics*: Updated values for t_{TR_S} for condition CL = 25 pF and CL = 50 pF *Table 15: VERY STRONG/VERY FAST I/O output characteristics*: – “tTR20-80” replaced by “tTR20-8_V” – “tTRTTL” replaced by “tTRTTL_V” – “$\Sigma t_{TR20-80}$” replaced by “$\Sigma t_{TR20-80\_V}$” *Table 19: PLL0 electrical characteristics*: – Added “f_{INFIN}” – Symbol “f_{INFIN}” : changed “C” by “—” in column “C” – $\lvert\Delta_{PLL0PHI0SPJ}\rvert$: changed “T” by “D” and added pk-pk to Conditions value – $\lvert\Delta_{PLL0PHI1SPJ}\rvert$: added pk-pk to Conditions value – The maximum value of $f_{PLL0PHI0}$ is changed from “400” to “FSYS” with a footnote. *Table 20: PLL1 electrical characteristics*: Added “f_{INFIN}”. *Table 21: External 40 MHz oscillator electrical specifications*: – Changed “i.e.” by “that is” in note “Amplitude on the EXTAL... – Changed table footnote 3 by: This value is determined by the crystal manufacturer and board design, and it can potentially be higher than the maximum provided. – Table footnote 1 updated: “DCF clients XOSC_LF_EN and XOSC_EN_40MHZ” changed by “XOSC_FREQ_SEL”

Table 59. Document revision history (continued)

Date	Revision	Changes
04-Jun-2018	3 (cont'd)	*Table 24: ADC pin specification*: – Updated Max value for C_S – For parameter C_{P2}, updated the max value from "1" to "2". – Changed Max value = 1 by 2 for Cp2 SARB channels *Table 25: SARn ADC electrical specification*: – Added symbols tADCINIT and tADCBIASINIT – Column "C" splitted and added "D" for I_{ADV_S} *Figure 11: Voltage monitor threshold definition*: Right blue line adjusted on the top figure. *Section 3.13.1: Power management integration*: Added sentence "It is recommended...device itself". *Table 28: Linear regulator specifications*: Updated values for symbol "ΔIDD_{MREG}", Min: 50 changed to -50. *Section 3.14: Flash*: Updated the section. *Table 41: CAN timing*: Added columns for "CC" and "D". *Section 4.4: Package thermal characteristics*: Removed table "Thermal characteristics for 144 exposed pad eTQFP package" *Figure 33: Ordering information scheme*: For Packing, replaced "R" with "X" and removed description related to "R". Updated the description of "X". Added *Table 52: RAM options* and *Table 51: Code Flash options*.
01-Dec-2020	4	The following are the changes in this version of the Datasheet. Minor formatting changes throughout the document. Updated Title of the document Updated the sub-title of the document Added picture and dimension for QFN48 Updated *Table 1: Device summary* Updated *Chapter 1: Introduction*: Removed "Document overview" section title. Updated section 1.2 Description to *Chapter 2: Description* *Chapter 4: Electrical characteristics* *Section 4.2: Absolute maximum ratings* *Table 4: Absolute maximum ratings*: – Added cross reference to footnote *2.* to all $V_{DD\_HV^*}$ and V_{IN} – Removed Symbol $V_{DD\_HV\_IO\_FLEX}$ for Parameter "I/O supply voltage"

Table 59. Document revision history (continued)

Date	Revision	Changes
01-Dec-2020	4 (Cont'd)	*Section 4.3: Operating conditions* *Table 5: Operating conditions*: – $V_{DD\_HV\_ADR\_S}$: removed line for C condition.: – T_J: changed value in column C from "P" to "C". – Removed Symbol $V_{DD\_HV\_IO\_FLEX}$ for Parameter "I/O supply voltage" *Section 4.5: Electromagnetic compatibility characteristics* Updated section title from Electromagnetic emission characteristics to Electromagnetic compatibility characteristics. Updated *Section 4.6: Temperature profile* *Section 4.7: Device consumption* *Table 8: Device consumption*: move table footnote *1.* from table title to "Value". *Section 4.9: Reset pad (PORST) electrical characteristics* *Figure 5: Startup Reset requirements*: deleted V_{DDMIN} *Section 4.10: PLLs* *Section 4.10.1: PLL0* *Table 19: PLL0 electrical characteristics*: changed condition from T to D for $\|\Delta_{PLL0PHI1SPJ}\|$, $\Delta_{PLL0LTJ}$ and I_{PLL0}. *Section 4.10.2: PLL1* *Table 20: PLL1 electrical characteristics*: changed condition from T to D for I_{PLL1} *Section 4.11: Oscillators* *Section 4.11.2: RC oscillator 16 MHz* *Table 22: Internal RC oscillator electrical specifications*: – updated Max value for I_{FIRC}. – Updated *2.* *Section 4.12: ADC system* *Figure 8: Input equivalent circuit (Fast SARn and SARB channels)*: added parameter "C_{EXT}: external capacitance" and component to scheme. *Table 24: ADC pin specification*: added row for symbol "C_{EXT} / SR" Updated *Section 4.12.1: ADC input description* Updated *Section 4.12.2: SAR ADC 12 bit electrical specification* *Section 4.13: Power management* *Section 4.13.1: Power management integration* *Table 27: External components integration*: – Updated Conditions for C_{BV}. – Updated notes content and numbering

Table 59. Document revision history (continued)

Date	Revision	Changes
01-Dec-2020	4 (Cont'd)	– Updated Min value for R_E – Updated Typ value for C_{LVN} – Added note 2 for C_{FLA} – Added note 6 for C_{ADC} *Section 4.13.3: Voltage monitors* *Table 30: Voltage monitor electrical characteristics*: added footnote "Even if LVD/HVD..." *Section 4.14: Flash* Updated *Table 31: Wait State configuration* Updated *Table 32: Flash memory program and erase specifications* Updated *Table 33: Flash memory Life Specification* *Section 4.15: AC Specifications* Updated *Figure 22: DSPI CMOS master mode — classic timing, CPHA = 1* *Chapter 5: Package information* Added introduction sentence in each Package section. Added sub-section "Package mechanical drawings and data information" and introduction sentence to the notes list. *Table 45: Package case numbers*: removed package reference column. *Figure 30: eTQFP64 package outline*: updated. *Figure 31: eTQFP64 section A-A*: added this figure. *Figure 32: eTQFP64 section B-B*: added this figure. *Table 46: eTQFP64 package mechanical data*: updated table, notes content and numbering. Moved notes to new section *Section 5.1.1: Package mechanical drawings and data information* *Figure 33: eTQFP64 leadframe pad design*: added this figure. *Table 47: eTQFP64 symbol definitions*: added this table. *Figure 34: eTQFP100 package outline*: updated. *Figure 35: eTQFP100 section A-A*: added this figure. *Figure 36: eTQFP100 section B-B*: added this figure. *Table 48: eTQFP100 package mechanical data*: updated table, notes content and numbering. Moved notes to new section *Section 5.2.1: Package mechanical drawings and data information* *Table 49: eTQFP100 symbol definitions*: added this table. *Figure 37: eTQFP100 leadframe pad design*: added this figure. *Figure 38: eTQFP144 package outline*: updated figure. *Table 50: eTQFP144 package mechanical data*: updated table, notes content and numbering.

Table 59. Document revision history (continued)

Date	Revision	Changes
01-Dec-2020	4 (Cont'd)	Moved notes to new section *Section 5.3.1: Package mechanical drawings and data information* Added *Section 5.4: QFN48 package information* *Section 5.5: Package thermal characteristics* Added *Section 5.5.3: QFN48* *Chapter 6: Ordering information* *Figure 43: Ordering information scheme*: – Added figure footnote – For Package: added information for QFN48