SPF5043Z

50 MHz to 4000 MHz Low-Noise Amplifier

SOT-343 Package

General Description

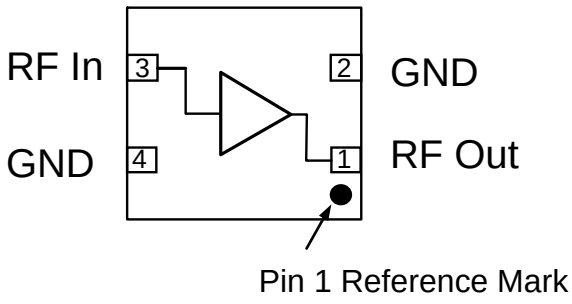
The SPF5043Z is a high-performance GaAs pHEMT MMIC LNA designed for operation from 50 MHz to 4000 MHz. The on-chip active bias network provides stable current over temperature and process threshold voltage variations.

The SPF5043Z offers ultra-low noise figure and high linearity performance in a gain block configuration. Its single-supply operation and integrated matching networks make implementation remarkably simple. The high maximum input power specification makes it ideal for high dynamic range receivers.

Product Features

- 0.8 dB Ultra-Low Noise Figure at 900 MHz
- 18.2 dB Gain at 900 MHz
- 35 dBm OIP3 High Linearity at 1900 MHz
- 22.7 dBm P1dB at 1900 MHz
- 3 V to 5 V Flexible, Single-Supply Operation
- 46mA I_{DQ}, Adjustable
- Broadband Internal Matching

Functional Block Diagram



Applications

- Cellular, PCS, W-CDMA, ISM and LTE
- Low Noise, High Linearity Gain Block Applications

Ordering Information

Part No.	Description
SPF5043Z	3000 pieces on a 7” Reel
SPF5043ZSR	100 pieces on a 7” Reel
SPF5043ZPCK1	400-3000 MHz EVB with 5pc sample bag

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−65°C to +150°C
Drain Voltage (V_D)	+5.5 V
Device Current, I_D	100 mA
Input Power (CW)	+25 dBm
Dissipated Power	330 mW

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_D	+4.75	+5	+5.25	V
Operating Temp. Range	−40		+85	°C
Junction Temperature (T_J)			150	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: V_D = +5 V, IDQ = 46 mA, Temp. = +25°C, 50Ω system, Qorvo broad application circuit

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		50		4000	MHz
Gain	900 MHz	16.7	18.2	19.7	dB
	1960 MHz	11.4	12.9	14.4	dB
Output P1dB	900 MHz	17.4	22.6		dBm
	1900 MHz		22.7		dBm
Output IP3	P_{OUT} -5 dBm/tone, Δf 1 MHz, 900MHz	30.0	33.0		dBm
	P_{OUT} -5 dBm/tone, Δf 1 MHz, 1900 MHz		35.0		dBm
Noise Figure	900 MHz		0.8	1.0	dB
	1900 MHz		0.8		dB
Reverse Isolation, |S12|	900 MHz		23.5		dB
	1900 MHz		19.0		dB
Input Return Loss	900 MHz	13.0	16.0		dB
	1900 MHz		17.5		dB
Output Return Loss	900 MHz	13.0	17.5		dB
	1900 MHz		16.5		dB
Drain Voltage, V_D			5	5.25	V
Drain Quiescent Current, I_{DQ}			46	54	mA
Thermal Resistance, θ_{jc}	Junction to case*		125		°C/W

*Ground Leads

Typical Performance – V_D +5 V Broadband Application Circuit

Test Conditions: V_D = +5 V, I_D = 46 mA, OIP3 Tone Spacing = 1 MHz & P_{OUT} 0 dBm/tone, T_{CASE} = 25°C, 50Ω system

Parameter	0.1GHz*	0.4GHz	0.9GHz	1.5GHz	1.9GHz	2.2GHz	2.5GHz	3.5GHz	3.8GHz	Unit
Small Signal Gain	23.5	21.6	18.2	14.8	13.1	11.9	10.8	8.0	7.0	dB
Noise Figure	0.65	0.61	0.74	0.82	0.78	0.84	0.96	1.34	1.49	dB
OIP3	30.5	31.0	33.0	34.5	35.0	35.5	36.5	38.5	37.5	dBm
Output P1dB	na	22.5	22.6	22.7	22.7	23.0	22.8	23.1	22.8	dBm
Input Return Loss	-13.0	-12.5	-15.5	-18.0	-17.5	-17.0	-16.0	-11.5	-10.5	dB
Output Return Loss	-22.0	-17.5	-20.0	-18.0	-17.0	-17.0	-16.5	-16.0	-13.5	dB
Reverse Isolation	-27.0	-26.0	-23.5	-20.5	-19.0	-18.0	-17.5	-15.0	-15.0	dB

*Tested with Bias Tee @ 100 MHz

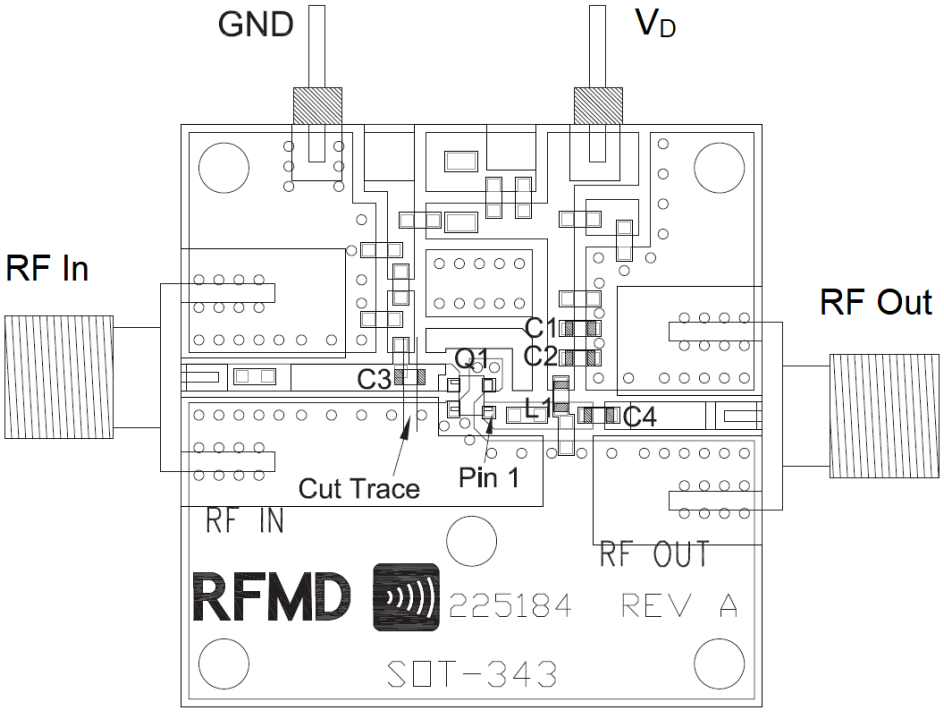
Typical Performance – V_D +3V Broadband Application Circuit

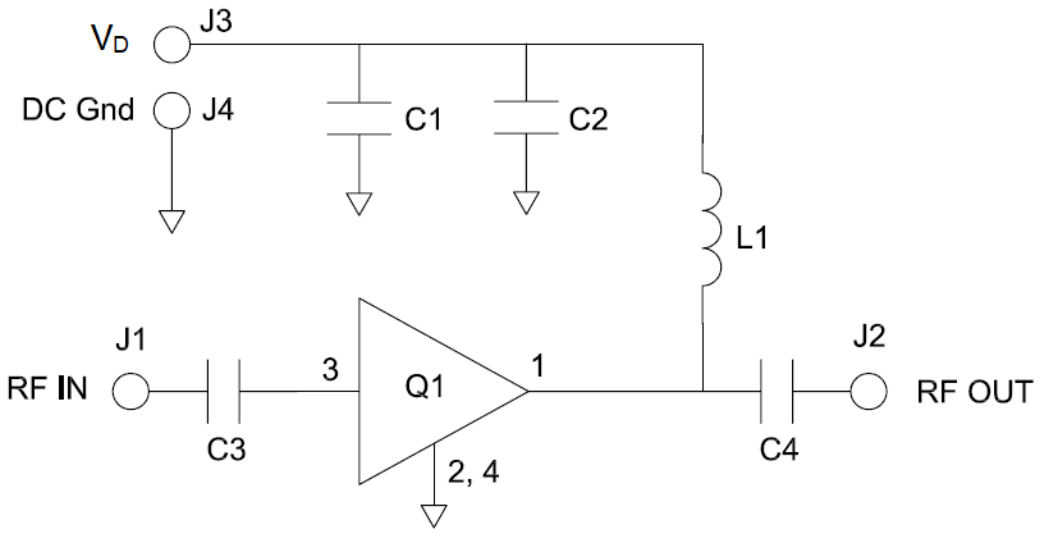
Test Conditions: V_D = +3 V, I_D = 25 mA, OIP3 Tone Spacing = 1 MHz & P_{OUT} 0 dBm/tone, T_{CASE} = 25°C, 50Ω system

Parameter	0.1GHz*	0.4GHz	0.9GHz	1.5GHz	1.9GHz	2.2GHz	2.5GHz	3.5GHz	3.8GHz	Units
Small Signal Gain	22.6	20.9	17.7	14.4	12.7	11.5	10.5	7.6	6.7	dB
Noise Figure	0.60	0.61	0.73	0.82	0.78	0.85	0.93	1.28	1.48	dB
OIP3	26.5	27.0	28.5	30.0	30.5	30.5	32.0	33.5	33.0	dBm
Output P1dB	na	19.3	19.5	19.9	20.0	20.3	20.2	20.3	19.7	dBm
Input Return Loss	-10.5	-11.0	-14.0	-16.5	-16.5	-16.0	-14.5	-10.5	-9.5	dB
Output Return Loss	-21.0	-21.5	-28.5	-24.5	-22.5	-22.5	-22.5	-20.0	-15.5	dB
Reverse Isolation	-26.0	-25.5	-22.5	-20.0	-18.0	-17.5	-16.5	-14.5	-14.0	dB

*Tested with Bias Tee @ 100 MHz

SPF5043ZPCK1 Evaluation Board Layout & Schematic





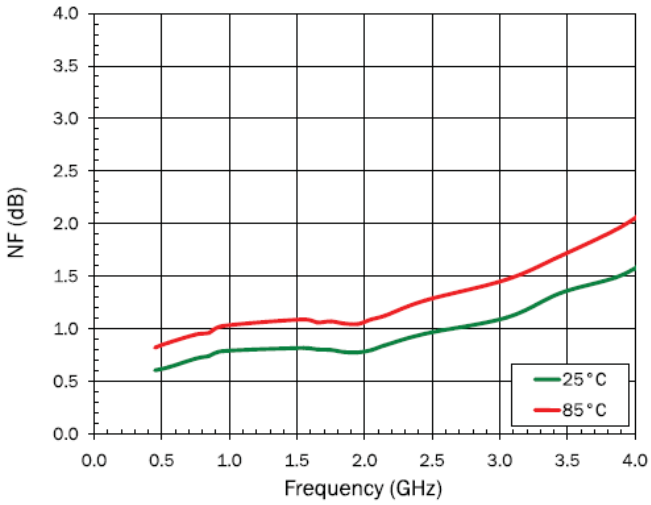
Bill of Material

Reference Des.	Value	Description	Manuf.	Part Number
Q1	n/a	LNA, 50MHz to 4000MHz Amp	Qorvo	SPF5043Z
C1	0.1 µF	CAP, 0.1 µF,10%, 16V, X7R, 0603	Murata	GRM188R71C104KA01D
C2, C3, C4	100 pF	CAP, 100 pF, 5%, 50V, C0G, 0603	Murata	GRM1885C1H101JA01D
L1	100 nH	IND, 100 nH, 5%, M/L, 0603	Toko	LL1608-FSLR10J

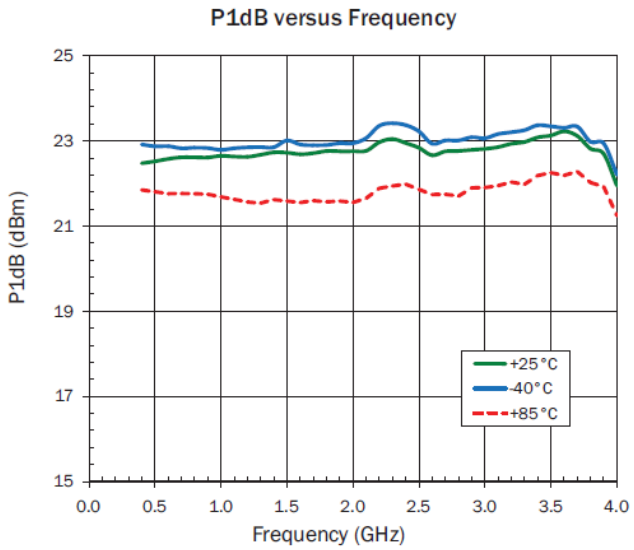
Performance Plots – V_D +5V

Test conditions unless otherwise noted: V_D = +5 V, I_D =46 mA

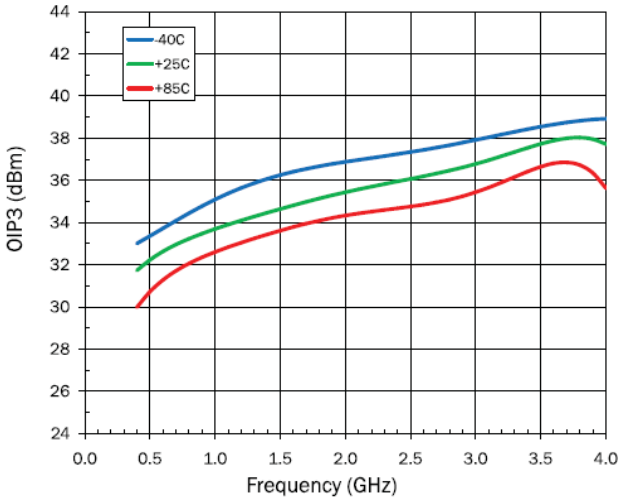
NF versus Frequency



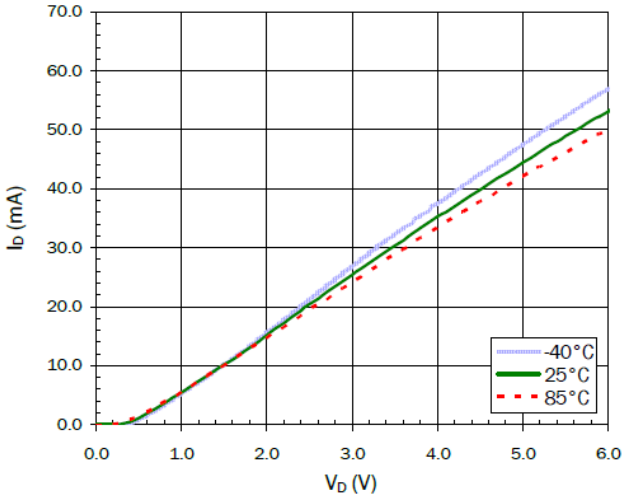
P1dB versus Frequency



OIP3 vs. Frequency (-5dBm/tone, 1MHz spacing)



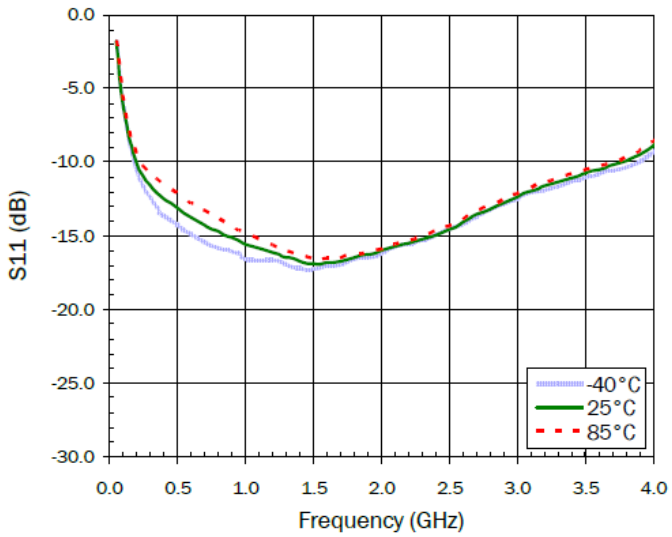
Device Current versus Voltage



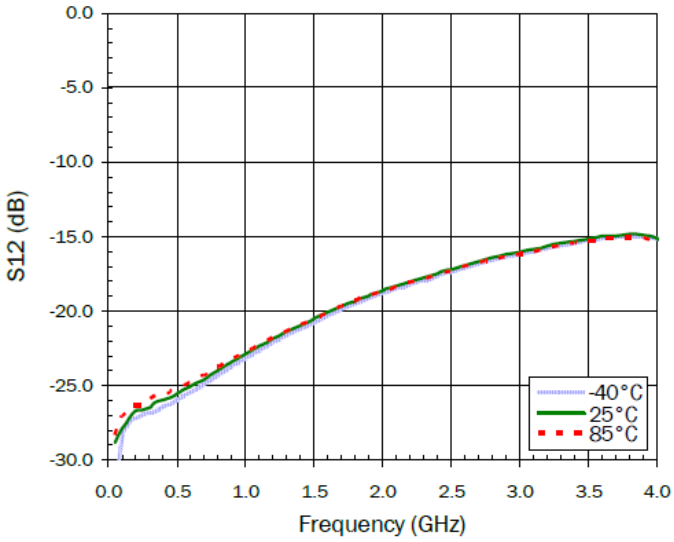
Performance Plots – V_D +5 V (Continue 1)

Test conditions unless otherwise noted: V_D = +5 V, I_D =46 mA

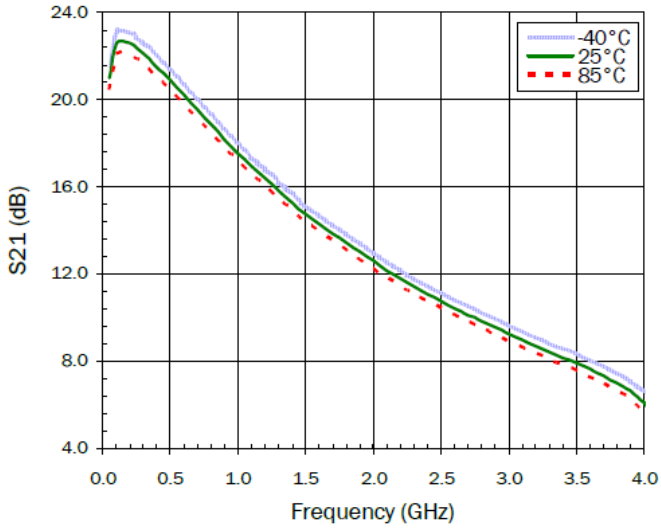
S11 versus Frequency



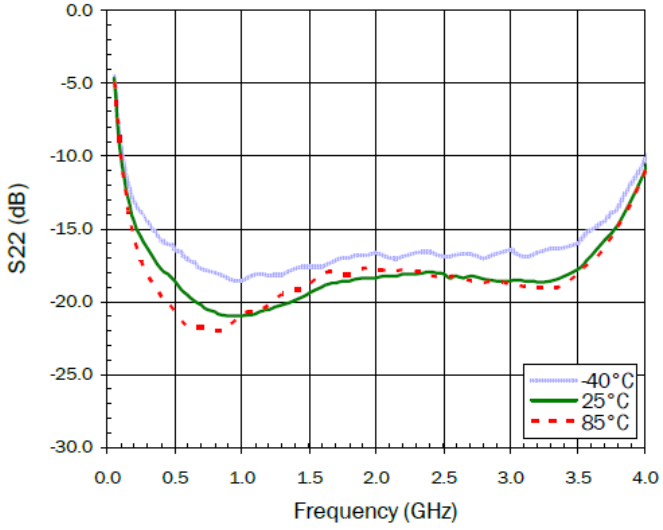
S12 versus Frequency



S21 versus Frequency



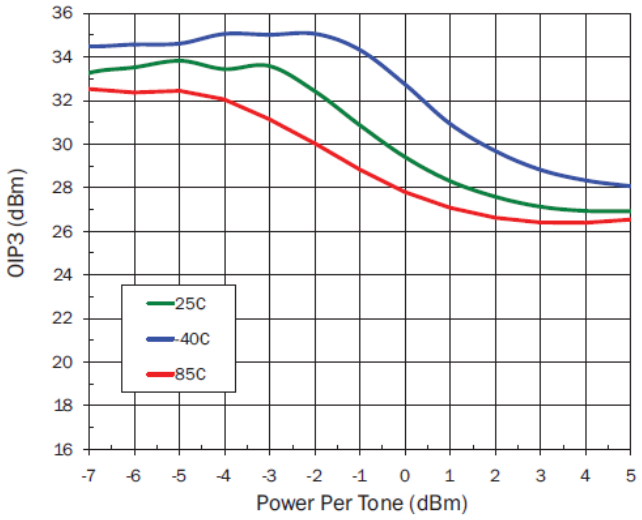
S22 versus Frequency



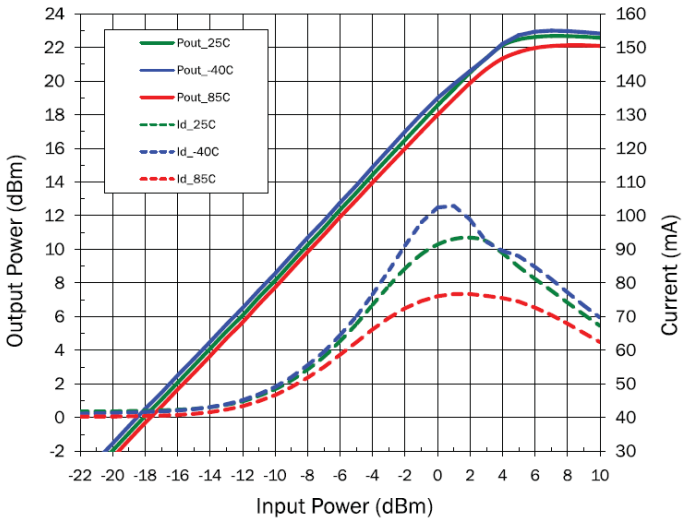
Performance Plots – V_D +5 V (Continue 2)

Test conditions unless otherwise noted: V_D = +5 V, I_D =46 mA, Temp.=+25°C

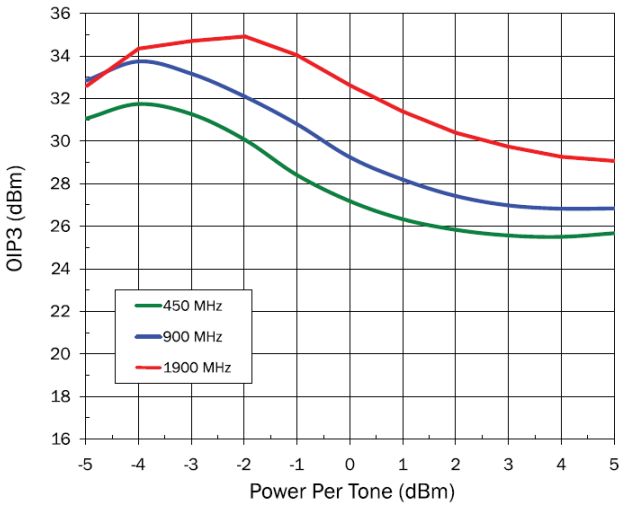
OIP3 versus Power Out (Vd = 5V, 900MHz)



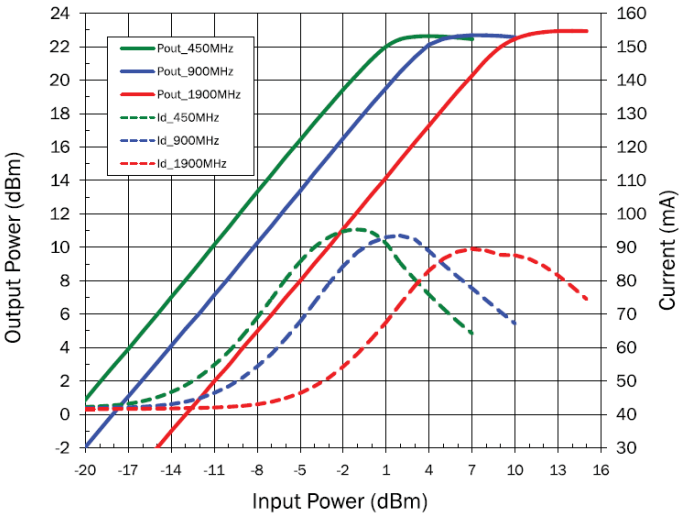
Output Power versus Input Power (Vd=5V, 900 MHz)



OIP3 versus Power Out (Vd = 5V, 25C)



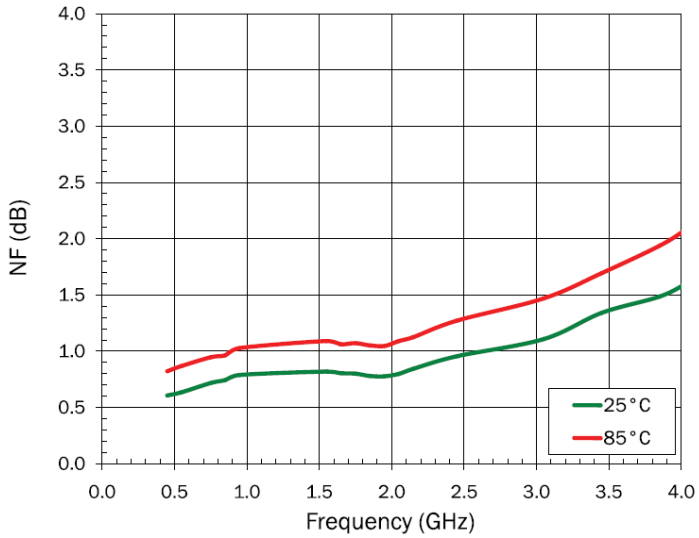
Output Power versus Input Power (Vd=5V)



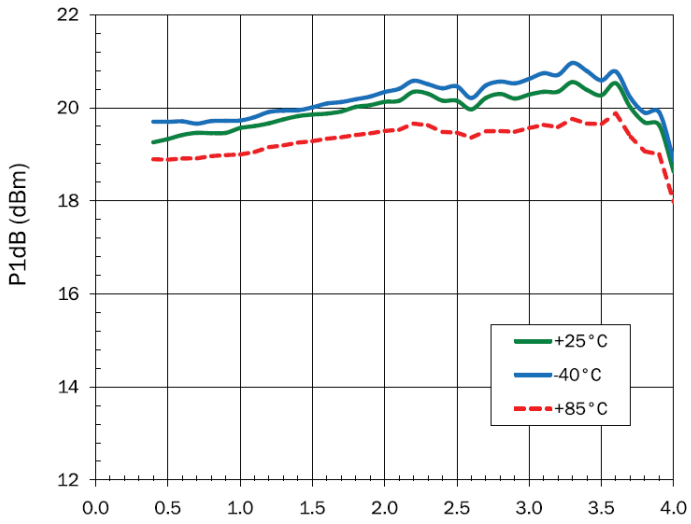
Performance Plots – V_D +3 V

Test conditions unless otherwise noted: V_D = +3 V, I_D =25 mA

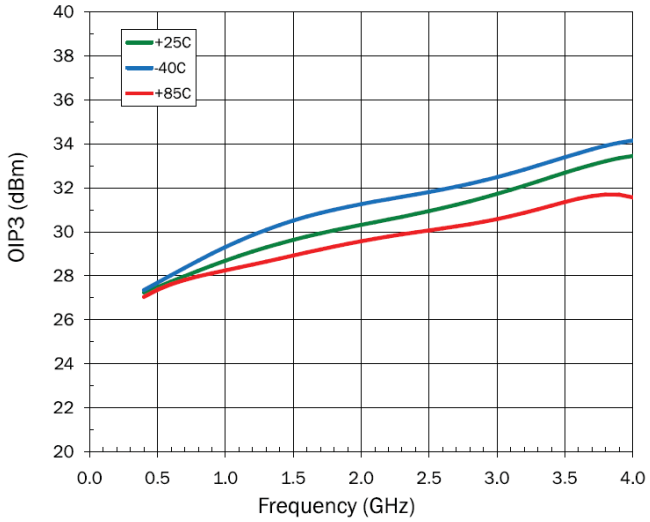
NF versus Frequency



P1dB versus Frequency



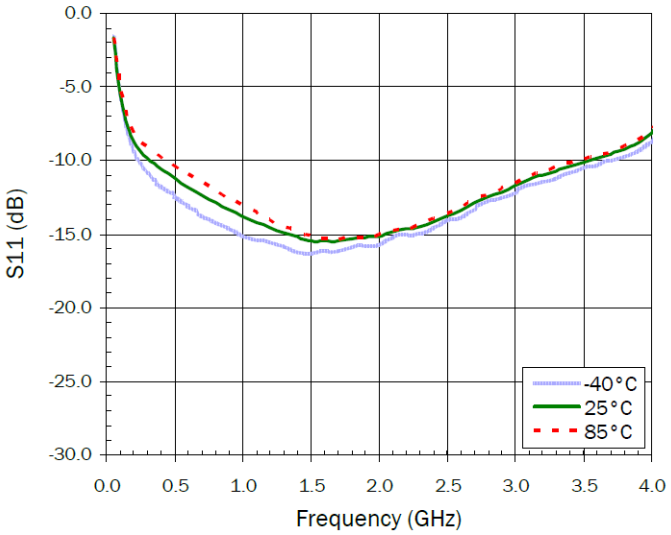
OIP3 vs. Frequency (-5dBm/tone, 1MHz spacing)



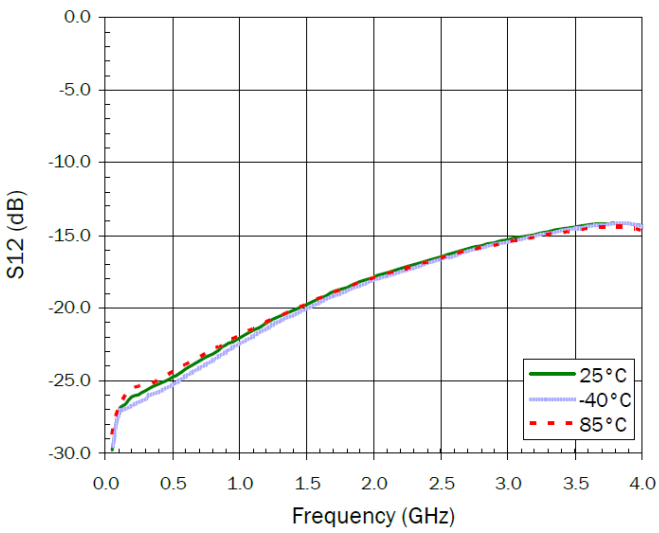
Performance Plots – V_D +3 V (Continue 1)

Test conditions unless otherwise noted: V_D = +3 V, I_D =25 mA

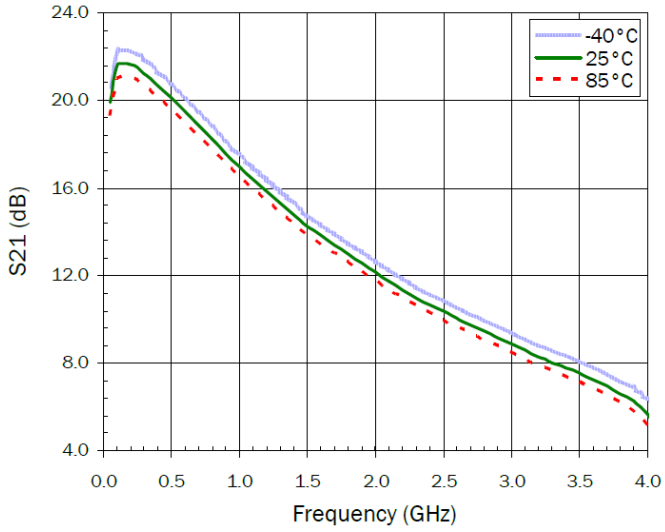
S11 versus Frequency



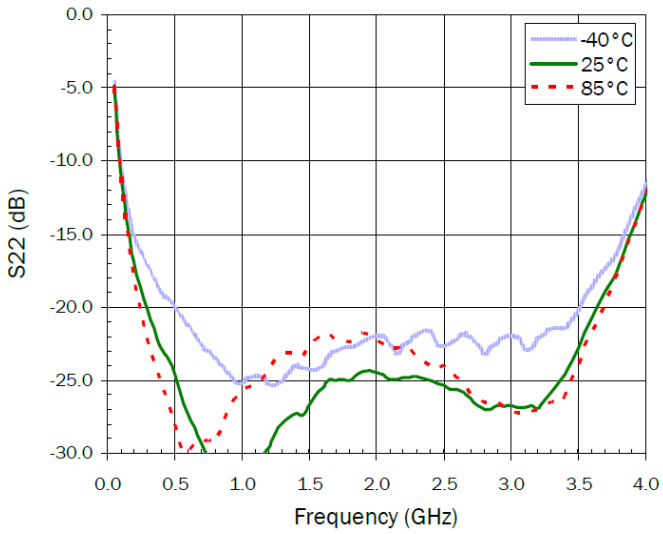
S12 versus Frequency



S21 versus Frequency



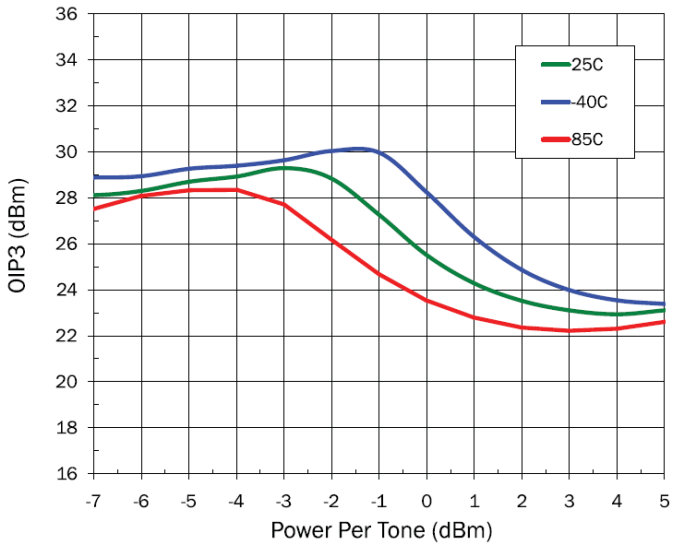
S22 versus Frequency



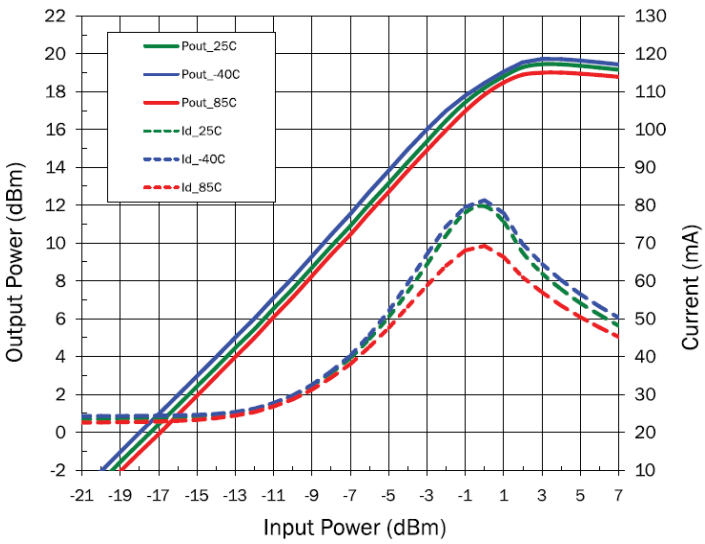
Performance Plots – V_D +3 V (Continue 2)

Test conditions unless otherwise noted: V_D = +3 V, I_D =25 mA, Temp.=+25°C

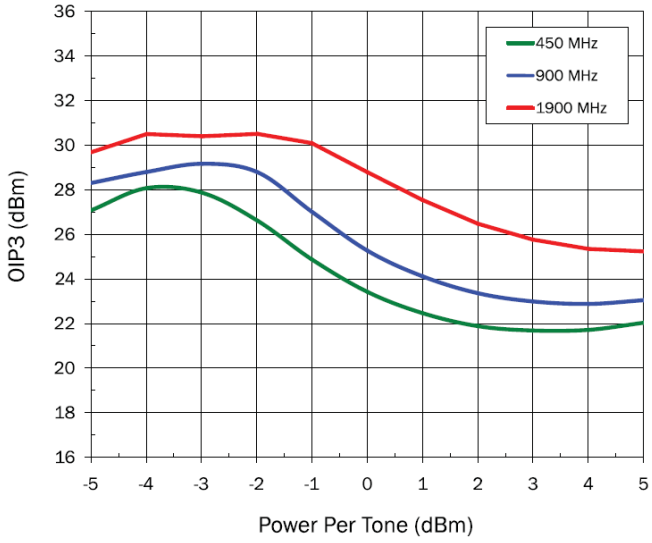
OIP3 versus Power Out (Vd = 3V, 900MHz)



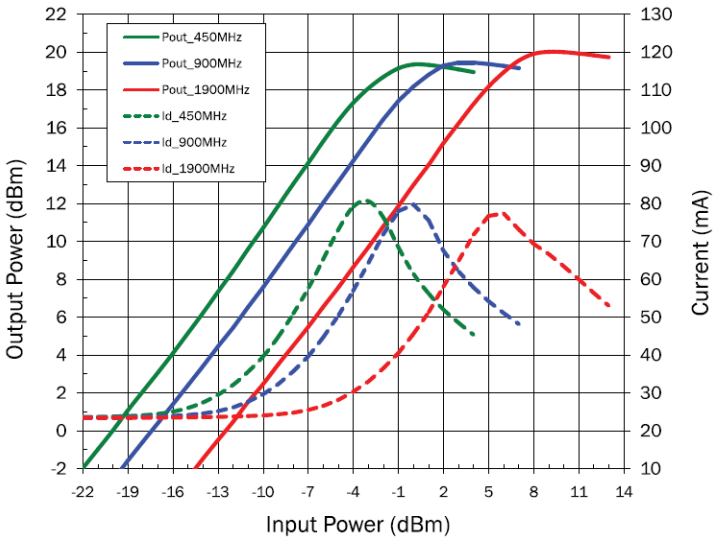
Output Power versus Input Power (Vd=3V, 900 MHz)



OIP3 versus Power Out (Vd = 3V, 25C)



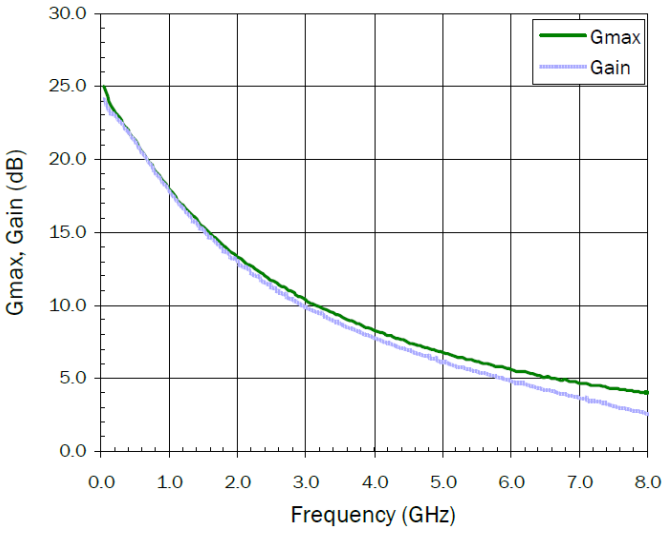
Output Power versus Input Power (Vd=3V)



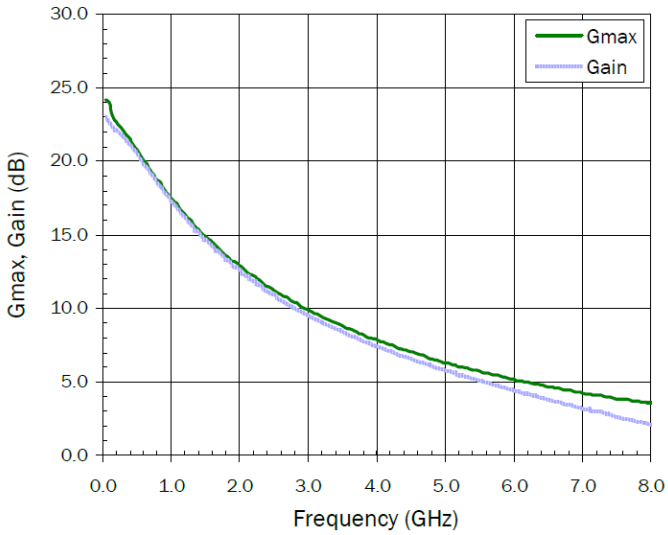
De-Embedded Device S-parameters*

Test conditions unless otherwise noted: Temp.=+25°C

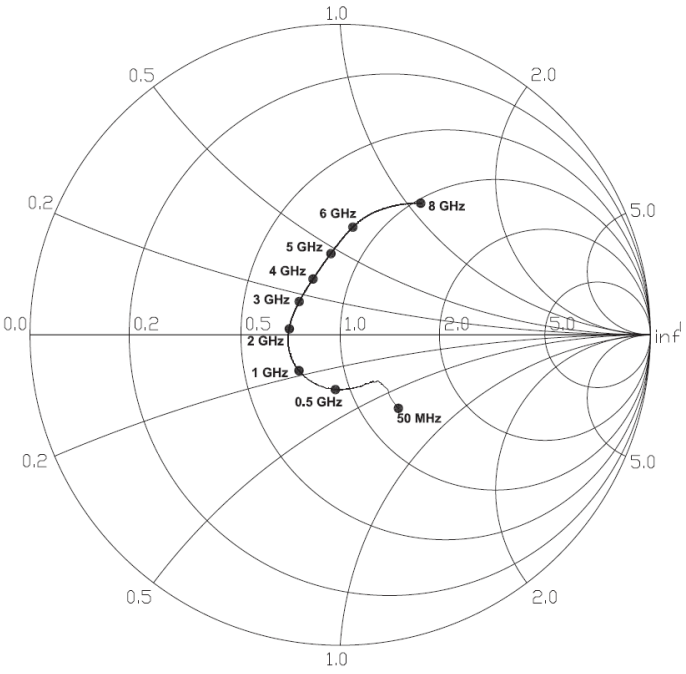
Gmax versus Frequency (5V,46mA)



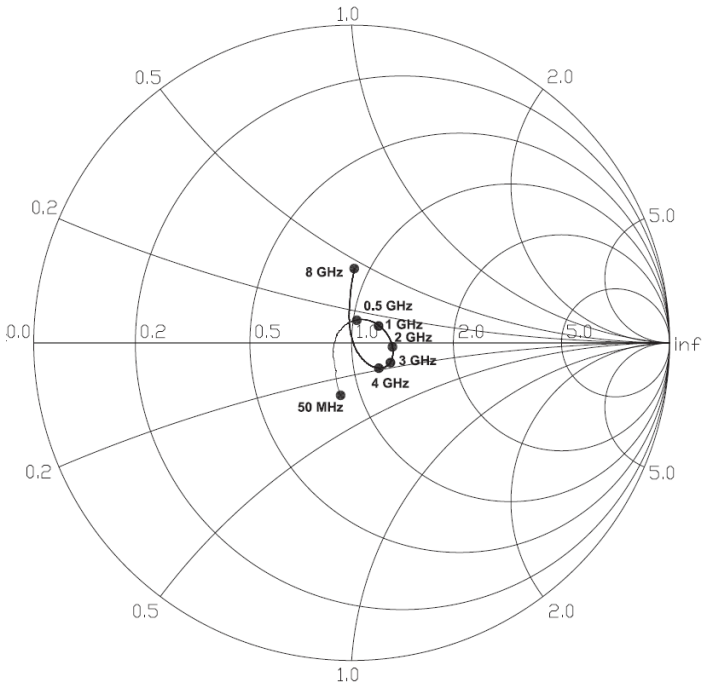
Gmax versus Frequency (3V, 25mA)



S11 versus Frequency (5V 46mA)



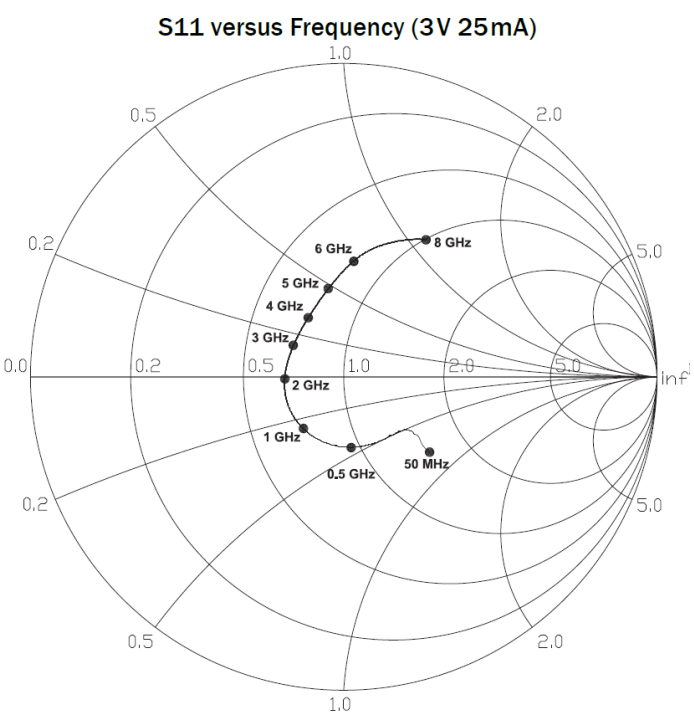
S22 versus Frequency (5V 46mA)

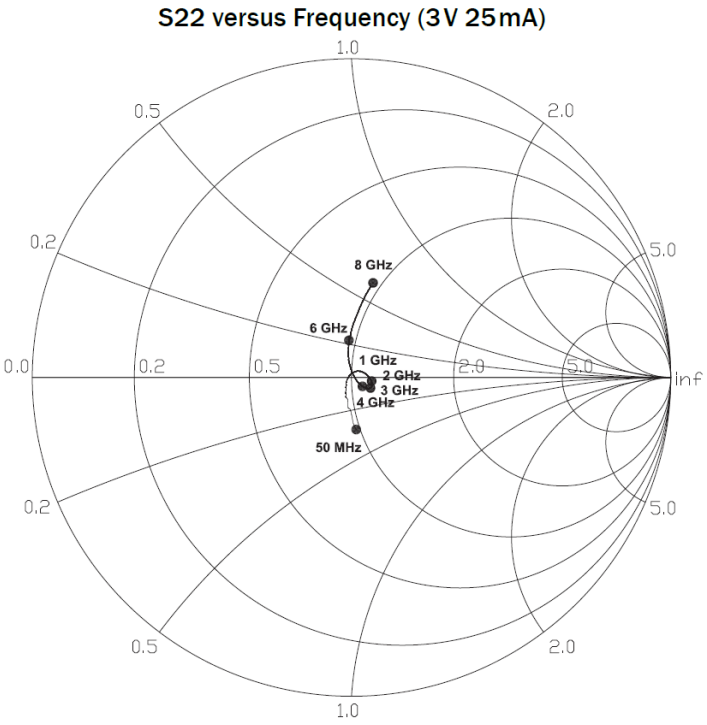


*Measured with Bias-T

De-embedded Device S-parameters* (Continue)

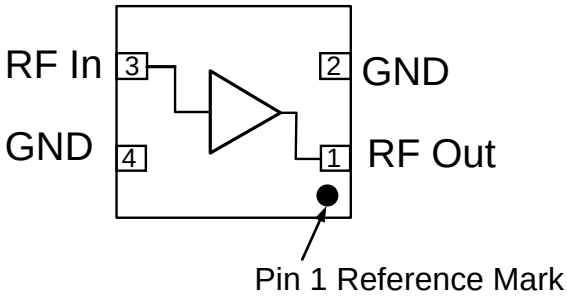
Test conditions unless otherwise noted: Temp.=+25°C





*Measured with Bias-T

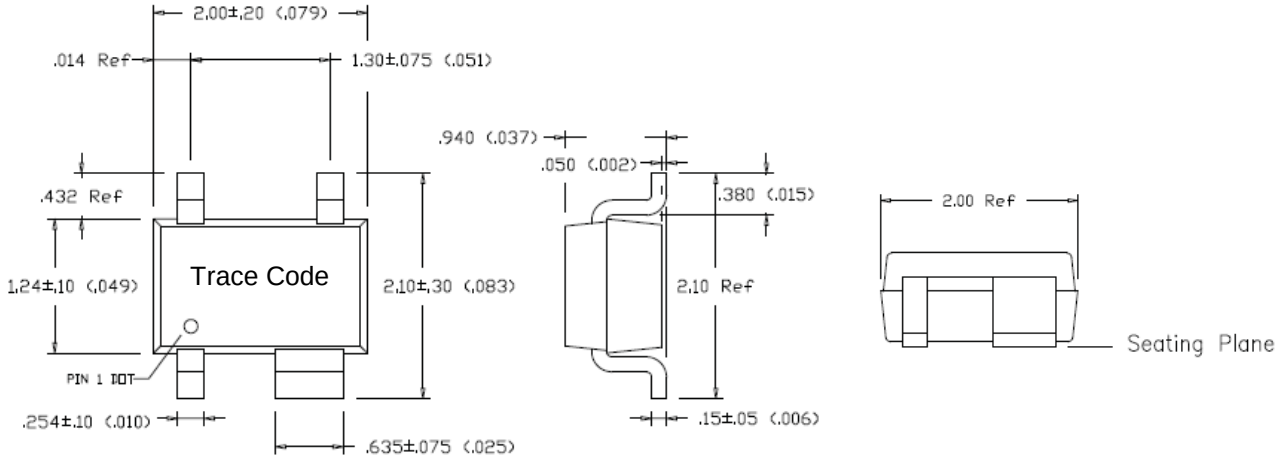
Pin Configuration and Description



Pin No.	Label	Description
1	RF Out	RF output and Drain DC input. Internally matched to 50Ω. External DC blocking capacitor is required for RF output.
2	GND	DC/RF ground connection.
3	RF In	RF input. This pin is internally DC coupled and RF matched to 50Ω. External DC blocking capacitor is required.
4	GND	DC/RF ground connection.

Device Package Information

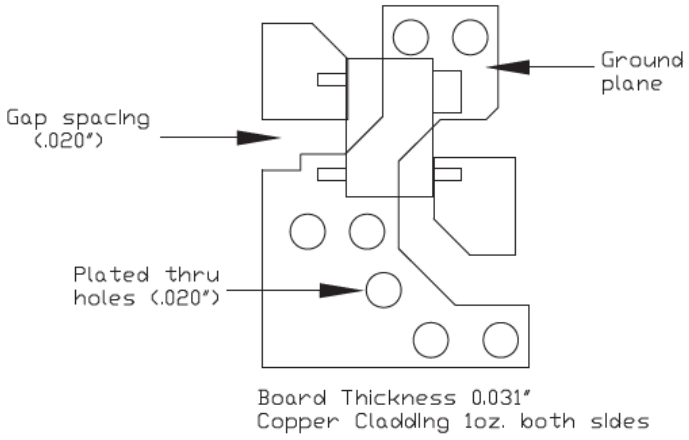
Marking and Dimensions



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012
4. Trace code to be assigned by sub-contractor

Recommended PCB Layout Pattern



Notes:

1. All dimensions are in inches. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.