Industrial Grade ECC SODIMM DDR4 3200 8GB Datasheet

(SQR-SD4I8G3K2SEBCB)

CONTENTS

Revision History

Rev	Date	Modification
1.0	20th Aug., 2020	Official released

1. Description

DDR4 SODIMM						
Part Number	Density	Speed	DIMM Organization	Number of DRAM	Number of rank	ECC
SQR-SD4I8G3K2SEBCB	8GB	PC4-3200	1Gx72	9	1	Y

SDRAM: SAMSUNG 1Gx8 C-die

2. Features

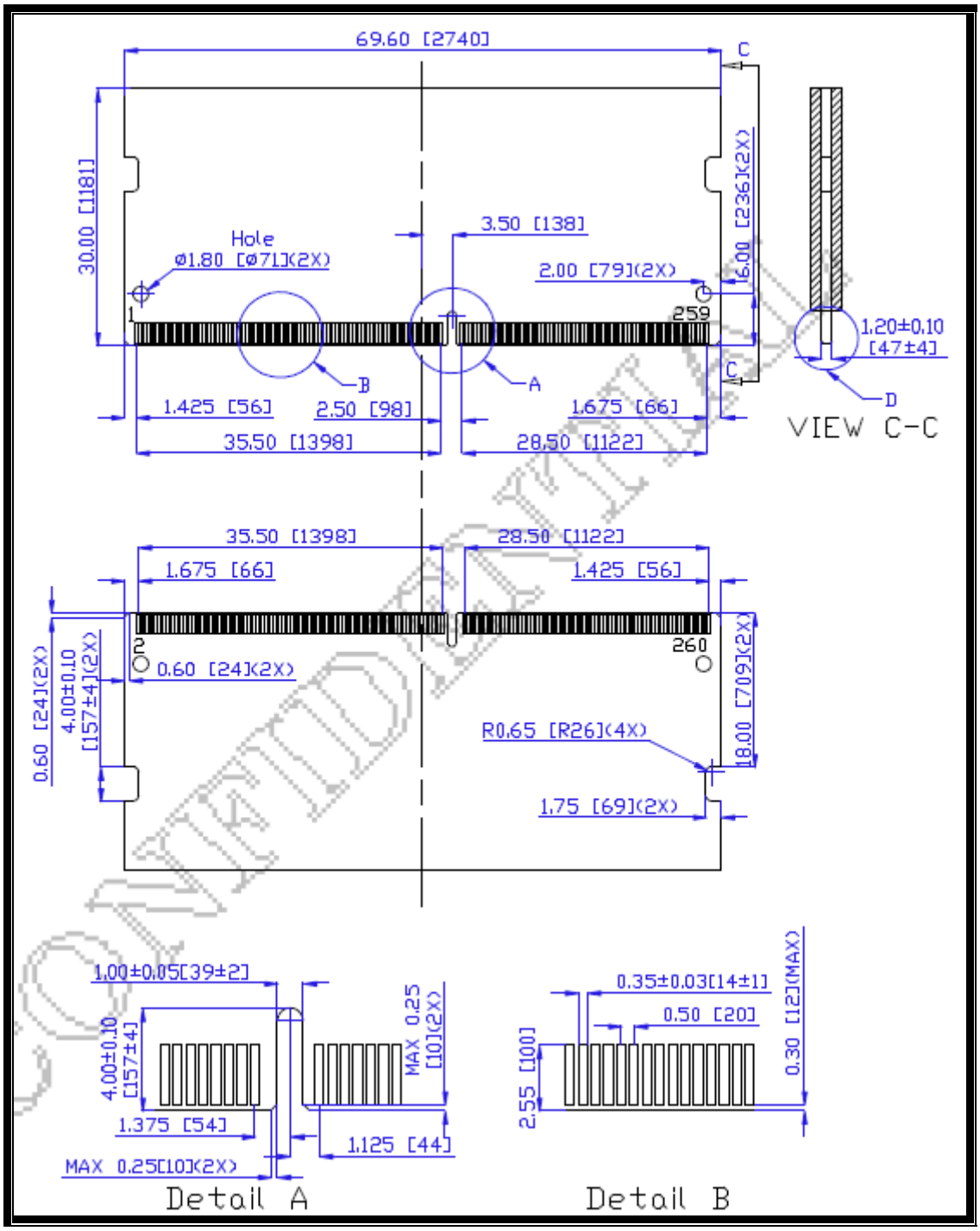
- Key Parameter

Industry Nomenclature	Data Rate MT/s			tRCD (ns)	tRP (ns)	tRC (ns)
	CL=19	**CL=21**	**CL=22**			
PC4-3200	2666	2933	3200	13.75	13.75	45.75

- JEDEC Standard 260-pin Small-Outline Dual In-Line Memory Module
- Intend for PC4-3200 applications
- Cl-tRCD-tRP: 22-22-22
- Inputs and Outputs are SSTL-12 compatible
- VDD=VDDQ= 1.2 Volt (1.14V~1.26V)
- VPP=2.5 Volt (2.375V~2.75V)
- VDDSPD=2.2-3.6V
- Low-Power auto self-refresh (LPASR)
- SDRAMs have 16 internal banks for concurrent operation (4 Bank Group of 4 banks each)
- Normal and Dynamic On-Die Termination for data, strobe and mask signals.
- Data bus inversion (DBI) for data bus
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the MRS
- Selectable BC4 or BL8 on-the fly (OTF)
- Golden Connector 30u”
- Fly-By topology
- Terminated control, command and address bus
- Programmable /CAS Latency: 10,11,12,13,14,15,16,17,18,19,20,22,24
- Operation temperature – Tcase (-40°C~85 °C)
- On-die VREFDQ generation and Calibration
- On-Board EEPROM
- Support ECC function

3. Dimension

- (8GB, 1Rank 1Gx8 DDR4 base ECC SODIMM)



Note: All dimensions are in millimeters (mils) and should be kept within a tolerance of ±0.15 (6), unless otherwise specified.

4. Pin Identification

Pin Name	Description	Pin Name	Description
A0–A16	SDRAM address bus	SCL	I^2C serial bus clock for SPD/TS
BA0, BA1	SDRAM bank select	SDA	I^2C serial bus data line for SPD/TS
BG0, BG1	SDRAM bank group select	SA0–SA2	I^2C slave address select for SPD/TS
RAS_n[1]	SDRAM row address strobe	PARITY	SDRAM parity input
CAS_n[2]	SDRAM column address strobe	VDD	SDRAM I/O & core power supply
WE_n[3]	SDRAM write enable	VPP	SDRAM activating power supply
CS0_n, CS1_n CS2_n, CS3_n	Rank Select Lines	C0, C1	Chip ID lines for 3DS components
CKE0, CKE1	SDRAM clock enable lines	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	SDRAM on-die termination control lines	VSS	Power supply return (ground)
ACT_n	SDRAM activate	VDDSPD	Serial SPD/TS positive power supply
DQ0–DQ63	DIMM memory data bus	ALERT_n	SDRAM ALERT_n
CB0–CB7	DIMM ECC check bits (for x72 module)		
DQS0_t–DQS8_t	SDRAM data strobes (positive line of differential pair)	RESET_n	Set SDRAMs to a Known State
DQS0_c–DQS8_c	SDRAM data strobes (negative line of differential pair)	EVENT_n	SPD signals a thermal event has occurred.
DM0_n–DM8_n, DBI0_n-DBI8_n	SDRAM data masks/data bus inversion (x8-based x72 DIMMs)	VTT	Termination supply for the Address, Command and Control bus
CK0_t, CK1_t	SDRAM clocks (positive line of differential pair)	NC	No connection
CK0_c, CK1_c	SDRAM clocks (negative line of differential pair)		

Note 1 RAS_n is a multiplexed function with A16.
Note 2 CAS_n is a multiplexed function with A15.
Note 3 WE_n is a multiplexed function with A14.

5. Pin Configurations

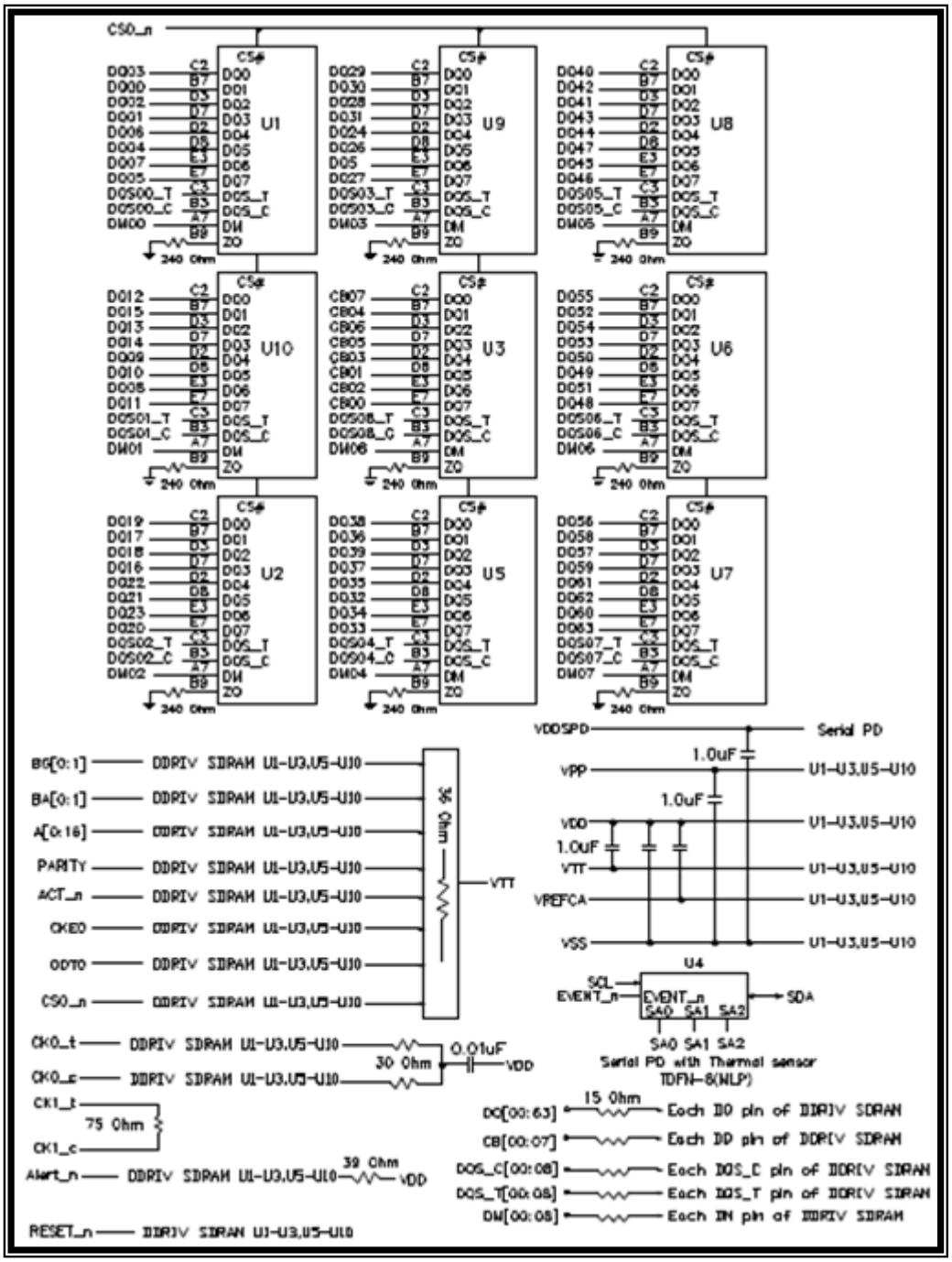
DDR4 1Gx8 base SODIMM

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VSS	2	VSS	67	DQ29	68	VSS	133	A1	134	EVENT_n, NF	199	DM5_n/ DBI5_n	200	DQS5_t
3	DQ5	4	DQ4	69	VSS	70	DQ24	135	VDD	136	VDD	201	VSS	202	VSS
5	VSS	6	VSS	71	DQ25	72	VSS	137	CK0_t	138	CK1_t/NF	203	DQ46	204	DQ47
7	DQ1	8	DQ0	73	VSS	74	DQS3_c	139	CK0_c	140	CK1_c/NF	205	VSS	206	VSS
9	VSS	10	VSS	75	DM3_n/ DBI3_n	76	DQS3_t	141	VDD	142	VDD	207	DQ42	208	DQ43
11	DQS0_c	12	DM0_n/ DBI0_n	77	VSS	78	VSS	143	PARITY	144	A0	209	VSS	210	VSS
13	DQS0_t	14	VSS	79	DQ30	80	DQ31	145	BA1	146	A10/AP	211	DQ52	212	DQ53
15	VSS	16	DQ6	81	VSS	82	VSS	147	VDD	148	VDD	213	VSS	214	VSS
17	DQ7	18	VSS	83	DQ26	84	DQ27	149	CS0_n	150	BA0	215	DQ49	216	DQ48
19	VSS	20	DQ2	85	VSS	86	VSS	151	WE_n/ A14	152	RAS_n/A16	217	VSS	218	VSS
21	DQ3	22	VSS	87	CB5/NC	88	CB4/NC	153	VDD	154	VDD	219	DQS6_c	220	DM6_n/ DBI6_n
23	VSS	24	DQ12	89	VSS	90	VSS	155	ODT0	156	CAS_n/A15	221	DQS6_t	222	VSS
25	DQ13	26	VSS	91	CB1/NC	92	CB0/NC	157	CS1_n	158	A13	223	VSS	224	DQ54
27	VSS	28	DQ8	93	VSS	94	VSS	159	VDD	160	VDD	225	DQ55	226	VSS
29	DQ9	30	VSS	95	DQS8_c	96	DM8_n/ DBI8_n/NC	161	ODT1	162	C0/ CS2_n/NC	227	VSS	228	DQ50
31	VSS	32	DQS1_c	97	DQS8_t	98	VSS	163	VDD	164	VREFCA	229	DQ51	230	VSS
33	DM1_n/DBI1_n	34	DQS1_t	99	VSS	100	CB6/NC	165	C1, CS3_n, NC	166	SA2	231	VSS	232	DQ60
35	VSS	36	VSS	101	CB2/NC	102	VSS	167	VSS	168	VSS	233	DQ61	234	VSS
37	DQ15	38	DQ14	103	VSS	104	CB7/NC	169	DQ37	170	DQ36	235	VSS	236	DQ57
39	VSS	40	VSS	105	CB3/NC	106	VSS	171	VSS	172	VSS	237	DQ56	238	VSS
41	DQ10	42	DQ11	107	VSS	108	RESET_n	173	DQ33	174	DQ32	239	VSS	240	DQS7_c
43	VSS	44	VSS	109	CKE0	110	CKE1	175	VSS	176	VSS	241	DM7_n/ DBI7_n	242	DQS7_t
45	DQ21	46	DQ20	111	VDD	112	VDD	177	DQS4_c	178	DM4_n/ DBI4_n	243	VSS	244	VSS
47	VSS	48	VSS	113	BG1	114	ACT_n	179	DQS4_t	180	VSS	245	DQ62	246	DQ63
49	DQ17	50	DQ16	115	BG0	116	ALERT_n	181	VSS	182	DQ39	247	VSS	248	VSS
51	VSS	52	VSS	117	VDD	118	VDD	183	DQ38	184	VSS	249	DQ58	250	DQ59
53	DQS2_c	54	DM2_n/ DBI2_n	119	A12	120	A11	185	VSS	186	DQ35	251	VSS	252	VSS
55	DQS2_t	56	VSS	121	A9	122	A7	187	DQ34	188	VSS	253	SCL	254	SDA
57	VSS	58	DQ22	123	VDD	124	VDD	189	VSS	190	DQ45	255	VDDSPD	256	SA0
59	DQ23	60	VSS	125	A8	126	A5	191	DQ44	192	VSS	257	VPP	258	VTT
61	VSS	62	DQ18	127	A6	128	A4	193	VSS	194	DQ41	259	VPP	260	SA1
63	DQ19	64	VSS	129	VDD	130	VDD	195	DQ40	196	VSS				
65	VSS	66	DQ28	131	A3	132	A2	197	VSS	198	DQS5_c				

Note:
1. NC = No Connect, RFU = Reserved for Future Use
2. Address A17 is only valid for 16 Gb x4 based SDRAMs.
3. RAS_n is a multiplexed function with A16.
4. CAS_n is a multiplexed function with A15.
5. WE_n is a multiplexed function with A14.

6. Block Diagram

- (8GB, 1 Rank 1Gx8 DDR4 SDRAMs)



Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

7. Environmental Requirements

DDR4 SODIMMs are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
TOPR	Operating Temperature (ambient)	-40 to +85	°C	3
TSTG	Storage Temperature	-50 to +100	°C	1
HOPR	Operating Humidity (relative)	10 to 90	%	
HSTG	Storage Humidity (without condensation)	5 to 95	%	1
PBAR	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1,2

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Up to 9850 ft.
3. The component maximum case temperature (TCASE) shall not exceed the value specified in the DDR4 DRAM component specification. JESD79-4
Follow JEDEC spec.

8. SDRAM Parameters by device density

RTT_Nom Setting	Parameter		8Gb	Units
tREFI	Average periodic refresh interval	-40°C≦**TCASE**≦**85**°C	7.8	µs
		85°C<**TCASE**≦**95**°C	3.9	µs

9. Parameter & Operating Conditions

SDRAM Absolute Maximum Ratings

Symbol	Parameter		Rating	Units	Note
T_{OPER}	Operation Temperature	Normal Operating Temp.	-40 to 85	°C	1,2
		Extended Temp.(optional)	85 to 95	°C	1,3
T_{STG}	Storage Temperature		-55 to 100	°C	4,5
V_{IN}, V_{OUT}	Voltage on any pins relative to Vss		-0.3 to +1.5	V	4
V_{DD}	Voltage on VDD supply relative to Vss		-0.3 to +1.5	V	4,6
V_{DDQ}	Voltage on VDDQ supply relative to Vss		-0.3 to +1.5	V	4,6

Note:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM.
For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85 °C under
all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 °C case temperature. Full specifications are supported in this range, but the following additional
conditions apply:
   a) Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to supplier data sheet and/or the DIMM SPD for option availability.
   b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 =0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 =0b). Please refer to the supplier data sheet and/or the DIMM SPD for Auto Self-Refresh option availability, Extended Temperature Range support and tREFI requirements in the Extended Temperature Range.
4. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
5. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
6. VDD and VDDQ must be within 300 mV of each other at all times;and VREF must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV

Operating Condition

Parameter	Symbol	Min	Nom	Max	Units	Notes
Supply Voltage	**VDD**	1.14	1.2	1.26	V	1
DRAM activating power supply	**VPP**	2.375	2.5	2.75	V	2
Input reference voltage command/ address bus	**VREFCA(DC)**	0.49 x VDD	0.5 x VDD	0.51 x VDD	V	3
Termination Voltage	**VTT**	0.49 × VDD	0.5 × VDD	0.51 × VDD	V	4

Note:
1. VDDQ tracks with VDD; VDDQ and VDD are tied together.
2. VPP must be greater than or equal to VDD at all times.
3. VREFCA must not be greater than 0.6 x VDD. When VDD is less than 500mV, VREF may be less than or equal to 300mV.
4. VTT termination voltages in excess of the specification limit adversely affect the voltage margins of command and address signals and reduce timing margins.

10. Operating, Standby, and Refresh Currents

8G ECC SODIMM (1Rank 1Gx8 DDR4 SDRAMs)

	Proposed Conditions	Value		Units
		IDD Max.	IPP Max.	
IDD0	Operating One Bank Active-Precharge Current (AL=0)CKE: High; External clock: On; tCK, nRC, nRAS, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: Highbetween ACT and PRE; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: VDDQ; DM_n:stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2;ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	279	36	mA
IDD0A	Operating One Bank Active-Precharge Current (AL=CL-1) AL = CL-1, Other conditions: see IDD0	297	36	mA
IDD1	Operating One Bank Active-Read-Precharge Current (AL=0)CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: Highbetween ACT, RD and PRE; Command, Address, Bank Group Address, Bank Address Inputs, Data IO: partially toggling; DM_n: stableat 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	306	36	mA
IDD1A	Operating One Bank Active-Read-Precharge Current (AL=CL-1) AL = CL-1, Other conditions: see IDD1	369	36	mA
IDD2N	Precharge Standby Current (AL=0)CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command,Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banksclosed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	180	27	mA
IDD2NA	Precharge Standby Current (AL=CL-1) AL = CL-1, Other conditions: see IDD2N	198	27	mA
IDD2NT	Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VSSQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: toggling according ;	198	27	mA

	Pattern Details: Refer to Component Datasheet for detail pattern			
IDD2NL	Precharge Standby Current with CAL enabled Same definition like for IDD2N, CAL enabled3	153	27	mA
IDD2NG	Precharge Standby Current with Gear Down mode enabled Same definition like for IDD2N, Gear Down mode enabled3	189	27	mA
IDD2ND	Precharge Standby Current with DLL disabled Same definition like for IDD2N, DLL disabled3	171	27	mA
IDD2N_par	Precharge Standby Current with CA parity enabled Same definition like for IDD2N, CA parity enabled3	189	27	mA
IDD2P	Precharge Power-Down Current CKE: Low; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL:0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	117	36	mA
IDD2Q	Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	180	36	mA
IDD3N	Active Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details:Refer to Component Datasheet for detail pattern	270	36	mA
IDD3NA	Active Standby Current (AL=CL-1) AL = CL-1, Other conditions: see IDD3N	288	36	mA
IDD3P	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: sRefer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	189	36	mA

IDD4R	Operating Burst Read Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 82; AL: 0; CS_n: High between RD; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless read data burst with different data between one burst and the next one according ; DM_n: stable at 1; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	1026	36	mA
IDD4RA	Operating Burst Read Current (AL=CL-1) AL = CL-1, Other conditions: see IDD4R	1098	36	mA
IDD4RB	Operating Burst Read Current with Read DBI Read DBI enabled3, Other conditions: see IDD4R	1044	36	mA
IDD4W	Operating Burst Write Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between WR; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless write data burst with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at HIGH; Pattern Details: Refer to Component Datasheet for detail pattern	954	36	mA
IDD4WA	Operating Burst Write Current (AL=CL-1) AL = CL-1, Other conditions: see IDD4W	1017	36	mA
IDD4WB	Operating Burst Write Current with Write DBI Write DBI enabled3, Other conditions: see IDD4W	963	36	mA
IDD4WC	Operating Burst Write Current with Write CRC Write CRC enabled3, Other conditions: see IDD4W	882	36	mA
IDD4W_par	Operating Burst Write Current with CA Parity CA Parity enabled3, Other conditions: see IDD4W	1071	36	mA
IDD5B	Burst Refresh Current (1X REF) CKE: High; External clock: On; tCK, CL, nRFC: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between REF; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: REF command every nRFC ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	2070	225	mA
IDD5F2	Burst Refresh Current (2X REF) tRFC=tRFC_x2, Other conditions: see IDD5B	1458	162	mA
IDD5F4	Burst Refresh Current (4X REF) tRFC=tRFC_x4, Other conditions: see IDD5B	1305	153	mA

IDD6N	Self Refresh Current: Normal Temperature Range TCASE: 0 - 85°C; Low Power Array Self Refresh (LP ASR) : Normal4; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n: stable at 1; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MIDLEVEL	189	36	mA
IDD6E	Self-Refresh Current: Extended Temperature Range) TCASE: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Extended4; CKE: Low; External clock: Off; CK_t and CK_c: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	288	45	mA
IDD6R	Self-Refresh Current: Reduced Temperature Range TCASE: 0 - TBD (~35-45)°C; Low Power Array Self Refresh (LP ASR) : Reduced4; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	126	45	mA
IDD6A	Auto Self-Refresh Current TCASE: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Auto4;Partial Array Self-Refresh (PASR): Full Array; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Auto Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	180	45	mA
IDD7	Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: CL-1; CS_n: High between ACT and RDA; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; DataIO: read data bursts with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	1422	99	mA
IDD8	Maximum Power Down Current TBD	99	27	mA

11. Serial Presence Detect

Byte	Description	Function Supported	Hex Value
0	Number of Bytes Used / Number of Bytes in SPD Device / CRC Coverage	512B Total, 384B Used	23
1	SPD Revision	Ver 1.1	11
2	Key Byte / DRAM Device Type	DDR4 SDRAM	0C
3	Key Byte / Module Type	72b SODIMM	09
4	SDRAM Density and Banks	8Gb, 4BG&4Banks	85
5	SDRAM Addressing	Row : 16, Column :10	21
6	SDRAM Device Type	Monolithinc Device	00
7	SDRAM Optional Features	Unlimited MAC	08
8	SDRAM Thermal and Refresh Option	Reserved	00
9	Other SDRAM Optional Features	sPPR supported	60
10	Reserved	Reserved	00
11	Module Nominal Voltage, VDD	1.2V	03
12	Module Organization	1Rx8	01
13	Module Memory Bus Width	64bit, ECC	0B
14	Module Thermal Sensor	With TS	80
15~16	Reserved	Reserved	00
17	Timebases	MTB 125ps, FTB 1ps	00
18	SDRAM Minimum Cycle Time(tckavg min)	0.625ns	05
19	SDRAM Minimum Cycle Time(tckavg max)	1.6ns	0D
20	Cas Latency Supported, First Byte	10,11,12,13,14,15,16,17,18,19,20,22,24	F8
21	Cas Latency Supported, Second Byte	10,11,12,13,14,15,16,17,18,19,20,22,24	BF
22	Cas Latency Supported, Third Byte	10,11,12,13,14,15,16,17,18,19,20,22,24	02
23	Cas Latency Supported, Fourth Byte	10,11,12,13,14,15,16,17,18,19,20,22,24	00
24	Minimum Cas Latency Time (tAAmin)	13.75ns	6E
25	Minimum RAS to CAS Delay Time(tRCD min)	13.75ns	6E

26	Minimum Raw Precharge Delay Time(tRP min)	13.75ns	6E
27	Upper Nibbles for tRASmin and tRCmin	tRAS=32ns, tRC=45.75ns	11
28	Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte	tRAS=32ns	00
29	Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte	tRC=45.75ns	6E
30	Minimum Refresh Recovery Delay Time (tRFC1min), LSB	350ns	F0
31	Minimum Refresh Recovery Delay Time (tRFC1min), MSB	350ns	0A
32	Minimum Refresh Recovery Delay Time (tRFC2min), LSB	260ns	20
33	Minimum Refresh Recovery Delay Time (tRFC2min), MSB	260ns	08
34	Minimum Refresh Recovery Delay Time (tRFC4min), LSB	160ns	00
35	Minimum Refresh Recovery Delay Time (tRFC4min), MSB	160ns	05
36	Minimum Four Active Window Time (tFAWmin), Most Significant Nibble	21ns	00
37	Minimum Four Activate Window Time (tFAWmin), Least Significant Byte	21ns	A8
38	Minimum Active to Active Delay Time (tRRD_smin), different Bank Group	2.5ns	14
39	Minimum Active to Active Delay Time (tRRD_Lmin), Same Bank Group	4.9ns	28
40	Minimum CAS to CAS Delay Time(tCCD_Lmin), same bank group	5.0ns	28
41	Upper Nibble for tWRmin	15ns	00
42	Minimum Write Recovery Time(tWRmin)	15ns	78
43	Upper Nibbles for tWTRmin	2.5ns	00
44	Minimum Write to Read Time(tWTR_smin), different bank group	2.5ns	14
45	Minimum Write to Read Time(tWTR_Lmin), same bank group	7.5ns	3C
46~59	Reserved	Reserved	00
60	Connector to SDRAM Bit Mapping		0C
61	Connector to SDRAM Bit Mapping		2B
62	Connector to SDRAM Bit Mapping		2D
63	Connector to SDRAM Bit Mapping		04
64	Connector to SDRAM Bit Mapping		16
65	Connector to SDRAM Bit Mapping		35

66	Connector to SDRAM Bit Mapping		23
67	Connector to SDRAM Bit Mapping		0D
68	Connector to SDRAM Bit Mapping		36
69	Connector to SDRAM Bit Mapping		0C
70	Connector to SDRAM Bit Mapping		2C
71	Connector to SDRAM Bit Mapping		0B
72	Connector to SDRAM Bit Mapping		03
73	Connector to SDRAM Bit Mapping		24
74	Connector to SDRAM Bit Mapping		35
75	Connector to SDRAM Bit Mapping		0C
76	Connector to SDRAM Bit Mapping		03
77	Connector to SDRAM Bit Mapping		2D
78~116	Reserved	Reserved	00
117	Fine Offset for Minimum CAS to CAS Delay Time(tCCD_Lmin), same bank group	5.0ns	00
118	Fine Offset for Minimum Activate to Acticate Delay Time(tRRD_L_min), Same Bank Group	4.9ns	9C
119	Fine Offset for Minimum Activate to Acticate Delay Time(tRRD_Smin), Different Bank Group	3.0ns	00
120	Fine Offset for Minimum Activate to Acticate/Refresh Delay Time(tRCmin)	45.75ns	00
121	Fine Offset for Minimum Row Precharge Delay Time(tRPmin)	13.75ns	00
122	Fine Offset for Minimum RAS to CAS Delay Time(tRCD_min)	13.75ns	00
123	Fine Offset for Minimum CAS Latency Delay Time(tAA_min)	13.75ns	00
124	Fine Offset for DRAM Maximum Cycle Time(tCKAVG_max)	1.6ns	E7
125	Fine Offset for DRAM Minimum Cycle Time(tCKAVG_min)	0.750ns	00
126	Cyclical Redundancy Code	-	53
127	Cyclical Redundancy Code	-	E6
128	Raw Card Extension, Module Nominal Height	29 < height<= 30 mm	0F
129	Module Maximum Thickness		11
130	Reference Raw Card Used	R/C D REV2.0	23

131	DIMM Module Attributes		00
132	RDIMM Thermal Heat Spreader Solution		00
133	Register Manufacturer ID Code, Least Signficant Byte		00
134	Register Manufacturer ID Code, Most Signficant Byte		00
135	Register Revision Number		00
136	Address Mapping from Register to DRAM		00
137	Register Ouput Drive Strength for Control		00
138	Register Output Strength for CK		00
139~253	Reserved	Reserved	00
254	Cyclical Redundancy Code	-	BE
255	Cyclical Redundancy Code	-	A2
256~319	Reserved	Reserved	00
320	Module Manufacturer's ID Code, Least Significant Byte	Advantech	8A
321	Module Manufacturer's ID Code, Most Significant Byte	Advantech	C8
322	Module Manufactoring Location	-	-
323	Module Manufactoring Date	Year	-
324	Module Manufactoring Date	Week	-
325~328	Module Serial Number	-	-
329~348	Module Part Number	SQR-SD4I8G3K2SEBCB	53 51 52 2D 53 44 34 49 38 47 33 4B 32 53 45 42 43 42 20 20
349	Module Revision Code	-	00
350	DRAM Manufacturer's ID Code, Least Sgnificant Byte	Samsung	80
351	DRAM Manufacturer's ID Code, Most Sgnificant Byte	Samsung	CE
352	DRAM Stepping	Ver 0.0	00
353~380	Module Manufacturer's Specific Data	Reserved	00
381	Module Manufacturer's Specific Data	Reserved	00
382~383	Reserved	Reserved	00
384~511	End User Programmable	Reserved	00