SRDA70-4
RailClamp®
Low Capacitance TVS Diode Array

PROTECTION PRODUCTS

Description

RailClamps are surge rated diode arrays designed to protect high speed data interfaces. The SRDA70-4 has been specifically designed to protect sensitive components which are connected to data and transmission lines from over-voltages caused by electrostatic discharge **(ESD)**, electrical fast transients **(EFT)**, and **lightning**.

The unique design of the SRDA70-4 integrates eight surge rated, low capacitance steering diodes in a low profile SO-8 package. During transient conditions, the steering diodes direct the transient to either the positive side of the power supply line or to ground. The SRDA70-4 may be used as a stand alone device or in conjunction with TVS diodes for enhanced protection.

The low capacitance array configuration allows the user to protect four high speed data or I/O lines. The low inductance construction minimizes voltage overshoot during high current surges.

Features

- Transient protection for high speed data lines to
  IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
  IEC 61000-4-4 (EFT) 40A (5/50ns)
  IEC 61000-4-5 (Lightning) 1kV, 24A (8/20µs)
- Array of surge rated diodes
- Protects four I/O lines
- Low capacitance for high-speed interfaces
- High surge capability
- Low forward voltage characteristics
- Solid-state silicon avalanche technology

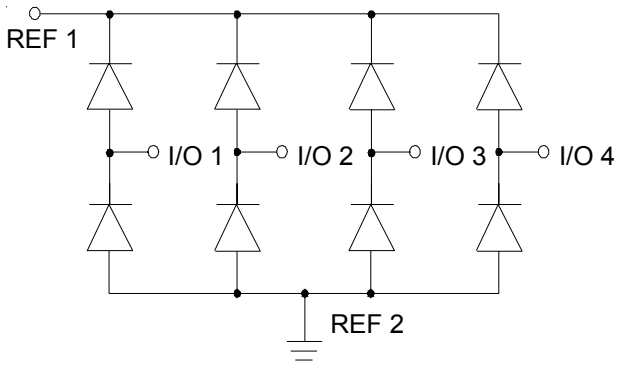
Mechanical Characteristics

- JEDEC SO-8 package
- UL 497B listed
- Molding compound flammability rating: UL 94V-0
- Marking : Part number, date code, logo
- Packaging : Tube or Tape and Reel per EIA 481
- RoHS/WEEE Compliant

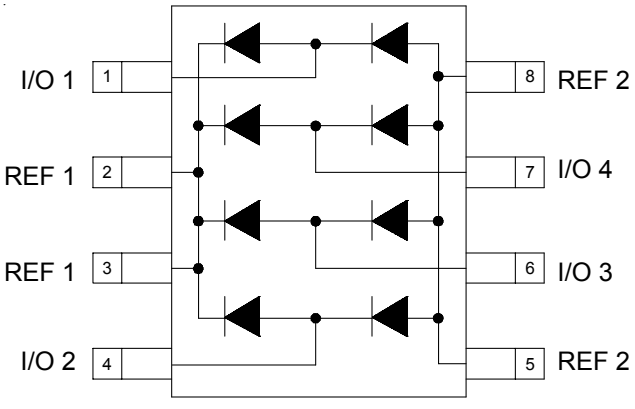
Applications

- Latch-Up Protection
- Microcontroller Input Protection
- Token Ring
- I^2C Bus Protection
- Video Line Protection
- Set Top Box I/O
- LAN/WAN Equipment

Circuit Diagram



Schematic and PIN Configuration



SO-8 (Top View)

Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Current (tp = 8/20μs)	I_{PP}	24	A
Rectifier Repetitive Peak Reverse Voltage	V_{RRM}	70	V
Thermal Resistance, Junction to Ambient	θ_{JA}	163	°C /W
Thermal Resistance, Junction to Case	θ_{JC}	38.8	°C /W
Lead Soldering Temperature	T_L	260 (10 sec.)	°C
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

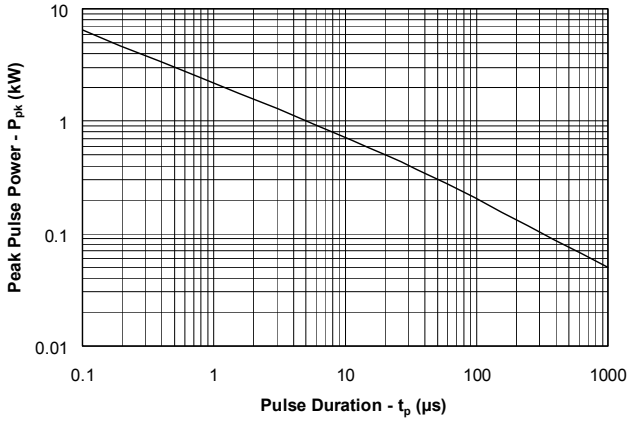
Electrical Characteristics

SRDA70-4

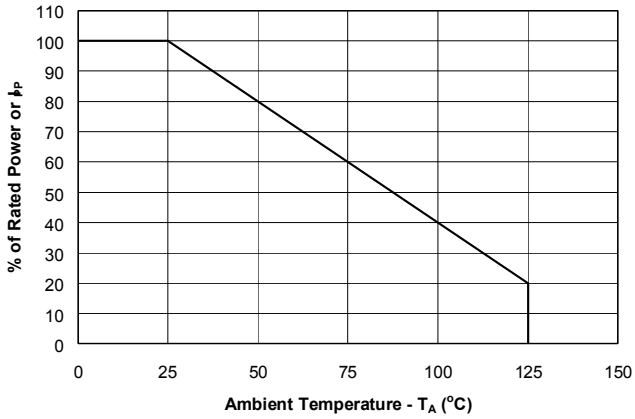
Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Rectifier Repetitive Peak reverse Voltage	V_{RRM}				70	V
Reverse Breakdown Voltage	V_{BR}	I_t = 50μA	85			V
Reverse Leakage Current	I_R	V_{RWM} = 70V, T=25°C			5	μA
Forward Voltage	V_F	I_{PP} = 1A, t_p = 8/20μs			1.3	V
Forward Voltage	V_F	I_{PP} = 10A, t_p = 8/20μs			3.3	V
Junction Capacitance	C_j	Between I/O pins and Ground V_R = 0V, f = 1MHz			15	pF
		Between I/O pins V_R = 0V, f = 1MHz		4		pF

Typical Characteristics

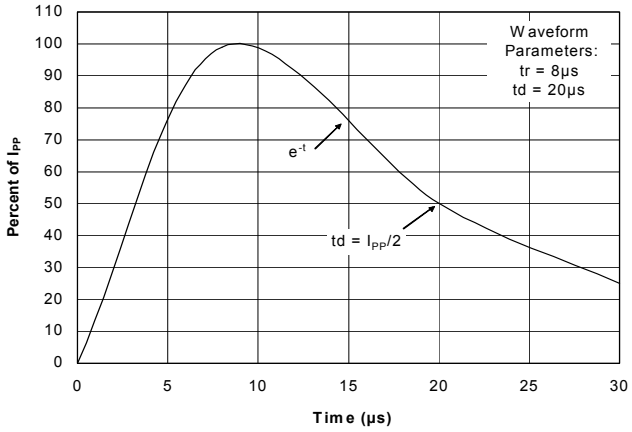
Non-Repetitive Peak Pulse Power vs. Pulse Time



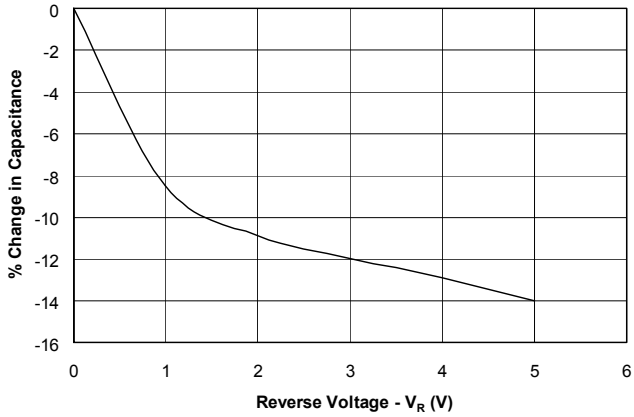
Power Derating Curve



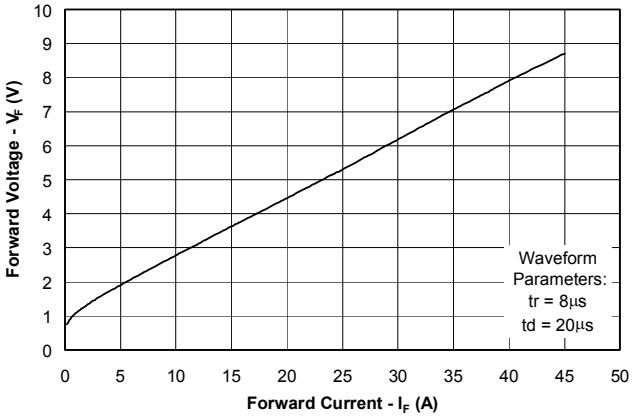
Pulse Waveform



Variation of Capacitance vs. Reverse Voltage



Foward Voltage vs. Forward Current



Applications Information

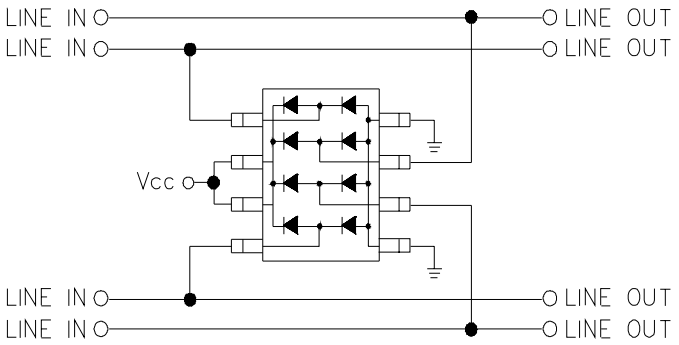
Device Connection Options for Protection of Four High-Speed Data Lines

The SRDA70-4 TVS is designed to protect four data lines from transient over-voltages by clamping them to a fixed reference. When the voltage on the protected line exceeds the reference voltage (plus diode V_F) the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. Data lines are connected at pins 1, 4, 6 and 7. The negative reference (REF2) is connected at pins 5 and 8. These pins should be connected directly to a ground plane on the board for best results. The path length is kept as short as possible to minimize parasitic inductance.

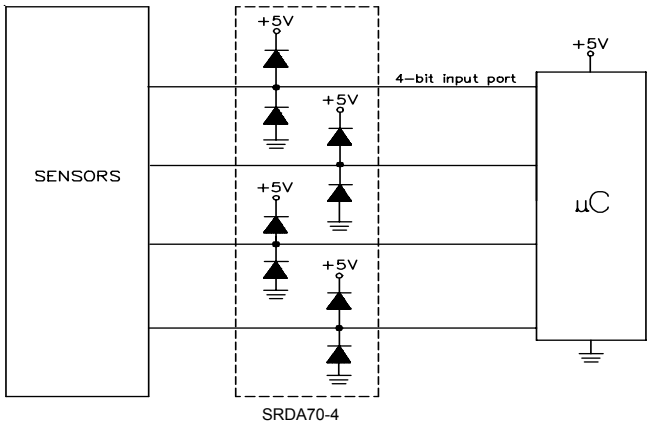
The positive reference (REF1) is connected at pins 2 and 3. The options for connecting the positive reference are as follows:

1. To protect data lines and the power line, connect pins 2 and 3 directly to the positive supply rail (V_{CC}). In this configuration the data lines are referenced to the supply voltage. An external TVS diode may be added between the supply rail and ground in order to prevent over-voltage on the supply rail.
2. The SRDA70-4 can be isolated from the power supply by adding a series resistor between pins 2 and 3 and V_{CC}. A value of 10kΩ is recommended. The internal steering diodes remain biased, providing the advantage of lower capacitance.
3. In applications where no positive supply reference is available, or complete supply isolation is desired, an external TVS diode may be used as the reference. The steering diodes will begin to conduct when the voltage on the protected line exceeds the working voltage of the TVS (plus one diode drop).

I/O Protection



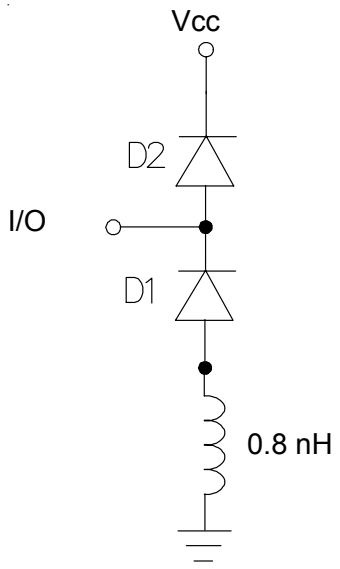
Microcontroller Protection



Matte Tin Lead Finish

Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

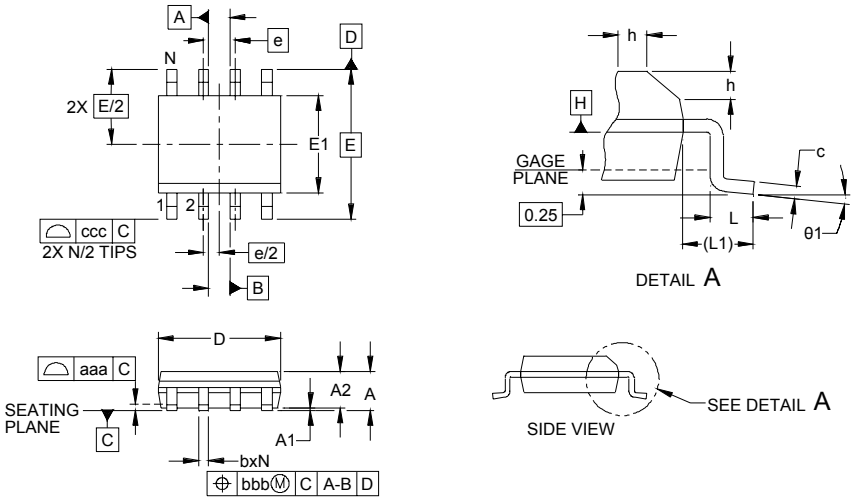
Applications Information - Spice Model



SRDA70-4 Spice Model

SRDA70-4 Spice Parameters			
Parameter	**Unit**	**D1 (LCRD)**	**D2 (LCRD)**
IS	Amp	3.54E-14	1.46E-14
BV	Volt	680	240
VJ	Volt	0.62	0.64
RS	Ohm	0.330	0.124
IBV	Amp	1E-3	1E-3
CJO	Farad	5.2E-12	6.2E-12
TT	sec	2.56E-9	2.56E-9
M	--	0.058	0.058
N	--	1.1	1.1
EG	eV	1.11	1.11

Outline Drawing - SO-8

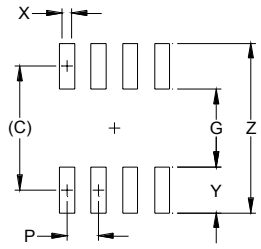


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.053	-	.069	1.35	-	1.75
A1	.004	-	.010	0.10	-	0.25
A2	.049	-	.065	1.25	-	1.65
b	.012	-	.020	0.31	-	0.51
c	.007	-	.010	0.17	-	0.25
D	.189	.193	.197	4.80	4.90	5.00
E1	.150	.154	.157	3.80	3.90	4.00
E	.236 BSC			6.00 BSC		
e	.050 BSC			1.27 BSC		
h	.010	-	.020	0.25	-	0.50
L	.016	.028	.041	0.40	0.72	1.04
L1	(.041)			(1.04)		
N	8			8		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.010			0.25		
ccc	.008			0.20		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MS-012, VARIATION AA.

Land Pattern - SO-8



DIM	INCHES	MILLIMETERS
C	(.205)	(5.20)
G	.118	3.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.291	7.40

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A, RLP NO. 300A.