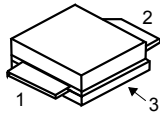


45 W, 28 V RF Power LDMOS transistor from 0.7 to 1.7 GHz


A2

Pin connection	
Pin	Connection
1	Gate
2	Drain
3	Source (bottom side)

Features

Order code	Frequency	V _{DD}	P _{OUT}	Gain	Efficiency
ST16045	1330 MHz	28 V	45 W	20 dB	55 %

- High efficiency and linear gain operations
- Integrated ESD protection
- Internally input matched for ease of use
- Large positive and negative gate / source voltage range
- In compliance with the 2002/95/EC European directive

Applications

- GPS
- Telecom
- Industrial, scientific and medical driver

Description

The **ST16045** is a 45 W, 28 V input matched LDMOS transistor designed for global positioning system and communication/ISM applications with frequencies from 700 to 1700 MHz. It can be used in class AB/B and class C for all typical modulation formats.



Product status link
ST16045

Product summary	
Order code	ST16045
Marking	ST16045
Package	A2
Packing	Tape and reel 13"
Base / Bulk Qty	160 / 160

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	65	V
V_{GS}	Gate-source voltage	-6 / +10	V
V_{DD}	Maximum operating voltage	32	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	+200	°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case $T_{case} = +85\text{ °C}$, $T_J = +200\text{ °C}$, DC test	0.7	°C/W

Table 3. ESD protection

Symbol	Parameter	Class
HBM	Human body model (per JESD22-A114)	2

2 Electrical characteristics

($T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified).

Table 4. Static (per side)

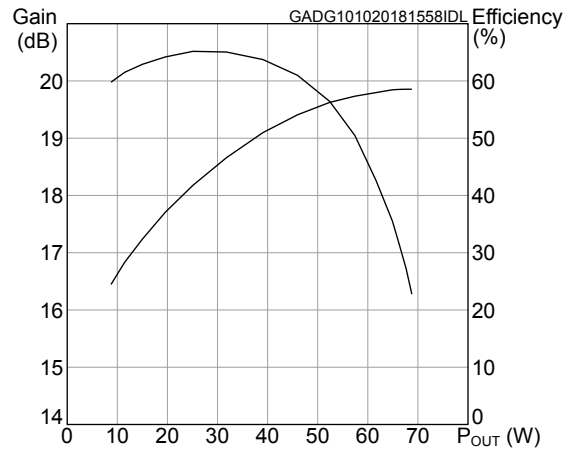
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 100\text{ }\mu\text{A}$	65			V
I_{DSS}	Zero-gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 28\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 50\text{ V}$			1	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = 10\text{ V}$			1	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = 28\text{ V}$, $I_D = 300\text{ }\mu\text{A}$	1.5		2.5	V
$V_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 1\text{ V}$, $I_D = 500\text{ mA}$		0.22		V

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
P_{OUT}	Output power	$V_{DD} = 28\text{ V}$, $I_{DQ} = 0.2\text{ A}$, $f = 1330\text{ MHz}$	-	45	-	W
Gain	Power gain		-	20	-	dB
Efficiency	Drain efficiency		-	55		%
VSWR	Load mismatch	$P_{OUT} = 50\text{ W}$ all phases	-		10:1	

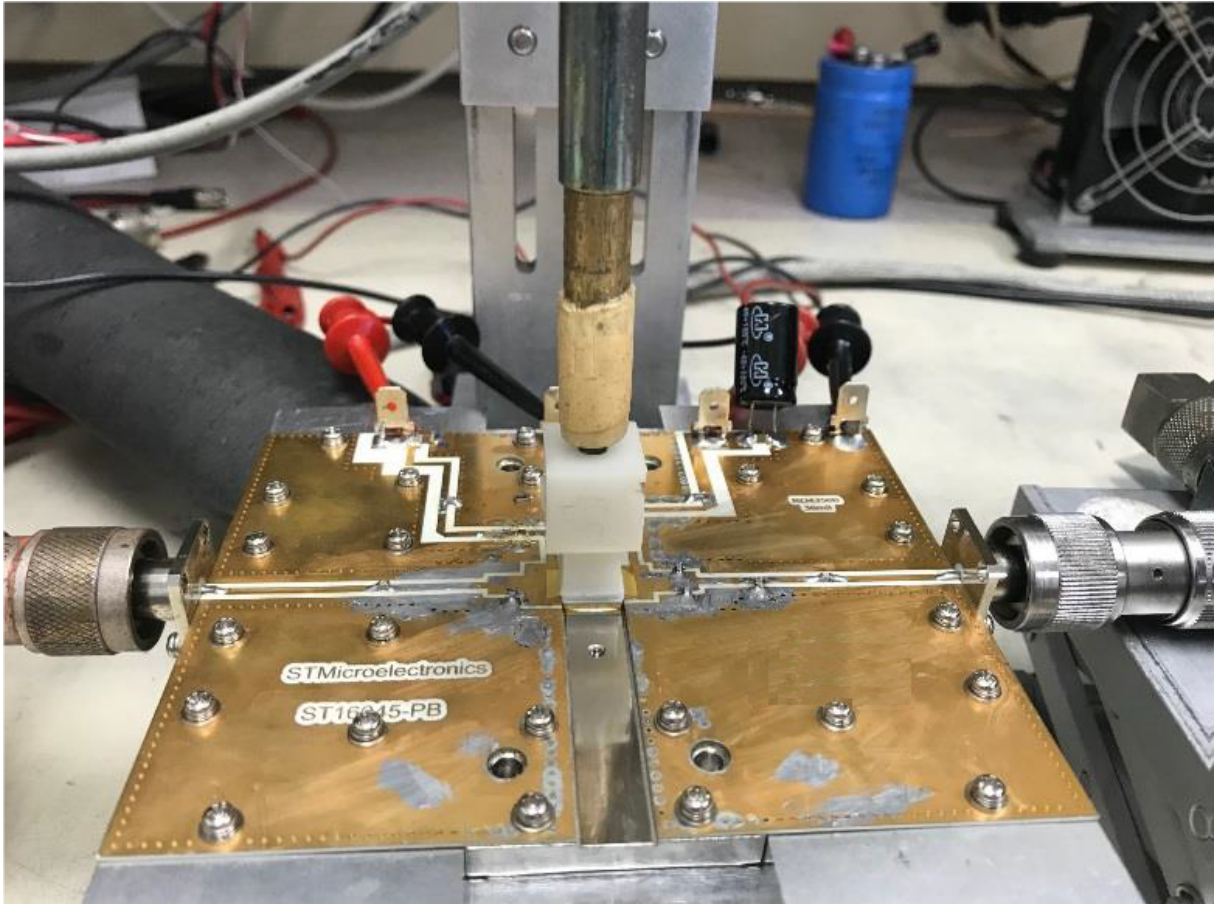
2.1 Electrical characteristics (curves)

Figure 1. Power gain and efficiency versus output power (f = 1330 MHz)



3 Test circuits

Figure 2. Circuit layout

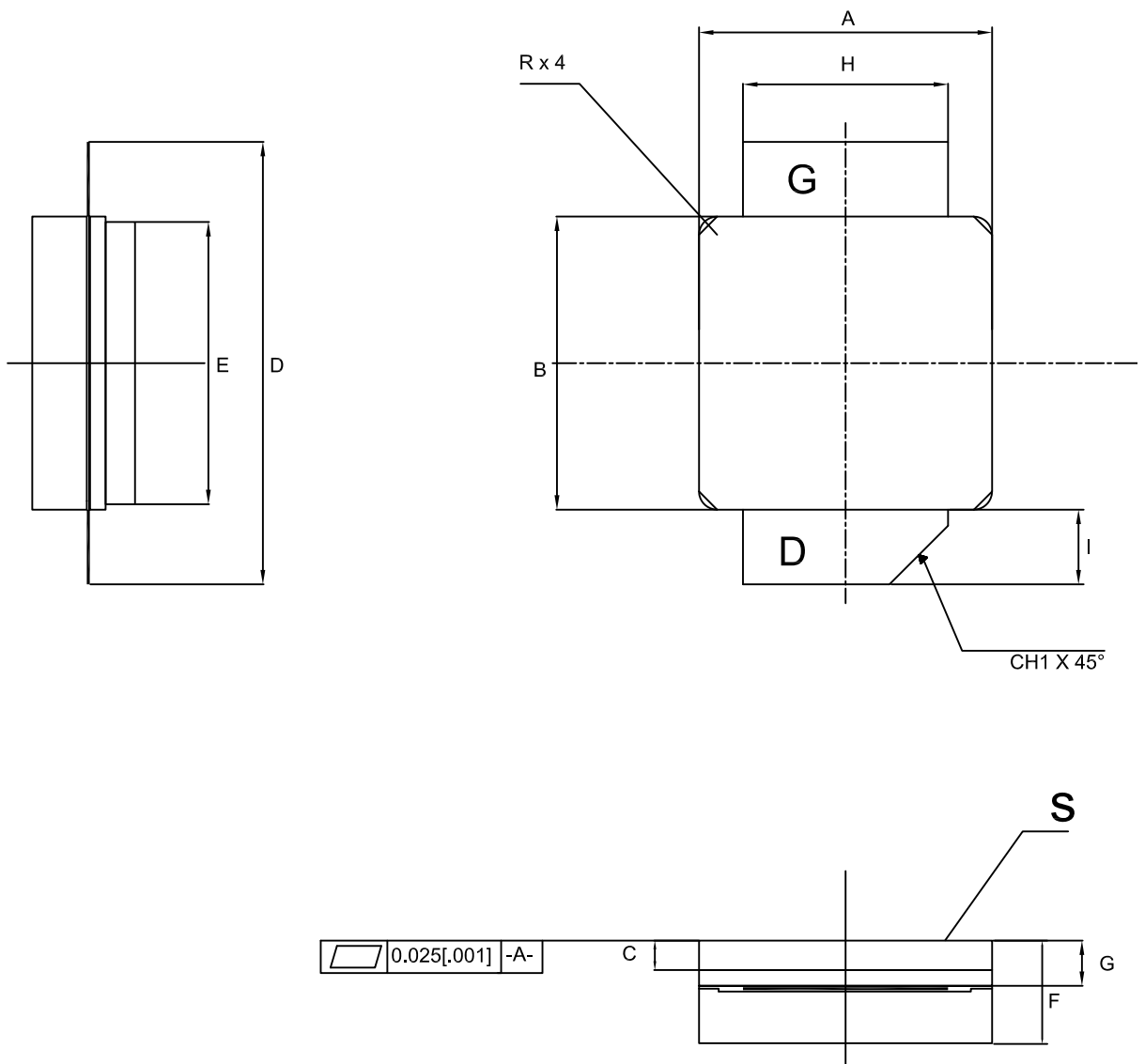


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 A2 package information

Figure 3. A2 package outline



DM00418526_2

Table 6. A2 mechanical data

Symbol	Millimetres		
	Min.	Typ.	Max.
A	10.03	10.16	10.29
B	10.03	10.16	10.29
C	0.89	1.02	1.15
D	15.21	15.34	15.47
E	9.65	9.78	9.91
F	3.43	3.56	3.69
G	1.44	1.57	1.70
H	6.98	7.11	7.24
I	2.08	2.59	3.10
CH1		2.03	
R			0.63

Revision history

Table 7. Document revision history

Date	Version	Changes
15-Oct-2018	1	Initial release.
23-Sep-2020	2	Updated Section Product status / summary, Table 5. Dynamic and Section 4.1 A2 package information.

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