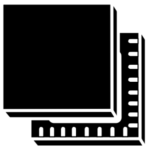
ST25R3918

Multi-purpose NFC transceiver

Datasheet - production data



VFQFPN32 (5x5 mm)

Features

- Operating modes
  - Reader/writer
  - Card emulation
  - Passive peer to peer
- RF communication
  - NFC-A / ISO14443A up to 848 kbit/s
  - NFC-B / ISO14443B up to 848 kbit/s
  - NFC-V / ISO15693 up to 53 kb/s
  - NFC-A / ISO14443A and NFC-F / FeliCa™ card emulation
  - Low level modes to implement MIFARE Classic® compliant or other custom protocols
- Key features
  - Dynamic power output (DPO) controls the field strength to stay within given limits
  - Active wave shaping (AWS) reduces over- and under-shoots
  - Noise suppression receiver (NSR) allows reception in noisy environment
  - Automatic gain control and squelch feature to maximize SNR
  - Low power capacitive and inductive card detection
  - Low power NFC passive target modes
  - Adjustable ASK modulation depth, from 5 to 40%
  - Integrated regulators to boost system PSRR
  - AM/PM and I/Q demodulator with baseband channel summation or automatic channel selection
  - Possibility to drive two independent single ended antennas
  - Measurement of antenna voltage amplitude and phase, RSSI, on-chip supply and regulated voltages
- External communication interfaces
  - 512-byte FIFO
  - Serial peripheral interface (SPI) up to 10 Mbit/s
  - I2C with up to 400 kbit/s in Fast-mode, 1 Mbit/s in Fast-mode Plus, and 3.4 Mbit/s in High-speed mode
- Electrical characteristics
  - Wide supply voltage and ambient temperature range (2.6 to 5.5 V from -40 °C to +105 °C, 2.4 to 5.5 V from -20 °C to +105 °C)
  - Wide peripheral communication supply range, from 1.65 to 5.5 V
  - Quartz oscillator capable of operating with 27.12 MHz crystal with fast start-up

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1 Applications

The ST25R3918 device is suitable for a wide range of NFC and HF RFID applications, among them

- General consumer electronics, IoT as well as NFC applications e.g. accessory recognition and parameter setting
- Brand protection, access control, customer interaction and consumer engagement
- Healthcare, gaming, beauty, power tools
- Enhanced user experience starting Apple® App Clips and Android™ Instant App via CE mode
- ISO14443 and ISO15693 compliant general purpose NFC device
- Contactless interface for programming and firmware updates
- Support of NFC Forum tag types 1, 2, 4 and 5 in reader mode
- Support of common proprietary protocols, such as MIFARE®, Kovio, CTS, B'.

2 Description

The ST25R3918 is a multipurpose NFC transceiver supporting NFC reader, passive peer to peer functionality and NFC card emulation mode.

This IC is optimized for IOT and other consumer or industrial applications where excellent analog performance is required.

The ST25R3918 is also optimized to achieve good read ranges with low output power, even under noisy and harsh environments, using noise reduction receiver technology.

This IC offers an advanced analog front end (AFE) and a highly integrated data framing system for NFC-A/B (ISO 14443A/B) reader including higher bit rates. NFC-V (ISO 15693) reader is supported up to 53 kbps via streaming mode to read cards.

ISO 18092 passive initiator and target and NFC-A / NFC-F card emulation are also available to ensure communication between end products. This enables device programming or simple NDEF data transfers to interact with Android™ phones or to use Apple®App Clips.

Special stream and transparent modes of the AFE and framing system can be used to implement other custom protocols in reader or card emulation mode.

The ST25R3918 includes a low power wakeup mode to scan for the presence of a card by performing a measurement of the amplitude or phase of the antenna signal. It also contains a low power RC oscillator and wake-up timer to automatically trigger the device after the configured time period and check for a presence of a tag.

The ST25R3918 is designed to operate from a wide power supply range (2.6 to 5.5 V from -40 °C to +105 °C, 2.4 to 5.5 V from -20 °C to +105 °C), and a wide peripheral IO voltage range (from 1.65 to 5.5 V).

2.1 System diagram

Figure 1 and *Figure 2* show the minimum system configuration for, respectively, single ended and differential antenna configurations. Both include the EMC filter.

Figure 1. Minimum system configuration - Single sided antenna driving

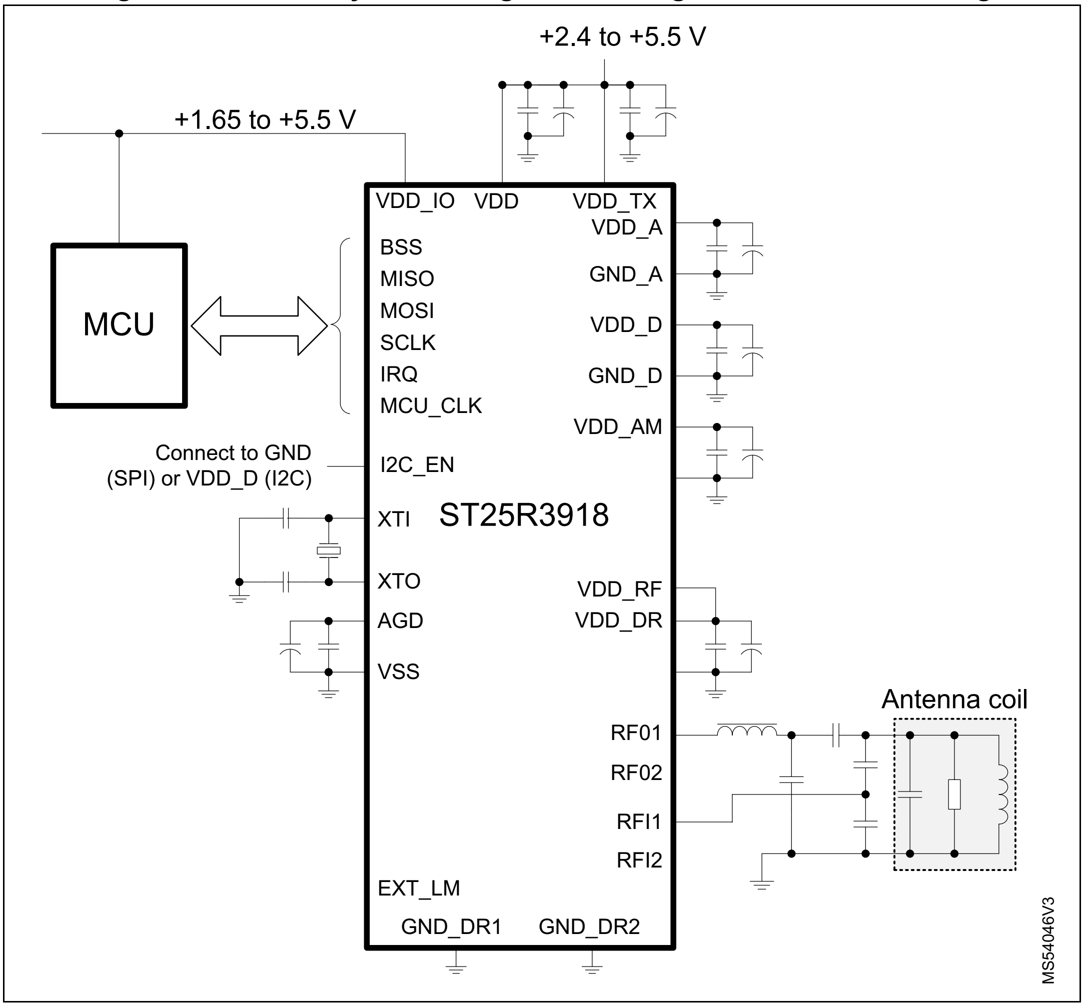
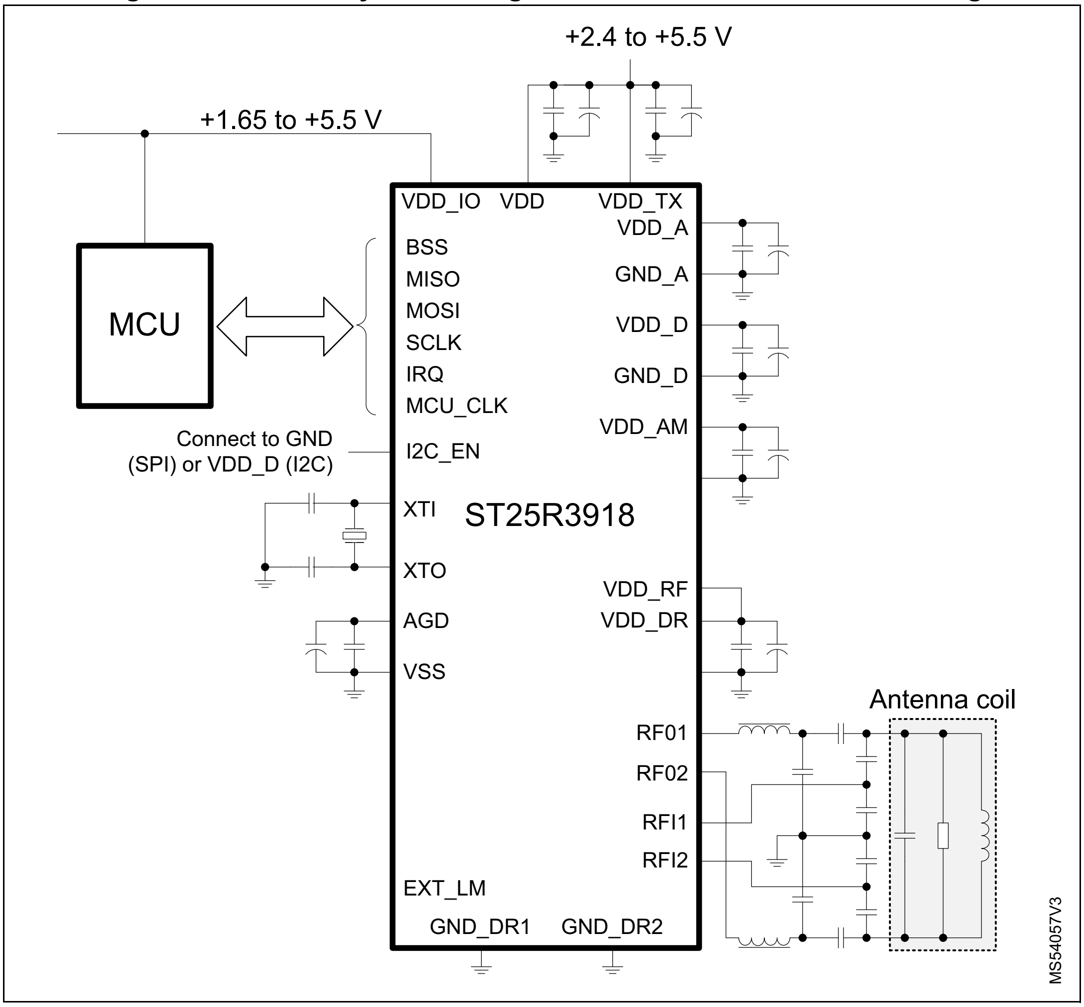


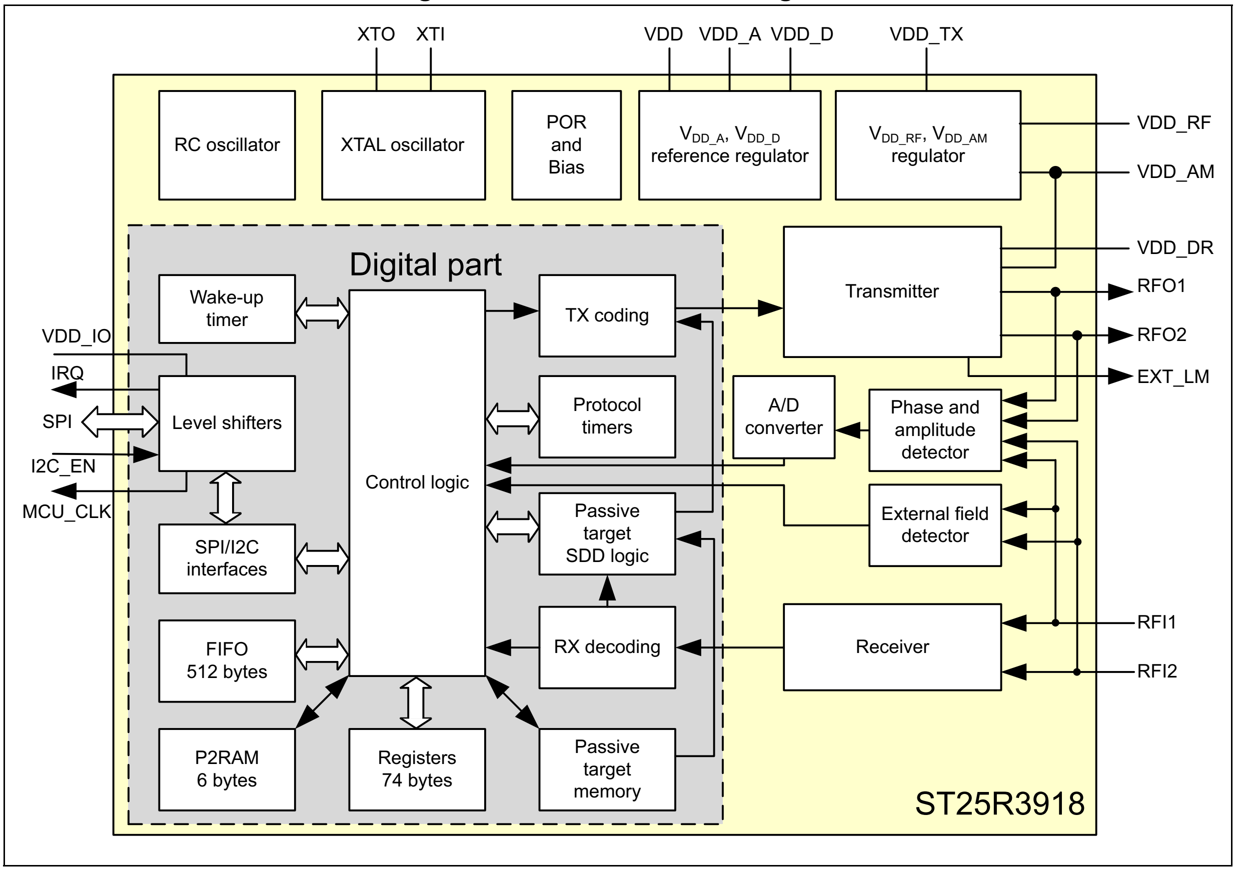
Figure 2. Minimum system configuration - Differential antenna driving



2.2 Block diagram

The ST25R3918 block diagram is shown in *Figure 3*. The main functions are described in the following subsections.

Figure 3. ST25R3918 block diagram



2.2.1 Transmitter

In reader mode, the transmitter drives an external antenna through pins RFO1 and RFO2 to generate the RF field. Single sided and differential antenna configurations are supported. The transmitter block also generates the OOK or AM modulation of the transmitted RF signal.

The transmitter can operate RFO1 and RFO2 independently, to drive up to two antennas in single ended configuration, or operate RFO1 and RFO2 together, to drive one antenna in differential configuration. The drivers are designed to drive directly one or more antennas integrated on the PCB, as well as antennas connected with 50 Ω cables. Some of the advanced features are not fully usable if the antenna is connected with a 50 Ω cable.

In card emulation mode, the transmitter generates the load modulation signal by changing the resistance of the internal antenna driver connected to the antenna via RFO1 and RFO2. To generate the load modulation signal, the transmitter can also drive an external MOS transistor via the EXT_LM pin.

2.2.2 Receiver

The receiver detects card modulation superimposed on the 13.56 MHz carrier signal. The receiver consists of two chains, built from a set of demodulators, followed by two gain and filtering stages and a final digitizer stage. The demodulators can operate as AM/PM demodulator or as I/Q demodulator. The filter characteristics can be adjusted to match the selected RF mode and bit rate, to optimize performance (subcarrier frequencies from 212 to 848 kHz are supported). Apart from the filter stage, the receiver incorporates several other features (AGC, squelch) that enable reliable operation in noisy conditions.

The receiver is connected to the antenna via the pins RFI1 and RFI2. The output of the receiver is connected to the framing block that decodes the demodulated and digitized subcarrier signal.

2.2.3 Phase and amplitude detector

The phase detector measures the phase difference between the transmitter output signals (RFO1 and RFO2) and the receiver input signals (RFI1 and RFI2).

The amplitude detector measures the amplitude of the differential RF carrier signal between the receiver inputs RFI1 and RFI2. This differential amplitude signal is directly proportional to the amplitude of the RF signal on the antenna LC tank.

The phase and amplitude detectors are used for several purposes:

- PM demodulation, by observing RFI1 and RFI2 phase variations (LF signal is fed to the receiver)
- Average phase difference between RFOx pins and RFIx pins, to check antenna tuning
- Measure amplitude of signal present on pins RFI1 and RFI2, proportional to the antenna voltage

2.2.4 A/D converter

A built-in A/D converter, whose input can be multiplexed from different sources, is used for the diagnostic functions and the low power card detection. The result of the A/D conversion is stored in a register that can be read through the host interface.

2.2.5 External field detector

This is a low power block used in the passive target mode to detect the presence of an external RF field. It supports two different external field detection thresholds, namely Peer detection and Collision avoidance threshold.

The Peer detection threshold is used in the passive peer to peer modes to detect when the peer device turns on its RF field.

The Collision avoidance threshold is used to detect the presence of an external RF field during the RF collision avoidance procedure.

2.2.6 Quartz crystal oscillator

The quartz crystal oscillator operates with 27.12 MHz crystals. At start-up the transconductance of the oscillator is increased to achieve a fast start-up. Since the start-up time varies with crystal type, temperature and other parameters, the oscillator amplitude is observed and an interrupt is generated when stable oscillator operation is reached.

The oscillator block also provides a clock signal to the external microcontroller (MCU_CLK), according to the settings in the *IO configuration register 1*.

2.2.7 Power supply regulators

The integrated power supply regulators ensures a high power supply rejection ratio (PSRR) for the complete system.

Three voltage regulators, one for the analog block, one for the digital block, and one for the RF output drivers, are available to decouple noise sources from the ST25R3918. A fourth voltage regulator generates the reference voltage for the analog receivers (AGDC, analog ground).

The RF output driver voltage regulator can be configured automatically by the ST25R3918 based on the systems power supply stability and RF output power (see *Section 4.4.10: Adjust regulators* for more details).

2.2.8 POR and bias

This block provides bias currents and reference voltages to all other blocks. It also incorporates a Power on Reset (POR) circuit that provides a reset at power-up and at low supply levels.

2.2.9 RC oscillator and Wake-up timer

The ST25R3918 include several possibilities for low power detection of a card presence (phase measurement, amplitude measurement). The RC oscillator and the register configurable Wake-up timer are used to periodically trigger the card presence detection in the low power card detection modes.

2.2.10 TX encoding

This block encodes the transmit frames according to the selected RF mode and bit rate. The SOF (start of frame), EOF (end of frame), CRC and parity bits are generated automatically. The data to transmit are taken from the FIFO.

In Stream mode the framing is bypassed. The FIFO data directly defines the modulation data sent to the transmitter.

In Transparent mode, the framing and FIFO are bypassed, and the MOSI pin directly drives the modulation of the transmitter.

2.2.11 RX decoding

This block decodes received frames according to the selected RF mode and bitrate. The SOF (start of frame), EOF (end of frame), CRC and parity bits are automatically checked, all of them (except the CRC bit) are removed by this block. The received data is written to the FIFO.

In Stream mode the framing is bypassed. The digitized subcarrier signal is directly stored in the FIFO.

In Transparent mode the framing and FIFO are bypassed. The digitized subcarrier signal directly drives the MISO pin.

2.2.12 FIFO

The ST25R3918 contains a 512-byte FIFO. Depending on the direction of the data transfer, it contains either data which has been received or data which is to be transmitted.

In reader mode the ST25R3918 can transmit frames of up to 8191 bytes length and receive frames of arbitrary length.

2.2.13 Control logic

The control logic contains I/O registers that define the operation of device.

2.2.14 Host interface

A 4-wire serial peripheral interface (SPI) and a 2-wire I2C interface are available to communicate with an external microcontroller. The pins for the SPI and the I2C interface are shared, and pin I2C_EN is used to select the active interface.

2.2.15 Passive target memory

The device contains a 48-byte RAM to store configuration data for the passive target and card emulation mode.

2.2.16 P2RAM

The P2RAM stores information on wafer number, die position, device subversion, and I2C address. The P2RAM is programmed during production.

3 Pin and signal description

Figure 4. ST25R3918 QFN32 pinout (top view)

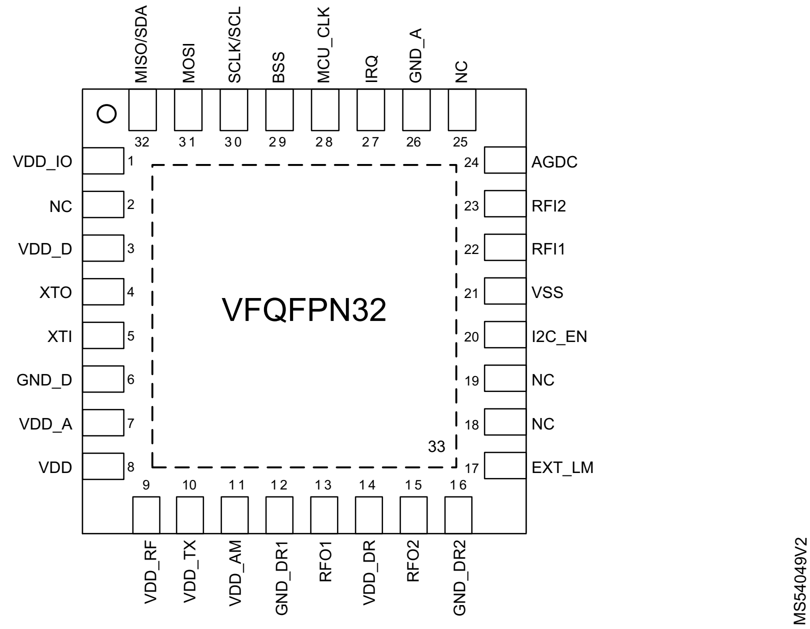


Table 1. ST25R3918 - VFQFPN32 pin assignment

VFQFPN32	Name	Type(1)	Description
1	VDD_IO	P	Positive supply for peripheral communication
2	NC	-	Do not connect
3	VDD_D	AO	Digital supply regulator output
4	XTO	AO	X'tal oscillator output
5	XTI	AI/DI	X'tal oscillator input, in test mode used as digital input (clock)
6	GND_D	P	Digital ground
7	VDD_A	AO	Analog supply regulator output
8	VDD	P	External positive supply
9	VDD_RF	AO	Regulated driver supply for antenna drivers
10	VDD_TX	P	External positive supply for the TX part
11	VDD_AM	AO	Regulated driver supply for AM modulation
12	GND_DR1	P	Antenna driver ground, including driver V_{SS}
13	RFO1	AO	Antenna driver output
14	VDD_DR	P	Antenna driver positive supply input
15	RFO2	AO	Antenna driver output
16	GND_DR2	P	Antenna driver ground, including driver V_{SS}
17	EXT_LM	AO	External load modulation MOS gate driver

Table 1. ST25R3918 - VFQFPN32 pin assignment (continued)

VFQFPN32	Name	Type(1)	Description
18	NC	-	Do not connect
19	NC	-	Do not connect
20	I2C_EN	DI	I2C interface enable (V_{DD_D} level)
21	VSS	P	Ground, die substrate potential
22	RFI1	AI	Receiver input
23	RFI2	AI	Receiver input
24	AGDC	AIO	Analog reference voltage
25	NC	-	Do not connect
26	GND_A	P	Analog ground
27	IRQ	DO	Interrupt request output
28	MCU_CLK	DO	Clock output for MCU
29	BSS	DI	SPI enable (active low)
30	SCLK	DI	SPI clock / I2C clock
31	MOSI	DI	SPI data input
32	MISO	DO_T	Serial peripheral interface data output / I2C data line
33	NA	P	Thermal pad

1. P: Power supply pin
AIO: analog I/O, AI: analog input, AO: analog output
DI: digital input, DIPD: digital input with pull-down, DO: digital output, DO_T: digital output/tri-state, DIO: digital bidirectional.

4 Application information

4.1 Power-on sequence

Once powered, the device enters the Power-down mode where the content of all registers is set to its default state.

To prevent the internal overheat protection to trigger below the junction temperature, the 3-byte frame FCh / 04h / 10h (register access / address / value) has to be sent after power-on and Set default command.

The next steps are basic configurations of the IC:

1. The *IO configuration register 1* and *IO configuration register 2* must be properly configured.
2. The internal voltage regulators have to be configured. It is recommended to use direct command Adjust regulators to improve the system PSRR.

After the sequence of events mentioned above the devices are ready to operate.

4.2 Operating modes

The ST25R3918 operating mode is defined by the contents of the *Operation control register*. At power-on all its bits are set to 0, the ST25R3918 is in Power-down mode. In this mode, the AFE static power consumption is minimized, as only the POR and part of the bias are active. The regulator itself is disabled.

The SPI/I2C is still functional in this mode and all required settings on the configuration registers can be done. The PT_memory and FIFO are not accessible in this mode.

Bit en (bit 7 of the *Operation control register*) is controlling the quartz crystal oscillator and regulators. When this bit is set, the device enters in Ready mode and the quartz crystal oscillator and regulators are enabled. An interrupt is sent to inform the microcontroller when the oscillator amplitude and frequency is stable. The PT_memory and FIFO are accessible in this mode.

The enable of the receiver and the transmitter block are separated, it is possible to operate one without switching on the other (control bits rx_en and tx_en). This feature can be used when the reader field has to be maintained while no response from a tag is expected.

Asserting the *Operation control register* bit wu while the other bits are set to 0 puts the ST25R3918 into the Wake-up mode, used to perform low power detection of card presence. In this mode the low power RC oscillator and register configurable wake-up timer are used to schedule periodic measurement(s). When a difference to the predefined reference is detected an interrupt is sent to wake up the MCU. Phase and amplitude measurement are available to trigger the wake-up.

4.2.1 Transmitter

The transmitter contains two identical push-pull driver blocks connected to pins RFO1 and RFO2. These drivers are differentially driving the external antenna LC tank. It is also possible to operate only one of the two drivers by setting the *IO configuration register 1* bit single and selecting which RFO/RFI to be use on bit rfo2.

Output resistance

Each driver is composed of eight segments having binary weighted output resistance. When all segments are turned on, the output resistance is typically 8 Ω. Usually all segments are turned on to define the normal transmission (non-modulated) level. It is also possible to switch off certain MSB segments when driving the non-modulated level to drive the circuitry with a higher impedance driver.

The bits d_res<3:0> in the *TX driver register* define the resistance during the normal transmission. The default setting is minimum available resistance.

When using the single driver mode, the number and therefore the cost of the antenna LC tank components is halved, but also the output power is reduced. In single mode it is possible to connect two antenna LC tanks to the two RFO outputs and multiplex between them by controlling the *IO configuration register 1* bit rfo2.

To transmit data, the transmitter output level needs to be modulated. AM and OOK modulation principles are supported. The type of modulation is defined by setting bit tr_am in the *Mode definition register*.

Driver TX modulation

During the OOK modulation (e.g. for ISO14443A) the transmitter drivers stop driving the carrier frequency. As a consequence the amplitude of the antenna LC tank oscillation decays, the time constant of the decay is defined with the LC tank Q factor.

AM modulation (for example ISO14443B) is done via an additional regulator providing the supply voltage V_{DD_AM}, used as the driver supply voltage during the modulation state.

The AM modulation level is set by am_mod3:0 bits in the *TX driver register*.

AM modulation has to be manually enabled and the level to be set correctly for the following protocols:

- ISO14443B
- ISO15693 (if not OOK)

Depending on the applicable standard the modulation index can be set in a range between 5 and 30% in the *TX driver register*.

Passive load modulation

The ST25R3918 enables passive load modulation using two different methods

- Internal driver load modulation
- Load modulation with an external MOS transistor and a diode that directly loads the antenna circuit

The driver load modulation is selected by bit lm_dri and the external MOS modulation is selected by lm_ext option bits.

Normally, the internal driver or the external load modulation should be used exclusively, but the device also allows simultaneous modulation.

The driver load modulation is based on the change of driver impedance. Typically, a high impedance during non-modulated state and a lower impedance for the modulated state is used. This yields modulation phase equal to passive tag modulation. It is also possible to reverse the polarity of the driver load modulation by using low impedance during non-modulated state and higher impedance for the modulated state.

During the non-modulated state the output impedance is defined by pt_res3:0 option bits. During modulation the output impedance is defined by ptm_res3:0 option bits.

Load modulation through an external MOS transistor and a diode is selected by the lm_ext option bit. In this case the EXT_LM pin is driven by the digital representation of the load modulation signal (848 kHz subcarrier or 424 / 212 kHz modulation signal). The EXT_LM is used to drive a gate of the external modulation MOS. The bit lm_ext_pol sets inverse polarity for the external load modulation.

The pt_res3:0 and ptm_res3:0 bits must be set prior entering passive target mode (reg 03h), because in passive target mode the resistance value propagates through the TX driver only when the extracted clock is available.

Driver load modulation is based on change of the driver impedance. Typically high impedance is used during non-modulated state, and decreased for modulated state, resulting in modulation phase equal to Passive tag modulation.

It is also possible to set inverse polarity driver load modulation by using low impedance during non-modulated state and higher impedance for the modulated state.

During non-modulated / modulated state the output impedance is defined, respectively, by pt_res3:0 / ptm_res3:0 option bits.

An external MOS transistor and a diode modulation is selected by lm_ext option bit. In this case the EXT_LM pin is driven by digital representation of the load modulation signal (848 kHz subcarrier or 424 / 212 kHz modulation signal). The EXT_LM is used to drive a gate of the external modulation MOS.

Bit lm_ext_pol sets inverse polarity for the External load modulation.

Bits pt_res<3:0> and ptm_res<3:0> must be set before entering Passive target mode (reg 03h), as in Passive target mode the resistance value propagates through the TX driver only when extracted clock is available (during PT data transmission, including FDT).

Slow transmitter ramping

When the transmitter is enabled it starts to drive the antenna LC tank with full power, the ramping of field emitted by antenna is defined by antenna LC tank Q factor.

However there are some reader systems where the reader field has to ramp up with a longer transition time when it is enabled. The STIF (Syndicat des transports d'Ile de France) specification requires a transition time from 10 to 90% of field longer than or equal to 10 µs.

The ST25R3918 supports slow transmitter ramping by collapsing VDD_RF regulated voltage when transmitter is disabled and ramping it when transmitter is enabled. Typical transition time is 15 µs at 3 V supply and 20 µs at 5 V supply.

Procedure to implement the slow transition:

1. When transmitter is disabled set *IO configuration register 2* bit slow_up to 1. Keep this state at least 2ms to allow discharge of V_{DD_RF}.
2. Enable transmitter, its output will ramp slowly
3. Before sending any command set the bit slow_up back to 0.

4.2.2 Receiver

The receiver performs demodulation of the tag subcarrier modulation that is superimposed on the 13.56 MHz carrier frequency. It performs AM/PM or I/Q demodulation, amplification, band-pass filtering and digitalization of subcarrier signals. It also performs RSSI measurement, automatic gain control (AGC) and Squelch function.

The reception chain has two separate channels for AM and PM demodulation. When both channels are active the selection for reception framing is done automatically by the receiver logic. The receiver is switched on when *Operation control register* bit rx_en is set to 1.

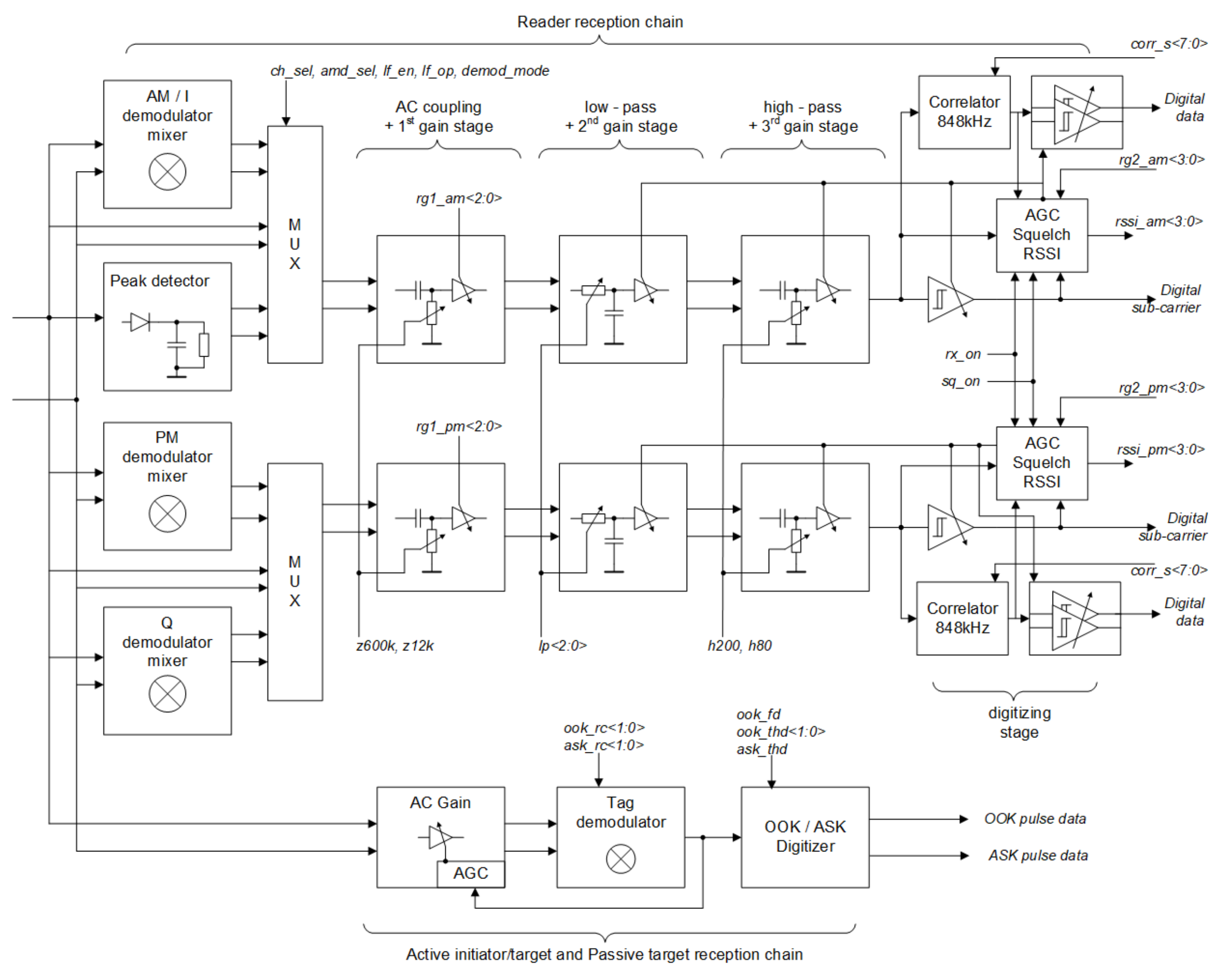
The *Operation control register* contains bits rx_chn and rx_man, which define whether only one or both demodulation channels are active:

- bit rx_man defines the channel selection mode when both channels are active (automatic or manual)
- bit ch_sel defines which channel is used for decoding.

Table 2. RX channel selection

rx_chn	rx_man	ch_sel	Selected reception channel
0	0	x	Automatic selection
0	1	0	AM or I channel
0	1	1	PM or Q channel
1	x	0	AM or I channel
1	x	1	PM or Q channel

Figure 5. Receiver block diagram



Demodulation stage

The first stage performs demodulation of the tag subcarrier response signal, superimposed on the HF field carrier. Two different blocks are implemented for the AM demodulation:

- peak detector
- AM/I or PM/Q demodulator mixer.

The choice of the used demodulator is made by the *Receiver configuration register 2* bit amd_sel.

The peak detector performs AM demodulation using a peak follower. Both the positive and negative peaks are tracked to suppress any common mode signals. Its demodulation gain is G = 0.7 and the input is taken from RFI1 demodulator input only.

The AM demodulator mixer uses synchronous rectification of both receiver inputs (RFI1 and RFI2). Its gain is G = 0.55. The PM demodulation is also done by a mixer. The PM demodulator mixer has differential outputs with 60 mV differential signal for 1% phase change (16.67 mV / °).

The I/Q demodulation is composed of two mixer circuits, driven with a 90° shifted local oscillator (LO) signals derived from the crystal oscillator. The outputs of the two mixers are connected to two equal base band reception chains and to the decoding logic.

Filtering and gain stages

The receiver chain has band pass filtering characteristics. The filtering is optimized to pass subcarrier frequencies while rejecting carrier frequency, low frequency noise and DC component. Filtering and gain is implemented in three stages, the first and the last stage have first order high pass characteristics while the mid stage has second order low-pass characteristic.

The gain and filtering characteristics can be optimized depending on the application by writing the *Receiver configuration register 1* (filtering), *Receiver configuration register 3* (primarily gain in first stage) and *Receiver configuration register 4* (gain in second and third stage).

The gain of first stage is around 20 dB and can be reduced in six 2.5 dB steps. There is also a special boost mode available, which increases the max gain by additional 5.5 dB. The first stage gain can only be modified by writing *Receiver configuration register 3*. The default setting of this register is the minimum gain. Default first stage zero is located at 60 kHz, it can also be lowered to 40 or 12 kHz by writing option bits in the *Receiver configuration register 1*. The first stage can be reconfigured to second order high-pass at 600 kHz by option bit z600k. The control of the first and third stage zeros is done with common control bits (see *Table 4*).

Table 3. Low-pass control

rec1<5>lp2	rec1<4>lp1	rec1<3>lp0	-1 dB point
0	0	0	1200 kHz
0	0	1	600 kHz
0	1	0	300 kHz
1	0	0	2 MHz
1	0	1	7 MHz
Others			Not used

Table 4. First and third zero setting

rec1<3>z600k	rec1<2>h200	rec1<1>h80	rec1<0>z12k	First stage zero	Third stage zero
0	0	0	0	60 kHz	400 kHz
0	1	0	0		200 kHz
0	0	1	0	40 kHz	80 kHz
0	0	0	1	12 kHz	200 kHz
0	0	1	1		80 kHz
0	1	0	1		200 kHz
1	0	0	0	600 kHz	400 kHz
1	1	0	0		200 kHz
Others				Not used	

The gain in the second and third stage is 23 dB and can be reduced in six 3 dB steps. Gain of these two stages is included in AGC and Squelch loops or can be manually set in

Receiver configuration register 4. Sending of direct command Reset RX Gain is necessary to initialize the AGC, Squelch and RSSI block. Sending this command clears the current Squelch setting and loads the manual gain reduction from *Receiver configuration register 4*. Second stage has a second order low-pass filtering characteristic, the pass band is adjusted according to subcarrier frequency using the bits lp2 to lp0 of the *Receiver configuration register 1*. See *Table 3* for -1 dB cut-off frequency for different settings.

Digitizing stage

The digitizing stage produces a digital representation of the sub-carrier signal coming from the receiver. This digital signal is then processed by the receiver framing logic. The digitizing stage consists of a window comparator with adjustable digitizing window (five possible settings, 3 dB steps, adjustment range from ±33 to ±120 mV). The adjustment of the digitizing window is included in the AGC and Squelch loops. The digitizing window can also be set manually in the *Receiver configuration register 4*.

AGC, Squelch and RSSI

As mentioned above, the second and third gain stage gain and the digitizing stage window are included in the AGC and Squelch loops. Eleven settings are available. The default state features minimum digitizer window and maximum gain. The first four steps increase the digitizer window in 3 dB steps, the next six steps reduce the gain in the second and third gain stage, again in 3 dB steps. The initial start setting for Squelch and AGC is defined in *Receiver configuration register 4*. The *Gain reduction state register* displays the actual state of gain resulting from Squelch, AGC and initial settings in *Receiver configuration register 4*.

Squelch

This feature is designed for operation in noisy environments. The noise can be misinterpreted as the start of tag response, resulting in decoding errors.

Automatic squelch is enabled by option bit sqm_dyn in the *Receiver configuration register 2*. It is activated automatically 18.88 µs after end of TX and is terminated at the moment the Mask receive timer (MRT) reaches the value defined in the *Squelch timer register*. This mode is primarily intended to suppress noise generated by tag processing during the time when the tag response is not expected (covered by MRT).

Squelch can operate in two modes, namely with ratios 1 and 6, selectable by pulz_61 bit in the *Receiver configuration register 2*.

Squelch ratio 1 means that system observes the subcarrier signal from the main digitizer and decrease the system gain to decrease the frequency of transitions. If there are more than two transitions on this output in a 50 µs time period, gain is reduced by 3 dB and output is observed during the following 50 µs. This procedure is repeated until number of transitions in 50 µs is lower or equal to 2 or until the maximum gain reduction is reached. This mode is intended for protocols where digitized subcarrier outputs are used.

Squelch ratio 6 means the system similarly observes and decreases the frequency seen at the window comparator set to 6 times the digitizing window. This mode is intended for protocols where output from correlators are used (ISO-A, ISO-B correlated reception).

The gain setting acquired by squelch is cleared by sending direct command *Reset RX gain*.

AGC

The AGC (automatic gain control) can reduce the gain to keep the receiver chain and input to the digitizing stage out of saturation. The demodulation process is also less influenced by system noise when the gain is properly adjusted.

The AGC logic starts operating when the signal rx_on is asserted to high and is reset when it is reset to low. The state of the receiver gain is stored in the *Gain reduction state register* during a high to low transition of bit rx_on. Reading this register later on gives information of the gain setting used during the last reception.

The AGC system comprises a window comparator and an AGC ratio that can be set to 3 or to 6. As an example, when the AGC ratio is set to 6 the window is six times larger than the data digitalization window comparator. When the AGC function is enabled the gain is reduced until there are no transitions on its output. Such procedure assures that the input to digitalization window comparator is up to 6 times larger than its window.

If the AGC ratio is set to three, the input to the digitalization window comparator is set to be up to 3 times larger than its window.

The AGC operation is controlled by the control bits agc_en, agc_m, agc_alg, and agc6_3 in *Receiver configuration register 2*.

The bit agc_m defines the AGC mode when two AGC modes are available. The AGC can operate during the complete RX process as long as the signal rx_on is high and it can be enabled only during first eight subcarrier pulses.

There are two AGC algorithms to choose from bit agc_alg. The AGC can start either by pre-setting (maximum digitizer window and maximum gain) or by resetting (minimum digitizer window and maximum gain) it. The algorithm with preset is faster and therefore recommended for protocols with short SOF (like ISO14443A at 106 kbps).

Correlator

The correlators correlate the incoming filtered subcarrier with 848 kHz. The aim of the correlation is to maximize the system sensitivity at 848 kHz, while rejecting other frequencies. There are two correlators in the system for AM (or I) channel and PM (or Q) channel.

Correlator settings are defined in *Correlator configuration register 1* and *Correlator configuration register 2*.

RSSI

The receiver also performs the RSSI (received signal strength indicator) measurement for both channels. The RSSI measurement is started after the rising edge of rx_on. It stays active while the signal rx_on is high and frozen while rx_on is low. It is a peak hold system where the value can only increase from initial 0 value. Every time the AGC reduces the gain the RSSI measurement is reset and starts from 0. The result of RSSI measurements is a 4-bit value that can be observed by reading the *RSSI display register*. The LSB step is 2.8 dB, the maximum value is Dh (13d).

Since the RSSI measurement is of peak hold type, the result does not follow any variations in the signal strength (the highest value will be kept). To follow RSSI variation it is possible to reset RSSI bits and restart the measurement by sending direct command *Clear RSSI*.

Clock extractor

The clock extractor observes the RFI1 and RFI2 differential signal and provides a clock signal synchronous with the incoming RF field. The extracted clock is used for synchronous demodulation, for correct frame delay time and for correct data timing during passive transmission. The clock extractor is active down to 60 mV_{PP} input signal.

4.2.3 Wake-up mode

Asserting the *Operation control register* bit wu while the other bits are set to 0 puts the ST25R3918 into the Wake-up mode, used to perform low power detection of card presence. The ST25R3918 features phase and amplitude measurement for the Wake-up mode. An integrated low power 32 kHz RC oscillator and register configurable Wake-up timer are used to schedule periodic detection.

Usually the presence of a card is detected by a so-called polling. In this process the reader field is periodically turned on and the controller checks whether a card is present using RF commands. This procedure consumes a lot of energy since reader field has to be turned on for 5 ms before a command can be issued.

Low power detection of card presence is performed by detecting a change in the reader environment, produced by a card. When a change is detected, an interrupt is sent to the controller. As a result, the controller can perform a regular polling loop.

In Wake-up mode the ST25R3918 periodically performs the configured reader environment measurements, and sends an IRQ to the controller when a difference to the configured reference value is detected.

Card detection

The presence of a card close to the reader antenna coil produces a change of the antenna LC tank signal phase and amplitude. The reader field activation time needed to perform the phase or the amplitude measurement is extremely short (~20 µs) compared to the activation time needed to send a protocol activation command.

The power level during the measurement can be lower than that during normal operation as the card does not have to be powered to produce a coupling effect. The emitted power can be reduced by changing the RFO driver resistance.

Registers from 32h to 3Ah are dedicated to Wake-up configuration and display. The *Wake-up timer control register* is the main Wake-up mode configuration register. The timeout period between the successive detections and the measurements to be used are selected in this register. Timeouts in the range from 10 to 800 ms are available, 100 ms being the default value.

Registers from 33h to 3Ah configure the possible detection measurements and store the results, four registers are used for each method.

An IRQ is sent when the difference between a measured value and reference value is larger than configured threshold value. There are two possibilities how to define the reference value:

- The ST25R3918 can calculate the reference based on previous measurements (auto-averaging)
- The controller determines the reference and stores it in a register.

The first register in the series of four is the *Amplitude measurement configuration register*. The difference to reference, which triggers the IRQ, the method of reference value definition, and the weight of last measurement result in case of auto-averaging are defined in this register. The next register stores the reference value when the reference is defined by the controller. The following two registers are display registers: the first one stores the auto-averaging reference, the second one stores the result of the last measurement.

Wake-up mode configuration registers must be configured before Wake-up mode is actually entered. Any modification of Wake-up mode configuration while it is active can result in unpredictable behavior.

Auto-averaging

In case of auto-averaging, the reference value is recalculated after every measurement. The last measurement value, the old reference value and the weight are used in this calculation. The following formula is used to calculate the new reference value:

new_reference = old_reference - (old_reference - measured_value) / weight

The calculation is done on 10 bits to have sufficient precision.

The auto-averaging process is initialized when Wake-up mode is entered for the first time after initialization (power-up or using *Set default* command). The initial value is taken from the measurement reference register (for example *Amplitude measurement reference register*) if the content of this register is not 0. If content of this register is 0, the result of the first measurement is taken as initial value.

Every measurement configuration register contains a bit defining whether the measurement that causes an interrupt is taken in account for the average value calculation (for example bit am_aam of *Amplitude measurement reference register*).

4.2.4 Quartz crystal oscillator

The quartz crystal oscillator operates with 27.12 MHz crystals; its operation is enabled when the *Operation control register* bit en is set to 1. An interrupt is sent to inform the microcontroller when the oscillator amplitude is sufficiently high, meaning that the frequency is stable (see *Main interrupt register*).

The status of oscillator can be observed by checking the *Auxiliary display register* bit osc_ok. This bit is set to 1 when the oscillator frequency is stable.

The oscillator is based on an inverter stage supplied by a controlled current source. A feedback loop controls the bias current to regulate amplitude on XTI pin to 1 V_{PP}. To enable a fast reader start-up, an interrupt is sent when the oscillator amplitude exceeds 750 mV_{PP}.

Division by two assures that the 13.56 MHz signal has a duty cycle of 50%, which is better for the transmitter performance (no PW distortion).

The oscillator output is also used to drive a clock signal output pin MCU_CLK, which can be used by the external microcontroller. The MCU_CLK pin is configured in the *IO configuration register 2*.

4.2.5 Timers

Several timers are integrated in the device, to eliminate the need to run counters in the controller, thus reducing the effort of code implementation and improve its portability to different controllers.

Every timer has one or more associated configuration registers in which the timeout duration and different operating modes are defined. These configuration registers have to be set while the corresponding timer is not running. Any modification of timer configuration while the timer is active can result in unpredictable behavior.

All timers are stopped by the direct command *Stop all activities*.

Mask receive timer (MRT)

In Reader mode this timer is blocking the receiver and reception process in framing logic by keeping the rx_on signal low after the end of TX during the time the tag reply is not expected. While Mask Receive timer is running the Squelch is automatically turned on when enabled. The MRT does not produce an IRQ.

The MRT timeout is configured in the *Mask receive timer register* and is automatically started at the end of data transmission (at the end of EOF).

The MRT can be triggered by direct command Start Mask-receive timer. In this case the squelch is enabled, according to the *Squelch timer register*.

In the NFCIP-1 Passive Target communication mode the MRT is started when the other device turns on its field and the external field detector signals I_eon.

MRT supports a longer timing needed for NFCIP1 by setting option bit mrt_step. The bit switches between fc / 64 and fc / 512 step size.

The MRT starts also in the low power Initial NFC target mode. After the initiator field has been detected the controller turns on the 27 kHz RC oscillator, regulator, crystal oscillator, receiver and MRT. After the MRT expires the receiver output starts to be observed to detect start of the initiator message.

For correct operation in the low power Initial NFC target mode the mrt_step = 1 must be used. The 27 kHz RC oscillator is used as a MRT clock source for the time before the crystal oscillator stabilises. This enables that the actual MRT time is a good approximation to the targeted time, also in case the crystal oscillator is not running yet.

No-response timer (NRT)

The purpose of this timer is intended to observe whether a response is detected during a configured time started by end of transmission. The I_nre flag in the *Timer and NFC interrupt register* is signaling interrupt events resulting from this timer timeout.

The NRT is configured by writing *No-response timer register 1* and *No-response timer register 2*). Operation options are defined by setting bits nrt_emv and nrt_step in the *Timer and EMV® control register*.

The NRT is automatically started at the end of transmission.

Bit nrt_step configures the time step of the No-response timer. Two steps are available, 64/fc (4.72 µs) and 4096/fc, covering, respectively, the range up to 309 ms and up to 19.8 s.

Bit nrt_emv controls the timer operation mode.

- When this bit is set to 0 (default mode) the IRQ is produced if the NRT expires before a start of a response is detected. The rx_on is set low to disable the receiver. In the opposite case, when the start of a tag reply is detected before timeout, the timer is stopped, and no IRQ is produced.
- When this bit is set to 1 the timer unconditionally produces an IRQ when it expires, it is also not stopped by direct command Stop all activities. This means that the IRQ is independent from whether or not a tag reply was detected. When a tag reply is being processed during a timeout, no other action is taken and the reply is normally received.

In the opposite case, when no tag response is being processed, the receiver is disabled.

The NRT can also be started using direct command Start No-response timer. The intention of this command is to extend the No-response timer timeout beyond the range defined in the No-response timer control registers. If this command is sent while the timer is running, it is reset and restarted.

The NRT can be terminated using direct command Stop No-response Timer or *Stop all activities*. The timer is terminated and no IRQ is sent. It is expected to be used in the nrt_emv mode, when the incoming reception does not stop the No-response timer.

In the Passive target mode the No-response timer has no task and is not automatically started.

General purpose (GP) timer

The triggering of the this timer is configured by setting the *Timer and EMV® control register*. It can be used to survey the duration of reception process (triggering by start of reception, after SOF) or to time out the PCD to PICC response time (triggered by end of reception, after EOF).

The GP timer can also be started by sending the direct command Start General purpose timer. If this command is sent while the timer is running, it is reset and restarted.

Wake-up (WU) timer

This timer is primarily used in the Wake-up mode, it can be used by sending the direct command Start Wake-up Timer. This command is accepted in any operation mode except Wake-up mode. When this command is sent the RC oscillator, which is used as clock source for wake-up timer is started, timeout is defined by setting the *Wake-up timer control register*. When the timer expires, an IRQ with the I_wt flag in the *Error and wake-up interrupt register* is sent.

The WU timer is used in the Power-down mode, in which other timers cannot be used because the crystal oscillator, which is the clock source for the other timers, is not running. Note that the tolerance of wake-up timer timeout is defined by tolerance of the RC oscillator.

In low-power bit-rate detection mode the WU timer is used for time out the temporary device enable after the initial peer field on was detected.

4.2.6 A/D converter

The ST25R3918 contains an 8-bit successive approximation A/D converter. Inputs can be multiplexed from different sources to be used in several direct commands and adjustment procedures. The result of the last conversion is stored in the *A/D converter output register*. Typical conversion time is 224/fc (16.5 µs).

The A/D converter has two operating modes, absolute and relative.

- In absolute mode the low reference is 0 V and the high reference is 2 V. This means that A/D converter input range is from 0 to 2V, 00h code means input is 0 V or lower, FFh means that input is 2 V - 1 LSB or higher, LSB being 7.8125 mV.
- In relative mode low reference is 1/11 of V_{DD_A} and high reference is 10/11 of V_{DD_A}, so the input range is from 1/11 V_{DD_A} to 10/11 V_{DD_A}.

Relative mode is only used in phase measurement (phase detector output is proportional to power supply). In all other cases absolute mode is used.

4.2.7 Phase and amplitude detector

This block is used to provide inputs to the A/D converter to perform measurements of amplitude and phase, expected by direct commands *Measure amplitude* and *Measure phase*.

Phase detector

The phase detector observes phase difference between the transmitter output signals (RFO1 and RFO2) and the receiver input signals RFI1 and RFI2, proportional to the signal on the antenna LC tank. These signals are first passed by digitizing comparators. Digitized signals are processed by a phase detector with a strong low-pass filter characteristics to get the average phase difference. The phase detector output is inversely proportional to the phase difference between the two inputs. The 90° phase shift results in $V_{DD\_A}/2$ output voltage, if both inputs are in phase the output voltage is V_{DD_A}, if they are in opposite phase the output voltage is 0 V. During execution of direct command *Measure phase* this output is multiplexed to the A/D converter input (A/D converter is in relative mode during the execution of this command). Since the A/D converter range is from 1/11 V_{DD_A} to 10/11 V_{DD_A} the actual phase detector range is from 17º to 163º. *Figure 6* and *Figure 7* show the two inputs and output of phase detector in case of 90º and 135º phase shift, respectively.

Figure 6. Phase detector inputs and output in case of 90º phase shift

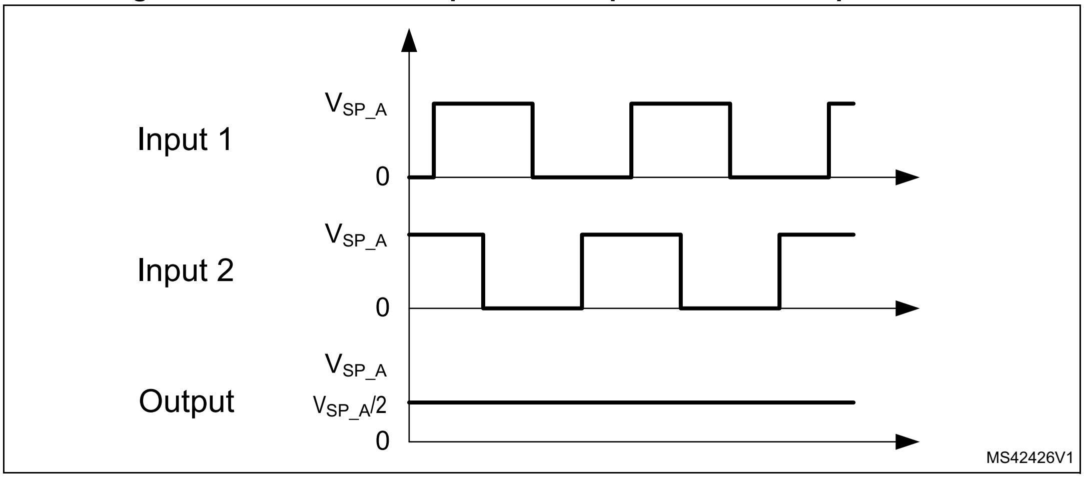
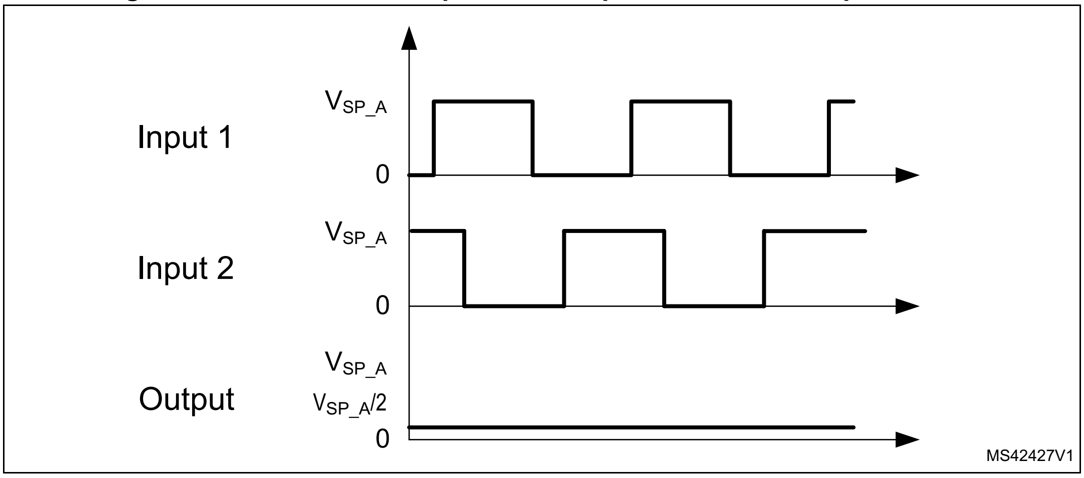


Figure 7. Phase detector inputs and output in case of 135º phase shift



Amplitude detector

Signals from pins RFI1 and RFI2 are used as inputs to the self-mixing stage. The output of this stage is a DC voltage proportional to the amplitude of signals on pins RFI1 and RFI2. During execution of direct command *Measure amplitude* this output is multiplexed to the A/D converter input.

4.2.8 External field detector

This block is used to detect the presence of an external device generating an RF field. It is used in Passive target modes. It is enabled by en_fd_c<1:0> option bits. The external field detector supports two different detection thresholds, namely Peer detection and Collision avoidance. The two thresholds can be independently set by writing the *External field detector activation threshold register*. The actual state of the detector output can be checked by reading the *Auxiliary display register*. Input to this block is the signal from the RFI1 pin.

For both thresholds there is a possibility to separately set the activation and deactivation levels.

If the External field level is not detected yet, the Activation threshold is used. If the External field level is detected, the Deactivation threshold is used.

The Activation threshold must be set higher than or equal to the Deactivation threshold.

If the Activation is higher than the Deactivation, the hysteresis is given by the difference between the two levels.

If the Activation and Deactivation levels are equal, there is no the hysteresis in the system and multiple field-on/off events can verify if the actual field level persists in proximity of the selected threshold.

Peer detection threshold

This threshold is used to detect the field emitted by peer NFC device with whom NFC communication is going on. It can be selected in the range from 75 to 800 mV_{PP}. When this threshold is enabled the detector is in low power mode. An interrupt is generated when an external field is detected and also when it is switched off. With such implementation it can also be used to detect the moment when the external field disappears. This can be used to detect the moment when the peer NFC device (either an initiator or a target) has stopped emitting an RF field.

The External Field Detector is enabled in low power Peer Detection mode by setting bits en_fd_c,1:0> in the *Operation control register*.

Collision avoidance threshold

This threshold is used during the RF collision avoidance sequence, which is executed by sending NFC Field ON commands (see *Section 4.4.5*). It can be selected in the range from 25 to 800 mV_{PP}.

4.2.9 Power supply system

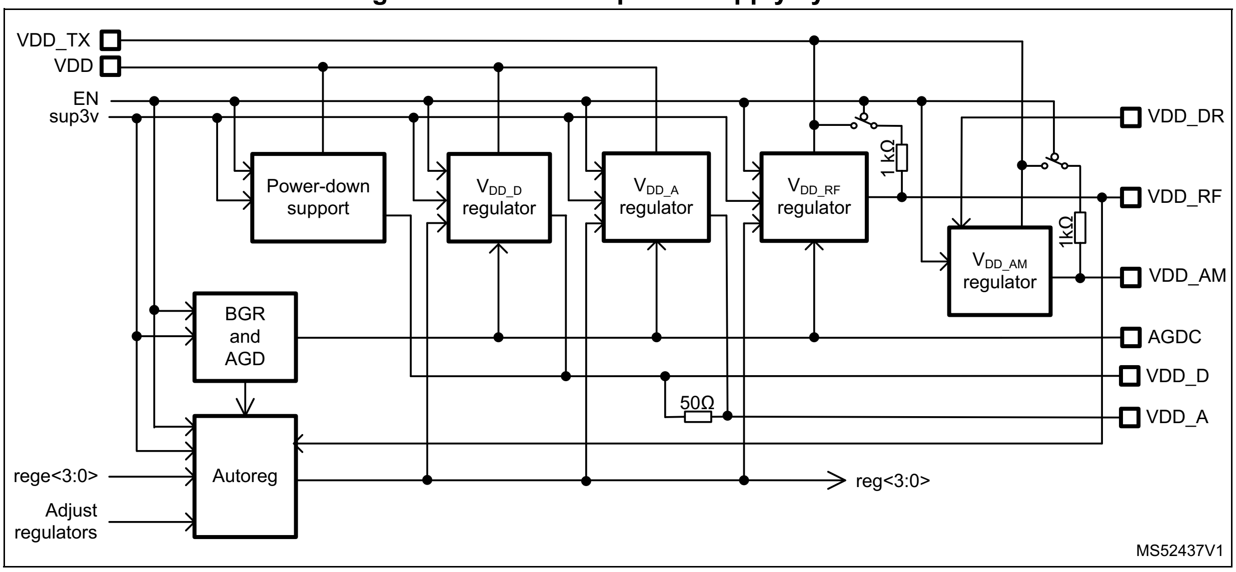
The ST25R3918 features three positive supply pins, VDD, VDD_TX and VDD_IO:

- VDD is the main power supply pin. It supplies the ST25R3918 blocks through two regulators (V_{DD_A}, V_{DD_D})
- VDD_TX is the transmitter supply pin. It supplies the transmitter via two regulators (V_{DD_RF}, V_{DD_AM}). V_{DD} range from 2.4 to 5.5 V is supported. VDD and VDD_TX must be connected to the same power supply.
- V_{DD_IO} is used to define supply level for digital communication pins (BSS, MISO, MOSI, SCLK, IRQ, MCU_CLK). Digital communication pins interface to the ST25R3918 logic through level shifters, therefore the internal supply voltage can be either higher or lower than V_{DD_IO}. V_{DD_IO} range from 1.65 to 5.5 V is supported.

Figure 8 details the building blocks of the ST25R3918 power supply system. It contains three regulators, a power-down support block, a block generating analogue reference voltage (AGDC) and a block performing automatic power supply adjustment procedure. The three regulators are providing supply to analogue blocks (V_{DD_A}), logic (V_{DD_D}) and transmitter (V_{DD_RF}). The use of V_{DD_A} and V_{DD_D} regulators is mandatory at 5 V power supply to provide regulated voltage to analogue and logic blocks, which use only 3.3 V. The use of V_{DD_A} and V_{DD_D} regulators at 3 V supply and V_{DD_RF} regulator at any supply voltage is recommended to improve system PSRR.

Regulated voltage can be adjusted automatically to have the maximum possible regulated voltage, while still having good PSRR. All regulator pins also have corresponding negative supply pins externally connected to ground potential (V_{SS}). *Figure 1* and *Figure 2* show typical application schematics with all regulators used. For regulators, the recommended blocking capacitors are 2.2 µF in parallel with 10 nF, for pin AGDC 1 µF in parallel with 10 nF is suggested.

Figure 8. ST25R3918 power supply system



Regulators have two basic operation modes depending on supply voltage, 3.3 V supply mode (max. 3.6 V) and 5 V supply mode (max 5.5 V). The supply mode is set by writing bit sup3V in the*IO configuration register 2*. Default setting is 5 V so this bit has to be set to 1 after power-up in case of 3.3 V supply.

In 3.3 V mode all regulators are set to the same regulated voltage in range from 2.4 to 3.4 V, while in 5 V only the V_{DD_RF} can be set in range from 3.6 to 5.1 V, while V_{DD_A} and V_{DD_D} are fixed to 3.4 V.

Figure 8 also shows the signals controlling the power supply system. The regulators are operating when signal en is high (en is configuration bit in *Operation control register*). When signal en is low the ST25R3918 is in low power Power-down mode. In this mode consumption of the power supply system is also minimized.

V_{DD_RF} regulator

The purpose of this regulator is to improve the PSRR of the transmitter (the noise of the transmitter power supply is emitted and fed back to the receiver). The V_{DD_RF} regulator operation is controlled and observed by writing and reading two regulator registers:

- *Regulator voltage control register* controls the regulator mode and regulated voltage. Bit reg_s controls regulator mode. If it is set to 0 (default state) the regulated voltage is set using direct command *Adjust regulators*. When bit reg_s is asserted to 1 regulated voltage is defined by bits rege_3 to rege_0 of the same register. The regulated voltage adjustment range depends on the power supply mode. In case of 5 V supply mode the adjustment range is between 3.6 and 5.1 V in steps of 120 mV, in case of 3.3 V supply mode the adjustment range is from 2.4 to 3.6 V with 100 mV steps.
- *Regulator display register* is a read only register that displays actual regulated voltage when regulator is operating. It is especially useful in case of automatic mode, since the actual regulated voltage, which is result of direct command *Adjust regulators*, can be observed.

If a transmitter output current higher than 85 mArms is required the V_{DD_RF} regulator cannot be used to supply the transmitter. VDD_RF and VDD_DR have to be externally connected to VDD_TX (connection of VDD_RF to supply voltage higher than V_{DD_TX} is not allowed).

The voltage drop of the transmitter current is the main source of the ST25R3918 power dissipation. This voltage drop is composed of a drop in the transmitter driver and of a drop in the V_{DD_RF} regulator. Due to this it is recommended to set the regulated voltage using direct command Adjust Regulators. It results in good power supply rejection ratio with relatively low dissipated power due to regulator voltage drop.

In Power-down mode the V_{DD_RF} regulator is not operating. VDD_RF pin is connected to VDD_TX through a 1 kΩ resistor. Connection through resistors assures smooth power-up of the system and a smooth transition from Power-down mode to other operating modes.

V_{DD_AM} regulator

This regulator is used to support the transmitter AM modulation. Its output voltage is used as transmitter supply during modulation phase. The output is internally connected to the transmitter. It requires decoupling capacitors (2.2 µF + 1 nF) at VDD_AM pin.

V_{DD_DR} is used as reference voltage, resulting in correct V_{DD_AM} voltage and modulation index at supply voltage between 2.4 and 5.5 V.

The output voltage and thus modulation setting is controlled by am_mod<3:0> option bits from 5 to 30% in 16 steps.

In Power-down mode the V_{DD_AM} regulator is not operating. VDD_AM pin is connected to VDD_TX through 1 kΩ resistor, as in the V_{DD_RF} regulator.

V_{DD_A} and V_{DD_D} regulators

V_{DD_A} and V_{DD_D} regulators are used to supply the ST25R3918 analog and digital blocks respectively. In 3.3 V mode V_{DD_A} and V_{DD_D} regulator are set to the same regulated voltage as the V_{DD_RF} regulator, in 5 V mode V_{DD_A} and V_{DD_D} regulated voltage is fixed to 3.4 V.

The use of V_{DD_A} and V_{DD_D} regulators is mandatory in 5 V mode since analog and digital blocks supplied with these two pins contain low voltage transistors which support maximum supply voltage of 3.6 V. In 3.3 V supply mode the use of regulators is strongly recommended to improve PSRR of analog processing.

For low cost applications it is possible to disable the V_{DD_D} regulator and to supply digital blocks through external short between V_{DD_A} and V_{DD_D} (configuration bit vspd_off in the *IO configuration register 2*).

Power-down support block

In the Power-down mode the regulators are disabled to save current. In this mode a low power Power-down support block that keeps V_{DD_D} and V_{DD_A} below 3.6 V is enabled. Typical regulated voltage in this mode is 3.1 V at 5 V supply and 2.2 V at 3 V supply. When 3.3 V supply mode is set this block is disabled, its output is connected to VDD through a 1 kΩ resistor.

Typical consumption of Power-down support block is 600 nA at 5 V supply.

Measurement of supply voltages

Using direct command *Measure power supply* it is possible to measure V_{DD} and regulated voltages V_{DD_A}, V_{DD_D} and V_{DD_RF}.

4.2.10 Overshoot / undershoot protection

The overshoot / undershoot protection mechanism makes it possible to control the transmitting waveform during challenging test conditions. This is accomplished by setting bit patterns in the corresponding registers that produce additional signals during the transition phase from modulated to unmodulated state or vice versa.

The operation of this protection is explained by using the overshoot registers. The overshoot mechanism is only effective when bits are written in ov_pattern<13:0>. Setting ov_pattern<13:0> to 0 implicitly disables the overshoot protection, as the configuration from *Mode definition register* and *TX driver register* is applied for all clock cycles after the transition.

The overshoot mode has to be set in control bits ov_tx_mode<1:0> and defines the drive level for the complete bit pattern. Three modes are available.

- ov_tx_mode<1:0> = 00b: the transmitter outputs are driven with V_{DD_DR} when the respective ov_pattern bit is 1.
- ov_tx_mode<1:0> = 01b: the transmitter outputs are driven with V_{DD_AM} when the respective ov_pattern bit is 1.
- ov_tx_mode<1:0> = 10b: the transmitter outputs are stopped (like Type A pause) when the respective ov_pattern bit is 1.

The overshoot protection pattern ov_pattern<13:0> is applied LSB first. For the first 14 clock cycles after the transition from modulated to unmodulated state, each of the 14 bits of the overshoot protection pattern specifies the driver configuration to apply. So ov_pattern<0>

defines which driver configuration to apply for the first clock cycle after the transition from modulated to unmodulated state, and ov_pattern<9> defines which driver configuration to apply for the tenth clock cycle after the transition from modulated to unmodulated state. From the 15th clock cycle on the settings from *TX driver register* are used.

The undershoot protection works in a similar manner for transitions from unmodulated state of the carrier to modulated state of the carrier.

4.2.11 Reader operation

The Ready mode has to be entered by setting the bit en of the *Operation control register*. In this mode the oscillator is started and the regulators are enabled. When the oscillator operation is stable an interrupt is sent and bit osc_ok indicates it.

The operation mode and data rate must be then configured by writing the *Mode definition register* and *Bit rate definition register*. The receiver and transmitter operation options related to operation mode have to be defined too. If the selected operation mode uses AM modulation for communication reader to tag the modulation depth must be configured.

Before sending any command to a transponder the transmitter and receiver have to be enabled by setting the bits rx_en and tx_en. Several NFC standards define a guard time (5 ms for ISO14443) requiring that the reader field must be turned on for some time before first command is sent. General purpose timer can be used to count this time or NFC Field On command with a defined time by the *NFC field on guard timer register*.

Preparation and execution of a transceive sequence:

- Execute the direct command *Stop all activities*
- Execute the direct command *Reset RX gain*
- Configure the timers accordingly
- Define the number of transmitted bytes in the *Number of transmitted bytes register 1* and *Number of transmitted bytes register 2*
- Write the bytes to be transmitted in the FIFO (not in the case of direct commands REQA and WUPA)
- Send one of the commands Transmit with CRC, Transmit without CRC, Transmit REQA or Transmit WUPA
- When all the data is transmitted an interrupt is sent to inform the microcontroller that the transmission is finished (IRQ due to end of transmission)

After the transmission is executed, the ST25R3918 receiver automatically starts to observe the RFI inputs to detect a transponder response. The RSSI and AGC (in case it is enabled) are started. The framing block processes the subcarrier signal from receiver and fills the FIFO with data. When the reception is finished and all the data is in the FIFO an interrupt is sent to the microcontroller (IRQ due to end of receive), and the *FIFO status register 1* and *FIFO status register 1* display the number of bytes in the FIFO so the microcontroller can proceed with data download.

If an error or bit collision is detected during reception, an interrupt with appropriate flag is sent, and the microcontroller must take appropriate action.

When data packets longer than FIFO have to be transmitted the sequence detailed above changes.

The FIFO is prepared with data before the transmission starts. An interrupt is sent during the transmission to signal when the remaining number of bytes is lower than the water level (IRQ due to FIFO water level). The microcontroller then adds more data in the FIFO. When all the data are transmitted an interrupt is sent to inform the microcontroller that the transmission is finished.

The situation during reception time is similar. When the FIFO is loaded with more data than the receive water level, an interrupt is sent and the microcontroller reads the data from the FIFO. When the reception is finished an interrupt is sent to the microcontroller (IRQ due to end of receive) the *FIFO status register 1* and *FIFO status register 1* display the number of bytes in the FIFO still to be read.

4.2.12 Listen mode

The ST25R3918 listen/target mode is activated by setting to 1 bit targ in the *Mode definition register*. There are various target or listening modes implemented depending on setting of the om<3:0> bits, refer to *Table 20: Target operation modes*.

The main modes are

- ISO14443A passive target mode
- Felica™ passive target mode

Fixed listen communication mode

Fixed communication mode is active when one of the target modes with om3=0 is selected. The other om bits control the type of communication.

Passive target

Communication can be performed by the host (through FIFO) or also by using automatic responses as referred in *Passive target definition register*.

These automatic responses include for NFC-A the complete anti-collision including SAK. Handling of RATS and HLTA is up to the host. For NFC-F only the SENSF_REQ is handled by sending SENSF_RES.

States of NFC-A can be handled by observing *Passive target display register* and *Passive target interrupt register* bits I_wu_a, I_wu_a*. Direct commands Go to sense and Go to sleep let the host influence the passive target states.

Responses to SENSF_REQ can be observed by thanks to bit I_wu_f.

The content of the automatic responses is defined by content of PT_Memory.

Bit rate detection mode

The Listen mode can also be started from the so-called Bit rate detection mode. In this mode the communication mode is not fixed. This mode is activated in case of Target mode together with bit om3 set to 1.

The other om bits define the technologies to be recognized. It is an extension of the Fixed listen communication mode.

Once the reception of the first frame starts, the Bit rate detection mode signals an IRQ I_nfct indicating that the bit rate has been identified and the host can retrieve the related information by reading nfc_rate on *Bit rate definition register*.

When the first frame has been fully received, the host can exit the Bit rate detection mode by setting the corresponding mode on om<3:0> bits in the *Mode definition register* to the corresponding fixed listen communication mode.

Bit d_ac_ap2p allows filtering of NFCIP-1 active frames.

Low power field detection

The Fixed listen communication and Bit rate detection modes can be enhanced in terms of power consumption by using the field detector in Low-power mode, putting the ST25R3918 in power-down mode (en = 0) while waiting for an external field from a peer/reader.

For this mode the Bit rate detection mode or the Fixed listen communication mode have to be selected, and bits en, rx_en and tx_en in the *Operation control register* need to be cleared to 0.

In this mode the field detector has to be configured to automatic or manual peer detection threshold.

On detection of external field (I_eon) the ST25R3918 temporarily enable the oscillator and the receiver. The host needs to confirm it by setting en and rx_en option bits in the *Operation control register* within 10 ms.

From this point on normal bit rate detection or normal target communication can be performed.

PT memory

The PT_Memory is used to store data for NFCIP-1 passive target and NFC-A card/listen mode. It is loaded via the host interface as described in *Section 4.3*.

Table 5. PT_Memory address space

Location	Description	Data usage	
0-9	NFCID1 (4/7/RFU bytes)	4 bytes: locations 0-3 7 bytes: locations 0-6	NFC-A anticollision
10,11	SENS_RES2:1	SENS_REQ response	
12	SELR_L1	SEL Level 1 response.	
13	SELR_L2	SEL Level 2 response	
14	SELR_L3	RFU	
15,16	NFCF_SC	System code (SC) in SENSF_REQ(1)	NFC-F anticollision
17-35	212/424 polling response	SENSF_RES format(2)	
36-47	TSN - Random numbers	Slot selection, 24 4-bit random numbers are stored(3) (4)	

1. SENSF_RES is transmitted in case received SC=NFCF_SC or SC=0xFFFF.
2. NFC-212/424k SENS_RES format, see *Table 6*. The last two bytes in SENSF_RES are transmitted based on the RC bytes in the SENSF_REQ.
3. The 4-bit slot numbers are sequentially used in the NFC212/424 Polling response. When only four TSN numbers remain unused, an IRQ with I_sl_wl bit is sent.
4. Depending on the number of slots in the Polling request, appropriate number of the MSB bits in the slot number is used.

Table 6. NFC-212/424k SENS_RES format

Byte 1	Bytes 2-9	Bytes 10-11	Bytes 12-14	Byte 15	Byte 16	Byte 17	Bytes 18-19
01h	NFCID2	PAD0	PAD1	MRTICHECK	MRTIUPDATE	PAD2	[RD]

4.3 Communication with an external microcontroller

The ST25R3918 communicates with a microcontroller either via an SPI interface or via an I2C interface. On both interfaces the ST25R3918 acts as a slave device, relying on the microcontroller to initiate all communication. To notify the microcontroller of completed commands or external events (e.g. peer device field on) the ST25R3918 signals an interrupt on the IRQ pin. The ST25R3918 can also provide a configurable clock signal to the microcontroller on the MCU_CLK pin.

4.3.1 Interrupt interface

There are four interrupt registers implemented in the ST25R3918:

- *Main interrupt register*
- *Timer and NFC interrupt register*
- *Error and wake-up interrupt register*
- *Passive target interrupt register*

When an interrupt condition is met the source of interrupt bit is set and the IRQ pin transitions to high. The microcontroller then reads the *Main interrupt register* to distinguish between different interrupt sources. After a particular interrupt register is read, its content is reset to 0.

The IRQ pin transitions to low after the interrupt bit(s) that caused its transition to high has (have) been read.

Note: There can be more than one interrupt bit set if the microcontroller does not immediately read the interrupt registers after the IRQ signal is set and another event causing an interrupt occurs. In this case the IRQ pin transitions to low after the last bit causing interrupt is read.

Note: It is recommended to set a safety timer on the host to cover the transceive window.

If an interrupt from a certain source is not required it can be disabled by setting the corresponding bit in the Mask interrupt registers. In case of masking a certain interrupt source the IRQ line is not set high, but the interrupt status bit is still set in IRQ status registers.

Reading the IRQ status registers presents and clears also the masked interrupt bits.

If some interrupts are masked, and set to 1 because of an IRQ event, and later on one of them unmasks the IRQ status bit that is already set, the IRQ line is immediately set to high. This notifies the host system that there are some interrupt events not yet read out.

Table 7. IRQ output

Name	Signal	Level	Description
IRQ	Digital output	CMOS	Interrupt output pin

IRQ line and IRQ status bits are cleared at:

- Set default
- Reading the IRQ status
- Stop all activities
- Clear FIFO.

FIFO water level and FIFO status registers, FIFO reset

The ST25R3918 features a 512 byte FIFO. The control logic shifts the data during transmission, which was previously loaded by the external microcontroller to the framing block and further to the transmitter. During reception, the demodulated data is stored in the FIFO and the external microcontroller can receive data at a later moment.

The *FIFO status register 2* also contains two bits that indicate that the FIFO was not correctly served during TX/RX process (FIFO overflow and FIFO underflow).

A FIFO overflow is set when too many data are written into the FIFO. When this bit is set during RX the external controller did not react on time on the water level IRQ and more than 512 bytes were written into the FIFO (including received CRC bytes). Consequently, the received data is corrupted. When an overflow happens during TX, it means that the controller has written more data than the FIFO size. The data to be transmitted is corrupted.

A FIFO underflow is set when data were read from an empty FIFO. When this bit is set during RX the external controller read more data than was actually received. When an underflow happens during TX, it means that the controller has failed to provide the quantity of data defined in the number of transmitted bytes registers on time.

FIFO pointers and FIFO status are reset at the start of each data reception (at I_rxs). They are also reset at Power-up and at commands Set Default and Clear FIFO. Reading out data from empty/cleared fifo shows data = 0.

MCU_CLK

The pin MCU_CLK can be used as clock source for the external microcontroller. Depending on the operation mode either a low frequency clock (32 kHz) from the RC oscillator or the clock signal derived from crystal oscillator is available on pin MCU_CLK. The MCU_CLK output pin is controlled by bits out_c<1:0> and lf_clk_off in the *IO configuration register 1*. Bits out_c<1:0> enable the use of pin MCU_CLK as clock source and define the division when the crystal oscillator is running (13.56, 6.78 and 3.39 MHz are available). Bit lf_clk_off controls the use of low frequency clock (32 kHz) when the crystal oscillator is not running. By default configuration, which is defined at power-up, the 3.39 MHz clock is selected and the low frequency clock is enabled.

If the Transparent mode (see *Section 4.4.13*) is used the use of MCU_CLK is mandatory since a clock synchronous with the field carrier frequency is needed to implement receive and transmit framing in the external controller. The use of MCU_CLK is recommended also when the internal framing is used. Using MCU_CLK as the microcontroller clock source generates noise, synchronous with the reader carrier frequency and therefore filtered out by the receiver, while using some other incoherent clock source can produce noise that perturbs the reception. Use of MCU_CLK is also better for EMC compliance.

4.3.2 Communication interface selection

The active communication interface is selected via the I2C_EN pin. If this pin is pulled to GND, the ST25R3918 operates in SPI mode. If this pin is pulled to V_{DD_D}, the ST25R3918 operate in I2C mode.

4.3.3 Serial peripheral interface (SPI)

The ST25R3918 has a standard serial peripheral interface with clock polarity of 0, a clock phase of 1, and an active low slave select signal. Communication starts with the MCU pulling BSS low. The MOSI pin is samples on the falling edge of SCLK, and the state of the

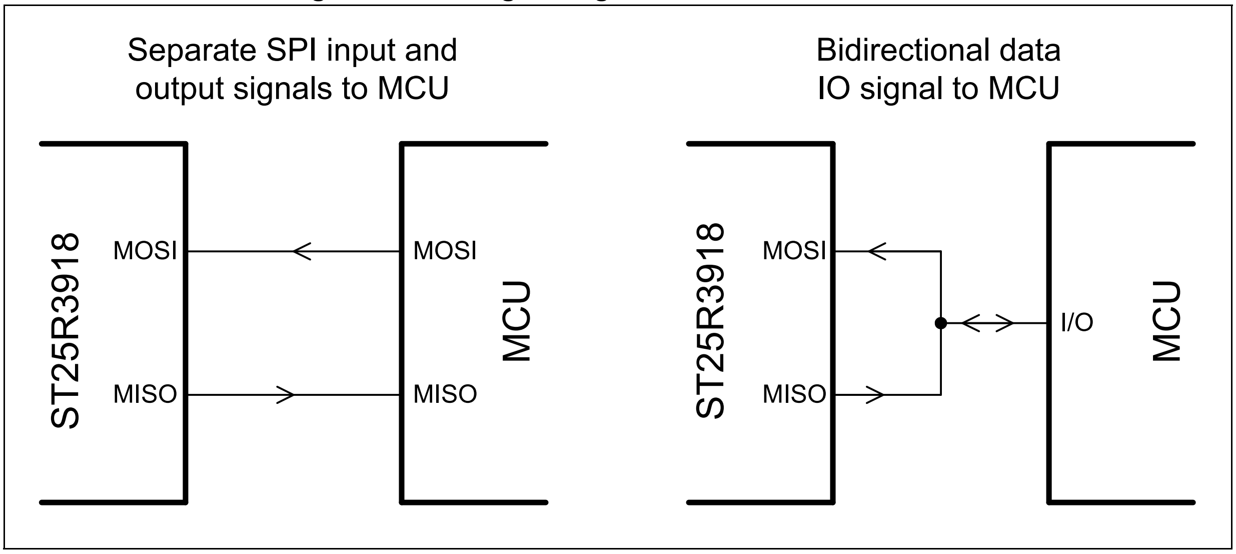
MISO pin is updated on the rising edge of the SCLK signal. Data are transferred byte-wise, most significant bit first. Read and Write commands support an address auto increment to reduce communication time. *Table 8* provides an overview of the SPI signals.

Table 8. Serial data interface (4-wire interface) signal lines

Name	Signal	Signal level	Description
I2C_EN	Digital input	CMOS	Pull to GND for SPI operation
BSS	Digital input		Active low - Slave select
MOSI	Digital input		Master out - Slave in (MCU → ST25R3918)
MISO	Digital output with tristate		Master in - Slave out (ST25R3918 → MCU)
SCLK	Digital input		Serial clock
IRQ	Digital output		Active high - Interrupt output pin

The MISO output is in tristate as long as no output data are available, hence MOSI and MISO can be externally shorted to create a three-wire SPI. During the time the MISO output is in tristate, it is also possible to switch on a 10 kΩ pull down, by activating option bits miso_pd1 and miso_pd2 in the *IO configuration register 2*.

Figure 9. Exchange of signals with a microcontroller



The first two bits of the first byte transmitted after the BSS high to low transition define the SPI operation mode. All Read and Write modes support address auto incrementing, which means that if, after the address and first data byte some additional data bytes are sent (or read), they are written to (or read from) addresses incremented by 1.

Table 9 shows available SPI operation modes. Register read and write operations are possible in all ST25R3918 operation modes. FIFO and PT_memory operations are possible in case en (bit 7 of the *Operation control register*) is set and the crystal oscillator is stable.

Some direct commands are accepted in all operation modes, others require en (bit 7 of the *Operation control register*) to be set and the crystal oscillator to be stable (see *Table 11*).

Table 9. SPI operation modes

Mode	Pattern (communication bits)								Related data
	Mode		Trailer						
	M1	M0	C5	C4	C3	C2	C1	C0	
Register write	0	0	A5	A4	A3	A2	A1	A0	Data byte (or more bytes in case of auto-incrementing)
Register read	0	1	A5	A4	A3	A2	A1	A0	
FIFO load	1	0	0	0	0	0	0	0	One or more bytes of FIFO data
PT_memory load A-config	1	0	1	0	0	0	0	0	Passive target memory, locations from 0 on.
PT_memory load F-config	1	0	1	0	1	0	0	0	Passive target memory, locations from 15 on.
PT_memory load TSN data	1	0	1	0	1	1	0	0	Passive target memory, locations from 36 on. The additional address allows reload of the TSN random numbers without rewriting the whole PT_memory
PT_memory read	1	0	1	1	1	1	1	1	Passive target memory, locations from 0 on. A 0 byte is presented to the passive target memory to support reading at all SPI speeds.
FIFO read	1	0		1	1	1	1	1	One or more bytes of FIFO data
Direct command	1	1	C5	C4	C3	C2	C1	C0	-

Writing data to addressable registers (Write mode)

Figure 10 and *Figure 11* show cases of writing, respectively, a single byte and multiple bytes with auto-incrementing address. After the SPI operation mode bits, the address of register to be written is provided. Then one or more data bytes are transferred from the SPI, always MSB to LSB. The data byte is written in register on falling edge of its last clock. If the register on the defined address does not exist or it is a read only register no write is performed.

Figure 10. SPI communication: writing a single byte

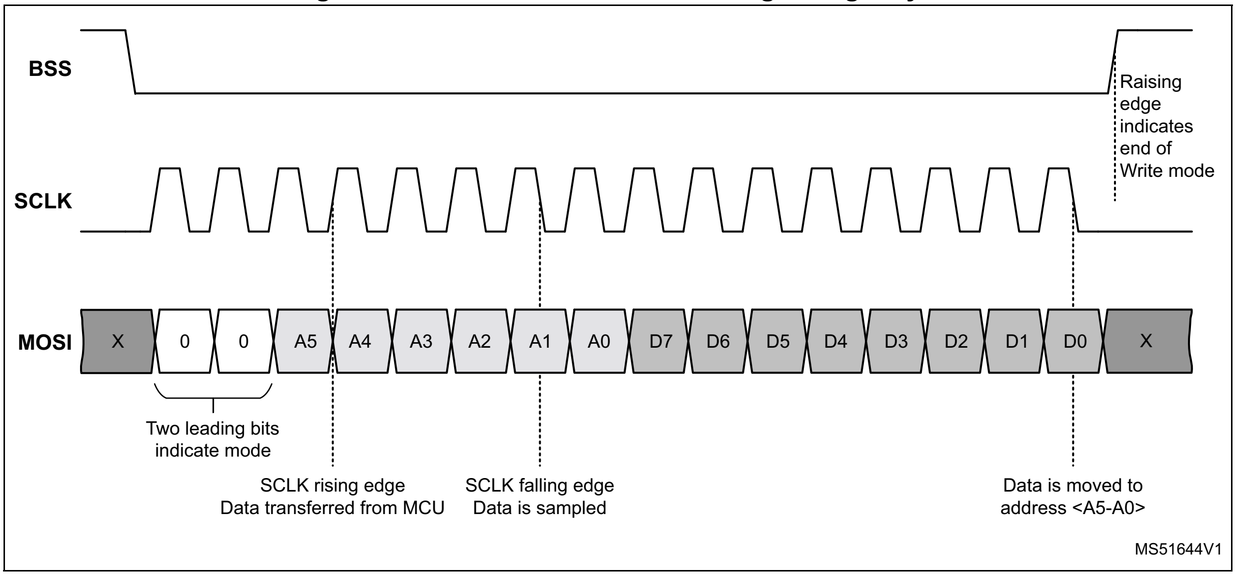
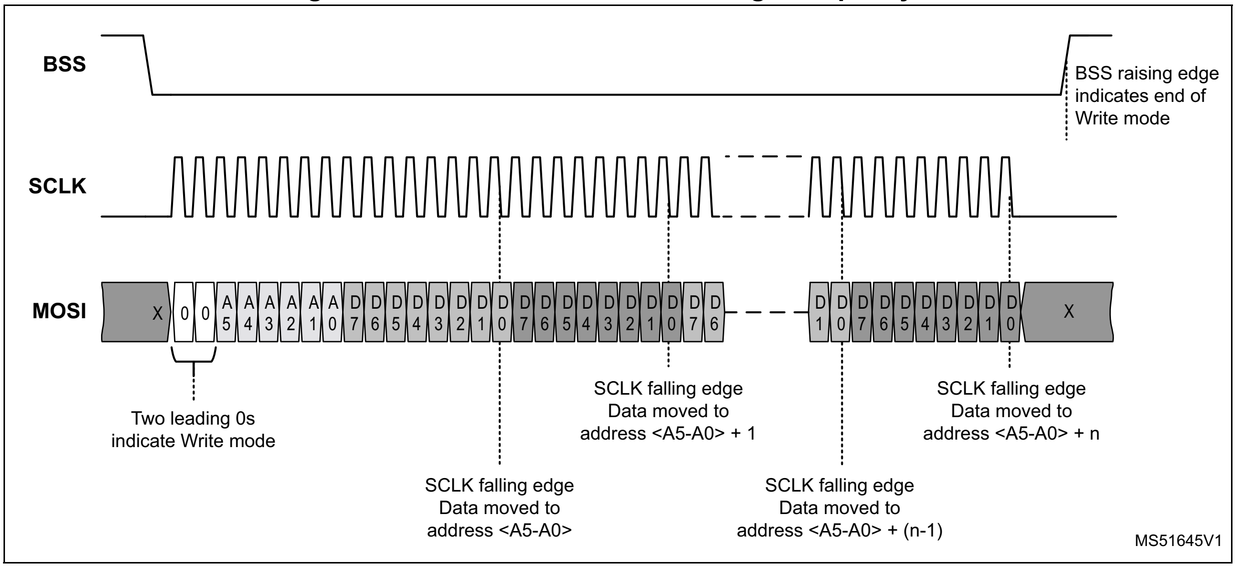


Figure 11. SPI communication: writing multiple bytes

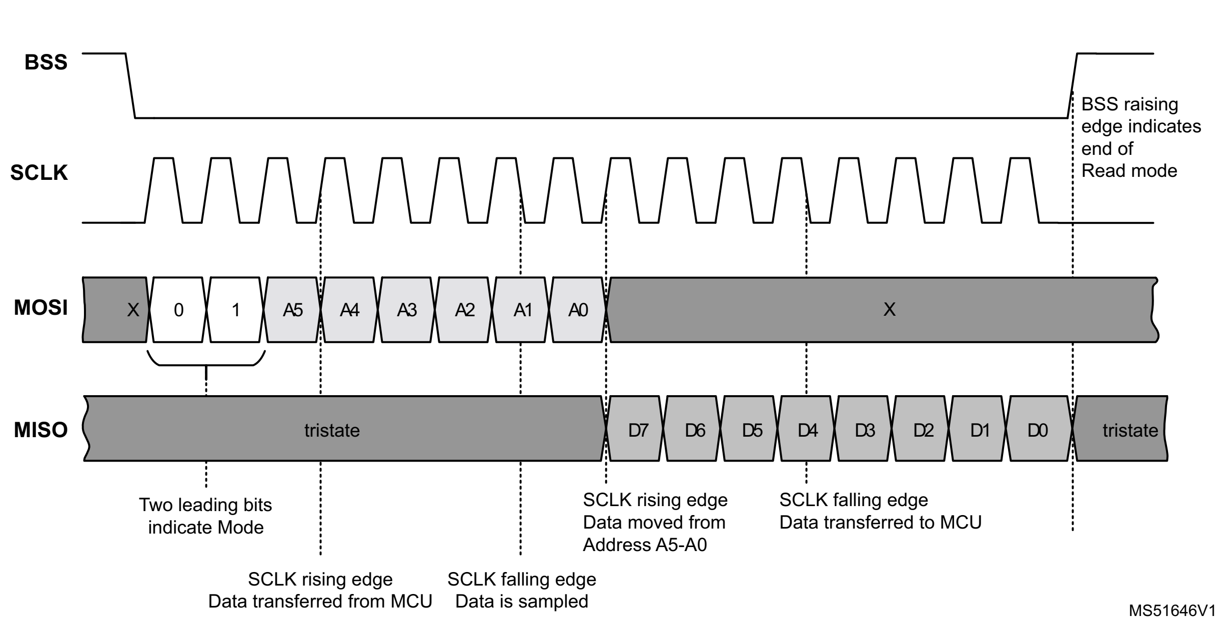


Reading data from addressable registers (Read register mode)

The SPI operation mode bits are followed by the address of the register to be read. Then one or more data bytes are transferred to MISO output (MSB first) for as long as SCLK is present. This mode also supports address auto-incrementing. If there is no register at a certain address, then all 0 data is sent to MISO.

Figure 12 is an example of reading a single byte.

Figure 12. SPI communication: reading a single byte



Read or write access to register space-B

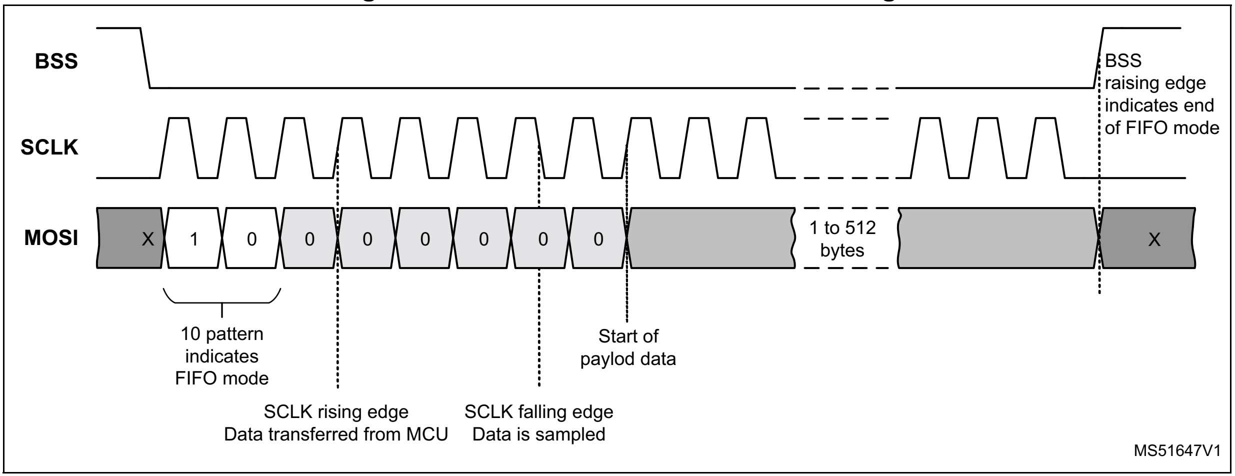
To access the register space-B the register read or write SPI sequence has to be prefixed with the byte FBh. Access to register space-B remains active until the rising edge of BSS.

Loading transmitting data into FIFO

Loading the transmitting data into the FIFO is similar to writing data into an addressable registers. The SPI sequence starts with SPI operation mode bits ‘10’ to indicate a FIFO operation followed by bits <C5:C0> set to 000000b. After the FIFO mode byte at least one and up to 512 data bytes must be sent.

Figure 13 shows how to load the transmitting data into the FIFO.

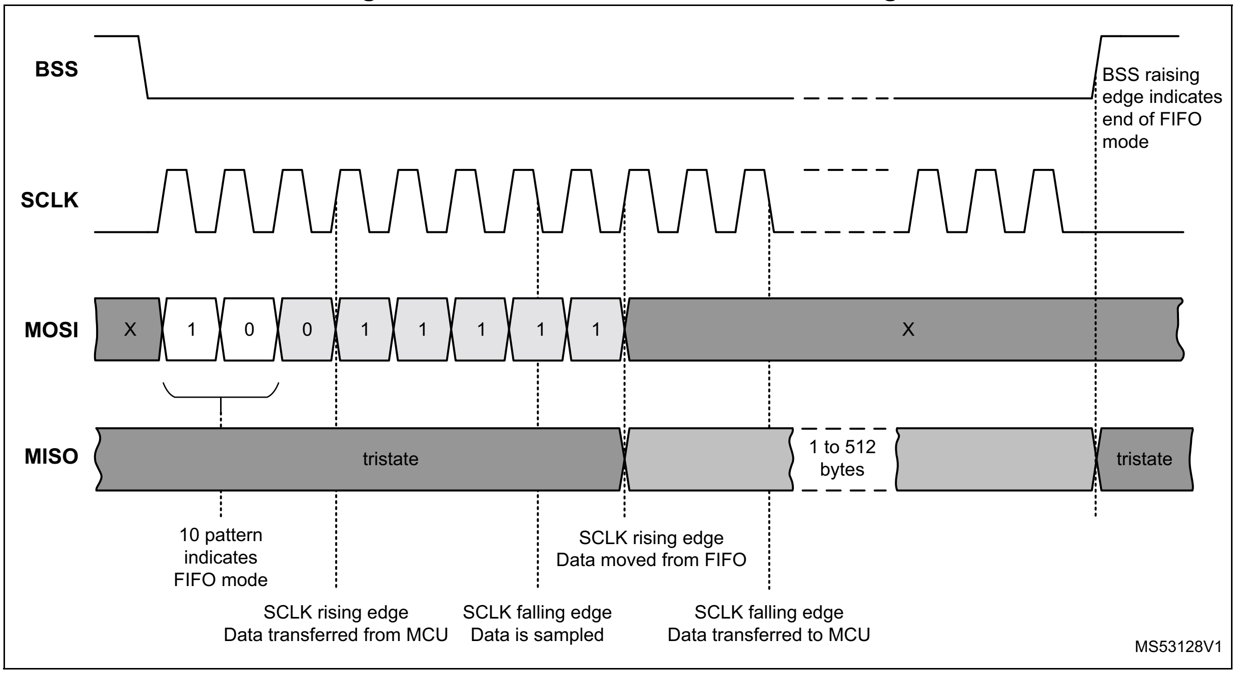
Figure 13. SPI communication: FIFO loading



Reading received data from FIFO

Reading received data from the FIFO is similar to reading data from an addressable registers. The SPI sequence starts with SPI operation mode bits ‘10’ to indicate a FIFO operation followed by <C5:C0> set to 011111b. After the mode byte the ST25R3918 will output the data from the FIFO as long as SCLK is present and BSS is kept low.

Figure 14. SPI communication: FIFO reading

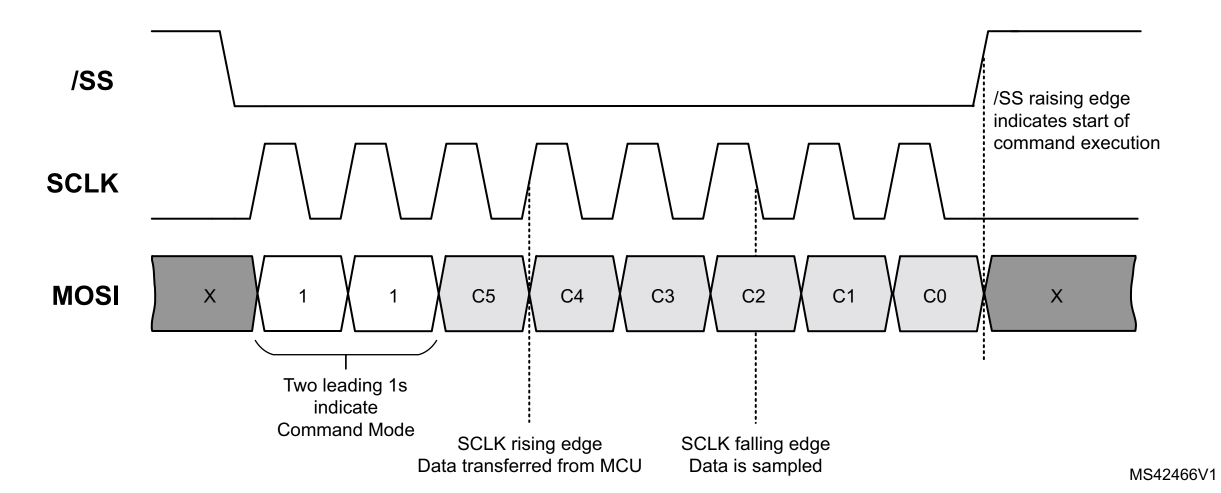


Direct command mode

Direct command mode has no arguments, so a single byte is sent. The byte starts with the SPI operation mode bits ‘11’ to indicate Direct Command Mode followed by the direct command code (see *Table 11*) in <C5:C0>, MSB first. Execution of the direct command starts with the rising edge of BSS (see *Figure 15*).

While the execution of some direct commands is immediate, there are others that start a process of certain duration (e.g. calibration, measurements). During the execution of such commands it is not allowed to start another activity over the SPI interface, an IRQ is sent. when the execution is terminated.

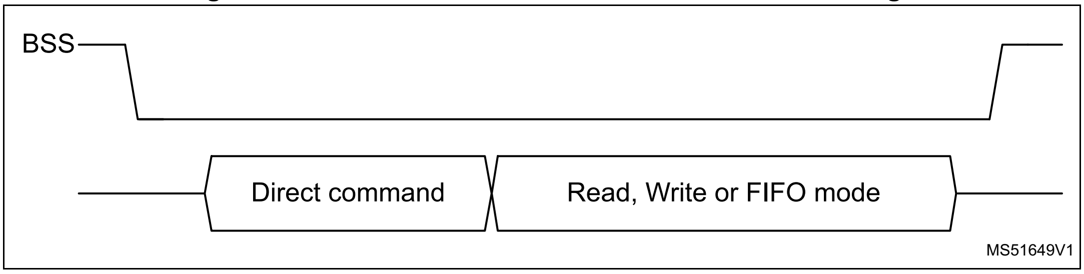
Figure 15. SPI communication: direct command



Direct command chaining

As shown in *Figure 16*, direct commands with immediate execution can be followed by another SPI mode (Read, Write or FIFO) without deactivating the BSS signal in between.

Figure 16. SPI communication: direct command chaining



Loading data in the PT_Memory (PT_Memory load)

Loading data into the PT_Memory is similar to loading data into the FIFO. There are three mode patterns available to load data into three different parts of the PT_memory, as indicated in *Table 9*. The first byte following the mode/address pattern is stored in the location detailed in *Table 9*, for consecutive bytes the address is automatically incremented and data are stored to consecutive addresses.

The user must take care that the number of loaded bytes fits the size of the selected PT_memory area, not to overwrite data in the following PT_memory areas.

4.3.4 I2C interface

The I2C address is 50h.This interface supports:

- Standard mode (100 kHz)
- Fast mode (400 kHz)
- Fast mode Plus (1 MHz)
- High speed mode (3.4 MHz)

Table 10 summarizes the I2C interface signals.

Table 10. I2C interface and interrupt signal lines

Name	Signal	Signal level	Description
I2C_EN	Digital input	CMOS	Pull to VDD_D for I2C operation
MISO (SDA)	Digital output		I2C data line
SCLK (SCL)	Digital input		I2C clock
IRQ	Digital output		Active high - Interrupt output pin

Writing data to addressable registers (Register Write mode)

After the I2C slave address the address of the register to be written is sent using the same Register Write mode byte as for SPI register write access. The Register Write mode byte is then followed by one or more data bytes. If more than one data byte is sent, the data is stored in subsequent registers starting form the initial register address by incrementing the target address by one for each new data byte.

Figure 17 and *Figure 18* show, respectively, how to write a single byte into a register and how to write multiple bytes into subsequent registers using address auto-incrementing.

Figure 17. Writing a single register

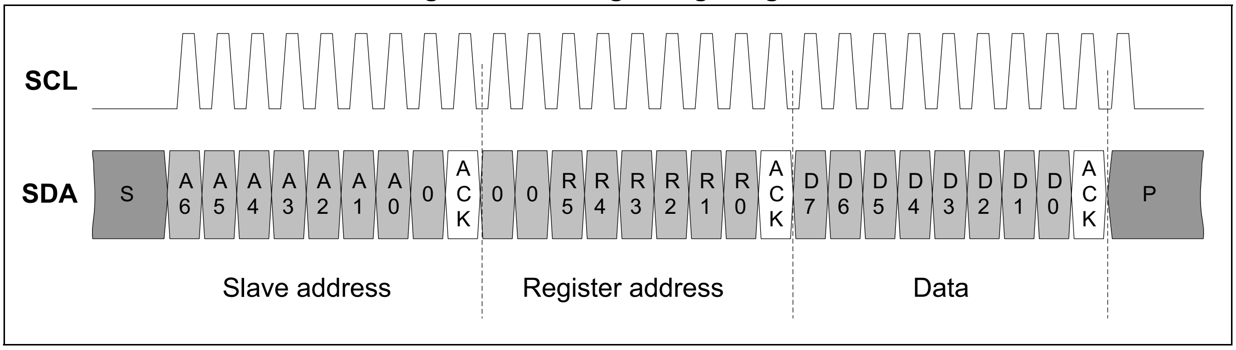
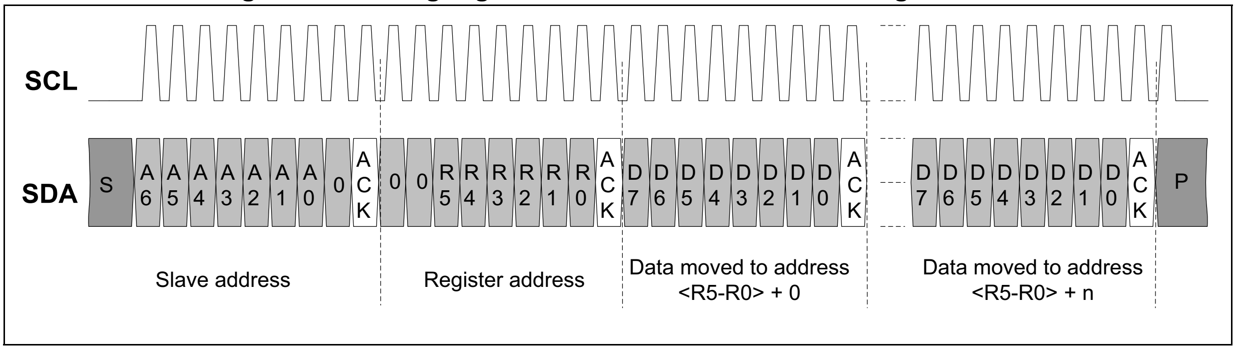


Figure 18. Writing register data with auto-incrementing address

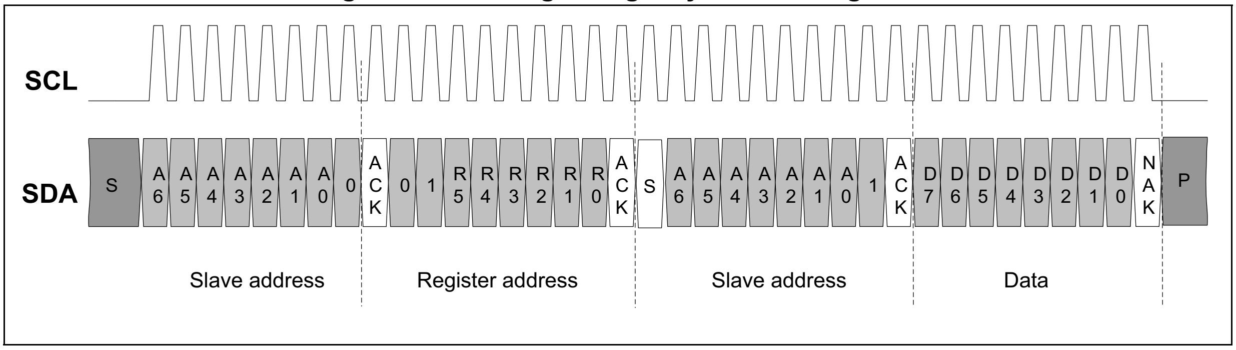


Reading data from addressable registers (Register Read mode)

After the I2C slave address the address of the register to be read is sent using the same Register Read mode byte of the SPI register read access. After the Register Read mode byte the ST25R3918 sends data bytes to the SDA output as long as the MCU keeps SCL. The Register Read mode also supports address auto-incrementing. If the addressed register does not exist, all 0 data is sent to SDA.

Figure 19 shows how to read a single byte from a register.

Figure 19. Reading a single byte from a register

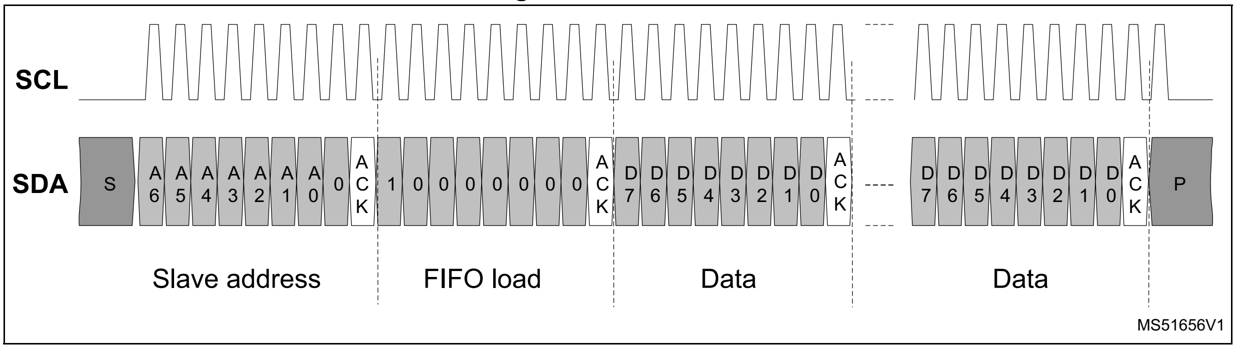


Loading data into FIFO or PT_Memory (FIFO/PT_Memory load)

Loading data into FIFO or PT_Memory is similar to writing data into addressable registers. After the I2C slave address the mode byte to trigger a load of the FIFO or selected PT_Memory area is sent (see *Table 9*) followed by the data bytes to be loaded.

Figure 20 shows how to load data into the FIFO.

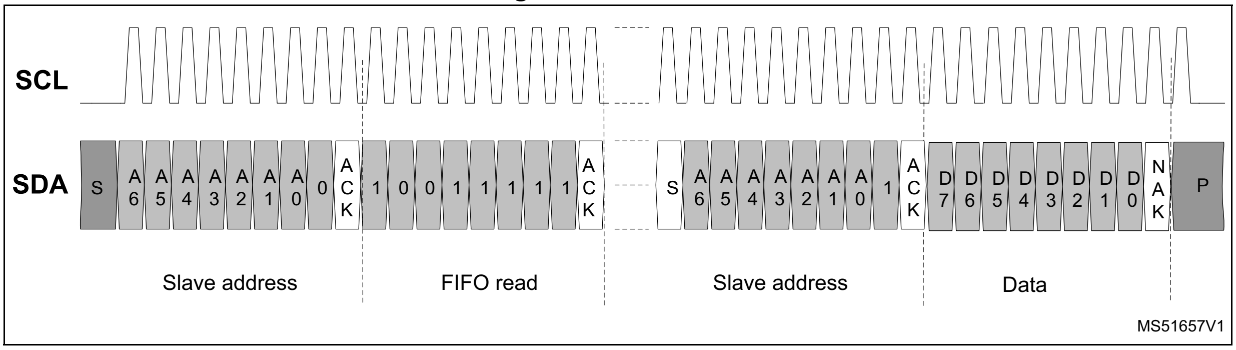
Figure 20. FIFO load



Reading data from the FIFO

Reading data from the FIFO is similar to reading data from addressable registers. After the I2C slave address the mode byte to trigger a read of the FIFO is sent. After receiving the FIFO read mode byte the ST25R3918 sends data bytes from the FIFO for as long as the MCU keeps reading the bus.

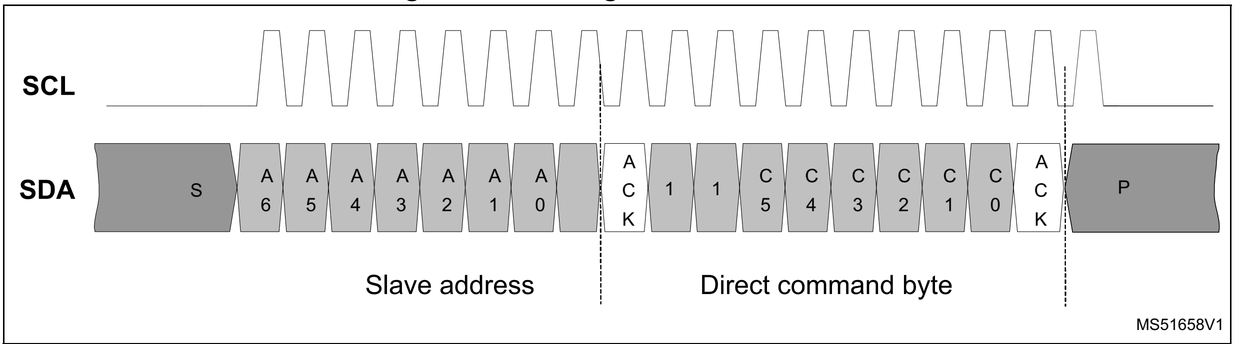
Figure 21. FIFO read



Direct command mode

After the I2C slave address the mode byte to trigger a direct command is sent. As for SPI some direct commands take some time to execute and no I2C access to the ST25R3918 must be performed until the execution of the direct command is completed. All such direct commands send an interrupt upon completion to notify the MCU that the I2C bus can be used again.

Figure 22. Sending a direct command



I2C access to register space-B

To access the register space-B, byte FBh has to be inserted between the I2C slave address and the register read or write mode byte. Access to register space-B remains active until an I2C Stop Condition is received.

Figure 23. Read and Write mode for register space-B access

Write to register space B

S	Slave address W	A	FBh	Register address	A	Data 0	A	Data 1	A	...	Data N	A	P

Read from register space B

S	Slave address W	A	FBh	Register address	A	Sr	Slave address R	A	Data 0	A	Data 1	A	...	Data N	N	P

Legend: S: Start, Sr: repeated Start, A: ACK, N: NAK, P: Stop.

I2C: transition to and termination of the Transparent mode

When the transparent mode command is received via I2C, the chip interface lines are switched to the Analogue front end as described in *Section 4.4.13: Transparent mode*.

Once in transparent mode the BSS signal is used to distinguish between I2C communication and transparent mode data as follows:

1. the BSS line must be set high before entering the transparent mode, and then kept high during the Transparent mode
2. the Transparent mode is terminated when the BSS line is set to low, followed by at least one SCL clock pulse
3. after the termination of the transparent mode the I2C interface can be used again.

I2C: master reads slave immediately after the first byte

If the I2C master omits the mode byte and reads the ST25R3918 immediately after the slave address, then, as shown in *Figure 24*, it will first output the byte FFh, followed by a register dump starting at addres 01h.

Figure 24. I2C master reads slave immediately after the first byte

S	Slave address R	A	Data FFh	A	Data register 01h	A	...	Data register n	N	P

Legend: S: Start, A: ACK, N: NAK, P: Stop.

This mode is incorporated for an easier the detection of I2C devices, but is not intended to be used in normal operation.

4.4 Direct commands

Table 11. List of direct commands

Code (hex)	Name	Comments	Chaining	Interrupt after termination	Operation mode(1)
C0, C1	Set default	Puts the ST25R3918 into power-up state	No	No	All
C2, C3	Stop all activities	Stops all activities: transmission, reception, direct command execution, timers	Yes	No	en
C4	Transmit with CRC	Starts a transmit sequence with automatic CRC generation	Yes	No	en
C5	Transmit without CRC	Starts a transmit sequence without automatic CRC generation	Yes	No	en
C6	Transmit REQA	Transmits REQA command (ISO14443A mode only)	Yes	No	en, tx_en
C7	Transmit WUPA	Transmits WUPA command (ISO14443A mode only)	Yes	No	en, tx_en
C8	NFC initial field ON	Performs Initial RF Collision avoidance and switches on the field	Yes	Yes	en
CD	Go to sense (Idle)	Puts the passive target logic into Sense (Idle) state	Yes	No	en, rx_en
CE	Go to sleep (Halt)	Puts the passive target logic into Sleep (Halt) state	Yes	No	en, rx_en
D0	Mask receive data	Stops receivers and RX decoders	Yes	No	All
D1	Unmask receive data	Starts receivers and RX decoders	Yes	No	All
D2	Change AM modulation state	Changes AM modulation state	Yes	No	en, tx_en
D3	Measure amplitude	Measures the amplitude of the signal present on RFI inputs and stores the result in the *A/D converter output register*	No	Yes	All(2)
D5	Reset RX gain	Resets receiver gain to the value in the *Receiver configuration register 4*	No	No	en
D6	Adjust regulators	Adjusts supply regulators according to the current supply voltage level	No	Yes	en
D8	Calibrate driver timing	Starts the driver timing calibration according to the setting in the *TX driver timing display register*	No	No	en
D9	Measure phase	Measures the phase difference between the signal on RFO and RFI	No	Yes	All(2)
DA	Clear RSSI	Clears the RSSI bits in the *RSSI display register* and restarts the measurement	Yes	No	en
DB	Clear FIFO	Clears FIFO	Yes	No	en

Table 11. List of direct commands (continued)

Code (hex)	Name	Comments	Chaining	Interrupt after termination	Operation mode[(1)]
DC	Enter Transparent mode	Enters in Transparent mode	No	No	en
DF	Measure power supply	-	No	Yes	en
E0	Start General purpose timer	-	Yes	No	en
E1	Start Wake-up timer	-	Yes	No	All except wu
E2	Start Mask-receive timer	Starts the mask-receive timer and squelch operation	Yes	No	en
E3	Start No-response timer	-	Yes	No	en
E8	Stop No-response timer	-	Yes	No	en
FA	RFU	Not used	-	-	-
FB	Register space-B access	Enables R/W access to register Space-B	Yes	No	all
Other codes	RFU	Not used	-	-	-

1. Defines which *Operation control register* bits have to be set in order to accept a particular command.
2. Measure amplitude and Measure phase can be used directly from power down mode. In this case the command temporarily enables the oscillator.

4.4.1 Set default

This direct command puts the ST25R3918 in the same state as power-up initialization:

- performs *Stop all activities* command
- resets all registers to their default state
- clears all collision bits

Results of previous calibration and adjust commands are lost. No IRQ due to termination of direct command is produced.

4.4.2 Stop all activities

This direct command stops any ongoing activities:

- performs *Clear FIFO* command
- stops data transmission and reception
- stops all timers, including FDT timer
- clears IRQ line an IRQ status bits
- stops Field ON commands

If Stop All Activities is received during RF collision avoidance, the field detection is terminated and field is not set, consequently no interrupts are sent

- stops automatic field ON (same as above)

This command does not update any register apart from the FIFO status registers. Therefore it does not disable the field detector in CE mode (if it was enabled), and it does not switch off the field (if it was enabled).

4.4.3 Clear FIFO

This direct command clears the FIFO and the FIFO status registers. It does not clear the IRQ line or IRQ status bits.

To prepare a transmission send this command first before writing data into the FIFO. If a Clear FIFO command is sent during an ongoing data transmission, then the data transmission is aborted and FIFO and FIFO status registers are cleared.

4.4.4 Transmit commands

The transmit direct commands are used to start a data transmission from the ST25R3918. They switch the device to reception mode after the transmission is completed.

Before sending commands Transmit with CRC and Transmit without CRC, direct command Clear FIFO has to be sent, followed by the definition of the number of transmitted bytes and writing data to be transmitted in FIFO.

Use the direct commands Transmit REQA and Transmit WUPA to transmit ISO14443A short frame commands REQA and WUPA respectively. It is not necessary to send the direct command Clear FIFO before these two commands.

If the antcl bit is set, then the number of valid bits in the last byte must be set to 0 (nbtx<2:0> in the *Number of transmitted bytes register 2*) prior to the direct command Transmit REQA or Transmit WUPA.

The direct commands Transmit REQA and Transmit WUPA automatically disable the CRC check of the response frame. The CRC check is enabled again after any of the below conditions:

- Transmit with CRC direct command
- Mask receive data direct command
- No Response timer expires

4.4.5 NFC field ON commands

The NFC field ON direct commands are used to perform RF collision avoidance. The external field detector must be enabled for these commands to work correctly.

To determine whether an external field is present the ST25R3918 compares the RF voltage level on the RFI1 pin with the collision avoidance threshold defined in the *External field detector activation threshold register*.

If no external field is detected, then the ST25R3918 transmitter is switched on automatically (bit tx_en in the *Operation control register* is set) and an I_apon IRQ is signaled. After the RF guard time defined in the *NFC field on guard timer register* has passed an I_cat IRQ is signaled. At this point the controller can initiate a data transmission using a transmit command.

If an external field is detected a I_cac IRQ is signaled, and the ST25R3918 transmitter stays off.

The direct command NFC initial field ON performs an Initial collision avoidance according to NFCIP-1 standard. See *Figure 25* and *Table 12* for details on the timing of these commands.

Figure 25. Direct command NFC initial field ON

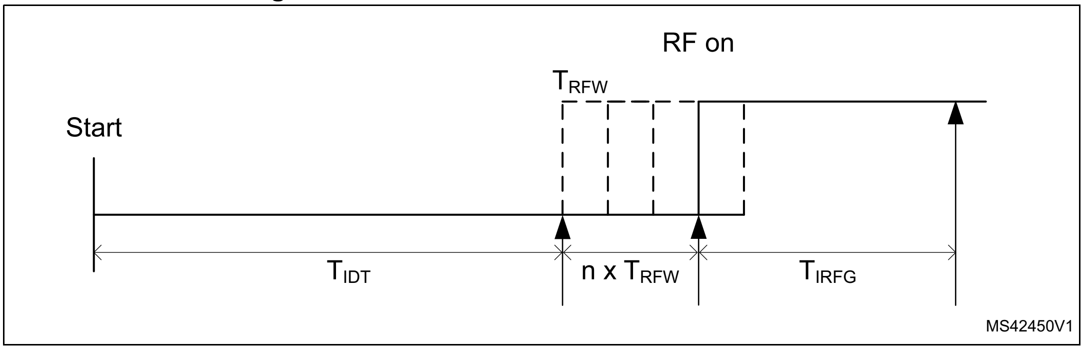


Table 12. Timing parameters of NFC field ON commands

Parameter	Symbol	Value	Unit	Notes
Initial delay time	T_{IDT}	4096	/ fc	NFC initial field ON
RF waiting time	T_{RFW}	512	/ fc	n = 0…3 based on nfc_n<1:0> in *Auxiliary definition register*
Initial guard time	T_{IRFG}	75 µs + NFC field on guard time	s	NFC field on guard time defined in the *NFC field on guard timer register*. NFCIP-1 T_{IRFG} requirement: 5 to 35 ms
Active guard time	T_{ARFG}	75 µs + NFC field on guard time	s	NFC field ON guard time defined in the *NFC field on guard timer register*. NFCPIP-1 T_{ARFG} requirement: > 75 µs + NFC field ON guard times (1024 / fc)

4.4.6 Mask receive data and Unmask receive data

The direct command Mask receive data disables processing of the receiver output by the RX decoders, RSSI measurement, and AGC operation.

The direct command Unmask receive data enables processing of the received data by the RX decoders, RSSI measurement and AGC operation. A common use of this command is to re-enable the receiver operation after it was masked by the command Mask receive data. If the Mask receive timer is still running while the direct command Unmask receive data is received, reception is enabled, and the Mask receive timer is reset.

In passive target (card emulation) mode, the Unmask receive data command prepares the RX decoders for a new data reception and clears the internal FDT timer. In passive target mode, this direct command must be used only if no further transmission from the ST25R3918 is planned and the device has to wait for the next command to be received.

4.4.7 Change AM modulation state

This command changes the AM modulation state from unmodulated to modulated, and vice versa. This can be used to measure the AM modulation index with the direct command

Measure amplitude. The command only affects the regulator state and not the resistive modulation state.

4.4.8 Measure amplitude

This command measures the amplitude of the RF signal on the RFI inputs and stores the result in the *A/D converter output register*.

This command enables the transmitter and amplitude detector. The transmitter drives the antenna, and the amplitude detector converts the differential RF signal received back between RFI1 and RFI2 into a proportional DC voltage. This DC voltage is converted with the A/D converter in absolute conversion mode into an 8-bit value and stored in the *A/D converter output register*.

The amplitude detector conversion gain is 0.6 V_{inPP} / V_{out} referenced to the RF signal on a single RFI pin. Thus, one LSB of the A/D converter output represents 13.02 mV_{PP} on either of the RFI inputs.

Note: The maximum allowed voltage level on an RFI pin is 3 V_{PP}. This results in 1.8 V output DC voltage of the amplitude detector and produces a value of E6h after A/D conversion.

Duration time: 25 µs max.

4.4.9 Reset RX gain

This command initializes the AGC, Squelch and RSSI block and resets the gain reduction to the value set in *Receiver configuration register 4*. Sending this command also stops any ongoing squelch process.

4.4.10 Adjust regulators

When this command is sent, then the transmitter and receiver are enabled to ensure a high current draw and the regulated voltage V_{DD_RF} is set 250 mV below the power supply level of V_{DD_TX}. Before sending the adjust regulator command it is required to toggle the bit reg_s by setting it first to 1 and then reset it to 0. After the adjustment is completed the state of the transmitter and receiver prior to the command execution is restored (either enabled or disabled).

Duration time: 5 ms max.

This command is not accepted if external definition of the regulated voltage is selected in the *Regulator voltage control register* (bit reg_s is set to 1).

4.4.11 Measure phase

This command measures the phase difference between the signals on the RFO outputs and the signals on the RFI inputs and stores the result in the *A/D converter output register*.

This command enables the transmitter and phase detector, and performs an A/D conversion of the output of the phase detector with the A/D converter in relative mode. The phase measurement results can be calculated using the following formulas:

- $0 \leq \Phi \leq 17°$: result = 255
- $17 < \Phi < 163°$: angle [°] = 17 + (1 -result / 255) * 146
- $163 \geq \Phi \geq 180°$: result = 0

Duration time: 25 µs max.

4.4.12 Clear RSSI

The receiver automatically clears the RSSI bits in the *RSSI display register* and starts a new measurement of the RSSI when a new reception is started (e.g. after a Transmit direct command). Since the RSSI bits store the peak value (peak-hold type) eventual variation of the receiver input signal will not be followed (this can happen in case of a long message or test procedure).

The direct command Clear RSSI clears the RSSI bits in the *RSSI display register*, and restarts the RSSI measurement. This allows to obtain multiple RSSI measurements during a single reception.

4.4.13 Transparent mode

This command sets the receiver and transmitter into the transparent mode. The device enters the transparent mode on the rising edge of the BSS signal of the SPI frame used to send the direct command. The transparent mode is maintained as long as signal BSS is kept high, that is, the following SPI command sent from the microcontroller will automatically stop the transparent mode.

4.4.14 Measure power supply

This command measures the power supply. The bits mpsv<2:0> in the *Regulator voltage control register* select which signal is measured. The result of the measurement is stored in the *A/D converter output register*.

For power supply measurements the selected supply input voltage is divided by three and measured with the A/D converter in absolute mode. This leads to a resolution of 23.4 mV per LSB for all power supply measurements.

Duration time: 25 µs max.

4.5 Registers

The ST25R3918 has two register spaces, each of them consists of up to 64 registers with address ranging from 00h to 3Fh:

1. register space A (Rs-A), see *Table 13*
2. register space B (Rs-B), see *Table 14*.

There are two types of registers implemented in the ST25R3918:

1. configuration registers: used to configure the device, can be written and read through the SPI or I2C interfaces
2. display registers: read only (RO), contain information about the state of the device.

Registers are set to their default value at power-up and after sending the direct command *Set default*. Bits set as RFU must be kept at their reset values unless otherwise specified.

Table 13. List of registers - Space A

Type	Address (hex)	Register space A (Rs-A)
IO configuration	00	*IO configuration register 1*
	01	*IO configuration register 2*
Operation control and mode definition	02	*Operation control register*
	03	*Mode definition register*
	04	*Bit rate definition register*
Protocol configuration	05	*ISO14443A and NFC 106kb/s settings register*
	06	*ISO14443B settings register 1*
	07	*ISO14443B settings register*
	08	*Passive target definition register*
	09	*Stream mode definition register*
	0A	*Auxiliary definition register*
Receiver configuration	0B	*Receiver configuration register 1*
	0C	*Receiver configuration register 2*
	0D	*Receiver configuration register 3*
	0E	*Receiver configuration register 4*
Timer definition	0F	*Mask receive timer register*
	10	*No-response timer register 1*
	11	*No-response timer register 2*
	12	*Timer and EMV® control register*
	13	*General purpose timer register 1*
	14	*General purpose timer register 2*
	15	*Reserved register*

Table 13. List of registers - Space A (continued)

Type	Address (hex)	Register space A (Rs-A)
Interrupt and associated reporting	16	*Mask main interrupt register*
	17	*Mask timer and NFC interrupt register*
	18	*Mask error and wake-up interrupt register*
	19	*Mask passive target interrupt register*
	1A	*Main interrupt register*
	1B	*Timer and NFC interrupt register*
	1C	*Error and wake-up interrupt register*
	1D	*Passive target interrupt register*
	1E	*FIFO status register 1*
	1F	*FIFO status register 2*
	20	*Collision display register*
	21	*Passive target display register*
Definition of number of transmitted bytes	22	*Number of transmitted bytes register 1*
	23	*Number of transmitted bytes register 2*
	24	*Bit rate detection display register*
A/D converter output	25	*A/D converter output register*
Antenna calibration	26	*Reserved register*
	27	*Reserved register*
Antenna driver and modulation	28	*TX driver register*
	29	*Passive target modulation register*
External field detector threshold	2A	*External field detector activation threshold register*
	2B	*External field detector deactivation threshold register*
Regulator	2C	*Regulator voltage control register*
Receiver state display	2D	*RSSI display register*
	2E	*Gain reduction state register*
Auxiliary display	31	*Auxiliary display register*

Table 13. List of registers - Space A (continued)

Type	Address (hex)	Register space A (Rs-A)
Wake-up	32	*Wake-up timer control register*
	33	*Amplitude measurement configuration register*
	34	*Amplitude measurement reference register*
	35	*Amplitude measurement auto-averaging display register*
	36	*Amplitude measurement display register*
	37	*Phase measurement configuration register*
	38	*Phase measurement reference register*
	39	*Phase measurement auto-averaging display register*
	3A	*Phase measurement display register*
IC identity	3F	*IC identity register*

Table 14. List of registers - Space B

Type	Address (hex)	Register space B (Rs-B)
Protocol configuration	05	*EMD suppression configuration register*
	06	*Subcarrier start timer register*
Receiver configuration	0B	*Passive target receiver configuration register 1*
	0C	*Correlator configuration register 1*
	0D	*Correlator configuration register 2*
Timer definition	0F	*Squelch timer register*
	15	*NFC field on guard timer register*
Antenna driver and modulation	28	*Auxiliary modulation setting register*
	29	*TX driver timing register*
External field detector threshold	2A	*Resistive AM modulation register*
	2B	*TX driver timing display register*
Regulator	2C	*Regulator display register*
Protection	30	*Overshoot protection configuration register 1*
	31	*Overshoot protection configuration register 2*
	32	*Undershoot protection configuration register 1*
	33	*Undershoot protection configuration register 2*

4.5.1 IO configuration register 1

Register space: A

Address: 00h

Type: RW

Table 15. IO configuration register 1

<table>
<tr><th>Bit</th><th>Name</th><th>Default</th><th colspan="3">Function</th><th>Comments</th></tr>
<tr><td>7</td><td>single</td><td>0</td><td colspan="3">0: Differential antenna driving
1: Only one RFO driver will be used</td><td>Chooses between single and differential antenna driving.</td></tr>
<tr><td>6</td><td>rfo2</td><td>0</td><td colspan="3">0: RFO1, RFI1
1: RFO2, RFI2</td><td>Chooses which output driver and which input will be used in case of single driving.</td></tr>
<tr><td>5</td><td>i2c_thd1</td><td>0</td><td colspan="3" rowspan="2">I2C t_{HD}: non hs-modes / hs-modes
00: 380 ns / 160 ns
01: 180 ns / 160 ns
10: 180 ns / 70 ns
11: 100 ns / 70 ns</td><td>-</td></tr>
<tr><td>4</td><td>i2c_thd0</td><td>0</td><td>-</td></tr>
<tr><td>3</td><td>RFU</td><td>0</td><td colspan="3">-</td><td>-</td></tr>
<tr><td rowspan="3">2</td><td rowspan="3">out_cl1</td><td rowspan="3">0</td><td>out_cl1</td><td>out_cl0</td><td>MCU_CLK</td><td rowspan="5">Selection of clock frequency on MCU_CLK output in case Xtal oscillator is running. With “11” MCU_CLK output is permanently low.</td></tr>
<tr><td>0</td><td>0</td><td>3.39 MHz</td></tr>
<tr><td>0</td><td>1</td><td>6.78 MHz</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">out_cl0</td><td rowspan="2">0</td><td>1</td><td>0</td><td>13.56 MHz</td></tr>
<tr><td>1</td><td>1</td><td>Disabled</td></tr>
<tr><td>0</td><td>lf_clk_off</td><td>0</td><td colspan="3">0: LF clock on MCU_CLK
1: No LF clock on MCU_CLK</td><td>By default the 32 kHz LF clock is present on MCU_CLK output when Xtal oscillator is not running and the MCU_CLK output is not disabled.</td></tr>
</table>

4.5.2 IO configuration register 2

Register space: A

Address: 01h

Type: RW

Table 16. IO configuration register 2

Bit	Name	Default	Function	Comments
7	sup3V	0	0: 5 V supply 1: 3.3 V supply	Set to 0 for 3.6 V < V_{DD} ≤ 5.5 V Set to 1 for 2.4 V ≤ V_{DD} ≤ 3.6 V
6	vspd_off	0	0: Enable V_{DD_D} regulator 1: Disable V_{DD_D} regulator	Used for low cost applications. When this bit is set: – at 3 V or 5 V supply VDD_D and VDD_A must be shorted externally
5	RFU	0	Not used	-
4	miso_pd2	0	1: Pull-down on MISO, when BSS is low and MISO is not driven by the ST25R3918.	Valid only in SPI mode.
3	miso_pd1	0	1: Pull-down on MISO when BSS is high	
2	io_drv_lvl	0	0: Normal IO driver level 1: Increase IO driving level	Increases IO driver strength of MISO, MCU_CLK an IRQ. Recommended to set to 1 for all I2C operation, and for SPI operation if V_{DD_IO} < 3.3 V.
1	am_ref_rf	0	0: V_{DD_AM} regulator reference from V_{DD_DR} 1: V_{DD_AM} regulator reference from V_{DD_RF}	Selects non modulated RF voltage level reference of the V_{DD_AM} voltage regulator.
0	slow_up	0	1: Slow ramp at Tx on	≥ 10 µs, 10% to 90%, for B

4.5.3 Operation control register

Address: 02h

Type: RW

Table 17. Operation control register[1]

Bit	Name	Default	Function	Comments
7	en	0	1: Enables oscillator and regulator (Ready mode)	-
6	rx_en	0	1: Enables Rx operation	-
5	rx_chn	0	0: Both, AM and PM, channels enabled 1: One channel enabled	If only one Rx channel is enabled, selection is done by the *Receiver configuration register 1* bit ch_sel.
4	rx_man	0	0: Automatic channel selection 1: Manual channel selection	If both Rx channels are enabled, chooses the method of channel selection, manual selection is done by the *Receiver configuration register 1* bit ch_sel.
3	tx_en	0	1: Enables Tx operation	This bit is automatically set by NFC Field ON commands and reset in NFC active communication modes after transmission is finished.
2	wu	0	1: Enables Wake-up mode	According to settings in *Wake-up timer control register*.
1	en_fd_c1	0	00: External field detector off. 01: Manually enable external field detector with collision avoidance detection threshold. 10: Manually enable external field detector with peer detection threshold. 11: Enable external field detector automatically.	01: External field detector with collision avoidance detection must be used in R/W mode when using NFC field on commands. 11: External field detector with peer detection/collision avoidance threshold activated automatically must be used in NFCIP-1 active communication (AP2P) and Passive target modes. en_fd_c<1:0> ≠ 0 and other bits in Operation control register set to 0 put the device in Low power initial NFC mode.
0	en_fd_c0	0		

1. Default setting takes place at power-up only.

4.5.4 Mode definition register

Register space: A

Address: 03h

Type: RW

Table 18. Mode definition register(1)

Bit	Name	Default	Function	Comments
7	targ	0	0: Initiator 1: Target	-
6	om3	0	Refer to *Table 19* and *Table 20*	Selection of operation mode. Different for initiator and target modes.
5	om2	0		
4	om1	0		
3	om0	1		
2	tr_am	0	0: OOK 1: AM	Selects RF modulation mode.
1	RFU	0	-	-
0	RFU	0	-	-

1. Register can be written only in case crystal clock is present and stable (oscok = 1).

Table 19. Initiator operation modes(1)

om3	om2	om1	om0	Comments
0	0	0	1	ISO14443A
0	0	1	0	ISO14443B
0	1	0	0	NFC Forum Type 1 tag (Topaz)
1	1	1	0	Sub-carrier stream mode
1	1	1	1	BPSK stream mode
Other combinations				RFU

1. If a non supported operation mode is selected the Tx/Rx operation is disabled.

Table 20. Target operation modes(1)

om3	om2	om1	om0	Comments
0	0	0	1	ISO14443A passive target mode
0	1	0	0	FeliCa™ passive target mode
1	x	x	x	Bit rate detection mode – om2: enable FeliCa™ bit rate detection mode – om1: RFU – om0: enable ISO14443A bit rate detection mode
Other combinations				Not allowed

1. The nfc_f0 = 1 must not be set in Bit rate detection mode (see *Table 22*).

4.5.5 Bit rate definition register

Register space: A

Address: 04h

Type: RW

Table 21. Bit rate definition register

Bit	Name	Default	Function	Comments
7	RFU	0	Refer to *Table 22*	-
6	RFU	0		-
5	tx_rate1	0		Selects bit rate for Tx.
4	tx_rate0	0		
3	RFU	0		-
2	RFU	0		-
1	rx_rate1	0		Selects bit rate for Rx.
0	rx_rate0	0		

Table 22. Bit rate coding(1)

rate3	rate2	rate1	rate0	Bit rate (kbit/s)	Comments
0	0	0	0	fc / 128 (~106)	-
0	0	0	1	fc / 64 (~212)	-
0	0	1	0	fc / 32 (~424)	-
0	0	1	1	fc / 16 (~848)	-
Other combinations				-	Not used

1. If a non supported bit rate is selected the Tx/Rx operation is disabled.

4.5.6 ISO14443A and NFC 106kb/s settings register

Register space: A

Address: 05h

Type: RW

Table 23. ISO14443A and NFC 106kb/s settings register

Bit	Name	Default	Function	Comments
7	no_tx_par	0	1: No parity bit is generated during Tx	Data stream is taken from FIFO, transmit to be done using command Transmit Without CRC(1).
6	no_rx_par	0	1: Receive and put in FIFO also the parity bit	When set to 1 received bit stream is put in the FIFO, no parity and CRC detection is done(1). Supported only for 106 kbit/s data rate.
5	nfc_f0	0	1: Support of NFCIP-1 Transport Frame format	Adds SB (F0) and LEN bytes during Tx and skip SB (F0) byte during Rx. Must not be set in bit rate detection mode.
4	p_len3	0	Refer to *Table 24*	Modulation pulse width, defined in number of 13.56 MHz clock periods.
3	p_len2	0		
2	p_len1	0		
1	p_len0	0		
0	antcl	0	0: Standard frame 1: ISO14443 anticollision frame	Must be set to 1 for reception of ISO14443A bit oriented anticollision frames in reader mode. Must be set to 0 for all other frames and modes.

1. Supported in reader modes only, not supported in card emulation modes.

Table 24. ISO14443A modulation pulse width

p_len3	p_len2	p_len1	p_len0	Pulse width in number of 1 / fc for different bit rates			
				fc / 128	fc / 64	fc / 32	fc / 16
0	1	1	1	42	-	-	-
0	1	1	0	41	24	-	-
0	1	0	1	40	23	-	-
0	1	0	0	39	22	13	-
0	0	1	1	38	21	12	8
0	0	1	0	37	20	11	7
0	0	0	1	36	19	10	6
0	0	0	0	35	18	9	5
1	1	1	1	34	17	8	4
1	1	1	0	33	16	7	3
1	1	0	1	32	15	6	2
1	1	0	0	31	14	5	-

Table 24. ISO14443A modulation pulse width (continued)

p_len3	p_len2	p_len1	p_len0	Pulse width in number of 1 / fc for different bit rates			
				fc / 128	fc / 64	fc / 32	fc / 16
1	0	1	1	30	13	-	-
1	0	1	0	29	12	-	-
1	0	0	1	28	-	-	-
1	0	0	0	27	-	-	-

4.5.7 ISO14443B settings register 1

Register space: A

Address: 06h

Type: RW

Table 25. ISO14443B settings register 1

<table>
<tr><th>Bit</th><th>Name</th><th>Default</th><th colspan="4">Function</th><th>Comments</th></tr>
<tr><td rowspan="2">7</td><td rowspan="2">egt2</td><td rowspan="2">0</td><td>egt2</td><td>egt1</td><td>egt0</td><td>Number of etu</td><td rowspan="6">EGT defined in number of etu</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">egt1</td><td rowspan="2">0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>⋮</td><td>⋮</td><td>⋮</td><td>⋮</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">egt0</td><td rowspan="2">0</td><td>1</td><td>1</td><td>0</td><td>6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>6</td></tr>
<tr><td>4</td><td>sof_0</td><td>0</td><td colspan="4">0: 10 etu
1: 11 etu</td><td>SOF, number of etu with logic 0</td></tr>
<tr><td>3</td><td>sof_1</td><td>0</td><td colspan="4">0: 2 etu
1: 3 etu</td><td>SOF, number of etu with logic 1</td></tr>
<tr><td>2</td><td>eof</td><td>0</td><td colspan="4">0: 10 etu
1: 11 etu</td><td>EOF, number of etu with logic 0</td></tr>
<tr><td>1</td><td>half</td><td>0</td><td colspan="4">0: SOF and EOF defined by sof_0, sof_1, and eof bit
1: SOF 10.5 etu logic 0, 2.5 etu logic 1, EOF: 10.5 etu logic 0</td><td>Sets SOF and EOF settings in middle of specification.</td></tr>
<tr><td>0</td><td>rx_st_om</td><td>0</td><td colspan="4">0: Start/stop bit must be present for Rx
1: Start/stop bit omission for Rx</td><td>SOF fixed to 10 low and 2 etu high, EOF not defined, put in FIFO last full byte.
CRC is not checked in this mode.
Supported only in a coherent reception mode.</td></tr>
</table>

4.5.8 ISO14443B settings register

Register space: A

Address: 07h

Type: RW

Table 26. ISO14443B and FeliCa settings register

Bit	Name	Default	Function	Comments
7	tr1_1	0	Refer to *Table 27*	-
6	tr1_0	0		
5	no_sof	0	1: No SOF PICC to PCD	According to ISO14443-3 chapter 7.10.3.3. Support of B'.
4	no_eof	0	1: No EOF PICC to PCD	According to ISO14443-3 chapter 7.10.3.3. Supported only in coherent reception mode.
3	RFU	0	-	-
2	RFU	0	-	-
1	RFU	0	-	-
0	RFU	0	-	-

Table 27. Minimum TR1 codings

tr1_1	tr1_0	Minimum TR1 for a PICC to PCD bit rate	
		fc / 128	>fc / 128
0	0	80 / fs	
0	1	64 / fs	32 / fs
1	0	Not used	
1	1	Not used	

4.5.9 Passive target definition register

Register space: A

Address: 08h

Type: RW

Table 28. NFCIP-1 passive target definition register

Bit	Name	Default	Function	Comments
7	fdel3	0	PCD to PICC FDT compensation. Frame compensation defined as fdel<3:0>*1 / fc	Valid for NFC-A CE mode – fdel = 0: Nominal FDT time in produced in logic. – fdel > 0: Shortens the FDT provided by logic. Due to signal processing delays fdel<3:0> = 2 is expected to be a good setting (best value dependents also on filter and antenna).
6	fdel2	0		
5	fdel1	0		
4	fdel0	0		
3	RFU	0	RFU	-
2	d_212/424_1r	0	0: Enable automatic SENSF_RES 1: Disable automatic SENSF_RES	Disables the automatic responses in passive target mode, and completely operates via FIFO.
1	RFU	0	RFU	
0	d_106_ac_a	0	0: Enable automatic anti-collision in NFC-A 1: Disable automatic anti-collision in NFC-A	

4.5.10 Stream mode definition register

Register space: A

Address: 09h

Type: RW

Table 29. Stream mode definition register

<table>
<tr><th>Bit</th><th>Name</th><th>Default</th><th colspan="3">Function</th><th>Comments</th></tr>
<tr><td>7</td><td>RFU</td><td>0</td><td colspan="3">-</td><td>-</td></tr>
<tr><td>6</td><td>scf1</td><td>0</td><td colspan="3" rowspan="2">Refer to Table 30</td><td rowspan="2">Sub-carrier frequency definition for Sub-carrier and BPSK stream mode.</td></tr>
<tr><td>5</td><td>scf0</td><td>0</td></tr>
<tr><td rowspan="3">4</td><td rowspan="3">scp1</td><td rowspan="3">0</td><td>scp1</td><td>scp0</td><td>Number of pulses</td><td rowspan="5">Number of sub-carrier pulses in report period for Sub-carrier and BPSK stream mode.</td></tr>
<tr><td>0</td><td>0</td><td>1 (BPSK only)</td></tr>
<tr><td>0</td><td>1</td><td>2 (BPSK only)</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">scp0</td><td rowspan="2">0</td><td>1</td><td>0</td><td>4</td></tr>
<tr><td>1</td><td>1</td><td>8</td></tr>
<tr><td>2</td><td>stx2</td><td>0</td><td colspan="3" rowspan="3">Refer to Table 31</td><td rowspan="3">Definition of time period for Tx modulator control (for Sub-carrier and BPSK stream mode).</td></tr>
<tr><td>1</td><td>stx1</td><td>0</td></tr>
<tr><td>0</td><td>stx0</td><td>0</td></tr>
</table>

Table 30. Sub-carrier frequency definition for Sub-carrier stream mode

scf1	scf0	Sub-carrier mode	BPSK mode
0	0	fc / 64 (212 kHz)	fc / 16 (848 kHz)
0	1	fc / 32 (424 kHz)	RFU
1	0	fc / 16 (848 kHz)	
1	1	fc / 8 (1695 kHz)	

Table 31. Definition of time period for Stream mode Tx modulator control

stx2	stx1	stx0	Time period
0	0	0	fc / 128 (106 kHz)
0	0	1	fc / 64 (212 kHz)
0	1	0	fc / 32 (424 kHz)
0	1	1	fc / 16 (848 kHz)
1	X	X	RFU

4.5.11 Auxiliary definition register

Register space: A

Address: 0Ah

Type: RW

Table 32. Auxiliary definition register

Bit	Name	Default	Function	Comments
7	no_crc_rx	0	0: Receive with CRC check 1: Receive without CRC check	Valid for all protocols, for ISO14443A REQA, WUPA and anticollision receive without CRC is done automatically(1).
6	RFU	0	-	-
5	nfc_id1	0	00: 4 bytes NFCID1 01: 7 bytes NFCID1 1x: RFU	Selects NFCID1 size.
4	nfc_id0	0		
3	mfaz_cl90	0	0: 0° shifted clock for phase measurement 1: 90° shifted clock for phase measurement	Affects also PM demodulation. Should be set to 0 for PM demodulation.
2	dis_corr	0	Refer to *Table 33*	Selects RW receiver operation.
1	nfc_n1	0	-	Value of n for direct commands NFC Initial Field ON (0...3)(2).
0	nfc_n0	0		

1. Receive without CRC is done automatically when REQA and WUPA commands are sent using, respectively, direct commands Transmit REQA and Transmit WUPA, and in case anticollision is performed setting bit antcl.
2. The value of nfc_n<1:0> must be set prior to the NFC Initial Field ON operation.

Table 33. RW receiver operation

Mode	dis_corr = 0	dis_corr = 1
ISO-A (106 to 848 kHz)	Correlator reception	NA
ISO-B (106 to 848 kHz)		Pulse reception (coherent)
NFC Forum Type 1 Tag (Topaz)		NA
Stream modes (scf<1:0> = 01, scp<1:0> = 11)		Pulse reception
Stream modes - Others	NA	Pulse reception

4.5.12 EMD suppression configuration register

Register space: B

Address: 05h

Type: RW

Table 34. EMD suppression configuration register

Bit	Name	Default	Function	Comments
7	emd_emv	0	0: Disable EMD suppression 1: Enable EMD suppression according to EMVCo	Bits no_rx_par and no_crc_rx must be set to 0, and bit nrt_emv must be set to 1 when emd_emv is enabled
6	rx_start_emv	0	0: Reception is enabled (I_rxs) only if the first four bits of the frame are error free 1: Reception is enabled (I_rxs) also if there is an error in the first four bits of the frame	Applies to ISO-A 106k only. Must be set to 1 for EMVCo compliance.
5	RFU	0	-	-
4	RFU	0	-	-
3	emd_thld3	0	If the received frame is less than emd_thld<3:0> bytes long then EMD suppression will trigger on reception errors	Must be set to 4 for EMVCo compliance.
2	emd_thld2	0		
1	emd_thld1	0		
0	emd_thld0	0		

4.5.13 Subcarrier start timer register

Register space: B

Address: 06h

Type: RW

Table 35. Subcarrier start timer register

Bit	Name	Default	Function	Comments
7:5	RFU	0	-	-
4:0	sst<4:0>	0	Subcarrier start time Step: 0.25 etu Range: 0 etu to 7.75 etu	Applies to ISO-B, 106 kb/s. If the time from the end of the MRT timer to the detection of a subcarrier is shorter than sst<4:0>, then a soft error interrupt is generated. If emd_emv = 1 the frame will be suppressed as EMD and a restart interrupt will be generated. Note that corr_s3 defines the length of subcarrier start detection and affects the correct sst<4:0> setting.

4.5.14 Receiver configuration register 1

Register space: A

Address: 0Bh

Type: RW

Table 36. Receiver configuration register 1

Bit	Name	Default	Function	Comments
7	ch_sel	0	0: Enable AM channel 1: Enable PM channel	If only one Rx channel is enabled in the *Operation control register* defines which channel is enabled. If both channels are enabled and manual channel selection is active defines which channel is used for receive framing.
6	lp2	0	Low-pass control (see *Table 3*)	-
5	lp1	0		
4	lp0	0		
3	z600k	0	First and third stage zero setting (see *Table 4*)	
2	h200	0		
1	h80	0		
0	z12k	0		

4.5.15 Receiver configuration register 2

Register space: A

Address: 0Ch

Type: RW

Table 37. Receiver configuration register 2

Bit	Name	Default	Function	Comments
7	demod_mode	0	0: AM/PM demodulation 1: I/Q demodulation	Selects demodulator operation mode. I/Q demodulation requires amd_sel = 1.
6	amd_sel	0	0: peak detector 1: mixer	Selects AM demodulator.
5	sqm_dyn	1	0: Squelch disabled 1: Automatic squelch activation after end of TX	Squelch is activated 18.88 µs after end of TX, and stops when the Mask receive timer reaches the sqt<7:0> setting.
4	pulz_61	0	0: Squelch ratio 1 1: Squelch ratio 6/3	Select squelch trigger level. Squelch triggers on signals that are 1 or 6/3 times larger than the digitizing threshold. – Ratio 1: recommended for ISO-A 106k correlator, ISO-A HBR/ISO-B pulse decoder and ISO-15693 – Ratio 6/3: recommended for ISO-A HBR/ISO-B correlator
3	agc_en	1	0: AGC disabled 1: AGC enabled	-
2	agc_m	1	0: AGC operates on first eight sub-carrier pulses 1: AGC operates during complete receive period	-
1	agc_alg	0	0: Algorithm with preset is used 1: Algorithm with reset is used	Algorithm with preset is recommended for protocols with short SOF (like ISO14443A fc / 128).
0	agc6_3	0	0: AGC ratio 3 1: AGC ratio 6	Select AGC trigger level. AGC triggers on signals 3 or 6 times above the minimum detectable signal level.

4.5.16 Receiver configuration register 3

Register space: A

Address: 0Dh

Type: RW

Table 38. Receiver configuration register 3

Bit	Name	Default	Function	Comments
7	rg1_am2	1	Gain reduction/boost in first gain stage of AM channel.	0: Full gain 1-6: Gain reduction 2.5 dB per step (15 dB total) 7: Boost + 5.5 dB
6	rg1_am1	1		
5	rg1_am0	0		
4	rg1_pm2	1	Gain reduction/boost in first gain stage of PM channel.	0: Full gain 1-6: Gain reduction 2.5 dB per step (15 dB total) 7: Boost + 5.5 dB
3	rg1_pm1	1		
2	rg1_pm0	0		
1	lf_en	0	0: HF signal on receiver input 1: LF signal on receiver input	-
0	lf_op	0	0: differential LF operation 1: LF input split (RFI1 to AM channel, RFI2 to PM channel)	-

4.5.17 Receiver configuration register 4

Register space: A

Address: 0Eh

Type: RW

Table 39. Receiver configuration register 4(1)

Bit	Name	Default	Function	Comments
7	rg2_am3	0	AM channel: gain reduction in second and third stage and digitizer	Only values from 0h to Ah are used: – settings 1h to 4h reduce gain by increasing the digitizer window in 3 dB steps – values from 5h to Ah additionally reduce the gain in second and third gain stage, always in 3 dB steps.
6	rg2_am2	0		
5	rg2_am1	0		
4	rg2_am0	0		
3	rg2_pm3	0	PM channel: gain reduction in second and third stage and digitizer	Only values from 0h to Ah are used: – settings 1h to 4h reduce gain by increasing the digitizer window in 3 dB steps – values from 5h to Ah additionally reduce the gain in second and third gain stage, always in 3 dB steps.
2	rg2_pm2	0		
1	rg2_pm1	0		
0	rg2_pm0	0		

1. Direct command *Reset RX gain* is necessary to load the value of this register into AGC, Squelch, and RSSI block.

4.5.18 Passive target receiver configuration register 1

Register space: B

Address: 0Bh

Type: RW

Table 40. P2P receiver configuration register 1

Bit	Name	Default	Function	Comments
7	ook_fd	0	OOK fast decay	-
6	ook_rc1	0	00 = 1.4 µs 01 = 1.0 µs 10 = 0.6 µs 11 = 0.2 µs	OOK RC time constant
5	ook_rc0	0		
4	ook_thd1	0	Refer to *Table 41*	OOK threshold level, depends on ook_rc<1:0> configuration.
3	ook_thd0	1		
2	ask_rc1	1	00 = 8.4 µs 01 = 6.8 µs 10 = 4.4 µs 11 = 2.4 µs	ASK RC time constant
1	ask_rc0	0		
0	ask_thd	0	0: 97% 1: 95%	ASK threshold level

Table 41. OOK threshold level settings

ook_thd<1:0>	ook_rc<1:0> = 0	ook_rc<1:0> > 0
00	55%	80%
01	45%	75%
10	35%	70%
11	25%	65%

4.5.19 Correlator configuration register 1

Register space: B

Address: 0Ch

Type: RW

Table 42. Correlator configuration register 1

Bit	Name	Default	Function		Comments
7	corr_s7	1	AGC = max |AM, PM|		-
6	corr_s6	0	ISO-A 106k	0: Collision detection level defined by corr_s<1:0> 1: Collision detection level equal to data slicer level	Selecting the collision detection level with corr_s<1:0> gives better detection of weak collisions. Setting the collision detection level equal to the data slicer gives better noise immunity.
			BPSK (1)	0: Correlator phase correction applied during the complete reception 1: No correlator phase correction after the first data bytes	No phase correction after start recommended for ISO-B 424 kb/s and 848 kb/s operation.
5	corr_s5	0	0: V_{ref} -50 mV setting, first squelch step -100 mV 1: V_{ref} -100 mV setting,first squelch step -200 mV		-
4	corr_s4	1	0: AM and PM correlation signals digitized separately 1: AM and PM correlation signals summed before digitizing (summation mode)		Summation mode is recommended for all correlation operations
3	corr_s3	0	0: RX bit rate 106kb/s = 17, RX bit rates 212 to 848 kb/s = 9 1: RX bit rate 106kb/s = 33, RX bit rates 212 to 848 kb/s = 17		BPSK start length setting (delay from the start of a tags subcarrier signal to the moment when a subcarrier start is detected). Then circuit starts observing for the first phase transition (9/17/33 ± 2 pilot pulses). At this moment the sst<4:0> check for TR0 is done.
2	corr_s2	0	ISO-A 106k	0: Normal data slicer 1: Fast data slicer	-
			BPSK(1)	0: Normal reference time constant 1: Long reference time constant (1.5x normal)	
1	corr_s1	1	ISO-A 106k	Collision level setting MSB	Collision detection level, compared to data detection level: – 00: 16% – 01: 28% – 10: 41% – 11: 53%
			BPSK(1)	Subcarrier end detection level 0: 100% 1: 66%	
0	corr_s0	1	ISO-A 106k	Collision level setting LSB	
			BPSK(1)	0: Subcarrier end detector disabled 1: Subcarrier end detector enabled	

1. BPSK options apply to ISO-A HBR and ISO-B (all bit rates).

4.5.20 Correlator configuration register 2

Register space: B

Address: 0Dh

Type: RW

Table 43. Correlator configuration register 2

Bit	Name	Default	Function	Comments
7	RFU	0	-	-
6	RFU	0		
5	RFU	0		
4	RFU	0		
3	RFU	0		
2	RFU	0		
1	corr_s9	0	0: Sleep mode disable set by timer 1: Sleep mode disable only on rx_on = 1	Correlator sleep mode option. Sleep start: 18 µs no output pulse. Stop with timer: – takes 18 µs (ISO-A/B, F424) – takes 42 µs (stream 15693, F212)
0	corr_s8	0	0: All other standards 1: 424 kHz subcarrier stream mode	Must be set to 1 for 424 kHz subcarrier stream mode.

4.5.21 Mask receive timer register

Register space: A

Address: 0Fh

Type: RW

Table 44. Mask receive timer register

Bit	Name	Default	Function	Comments
7	mrt7	0	mrt_step = 0: Step: 64 / fc (4.72 µs) Range: 256 / fc (~18.88 µs) to 16320 / fc (~1.2 ms) mrt_step = 1: Step: 512 / fc (37.78 µs) Range: 2048 / fc (151 µs) to 130560 / fc (9.62 ms)	Set time after end of TX during which the receiver output is ignored (masked). The minimum mask receive time of 18.88 µs covers the transients in receiver after end of transmission.
6	mrt6	0		
5	mrt5	0		
4	mrt4	0		
3	mrt3	1		
2	mrt2	0		
1	mrt1	0		
0	mrt0	0		

4.5.22 No-response timer register 1

Register space: A

Address: 10h

Type: RW

Table 45. No-response timer register 1

Bit	Name	Default	Function	Comments
7	nrt15	0	No-response timer definition MSB bits nrt_step = 0: Step: 64 / fc (4.72 µs), Range: 309 ms nrt_step = 1: Step: 4096 / fc (302 µs) Range: 19.8 s.	Defines timeout after end of Tx. If this timeout expires without detecting a response a No-response interrupt is sent. In NFC mode the No-response timer is started only when external field is detected. All 0: No-response timer is not started. No-response timer is reset and restarted with Start No-response timer direct command.
6	nrt14	0		
5	nrt13	0		
4	nrt12	0		
3	nrt11	0		
2	nrt10	0		
1	nrt9	0		
0	nrt8	0		

4.5.23 No-response timer register 2

Register space: A

Address: 11h

Type: RW

Table 46. No-response timer register 2

Bit	Name	Default	Function	Comments
7	nrt7	0	No-response timer definition LSB bits	-
6	nrt6	0		
5	nrt5	0		
4	nrt4	0		
3	nrt3	0		
2	nrt2	0		
1	nrt1	0		
0	nrt0	0		

4.5.24 Timer and EMV® control register

Register space: A

Address: 12h

Type: RW

Table 47. Timer and EMV control register

Bit	Name	Default	Function	Comments
7	gptc2	0	General purpose timer trigger source. Refer to *Table 48*.	-
6	gptc1	0		
5	gptc0	0		
4	RFU	0	-	-
3	mrt_step	0	0: 64 / fc 1: 512 / fc	Mask receive timer step size
2	RFU	0	-	-
1	nrt_emv	0	1: No-response timer EMV mode	-
0	nrt_step	0	0: 64 / fc 1: 4096 / fc	No-response timer step size.

Table 48. Trigger sources

gptc2	gptc1	gptc0	Trigger source
X	X	X	The timer starts always with direct command Start General purpose timer.
0	0	0	No additional trigger source.
0	0	1	Additionally starts at End of RX (after EOF).
0	1	0	Additionally starts at Start of RX.
0	1	1	Additionally starts at End of TX.
1	0	0	RFU
1	0	1	
1	1	0	
1	1	1	

4.5.25 General purpose timer register 1

Register space: A

Address: 13h

Type: RW

Table 49. General purpose timer register 1

Bit	Name	Default	Function	Comments
7	gpt15	-	General purpose timeout definition MSB bits Defined in steps of 8 / fc (590 ns) Range from 590 ns to 38,7 ms	-
6	gpt14	-		
5	gpt13	-		
4	gpt12	-		
3	gpt11	-		
2	gpt10	-		
1	gpt9	-		
0	gpt8	-		

4.5.26 General purpose timer register 2

Register space: A

Address: 14h

Type: RW

Table 50. General purpose timer register 2

Bit	Name	Default	Function	Comments
7	gpt7	-	General purpose timeout definition LSB bits Defined in steps of 8 / fc (590 ns) Range from 590 ns to 38,7 ms	-
6	gpt6	-		
5	gpt5	-		
4	gpt4	-		
3	gpt3	-		
2	gpt2	-		
1	gpt1	-		
0	gpt0	-		

4.5.27 Reserved register

Register space: A

Address: 15h

Type: R

Table 51. Reserved register

Bit	Name	Default	Function	Comments
7	RFU	0	-	-
6	RFU	0	-	-
5	RFU	0	-	-
4	RFU	0	-	-
3	RFU	0	-	-
2	RFU	0	-	-
1	RFU	0	-	-
0	RFU	0	-	-

4.5.28 Squelch timer register

Register space: B

Address: 0Fh

Type: RW

Table 52. Squelch timer register

Bit	Name	Default	Function	Comments
7	sqt7	0	Squelch Timer Step, Range: same as *Mask receive timer register*, including mrt_step selection	Squelch is enabled ~20 µs after the end of reader data transmission – sqt<7:0> > 5: Squelch stops after the time defined by sqt<7:0>. Gain reduction due to squelch is locked and used as a starting point for AGC. – Sqt<7:0> ≤ 5 or sqt<7:0> ≥ mrt<7:0>: Squelch is enabled until the MRT expires.
6	sqt6	0		
5	sqt5	0		
4	sqt4	0		
3	sqt3	0		
2	sqt2	0		
1	sqt1	0		
0	sqt0	0		

4.5.29 NFC field on guard timer register

Register space: B

Address: 15h

Type: RW

Table 53. NFC field on guard timer register

Bit	Name	Default	Function	Comments
7	nfc_gt7	0	NFC field on guard timer Step: 2048 / fc (151 µs) Range: 38.66 ms	Used by NFC field on commands. The value nfc_gt<7:0> is added to the initial 75 µs in T_{IRFG} and T_{ARFG}. Set to 33 for T_{IRFG} (75 µs + 4.984 ms= 5.06 ms) Set to 0 for T_{ARFG} (75 µs + 0 ms = 75 µs)
6	nfc_gt6	0		
5	nfc_gt5	1		
4	nfc_gt4	1		
3	nfc_gt3	0		
2	nfc_gt2	0		
1	nfc_gt1	1		
0	nfc_gt0	1		

4.5.30 Mask main interrupt register

Register space: A

Address: 16h

Type: RW

Table 54. Mask main interrupt register

Bit	Name	Default	Function	Comments
7	M_osc	0	1: Mask IRQ when oscillator frequency is stable	-
6	M_wl	0	1: Mask IRQ due to FIFO water level	-
5	M_rxs	0	1: Mask IRQ due to start of receive	-
4	M_rxe	0	1: Mask IRQ due to end of receive	-
3	M_txe	0	1: Mask IRQ due to end of transmission	-
2	M_col	0	1: Mask IRQ due to bit collision	-
1	M_rx_rest	0	1: Mask IRQ due to automatic reception restart	-
0	RFU	0	Not used	-

4.5.31 Mask timer and NFC interrupt register

Register space: A

Address: 17h

Type: RW

Table 55. Mask timer and NFC interrupt register

Bit	Name	Default	Function	Comments
7	M_dct	0	1: Mask IRQ due to termination of direct command	-
6	M_nre	0	1: Mask IRQ due to No-response timer expire	-
5	M_gpe	0	1: Mask IRQ due to general purpose timer expire	-
4	M_eon	0	1: Mask IRQ due to detection of external field higher than Target activation level	-
3	M_eof	0	1: Mask IRQ due to detection of external field drop below Target activation level	-
2	M_cac	0	1: Mask IRQ due to detection of collision during RF Collision Avoidance	-
1	M_cat	0	1: Mask IRQ after minimum guard time expire	-
0	M_nfct	0	1: Mask IRQ when in target mode the initiator bit rate has been recognized	-

4.5.32 Mask error and wake-up interrupt register

Register space: A

Address: 18h

Type: RW

Table 56. Mask error and wake-up interrupt register

Bit	Name	Default	Function	Comments
7	M_crc	0	1: Mask IRQ due to CRC error	-
6	M_par	0	1: Mask IRQ due to parity error	-
5	M_err2	0	1: Mask IRQ due to soft framing error	-
4	M_err1	0	1: Mask IRQ due to hard framing error	-
3	M_wt	0	1: Mask IRQ due to wake-up timer interrupt	-
2	M_wam	0	1: Mask Wake-up IRQ due to amplitude measurement	-
1	M_wph	0	1: Mask Wake-up IRQ due to phase measurement.	-
0	M_wcap	0	1: Mask Wake-up IRQ due to capacitance measurement	-

4.5.33 Mask passive target interrupt register

Register space: A

Address: 19h

Type: RW

Table 57. Mask passive target interrupt register

Bit	Name	Default	Function	Comments
7	RFU	0	-	-
6	M_sl_wl	0	1: Mask IRQ for Passive target slot number water level	-
5	M_apon	0	1: Mask IRQ due to Active PP Field on event	-
4	M_rxe_pta	0	1: Mask IRQ due to end of receive when the device is handling the response	-
3	M_wu_f	0	1: Mask IRQ NFC 212/424 kb/s passive target active	-
2	RFU	0	-	-
1	M_wu_a*	0	1: Mask IRQ NFC 106 kb/s passive target Active*	-
0	M_wu_a	0	1: Mask IRQ NFC 106 kb/s passive target Active	-

4.5.34 Main interrupt register

Register space: A

Address: 1Ah

Type: R

Table 58. Main interrupt register

Bit	Name	Default	Function	Comments
7	I_osc	-	IRQ when oscillator frequency is stable	Set after oscillator is started by setting *Operation control register* bit en.
6	I_wl	-	IRQ due to FIFO water level	Set during receive, if more than 300 bytes are in the FIFO. Set during transmit, if less than 200 bytes are in the FIFO.
5	I_rxs	-	IRQ due to start of receive	-
4	I_rxe	-	IRQ due to end of receive	-
3	I_txe	-	IRQ due to end of transmission	-
2	I_col	-	IRQ due to bit collision	-
1	I_rx_rest	-	IRQ due to automatic reception restart	Set when a frame is suppressed as EMD
0	RFU	-	-	-

4.5.35 Timer and NFC interrupt register

Register space: A

Address: 1Bh

Type: R

Table 59. Timer and NFC interrupt register(1)

Bit	Name	Default	Function	Comments
7	I_dct	-	IRQ due to termination of direct command	-
6	I_nre	-	IRQ due to No-response timer expire	-
5	I_gpe	-	IRQ due to general purpose timer expire	-
4	I_eon	-	IRQ due to detection of external field higher than Target activation level	-
3	I_eof	-	IRQ due to detection of external field drop below Target activation level	-
2	I_cac	-	IRQ due to detection of collision during RF collision avoidance	I-cac must be cleared before collision avoidance.
1	I_cat	-	IRQ after minimum guard time expire	An external field was not detected during RF collision avoidance, field was switched on, IRQ sent after minimum guard time according to NFCIP-1.
0	I_nfct	-	IRQ when in target mode the initiator bit rate was recognized	-

1. After register has been read, its content is set to 0.

4.5.36 Error and wake-up interrupt register

Register space: A

Address: 1Ch

Type: R

Table 60. Error and wake-up interrupt register(1)

Bit	Name	Default	Function	Comments
7	I_crc	-	CRC error	-
6	I_par	-	Parity error	-
5	I_err2	-	Soft framing error	Framing error that does not result in corrupted Rx data.
4	I_err1	-	Hard framing error	Framing error that results in corrupted Rx data.
3	I_wt	-	Wake-up timer interrupt	Timeout after execution of Start Wake-Up Timer command in case option with IRQ at every timeout is selected.
2	I_wam	-	Wake-up interrupt due to amplitude measurement	Result of amplitude measurement Δam larger than reference.
1	I_wph	-	Wake-up interrupt due to phase measurement.	Result of phase measurement Δpm larger than reference.
0	I_wcap	-	Wake-up interrupt due to capacitance measurement	Result of capacitance measurement Δcm larger than reference.

1. After Main interrupt register has been read, its content is set to 0.

4.5.37 Passive target interrupt register

Register space: A

Address: 1Dh

Type: R

Table 61. Passive target interrupt register[(1)]

Bit	Name	Default	Function	Comments
7	RFU	-	RFU	-
6	I_sl_wl	-	IRQ for passive target slot number water level	Sent if four unused slot numbers (TSN) remain in PT_memory.
5	I_apon	-	IRQ due to field on event	Sent after RF collision avoidance, if there was no collision and field was turned on.
4	I_rxe_pta	-	IRQ due to end of receive, the device is handling the response	Sent in passive target mode when NFC-A anti-collision or NFC-F SENSF_RES is automatically sent (MCU action required).
3	I_wu_f	-	NFC 212/424kb/s passive target 'Active' interrupt	Sent after NFC 212/424 kb/s automatic response to SENSF_REQ was sent.
2	RFU	-	RFU	-
1	I_wu_a*	-	Passive target Active* interrupt	Sent when Active* state is reached.
0	I_wu_a	-	Passive target Active interrupt	Sent when Active state is reached.

1. After register has been read, its content is set to 0.

4.5.38 FIFO status register 1

Register space: A

Address: 1Eh

Type: R

Table 62. FIFO status register 1

Bit	Name	Default	Function	Comments
7	fifo_b7	-	Number of bytes in the FIFO (LSB)	Valid range is from 0 to 512.
6	fifo_b6	-		
5	fifo_b5	-		
4	fifo_b4	-		
3	fifo_b3	-		
2	fifo_b2	-		
1	fifo_b1	-		
0	fifo_b0	-		

4.5.39 FIFO status register 2

Register space: A

Address: 1Fh

Type: R

Table 63. FIFO status register 2

Bit	Name	Default	Function	Comments
7	fifo_b9	-	Number of bytes in the FIFO (MSB)	-
6	fifo_b8	-		-
5	fifo_unf	-	1: FIFO underflow	-
4	fifo_ovr	-	1: FIFO overflow	-
3	fifo_lb2	-	Number of bits in the last FIFO byte if it was not complete	The received bits are stored in the LSB part of the last byte in the FIFO. If l_err1 is set then fifo_lb<2:0> dos not contain valid data.
2	fifo_lb1	-		
1	fifo_lb0	-		
0	np_lb	-	1: Parity bit is missing in the last byte	The bit is set if the last received byte is complete with 8 data bits but the parity bit is missing. If l_err1 is set then np_lb does not contain valid data.

4.5.40 Collision display register

Register space: A

Address: 20h

Type: R

Table 64. Collision display register

Bit	Name	Default	Function	Comments
7	c_byte3	-	Number of full bytes before the bit collision happened.	The *Collision display register* range covers ISO14443A anticollision command. If collision (or framing error interpreted as collision) happens in a longer message, the *Collision display register* is not set. If I_err1 is set then c_byte<3:0> and c_bit<2:0> do not contain valid data.
6	c_byte2	-		
5	c_byte1	-		
4	c_byte0	-		
3	c_bit2	-	Number of bits before the collision in the byte where the collision happened	
2	c_bit1	-		
1	c_bit0	-		
0	c_pb	-	1: Collision in parity bit 0: no collision	This error is reported if the first detected collision is in a parity bit. If I_err1 is set then c_pb dos not contain valid data.

4.5.41 Passive target display register

Register space: A

Address: 21h

Type: R

Table 65. Passive target display register

Bit	Name	Default	Function	Comments
7	RFU	-	-	-
6	RFU	-	-	-
5	RFU	-	-	-
4	RFU	-	-	-
3	pta_state3	-	0000: POWER OFF 0001: IDLE 0010: READY_L1 0011: READY_L2 0100: RFU 0101:ACTIVE 0110: RFU 1001: HALT 1010: READY_L1* 1011: READY_L2* 1100: RFU 1101: ACTIVE*	ISO-A passive target states. In ACTIVE or ACTIVE* state, the MCU must handle all commands, including SENSE/IDLE and SLEEP/HALT.
2	pta_state2	-		
1	pta_state1	-		
0	pta_state0	-		

4.5.42 Number of transmitted bytes register 1

Register space: A

Address: 22h

Type: RW

Table 66. Number of transmitted bytes register 1

Bit	Name	Default	Function	Comments
7	ntx12	0	Number of full bytes to be transmitted, MSB bits first.	Maximum supported number of bytes is 8191.
6	ntx11	0		
5	ntx10	0		
4	ntx9	0		
3	ntx8	0		
2	ntx7	0		
1	ntx6	0		
0	ntx5	0		

4.5.43 Number of transmitted bytes register 2

Register space: A

Address: 23h

Type: RW

Table 67. Number of transmitted bytes register 2(1) (2)

Bit	Name	Default	Function	Comments
7	ntx4	0	Number of full bytes to be transmitted, MSB bits first.	Maximum supported number of bytes is 8191.
6	ntx3	0		
5	ntx2	0		
4	ntx1	0		
3	ntx0	0		
2	nbtx2	0	Number of bits to transmit after the last full byte. Set to 000 to transmit only full bytes.	Bit transmission starts from LSB. Applicable for ISO14443A: – bit oriented anticollision frame when last byte is a split byte – Tx is done without parity bit generation
1	nbtx1	0		
0	nbtx0	0		

1. If anctl bit is set while card is in idle state and nbtx is not 000, then i_par will be triggered during REQA and WUPA direct command is issued.

2. Transmission of short or incomplete messages only works for ISO-A/B using the command Transmit without CRC.

4.5.44 Bit rate detection display register

Register space: A

Address: 24h

Type: R

Table 68. Bit rate detection display register

Bit	Name	Default	Function	Comments
7	RFU	-	-	-
6	RFU	-	-	-
5	nfc_rate1	-	Refer to *Table 22*	Result of automatic bit rate detection in the bit rate detection target mode.
4	nfc_rate0	-		
3	ppt2_on	-	1: PP_{ON2} timer is running	State of internal timers.
2	gpt_on	-	1: General purpose timer is running	
1	nrt_on	-	1: No-response timer is running	
0	mrt_on	-	1: Mask receive timer is running	

4.5.45 A/D converter output register

Register space: A

Address: 25h

Type: R

Table 69. A/D converter output register

Bit	Name	Default	Function	Comments
7	ad7	-	Displays the result of the last A/D conversion.	-
6	ad6	-		
5	ad5	-		
4	ad4	-		
3	ad3	-		
2	ad2	-		
1	ad1	-		
0	ad0	-		

4.5.46 Reserved register

Register space: A

Address: 26h

Type: R

Table 70. Reserved register

Bit	Name	Default	Function	Comments
7	RFU	0	-	-
6	RFU	0	-	-
5	RFU	0	-	-
4	RFU	0	-	-
3	RFU	0	-	-
2	RFU	0	-	-
1	RFU	0	-	-
0	RFU	0	-	-

4.5.47 Reserved register

Register space: A

Address: 27h

Type: R

Table 71. Reserved register

Bit	Name	Default	Function	Comments
7	RFU	0	-	-
6	RFU	0	-	-
5	RFU	0	-	-
4	RFU	0	-	-
3	RFU	0	-	-
2	RFU	0	-	-
1	RFU	0	-	-
0	RFU	0	-	-

4.5.48 TX driver register

Register space: A

Address: 28h

Type: RW

Table 72. TX driver register

Bit	Name	Default	Function	Comments
7	am_mod3	0	AM modulation index (see *Table 73*)	-
6	am_mod2	1		
5	am_mod1	1		
4	am_mod0	1		
3	d_res3	0	RFO driver resistance (see *Table 74*)	-
2	d_res2	0		
1	d_res1	0		
0	d_res0	0		

Table 73. AM modulation index

am_mod<3:0>	Modulation (%)
0	5
1	6
2	7
3	8
4	9
5	10
6	11
7	12
8	13
9	14
10	15
11	17
12	19
13	22
14	26
15	40

Table 74. RFO driver resistance

d_res<3:0>	Driver output resistance (normalized)(1)
2	1
3-4	2
5-14	4
15	High Z

1. The value has to be multiplied by the RFO resistance from *Section 5.4: Electrical characteristics* to obtain the driver output resistance for the corresponding d_res setting.

4.5.49 Auxiliary modulation setting register

Register space: B

Address: 28h

Type: RW

Table 75. Auxiliary modulation setting register

Bit	Name	Default	Function	Comments
7	dis_reg_am	0	0: Regulator AM enabled 1: Regulator AM disabled	Uses am_mod<3:0> to set the modulation index for regulator based AM modulation. Logic of this bit is inverted. Set to 0 to enable regulator AM.
6	lm_ext_pol	0	0: Normal polarity 1: Inverse polarity	Normal polarity: LM_EXT pin load modulation signal is active high. Inverse polarity: LM_EXT pin load modulation signal is active low.
5	lm_ext	0	0: External load modulation disabled 1: External load modulation enabled	Enables output of load modulation signal on LM_EXT pin.
4	lm_dri	1	0: Driver load modulation disabled 1: Driver load modulation enabled	Uses *Passive target modulation register* to set driver load modulation resistance.
3	res_am	0	0: Resistive AM modulation disabled 1: Resistive AM modulation enabled	Uses md_res<6:0> to configure resistive AM modulated driver resistance.
2	RFU	0	-	-
1	RFU	0	-	-
0	RFU	0	-	-

4.5.50 Passive target modulation register

Register space: A

Address: 29h

Type: RW

Table 76. Passive target modulation register

Bit	Name	Default	Function	Comments
7	ptm_res3	0	Refer to *Table 77*	RFO resistance during passive load modulation, modulated state. ptm_res<3:0> must be set before the *Mode definition register* is set to passive target mode.
6	ptm_res2	1		
5	ptm_res1	1		
4	ptm_res0	1		
3	pt_res3	0		RFO resistance during passive load modulation, unmodulated state. pt_res<3:0> must be set before the *Mode definition register* is set to passive target mode.
2	pt_res2	0		
1	pt_res1	0		
0	pt_res0	0		

Table 77. Passive target modulated and unmodulated state driver output resistance

ptm_res<3:0> pt_res<3:0>	Driver output resistance R_{RFO} (normalized)(1)
0	0.25
1	0.50
2	1.00
3	2.00
4	3.05
5	4.00
6	6.40
7	8.00
8	9.15
9	10.68
10	12.80
11	16.00
12	21.33
13	32.00
14	64.00
15	High Z

1. The value has to be multiplied by the RFO resistance from *Section 5.4: Electrical characteristics* to obtain the driver output resistance for the corresponding ptm/pt_res setting.

4.5.51 TX driver timing register

Register space: B

Address: 29h

Type: RW

Table 78. TX driver timing register

Bit	Name	Default	Function	Comments
7	d_rat_t3	0	Driver transient ratio target (in number of non-overlap times in one RF period)	The value presents the target ratio between one RF period and whole non-overlap time (both sides L to H and H to L). The system starts with the slowest available transient and measures the ratio. If this is lower than targeted the system switches to faster transient. The procedure is repeated until the target ratio is reached (or exceeded for the first time). There are five steps available, procedure can take up to ten RF periods.
6	d_rat_t2	1		
5	d_rat_t1	1		
4	d_rat_t0	1		
3	d_tim_man	1	0: Use automatically acquired timing setting 1: Use manual timing setting	-
2	d_tim_m2	1	000: Slow 001: Medium slow 010: Nominal 011: Medium fast 1xx: Fast	Manual driver timing, used if d_tim_man is set to 1.
1	d_tim_m1	0		
0	d_tim_m0	0		

4.5.52 External field detector activation threshold register

Register space: A

Address: 2Ah

Type: RW

Table 79. External field detector activation threshold register[(1)]

Bit	Name	Default	Function	Comments
7	RFU	0	Not used	-
6	trg_l2	0	Peer detection threshold. Refer to *Table 83*.	-
5	trg_l1	1		
4	trg_l0	1		
3	rfe_t3	0	Collision avoidance threshold. Refer to *Table 84*.	-
2	rfe_t2	0		
1	rfe_t1	1		
0	rfe_t0	1		

1. The value of rfe_3 (see *Table 84*) must be the same for the activation and deactivation thresholds.

4.5.53 Resistive AM modulation register

Register space: B

Address: 2Ah

Type: RW

Table 80. Resistive AM modulation register

Bit	Name	Default	Function	Comments
7	fa3_f	0	0: Use normal non-overlap 1: Use minimum non-overlap	-
6	md_res6	0	Refer to *Table 81*.	Resistive AM modulated state driver output resistance.
5	md_res5	0		
4	md_res4	0		
3	md_res3	0		
2	md_res2	0		
1	md_res1	0		
0	md_res0	0		

Table 81. Resistive AM modulated state driver output resistance

md_res<6:0>	Driver output resistance R_{RFO} (normalized)(1)	md_res<6:0>	Driver output resistance R_{RFO} (normalized)(1)
64	1.02	96	2.06
65	1.03	97	2.13
66	1.05	98	2.21
67	1.07	99	2.29
68	1.08	100	2.37
69	1.10	101	2.46
70	1.12	102	2.56
71	1.14	103	2.67
72	1.16	104	2.78
73	1.19	105	2.91
74	1.21	106	3.05
75	1.23	107	3.20
76	1.26	108	3.37
77	1.28	109	3.56
78	1.31	110	3.76
79	1.33	111	4.00
80	1.36	112	4.27
81	1.39	113	4.57

Table 81. Resistive AM modulated state driver output resistance (continued)

md_res<6:0>	Driver output resistance R_{RFO} (normalized)(1)	md_res<6:0>	Driver output resistance R_{RFO} (normalized)(1)
82	1.42	114	4.92
83	1.45	115	5.33
84	1.49	116	5.82
85	1.52	117	6.40
86	1.56	118	7.11
87	1.60	119	8.00
88	1.64	120	9.14
89	1.68	121	10.67
90	1.73	122	12.80
91	1.78	123	16.00
92	1.83	124	21.33
93	1.88	125	32.00
94	1.94	126	64.00
95	2.00	127	HighZ

1. The value has to be multiplied by the RFO resistance from *Section 5.4: Electrical characteristics* to obtain the driver output resistance for the corresponding md_res setting.

4.5.54 External field detector deactivation threshold register

Register space: A

Address: 2Bh

Type: RW

Table 82. External field detector deactivation threshold register(1)

<table>
<tr><th>Bit</th><th>Name</th><th>Default</th><th>Function</th><th>Comments</th></tr>
<tr><td>7</td><td>RFU</td><td>0</td><td>Not used</td><td>-</td></tr>
<tr><td>6</td><td>trg_ld2</td><td>0</td><td rowspan="3">Deactivation peer detection threshold (see Table 83).</td><td rowspan="3">-</td></tr>
<tr><td>5</td><td>trg_ld1</td><td>1</td></tr>
<tr><td>4</td><td>trg_ld0</td><td>1</td></tr>
<tr><td>3</td><td>rfe_td3</td><td>0</td><td rowspan="4">Deactivation collision avoidance threshold (see Table 84).</td><td rowspan="4">-</td></tr>
<tr><td>2</td><td>rfe_td2</td><td>0</td></tr>
<tr><td>1</td><td>rfe_td1</td><td>1</td></tr>
<tr><td>0</td><td>rfe_td0</td><td>1</td></tr>
</table>

1. The value of rfe_3 (see *Table 84*) must be the same for the activation and deactivation thresholds.

Table 83. Peer detection threshold as seen on RFI1 input

trg_l2	trg_l1	trg_l0	Peer detection threshold voltage (mV_{pp}) on RFI1
0	0	0	75
0	0	1	105
0	1	0	150
0	1	1	205
1	0	0	290
1	0	1	400
1	1	0	560
1	1	1	800

Table 84. Collision avoidance threshold as seen on RFI1 input

rfe_3	rfe_2	rfe_1	rfe_0	Collision avoidance threshold voltage (mV_{pp}) on RFI1
0	0	0	0	75
0	0	0	1	105
0	0	1	0	150
0	0	1	1	205
0	1	0	0	290
0	1	0	1	400
0	1	1	0	560
0	1	1	1	800
1	0	0	0	25
1	0	0	1	33
1	0	1	0	47
1	0	1	1	64
1	1	0	0	90
1	1	0	1	125
1	1	1	0	175
1	1	1	1	250

4.5.55 TX driver timing display register

Register space: B

Address: 2Bh

Type: R

Table 85. TX driver timing display register

Bit	Name	Default	Function	Comments
7	d_rat_r3	-	Driver Transient ratio readout (in number of non-overlap times in one RF period)	Driver transient ratio readout
6	d_rat_r2	-		
5	d_rat_r1	-		
4	d_rat_r0	-		
3	RFU	-	-	-
2	d_tim_r2	-	000: Slow 001: Medium slow 010: Nominal 011: Medium fast 1xx: Fast	Driver timing readout
1	d_tim_1	-		
0	d_tim_0	-		

4.5.56 Regulator voltage control register

Register space: A

Address: 2Ch

Type: RW

Table 86. Regulator voltage control register

Bit	Name	Default	Function	Comments
7	reg_s	0	0: Regulated voltages are defined by result of Adjust Regulators command 1: Regulated voltages are defined by rege_x bits written in this register	Defines mode of regulator voltage setting.
6	rege_3	0	External definition of regulated voltage (see *Table 88*). In 5 V mode V_{DD_D} and V_{DD_A} regulators are set to 3.4 V	In 5 V mode V_{DD_D} and V_{DD_A} regulators are set to 3.4 V. In 3.3 V mode V_{DD_D} and V_{DD_A} regulators are set to the same value as V_{DD_RF}.
5	rege_2	0		
4	rege_1	0		
3	rege_0	0		
2	mpsv2	0	000: V_{DD} 001: V_{DD_A} 010: V_{DD_D} 011: V_{DD_RF} 100: V_{DD_AM} 101: RFU 110: RFU 111: RFU	Defines source of direct command *Measure power supply*.
1	mpsv1	0		
0	mpsv0	0		

4.5.57 Regulator display register

Register space: B

Address: 2Ch

Type: R

Table 87. Regulator display register

Bit	Name	Default	Function	Comments
7	reg_3	-	Voltage regulator setting after *Adjust regulators* command. Refer to *Table 88* for definition.	-
6	reg_2	-		
5	reg_1	-		
4	reg_0	-		
3	RFU	-	-	-
2	RFU	-	-	-
1	RFU	-	-	-
1	RFU	-	-	-

Table 88. Regulated voltages

reg_3	reg_2	reg_1	reg_0	Typical regulated voltage (V)	
rege_3	rege_2	rege_1	rege_0	5 V mode	3.3 V mode
1	1	1	1	5.1	3.4
1	1	1	0	5.0	3.3
1	1	0	1	4.9	3.2
1	1	0	0	4.8	3.1
1	0	1	1	4.7	3.0
1	0	1	0	4.6	2.9
1	0	0	1	4.5	2.8
1	0	0	0	4.4	2.7
0	1	1	1	4.3	2.6
0	1	1	0	4.2	2.5
0	1	0	1	4.1	2.4
0	1	0	0	4.0	-
0	0	1	1	3.9	-
0	0	1	0	3.8	-
0	0	0	1	3.7	-
0	0	0	0	3.6	-

4.5.58 RSSI display register

Register space: A

Address: 2Dh

Type: R

Table 89. RSSI display register

Bit	Name	Default	Function	Comments
7	rssi_am_3	-	AM channel RSSI peak value. Refer to *Table 90* for definition.	Stores the AM channel RSSI peak value until the start of the next reception, or until the *Clear RSSI* command is sent.
6	rssi_am_2	-		
5	rssi_am_1	-		
4	rssi_am_0	-		
3	rssi_pm_3	-	PM channel RSSI peak value. Refer to *Table 90* for definition.	Stores the PM channel RSSI peak value until the start of the next reception, or until the *Clear RSSI* command is sent.
2	rssi_pm_2	-		
1	rssi_pm_1	-		
0	rssi_pm_0	-		

Table 90. RSSI

rssi_3	rssi_2	rssi_1	rssi_0	Typical signal on RFI1 (mV_{rms})
0	0	0	0	≤20
0	0	0	1	>20
0	0	1	0	>27
0	0	1	1	>37
0	1	0	0	>52
0	1	0	1	>72
0	1	1	0	>99
0	1	1	1	>136
1	0	0	0	>190
1	0	0	1	>262
1	0	1	0	>357
1	0	1	1	>500
1	1	0	0	>686
1	1	0	1	>950
1	1	1	0	>1150
1	1	1	1	

4.5.59 Gain reduction state register

Register space: A

Address: 2Eh

Type: R

Table 91. Gain reduction state register

Bit	Name	Default	Function	Comments
7	gs_am_3	-	Refer to rg2_am<3:0> for value explanation.	Overall AM channel second and third stage gain reduction (includes register gain reduction, squelch and AGC).
6	gs_am_2	-		
5	gs_am_1	-		
4	gs_am_0	-		
3	gs_pm_3	-	Refer to rg2_pm<3:0> for value explanation.	Overall PM channel second and third stage gain reduction (includes register gain reduction, squelch and AGC).
2	gs_pm_2	-		
1	gs_pm_1	-		
0	gs_pm_0	-		

4.5.60 Auxiliary display register

Register space: A

Address: 31h

Type: R

Table 92. Auxiliary display register

Bit	Name	Default	Function	Comments
7	a_cha	-	0: AM 1: PM	Receiver channel used in ongoing/last reception.
6	efd_o	-	1: External field detected	External field detector output.
5	tx_on	-	1: Transmission is active	Data transmission due to automatic handling of CE mode collision avoidance are not indicated.
4	osc_ok	-	1: Xtal oscillation is stable	Indication that Xtal oscillator is active and its output is stable.
3	rx_on	-	1: Receive decoder is enabled	-
2	rx_act	-	1: Receive decoder is receiving a message	-
1	en_peer	-	1: External field detector is active in Peer detection mode	-
0	en_ac	-	1: External field detector is active in RF collision avoidance mode	-

4.5.61 Overshoot protection configuration register 1

Register space: B

Address: 30h

Type: RW

Table 93. Overshoot protection configuration register 1

Bit	Name	Default	Function	Comments
7	ov_tx_mode1	0	00: Drive with V_{DD_DR} 01: Drive with V_{DD_AM} 10: Driver stop (at GND / V_{DD_DR}) 11: RFU	Selects RF drive level to apply when ov_patternX is set to 1.
6	ov_tx_mode0	0		
5	ov_pattern13	0	-	-
4	ov_pattern12	0	-	-
3	ov_pattern11	0	-	-
2	ov_pattern10	0	-	-
1	ov_pattern9	0	-	-
0	ov_pattern8	0	-	-

4.5.62 Overshoot protection configuration register 2

Register space: B

Address: 31h

Type: RW

Table 94. Overshoot protection configuration register 2

Bit	Name	Default	Function	Comments
7	ov_pattern7	0	-	-
6	ov_pattern6	0	-	-
5	ov_pattern5	0	-	-
4	ov_pattern4	0	-	-
3	ov_pattern3	0	-	-
2	ov_pattern2	0	-	-
1	ov_pattern1	0	-	-
0	ov_pattern0	0	-	-

4.5.63 Undershoot protection configuration register 1

Register space: B

Address: 32h

Type: RW

Table 95. Undershoot protection configuration register 1

Bit	Name	Default	Function	Comments
7	un_tx_mode1	0	00: Drive with V_{DD_DR} 01: Drive with V_{DD_AM} 10: Driver stop (at GND / V_{DD_DR}) 11: RFU	Selects RF drive level to apply when un_patternX is set to 1.
6	un_tx_mode0	0		
5	un_pattern13	0	-	-
4	un_pattern12	0	-	-
3	un_pattern11	0	-	-
2	un_pattern10	0	-	-
1	un_pattern9	0	-	-
0	un_pattern8	0	-	-

4.5.64 Undershoot protection configuration register 2

Register space: B

Address: 33h

Type: RW

Table 96. Undershoot protection configuration register 2

Bit	Name	Default	Function	Comments
7	un_pattern7	0	-	-
6	un_pattern6	0	-	-
5	un_pattern5	0	-	-
4	un_pattern4	0	-	-
3	un_pattern3	0	-	-
2	un_pattern2	0	-	-
1	un_pattern1	0	-	-
0	un_pattern0	0	-	-

4.5.65 Wake-up timer control register

Register space: A

Address: 32h

Type: RW

Table 97. Wake-up timer control register

Bit	Name	Default	Function	Comments
7	wur	0	0: 100 ms 1: 10 ms	Wake-up timer range
6	wut2	0	Refer to *Table 98*	Wake-up timer timeout value
5	wut1	0		
4	wut0	0		
3	wto	0	1: IRQ at every timeout	-
2	wam	0	1: At timeout perform amplitude measurement	Generates I_wam interrupt if amplitude difference is larger than Δam.
1	wph	0	1: At timeout perform phase measurement	Generates I_wph interrupt if phase difference is larger than Δpm.
0	wcap	0	1: At timeout perform capacitance measurement	Generates I_wcap interrupt if capacitance difference is larger than Δcm.

Table 98. Typical wake-up time

wut2	wut1	wut0	100 ms range (wur = 0)	10 ms range (wur = 1)
0	0	0	100 ms	10 ms
0	0	1	200 ms	20 ms
0	1	0	300 ms	30 ms
0	1	1	400 ms	40 ms
1	0	0	500 ms	50 ms
1	0	1	600 ms	60 ms
1	1	0	700 ms	70 ms
1	1	1	800 ms	80 ms

4.5.66 Amplitude measurement configuration register

Register space: A

Address: 33h

Type: RW

Table 99. Amplitude measurement configuration register

Bit	Name	Default	Function	Comments
7	am_d3	0	Definition of Δam (difference vs. reference that triggers interrupt)	-
6	am_d2	0		
5	am_d1	0		
4	am_d0	0		
3	am_aam	0	0: Exclude the IRQ measurement 1: Include the IRQ measurement	Includes/excludes the measurement that causes IRQ (having difference > Δam to reference) in auto-averaging.
2	am_aew1	0	00: 4 01: 8 10: 16 11: 32	Weight of last measurement result for auto-averaging.
1	am_aew2	0		
0	am_ae	0	0: Use *Amplitude measurement reference register*	Selects reference value for amplitude measurement Wake-up mode.

4.5.67 Amplitude measurement reference register

Register space: A

Address: 34h

Type: RW

Table 100. Amplitude measurement reference register

Bit	Name	Default	Function	Comments
7	am_ref7	0	-	-
6	am_ref6	0	-	-
5	am_ref5	0	-	-
4	am_ref4	0	-	-
3	am_ref3	0	-	-
2	am_ref2	0	-	-
1	am_ref1	0	-	-
0	am_ref0	0	-	-

4.5.68 Amplitude measurement auto-averaging display register

Register space: A

Address: 35h

Type: R

Table 101. Amplitude measurement auto-averaging display register

Bit	Name	Default	Function	Comments
7	amd_aad7	0	-	-
6	amd_aad6	0	-	-
5	amd_aad5	0	-	-
4	amd_aad4	0	-	-
3	amd_aad3	0	-	-
2	amd_aad2	0	-	-
1	amd_aad1	0	-	-
0	amd_aad0	0	-	-

4.5.69 Amplitude measurement display register

Register space: A

Address: 36h

Type: R

Table 102. Amplitude measurement display register

Bit	Name	Default	Function	Comments
7	am_amd7	0	-	-
6	am_amd6	0	-	-
5	am_amd5	0	-	-
4	am_amd4	0	-	-
3	am_amd3	0	-	-
2	am_amd2	0	-	-
1	am_amd1	0	-	-
0	am_amd0	0	-	-

4.5.70 Phase measurement configuration register

Register space: A

Address: 37h

Type: RW

Table 103. Phase measurement configuration register

Bit	Name	Default	Function	Comments
7	pm_d3	0	Definition of Δpm (difference to reference that triggers interrupt)	-
6	pm_d2	0		
5	pm_d1	0		
4	pm_d0	0		
3	pm_aam	0	0: Exclude the IRQ measurement 1: Include the IRQ measurement	Includes/excludes the measurement value that triggered the I_wph interrupt in the auto-averaging.
2	pm_aew1	0	00: 4 01: 8 10: 16 11: 32	Weight of last measurement result for auto-averaging.
1	pm_aew0	0		
0	pm_ae	0	0: Use *Phase measurement reference register* 1: Use phase measurement auto-averaging as reference	Selects reference value for phase measurement Wake-up mode.

4.5.71 Phase measurement reference register

Register space: A

Address: 38h

Type: RW

Table 104. Phase measurement reference register

Bit	Name	Default	Function	Comments
7	pm_ref7	0	-	-
6	pm_ref6	0	-	-
5	pm_ref5	0	-	-
4	pm_ref4	0	-	-
3	pm_ref3	0	-	-
2	pm_ref2	0	-	-
1	pm_ref1	0	-	-
0	pm_ref0	0	-	-

4.5.72 Phase measurement auto-averaging display register

Register space: A

Address: 39h

Type: R

Table 105. Phase measurement auto-averaging display register

Bit	Name	Default	Function	Comments
7	pm_aad7	0	-	-
6	pm_aad6	0	-	-
5	pm_aad5	0	-	-
4	pm_aad4	0	-	-
3	pm_aad3	0	-	-
2	pm_aad2	0	-	-
1	pm_aad1	0	-	-
0	pm_aad0	0	-	-

4.5.73 Phase measurement display register

Register space: A

Address: 3Ah

Type: R

Table 106. Phase measurement display register

Bit	Name	Default	Function	Comments
7	pm_amd7	0	0	-
6	pm_amd6	0	0	-
5	pm_amd5	0	0	-
4	pm_amd4	0	0	-
3	pm_amd3	0	0	-
2	pm_amd2	0	0	-
1	pm_amd1	0	0	-
0	pm_amd0	0	0	-

4.5.74 IC identity register

Register space: A

Address: 3Fh

Type: R

Table 107. IC identity register

Bit	Name	Default	Function	Comments
7	ic_type4	0	IC type code 00101: ST25R3918	5-bit IC type code
6	ic_type3	0		
5	ic_type2	1		
4	ic_type1	0		
3	ic_type0	1		
2	ic_rev2	0	IC revision code 010: rev 3.1	3-bit IC revision code
1	ic_rev1	1		
0	ic_rev0	0		

5 Electrical characteristics

5.1 Absolute maximum ratings

Any stress beyond the limits listed in *Table 108* can cause permanent damage to the device. These are stress ratings only.

Functional operation of the device at these or any other conditions beyond those indicated in *Table 108* is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

Table 108. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}, V_{DD_TX} (1)	Positive supply voltage	-0.3	6.0	V
V_{DD}, V_{DD_TX} (1)(2)	Positive supply voltage when option bit sup3V is set	-0.3	5	
$\Delta_{VDD\text{-}VDD\_TX}$ (1)	Difference between V_{DD} and V_{DD_TX}	-0.3	0.3	
V_{DD_IO} (1)	Peripheral communication supply voltage	-0.3	6	
V_{GND} (1)	Negative supply voltage	-0.3	0.3	
V_{pIO} (1)	Voltage for peripheral IO communication pins (27 to 32)	-0.3	6	
V_{p5V} (1)	Voltage for other pins (9, 11, 13, 14, 15, and 17) in the 5 V domain	-0.3	6	
V_{p3V} (1)	Voltage for other pins (2 to 5, 7, 18, 19, 20 and 22 to 25) in the 3 V domain	-0.3	5	
I_{scr}	Input current (latch-up immunity) according to JESD78	-100	100	mA
I_{VDD_LDO}	Maximum driver current using internal voltage regulator	-	85 (3)	mA
I_{VDD_EXT} (4)	Peak current supplied from an external source, internal voltage regulator bypassed		125 (5)	
ESD voltage	Electrostatic discharge voltage according to JS-001, human body model	-	2000	V
T_{strg}	Storage temperature	-65	150	°C
T_{body}	Package body temperature according to IPC/JEDEC J-STD-020 (6)	-	260	
T_{Jun}	Junction temperature	-40	125	
-	Humidity non-condensing	5	85	%

1. Referenced to V_{SS}.
2. Bit sup3V set to 1 in *IO configuration register 2*.
3. Provide good thermal management to ensure that junction temperature remains below the specified value.
4. VDD_RF is connected to VDD_TX to bypass the internal voltage regulator.
5. Peak current with RF driver externally supplied. Provide good thermal management to ensure that junction temperature remains below the specified value.
6. Reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices".

5.2 Operating conditions

All defined tolerances for external components in this specification need to be ensured over the whole operation conditions range and also over lifetime.

Table 109. Operating conditions

Symbol	Parameter	Min	Max	Unit
V_{DD}, V_{DD_TX}[1] [2]	Positive supply voltage (pins 8 and 10), T_{amb} = -40 to 105 °C, rege <3:0> ≥ 07h	2.6	5.5	V
	Positive supply voltage (pins 8 and 10), T_{amb} = -20 to 105 °C	2.4	5.5	
	Positive supply voltage when option bit sup3V is set[3], T_{amb} = -40 to 105 °C, rege <3:0> ≥ 07h	2.6	3.6	
	Positive supply voltage when option bit sup3V is set[3], T_{amb} = -20 to 105 °C	2.4	3.6	
V_{DD_DR}[1]	Driver positive supply voltage when driver is directly supplied (pin 14) Mandatory condition: $V_{DD\_DR} \leq V_{DD}$, V_{DD_TX}	2.4	5.5	V
$\Delta_{VDD\text{-}VDD\_TX}$[1]	Difference between V_{DD} and V_{DD_TX}	-0.2	0.2	
V_{DD_IO}[1]	Peripheral communication supply voltage (pin 1)	1.65	5.5	
V_{GND}[1]	Negative supply voltage (pins 6, 12, 16 and 26)	0	0	
V_{pIO}[1]	Voltage for peripheral IO communication pins (27 to 32)	0	5.5	
V_{p5V}[1]	Voltage for other pins (9, 11, 13, 14, 15 and 17) in the 5 V domain	0	5.5	
V_{p3V}[1]	Voltage for other pins (5, 7, 18 to 20 and 22 to 24) in the 3 V domain	0	3.6	
$T_{(amb,\ VFQFPN32)}$[4]	Ambient temperature range for VFQFPN32 package	-40	105	°C
V_{RFI_A}	RFI input amplitude[5]	0.15	3	V_{PP}

1. Referenced to V_{SS}.
2. If power supply is lower than 2.6 V, PSSR cannot be improved using internal regulators (minimum regulated voltage is 2.4 V).
3. Bit sup3V set to 1 in *IO configuration register 2*.
4. The device must be mounted on a PCB with sufficient heat dissipation.
5. The minimum RFI input signal definition is meant for NFC active P2P reception and NFC passive target reception. In HF reader mode and NFC transmit mode the recommended signal level is 2.5 V_{PP}.

5.3 DC/AC characteristics for digital inputs and outputs

Table 110. Characteristics of CMOS I/Os(1)

Type	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Inputs(2)	V_{IH}	High level input voltage	-	0.8 * V_{DD_IO}	-	-	V
	V_{IL}	Low level input voltage	-	-	-	0.2 * V_{DD_IO}	V
	I_{LEAK}	Input leakage current	V_{DD_IO} = 5.5 V	-1	-	1	µA
Output	V_{OH}	High level output voltage	I_{source} = 1 mA V_{DD_IO} = 3.3 to5.5 V, io_drv_lvl=0	0.9 * V_{DD_IO}	-	-	V
			I_{source} = 0.5 mA V_{DD_IO} < 3.3 V io_drv_lvl = 1		-	-	
	V_{OL}	Low level output voltage	I_{source} = 1 mA V_{DD_IO} = 3.3 to V, io_drv_lvl=0	-	-	0.1 * V_{DD_IO}	
			I_{source} = 0.5 mA V_{DD_IO} < 3.3 V io_drv_lvl = 1	-	-	0.1 * V_{DD_IO}	
	C_L	Capacitive load	-	-	-	50	pF
	R_O	Output resistance	V_{DD_IO} = 3.3 V	-	250	500	Ω
	R_{PD}	Pull-down resistance pin MISO(3)	V_{DD_IO} = 3.3 V	-	10	13	kΩ

1. Minimum and maximum values tested in production at 25 °C, other values characterized only.
2. Pins BSS, MOSI and SCLK.
3. Use bits miso_pd1 and miso_pd2 in the *IO configuration register 2* to control the optional pull down on the MISO pin.

5.4 Electrical characteristics

Table 111. ST25R3918 electrical characteristics (V_{DD} = 3.3 V) (1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{PD}	Supply current in Power-down mode	T_{Jun} = -40 °C to 25 °C (3)	-	0.8	2.5	µA
		T_{Jun} = 85 °C (3)	-	2	20	
		T_{Jun} = 125 °C (3)	-	12	60	
I_{NFCT}	Supply current in Initial NFC target mode	T_{Jun} = -40 °C to 25 °C (4)	-	3.5	7.0	µA
		T_{Jun} = 85 °C (4)	-	5	20	
		T_{Jun} = 125 °C (4)	-	14	60	
I_{WU}	Supply current in Wake-up mode (logic and RC oscillator)	T_{Jun} = -40 °C to 25 °C (5)	-	3.0	6.3	µA
		T_{Jun} = 85 °C (5)		2.8	20	
		T_{Jun} = 125 °C (5)		15	60	
I_{RD}	Supply current in Ready mode	(6)	-	4.5	7.5	mA
I_{AL}	Supply current all active	(7)	-	16	23	
I_{AL-AM}	Supply current all active, AM	(8)	-	17	26	
I_{AL1}	Supply current all active single RX channel	(9)	-	11	16	
R_{RFO}	RFO1 and RFO2 driver output resistance	I_{RFO} = 10 mA	-	6.8	16	Ω
V_{RFI}	RFI input sensitivity	(10) (11)	-	0.5	-	mV_{rms}
R_{RFI}	RFI input resistance	-	-	12	16	kΩ
V_{POR}	Power on reset voltage	-	1.0	1.45	2.0	V
V_{AGDC}	AGDC voltage	(6) (12)	1.4	1.5	1.6	
V_{REG}	Regulated voltage	(13)	2.65	3.00	3.20	

1. 3.3 V supply mode with V_{DD} = 3.3 V, unless specified otherwise. Regulated voltages are set at 3.0 V (unless specified otherwise), 27.12 MHz Xtal connected to XTO and XTI.
2. Minimum and maximum values tested in production at 25 °C, other temperature values evaluated by characterization.
3. Registers 00h to 07h (no clock on MCU_CLK), 01h to 80h (3 V supply mode), other registers in default state.
4. Registers 00h to 07h (no clock on MCU_CLK), 01h to 80h (3 V supply mode), 02h to 03h (external field detector enable), 03h to E8h (enable NFC Target mode), other registers in default state.
5. Registers 00h to 07h (no clock on MCU_CLK), 01h to 80h (3 V supply mode), 02h to 04h (enable Wake-up mode), 32h to 08h (100 ms timeout, IRQ at every timeout), other registers in default state.
6. Registers 00h to 07h (no clock on MCU_CLK), 01h to C0h (3 V supply mode, disable VDD_D), 02h to 80h (en = 1), 2Ch to D8h (3.0 V regulator), other registers in default state, short VDD_A and VDD_D.
7. Registers 00h to 07h (no clock on MCU_CLK), 01h to C0h (3 V supply mode, disable VDD_D), 02h to C8h (enable RX, enable TX), 28h to 7Fh (RFO segments disabled), 2Ch to D8h (3.0 V regulator), other registers in default state, short VDD_A and VDD_D.
8. Registers 00h to 07h (no clock on MCU_CLK), 01h to C0h (3 V supply mode, disable VDD_D), 02h to C8h (enable RX, enable TX), 03h to 14h (AM modulation), 28h to 7Fh (RFO segments disabled), 2Ch to D8h (3.0 V regulator), other registers in default state, short VDD_A and VDD_D.
9. Registers 00h to 07h (no clock on MCU_CLK), 01h to C0h (3 V supply mode, disable VDD_D), 02h to E8h (enable RX, 1 RX channel, enable TX), 28h to 7Fh (RFO segments disabled), 2Ch to D8h (3.0 V regulator), other registers in default state, short VDD_A and VDD_D.
10. f_{SUB} = 848 kHz, AM channel with peak detector input stage selected.
11. Specified by design, not tested in production.
12. Evaluated by characterization, not tested in production.

13. Manual regulator mode, V_{DD} = 3.6 V, regulated voltage set to 3.0 V, measured on pin VDD_RF: register 00h set to 0Fh, register 01h set to 80h (3 V supply mode), register 02h set to E8h (one channel RX, enable TX), 2Ch to D8h (3.0 V regulator), other registers in default state.

Table 112. ST25R3918 electrical characteristics (V_{DD} = 5.5 V) (1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{PD}	Supply current in Power-down mode	T_{Jun} = -40 to 25 °C (3)	-	1	3	µA
		T_{Jun} = 125 °C (3)	-	-	90	
		T_{Jun} = 85 °C	-	2.5	25	
I_{NFCT}	Supply current in initial NFC target mode	T_{Jun} = -40 to 25 °C (4)	-	3.4	8	
		T_{Jun} = 125 °C (4)	-	35	90	
		T_{Jun} = 85 °C	-	5	25	
I_{WU}	Supply current in Wake-up mode (logic and RC oscillator)	T_{Jun} = -40 to 25 °C (5)	-	3	8	
		T_{Jun} = 125 °C (5)	-	15	90	
		T_{Jun} = 85 °C		5	25	
I_{RD}	Supply current in Ready mode	(6)	-	5.6	7.5	mA
I_{AL}	Supply current all active	(7)	-	15.0	23.0	
I_{AL-AM}	Supply current all active, AM	(8)	-	16.0	26.0	
I_{AL1}	Supply current all active single RX channel	(9)	-	11.0	16.0	
R_{RFO}	RFO1 and RFO2 driver output resistance	I_{RFO} = 10 mA (10)	-	6.8	16	Ω
R_{RFI}	RFI input resistance	(10) (11)	-	12	16	kΩ
V_{POR}	Power on reset voltage	-	1.00	1.45	2.00	V
V_{AGDC}	AGDC voltage	(7)	1.40	1.50	1.60	
V_{REG}	Regulated voltage	(7) (10)	4.3	4.6	5.0	

1. Minimum and maximum values tested in production at 25 °C, other temperature values evaluated by characterization.
2. 5.0 V supply mode with V_{DD} = 5.5 V unless specified otherwise. Regulated voltages set to 5.1 V (unless specified otherwise), 27.12 MHz Xtal connected to XTO and XTI.
3. Registers 00h to 07h (no clock on MCU_CLK), 01h to 00h (5 V supply mode), other registers in default state.
4. Registers 00h to 07h (no clock on MCU_CLK), 01h to 00h (5 V supply mode), 02h to 03h (external field detector enable), 03h to E8h (enable NFC Target mode), other registers in default state.
5. Registers 00h to 07h (no clock on MCU_CLK), 01h to 00h (5 V supply mode), 02h to 04h (enable Wake-up mode), 32h to 08h (100 ms timeout, IRQ at every timeout), other registers in default state.
6. Registers 00h to 07h (no clock on MCU_CLK), 01h to 40h (5 V supply mode, disable VDD_D), 02h to 80h (en = 1), 2Ch to F8h (5.1 V regulator), other registers in default state, short VDD_A and VDD_D.
7. Registers 00h to 07h (no clock on MCU_CLK), 01h to 40h (5 V supply mode, disable VDD_D), 02h to C8h (enable RX, enable TX), 28h to 7Fh (RFO segments disabled), 2Ch to F8h (5.1 V regulator), other registers in default state, short VDD_A and VDD_D.
8. Registers 00h to 07h (no clock on MCU_CLK), 01h to 40h (5 V supply mode, disable VDD_D), 02h to C8h (enable RX, enable TX), 03h to 14h (AM modulation), 28h to 7Fh (RFO segments disabled), 2Ch to F8h (5.1 V regulator), other registers in default state, short VDD_A and VDD_D.
9. Registers 00h to 07h (no clock on MCU_CLK), 01h to 40h (5 V supply mode, disable VDD_D), 02h to E8h (enable RX, 1 RX channel, enable TX), 28h to 7Fh (RFO segments disabled), 2Ch to D8h (4.7 V regulator), other registers in default state, short VDD_A and VDD_D.
10. Evaluated by characterization, not tested in production.

11. f_{SUB} = 848 kHz, AM channel with peak detector input stage selected.

Table 113. ST25R3918 electrical characteristics (V_{DD} = 2.4 V) (1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{PD}	Supply current in Power-down mode	T_{Jun} = -40 to 25 °C (3)	-	0.5	2.2	µA
		T_{Jun} = 85 °C (3)	-	1.5	15	
		T_{Jun} = 125 °C (3)		7.0	50	
I_{NFCT}	Supply current in initial NFC target mode	T_{Jun} = -40 to 25 °C (4)	-	1.5	5	
		T_{Jun} = 85 °C (4)	-	2	15	
		T_{Jun} = 125 °C (4)		8	50	
I_{WU}	Supply current in Wake-up mode (logic and RC oscillator)	T_{Jun} = -40 to 25 °C (5)	-	1.8	5	
		T_{Jun} = 85 °C (5)	-	2.7	15	
		T_{Jun} = 125 °C (5)		9	50	
I_{RD}	Supply current in Ready mode	(6)	-	3.4	7.5	mA
I_{AL}	Supply current all active	(7)	-	11	23	
I_{AL-AM}	Supply current all active, AM	(8)	-	12.5	26	
I_{AL1}	Supply current all active single RX channel	(9)	-	10	16	
R_{RFO}	RFO1 and RFO2 driver output resistance	I_{RFO} = 10 mA (10)	-	6.8	16	Ω
R_{RFI}	RFI input resistance	(10) (11)	-	12	16	kΩ
V_{POR}	Power on reset voltage	-	1.00	1.45	2.00	V
V_{AGDC}	AGDC voltage	(7)	1.40	1.50	1.60	
V_{REG}	Regulated voltage	(7) (10)	2.20	2.40	2.45	

1. Minimum and maximum values tested in production at 25 °C, other temperature values evaluated by characterization.
2. 3.3 V supply mode with V_{DD} = 2.4 V unless specified otherwise. Regulated voltages set to 2.4 V (unless specified otherwise), 27.12 MHz Xtal connected to XTO and XTI.
3. Registers 00h to 07h (no clock on MCU_CLK), 01h to 80h (3 V supply mode), other registers in default state.
4. Registers 00h to 07h (no clock on MCU_CLK), 01h to 80h (3 V supply mode), 02h to 03h (external field detector enable), 03h to E8h (enable NFC Target mode), other registers in default state.
5. Registers 00h to 07h (no clock on MCU_CLK), 01h to 80h (3 V supply mode), 02h to 04h (enable Wake-up mode), 32h to 08h (100 ms timeout, IRQ at every timeout), other registers in default state.
6. Registers 00h to 07h (no clock on MCU_CLK), 01h to C0h (3 V supply mode, disable VDD_D), 02h to 80h (en = 1), 2Ch to A8h (2.4 V regulator), other registers in default state, short VDD_A and VDD_D.
7. Registers 00h to 07h (no clock on MCU_CLK), 01h to C0h (3 V supply mode, disable VDD_D), 02h to C8h (enable RX, enable TX), 28h to 7Fh (RFO segments disabled), 2Ch to A8h (2.4 V regulator), other registers in default state, short VDD_A and VDD_D.
8. Registers 00h to 07h (no clock on MCU_CLK), 01h to C0h (3 V supply mode, disable VDD_D), 02h to C8h (enable RX, enable TX), 03h to 14h (AM modulation), 28h to 7Fh (RFO segments disabled), 2Ch to A8h (2.4 V regulator), other registers in default state, short VDD_A and VDD_D.
9. Registers 00h to 07h (no clock on MCU_CLK), 01h to C0h (3 V supply mode, disable VDD_D), 02h to E8h (enable RX, 1 RX channel, enable TX), 28h to 7Fh (RFO segments disabled), 2Ch to A8h (2.4 V regulator), other registers in default state, short VDD_A and VDD_D.
10. Evaluated by characterization, not tested in production.
11. f_{SUB} = 848 kHz, AM channel with peak detector input stage selected.

5.5 SPI interface characteristics

Table 114. SPI characteristics (5 MHz) (1)

Operation	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
General	T_{SCLK}	SCLK period	$T_{SCLK} = T_{SCLKL} + T_{SCLKH}$	-	200	-	ns
	T_{SCLKL}	SCLK low	-	95	-	-	
	T_{SCLKH}	SCLK high	-	95	-	-	
	T_{SSH}	SPI reset (BSS high)	-	100	-	-	
	T_{NCSL}	BSS falling to SCLK rising	First SCLK pulse	25	-	-	
	T_{NCSH}	SCLK falling to BSS rising	Last SCLK pulse	25	-	-	
	T_{DIS}	Data in setup time	-	10	-	-	
	T_{DIH}	Data in hold time	-	10	-	-	
Read	T_{DOD}	Data out delay	$C_{load} \leq 50$ pF, V_{DD_IO} = 1.65 to 3.0 V	-	80	95	
			$C_{load} \leq 50$ pF, V_{DD_IO} = 3.0 to 5.5 V	-	-	70	
	T_{DOHZ}	Data out to high impedance delay	$C_{load} \leq 50$ pF	-	20	-	

1. Evaluated by characterization, not tested in production.

Table 115. SPI characteristics (5 MHz < 1 / T_{SCLK} < 10 MHz) (1)

Operation	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
General	T_{SCLK}	SCLK period	$T_{SCLK} = T_{SCLKL} + T_{SCLKH}$	100	-	-	ns
	T_{SCLKL}	SCLK low	-	40	-	-	
	T_{SCLKH}	SCLK high	-	40	-	-	
	T_{SSH}	SPI reset (BSS high)	-	100	-	-	
	T_{NCSL}	BSS falling to SCLK rising	First SCLK pulse	25	-	-	
	T_{NCSH}	SCLK falling to BSS rising	Last SCLK pulse	25	-	-	
	T_{DIS}	Data in setup time	-	10	-	-	
	T_{DIH}	Data in hold time	-	10	-	-	
Read	T_{DOD}	Data out delay	$C_{load} \leq 50$ pF, V_{DD_IO} = 3.0 to 5.5 V	-	55	70	
	T_{DOHZ}	Data out to high impedance delay	$C_{load} \leq 50$ pF	-	20	-	

1. Evaluated by characterization, not tested in production.

Figure 26. SPI timing diagram - General operation

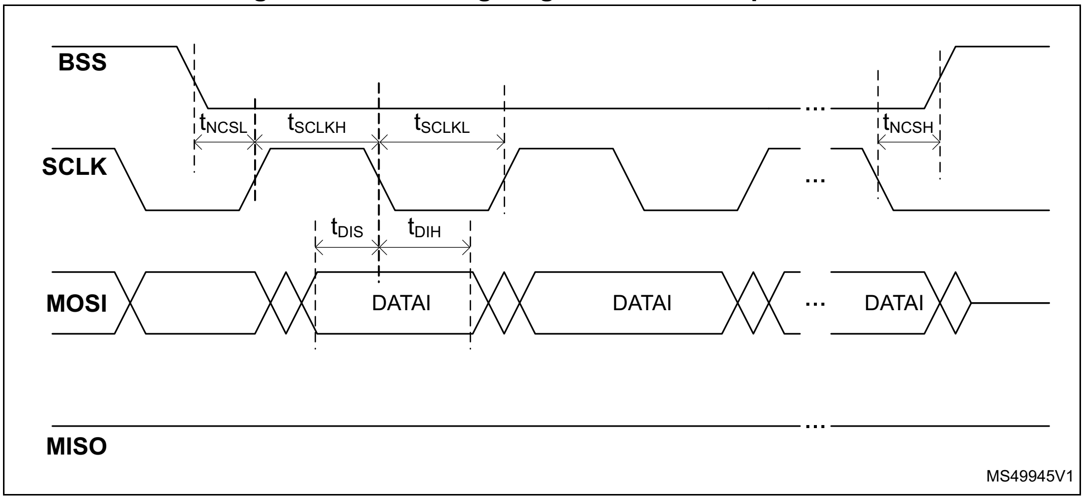
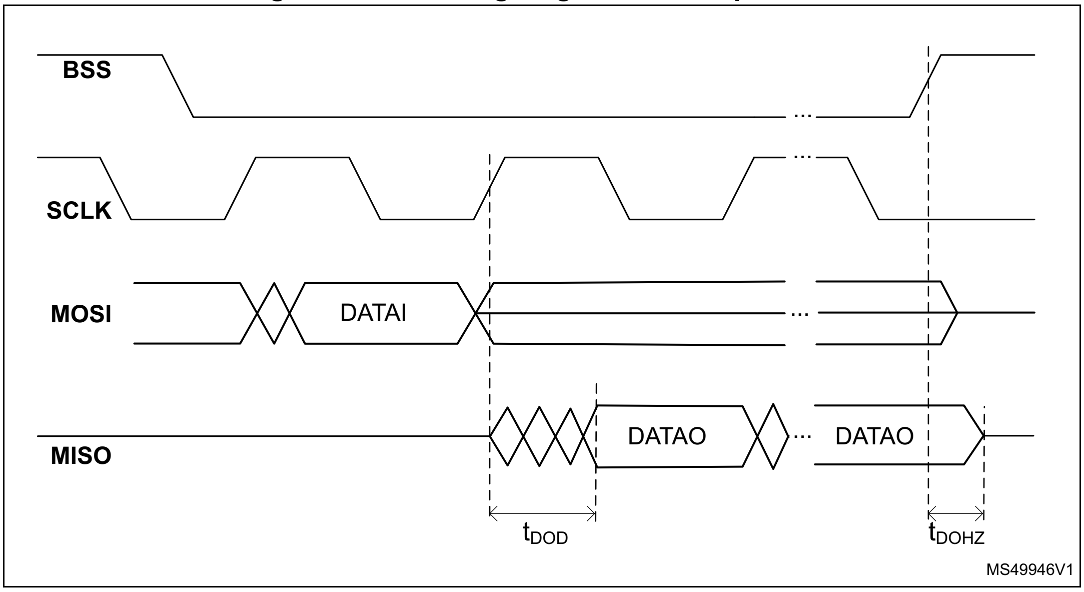


Figure 27. SPI timing diagram - Read operation



5.6 I2C interface characteristics

Transition from 100 kHz / 400 kHz / 1 MHz mode to 3.4 MHz mode (High speed mode) is done via Master code 00001XXX, as described in the I2C specification.

Table 116. AC measurement conditions

Symbol	Parameter	Min	Max	Unit
C_{BUS}	Load capacitance	100		pF
-	SCL input rise/fall time, SDA input fall time	-	50	ns

Table 117. AC measurement conditions - I2C configuration

Mode	Rate	Setting
S	100 kHz	i2c_thd = 00b, io_drv_lvl = 1b
F	400 kHz	i2c_thd = 01b, io_drvl_lvl = 1b
F+	1000 kHz	i2c_thd = 11b, Io_drv_lvl = 1b
HS	3400 kHz	i2c_thd = 11b, io_drv_lvl = 1b

Table 118. Input parameters(1)

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance (SDA)	-	-	15	pF
	Input capacitance (SCL)	-	-	15	

1. Evaluated by characterization, not tested in production.

Table 119. DC characteristics(1)

Symbol	Parameter	Conditions (in addition to those in *Table 116* and *Table 117*)	Min	Max	Unit
I_{LI}	Input leakage current (SCL, SDA)	$V_{IN} = V_{SS}$ or V_{CC}, device in Standby mode	-	± 10	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}	-	± 10	
V_{IL}	Input low voltage (SCL, SDA)	-	-0.4	0.2 V_{DD_IO}	V
V_{IH}	Input high voltage (SCL, SDA)	-	0.8 V_{DD_IO}	V_{DD_IO} + 0.4	
V_{OL}	Output low voltage	V_{DD_IO} = 1.65 V, I_{OL} = 2.5 mA	-	0.1 V_{DD_IO}	
		V_{DD_IO} = 2.4 V, I_{OL} = 3.0 mA	-	0.1 V_{DD_IO}	
		V_{DD_IO} = 3.3 V, I_{OL} = 8 mA	-	0.1 V_{DD_IO}	
		V_{DD_IO} = 5.5 V, I_{OL} = 8 mA	-	0.1 V_{DD_IO}	

1. Evaluated by characterization, not tested in production.

Table 120. 100 kHz AC characteristics[(1)]

Symbol	Alt.	Parameter	Min	Max	Unit
f_C	f_{SCL}	Clock frequency	-	100	kHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	4000	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	4700	-	
t_{QL1QL2}	t_F	SDA (out) fall time	-	300	
t_{DXCH}	$t_{SU:DAT}$	Data in set up time	250	-	
$t_{CLDX}X$	$t_{HD:DAT}$	Data in hold time	5000	-	
t_{CLQX}	t_{DH}	Data out hold time	50	-	
t_{CLQV}	t_{AA}	Clock low to next data valid (access time)	-	3450	
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	4700	-	
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	4000	-	
t_{CHDH}	$t_{SU:STO}$	Stop condition set up time	4000	-	
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	4700	-	
t_{NS}[(2)]	-	Pulse width ignored (input filter on SCL and SDA), single glitch	-	40	

1. Conditions in addition to those specified in Table 116 and Table 117.
2. Evaluated by characterization, not tested in production.

Table 121. 400 kHz AC characteristics[(1) (2)]

Symbol	Alt.	Parameter	Min	Max	Unit
f_C	f_{SCL}	Clock frequency	-	400	kHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	600	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	1300	-	
t_{QL1QL2}	t_F	SDA (out) fall time	-	300	
t_{DXCH}	$t_{SU:DAT}$	Data in set up time	100	-	
$t_{CLDX}X$	$t_{HD:DAT}$	Data in hold time	0	-	
t_{CLQX}	t_{DH}	Data out hold time	50	-	
t_{CLQV}	t_{AA}	Clock low to next data valid (access time)	-	900	
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	600	-	
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	600	-	
t_{CHDH}	$t_{SU:STO}$	Stop condition set up time	600	-	
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	1300	-	
t_{NS}	-	Pulse width ignored (input filter on SCL and SDA), single glitch	-	40	

1. Conditions in addition to those specified in Table 116 and Table 117.
2. Evaluated by characterization, not tested in production.

Table 122. 1 MHz AC characteristics(1)(2)

Symbol	Alt.	Parameter	Min	Max	Unit
f_C	f_{SCL}	Clock frequency	-	1	MHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	260	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	500	-	
t_{QL1QL2}	t_F	SDA (out) fall time	-	120	
t_{DXCH}	$t_{SU:DAT}$	Data in set up time	50	-	
$t_{CLDX}X$	$t_{HD:DAT}$	Data in hold time	0	-	
t_{CLQX}	t_{DH}	Data out hold time	50	-	
t_{CLQV}	t_{AA}	Clock low to next data valid (access time)	-	450	
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	250	-	
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	250	-	
t_{CHDH}	$t_{SU:STO}$	Stop condition set up time	250	-	
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	500	-	
t_{NS}	-	Pulse width ignored (input filter on SCL and SDA), single glitch	-	40	

1. Conditions in addition to those specified in Table 116 and Table 117.
2. Evaluated by characterization, not tested in production.

Table 123. 3.4 MHz AC characteristics(1)(2)(3)

Symbol	Alt.	Parameter	Min	Max	Unit
f_C	f_{SCL}	Clock frequency	-	3.4	MHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	80	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	160	-	
t_{QL1QL2}	t_F	SDA (out) fall time (10-100 pF)	-	41	
t_{DXCH}	$t_{SU:DAT}$	Data in set up time	25	-	
$t_{CLDX}X$	$t_{HD:DAT}$	Data in hold time	0	-	
t_{CLQX}	t_{DH}	Data out hold time	20	-	
t_{CLQV}	t_{AA}	Clock low to next data valid	-	150	
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	160	-	
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	160	-	
t_{CHDH}	$t_{SU:STO}$	Stop condition set up time	160	-	
t_{NS}	-	Pulse width ignored (input filter on SCL and SDA), single glitch	-	10	

1. Conditions in addition to those specified in Table 116 and Table 117.
2. Evaluated by characterization, not tested in production.
3. V_{DD_IO} supply must not exceed V_{DD}.

Figure 28. R_{Pmin} vs. V_{DD}, f_c = 3.4 MHz

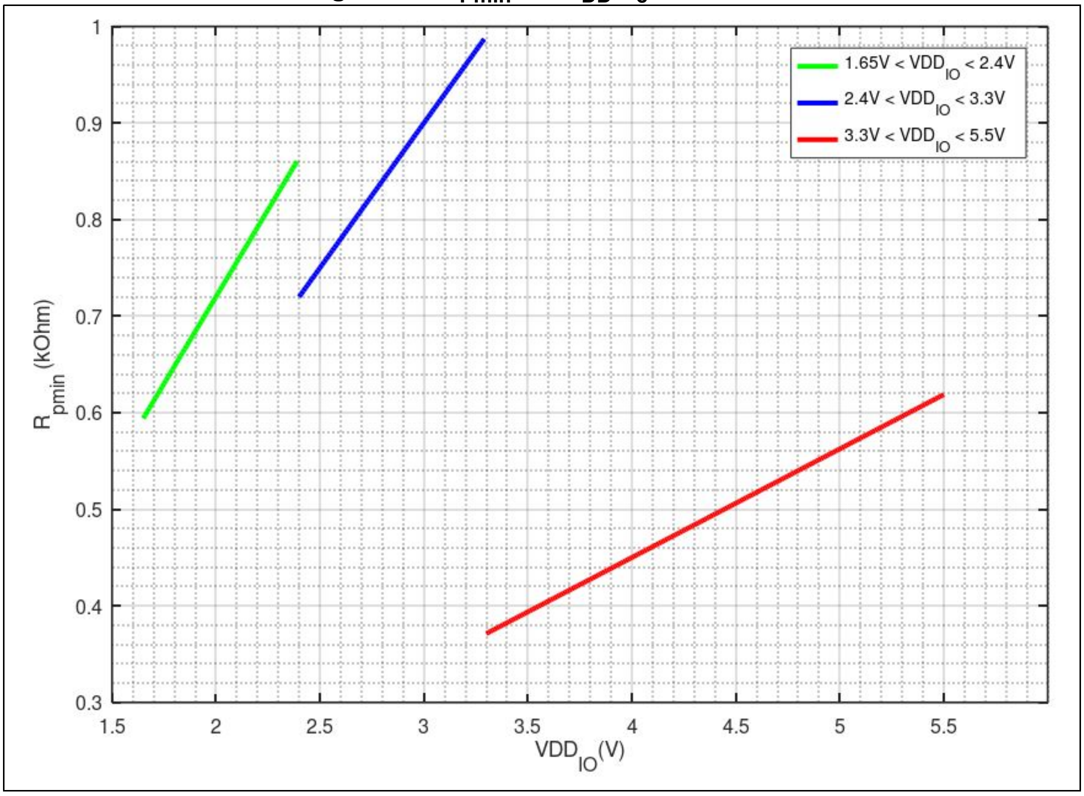


Figure 29. Maximum R_{bus} value vs. bus parasitic capacitance, f_c = 3.4 MHz

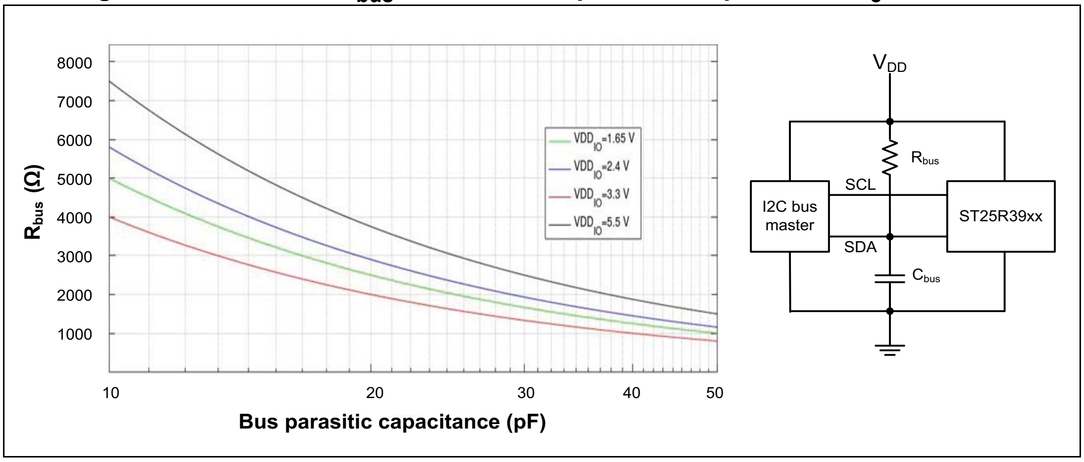


Figure 30. I2C AC waveforms

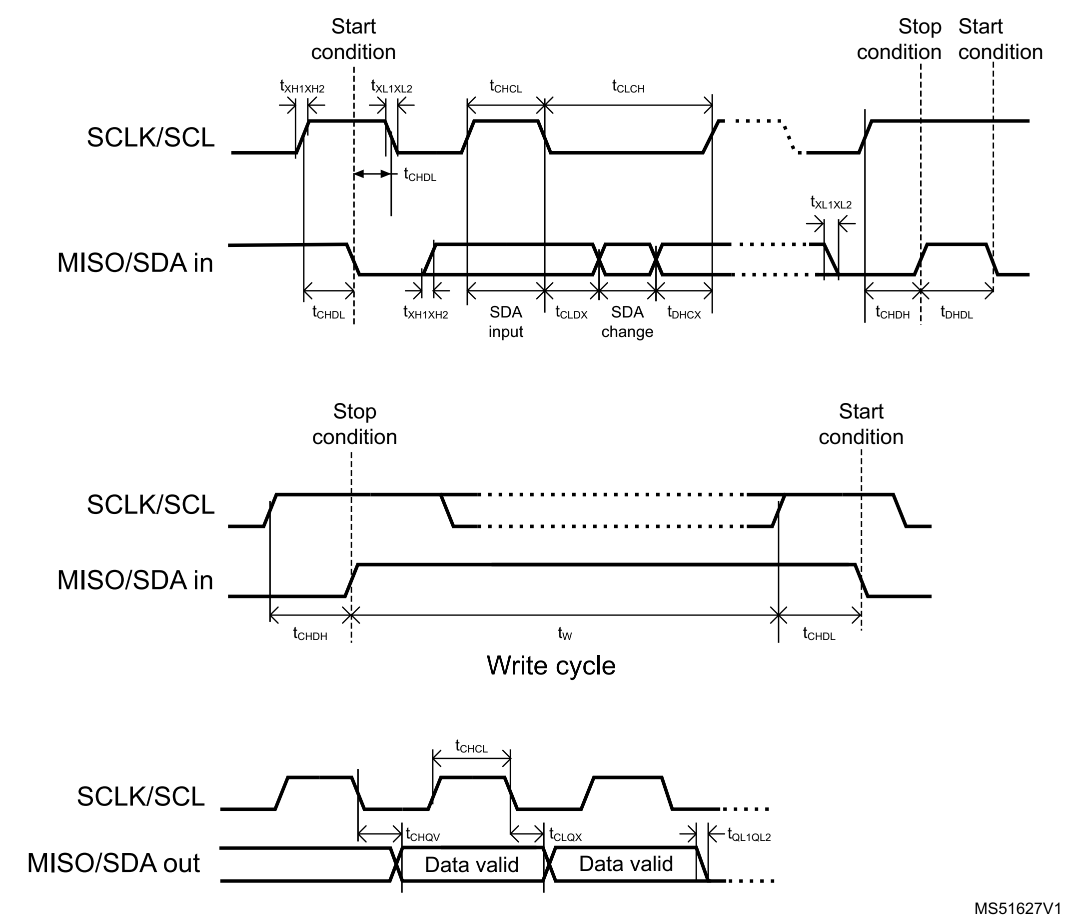
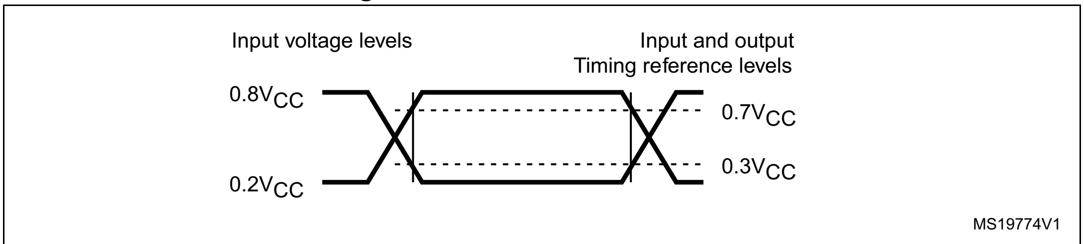


Figure 31. I2C AC measurements



6 Package information

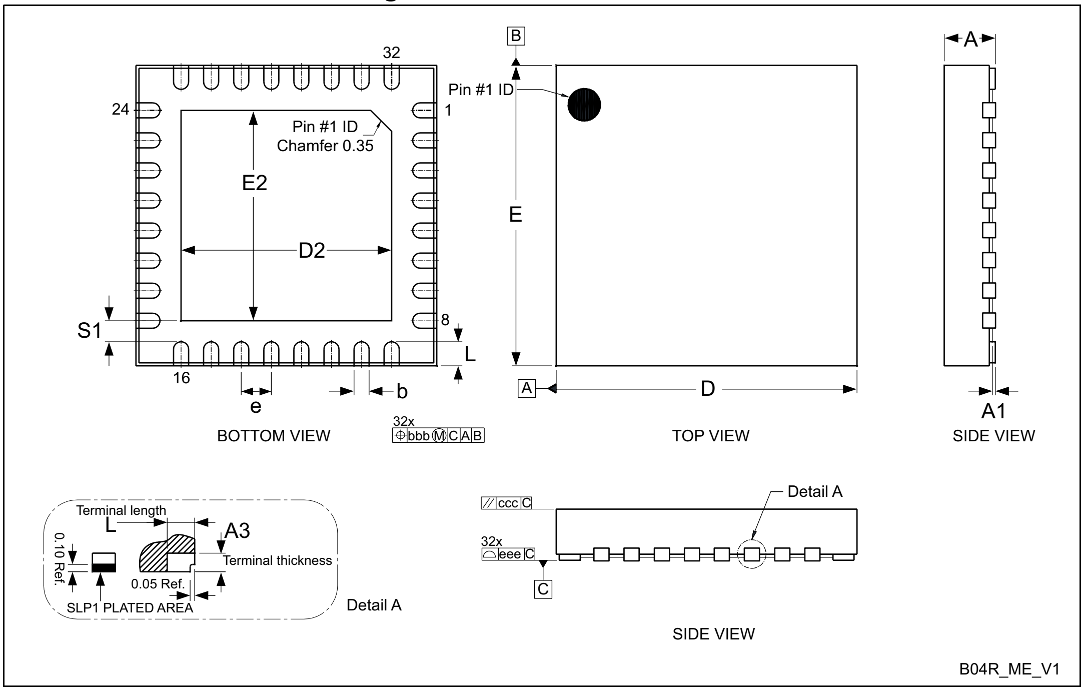
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at *www.st.com*.

ECOPACK is an ST trademark.

6.1 VFQFPN32 package information

VFQFPN32 is a 32-pin, 5x5 mm, 0.5 mm pitch, very thin fine pitch quad flat no lead package.

Figure 32. VFQFPN32 outline



1. Drawing is not to scale.
2. Coplanarity applies to the exposed pad as well as to the terminal.

Table 124. VFQFPN32 mechanical data

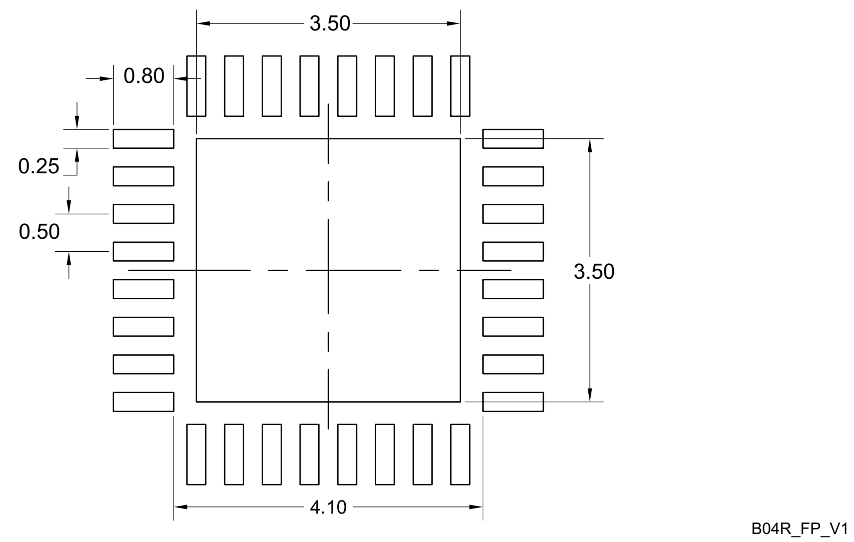
Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	0.800	0.900	1.000	0.0315	0.0354	0.0394
A1	0	-	0.050	0	-	0.0020
A3		0.200			0.0079	
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
b	0.180	0.250	0.300	0.0071	0.0098	0.0118

Table 124. VFQFPN32 mechanical data (continued)

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
D	5.000			0.1969		
D2	3.400	3.500	3.600	0.1339	0.1378	0.1417
E	5.000			0.1969		
E2	3.400	3.500	3.600	0.1339	0.1378	0.1417
e	0.500			0.0197		
S1	0.350			0.0138		
bbb	-	0.100	-	-	0.0039	-
ccc	-	0.100	-	-	0.0039	-
eee	-	0.080	-	-	0.0031	-

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 33. VFQFPN32 footprint example



1. Dimensions are expressed in millimeters.

7 Ordering information

Example: ST25 R 3918 A QW T

Device type

ST25 = NFC/RFID tags and readers

Product type

R = NFC/HF reader

Product feature

3918 = Multi-purpose NFC transceiver

Ambient temperature range

A = -40 °C to 105 °C

Package/Packaging

QW = 32-pin VFQFPN (5 x 5 mm) with wettable flanks

Tape and reel

T = 4000 pcs/reel

Note: Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device contact your nearest ST sales office.

8 Revision history

Table 125. Document revision history

Date	Revision	Changes
19-Mar-2021	1	Initial release.
08-Aug-2021	2	Updated *Figure 1: Minimum system configuration - Single sided antenna driving* and *Figure 2: Minimum system configuration - Differential antenna driving*. Updated *Section 4.4.2: Stop all activities* and *Section 4.4.5: NFC field ON commands*. Updated *Table 1: ST25R3918 - VFQFPN32 pin assignment*, *Table 10: I2C interface and interrupt signal lines*, *Table 11: List of direct commands*, *Table 12: Timing parameters of NFC field ON commands*, *Table 32: Auxiliary definition register* and its footnote *2*, *Table 108: Absolute maximum ratings*, *Table 109: Operating conditions* and footnote *1* of *Table 113: ST25R3918 electrical characteristics (VDD = 2.4 V)*. Added footnotes to tables *74*, *77*, *81*, *111*, *112* and *113*. Removed former *Figure 29: Direct command NFC response field ON*. Minor text edits across the whole document.
13-Apr-2022	3	Updated *Features* and *Section 4.5: Registers*. Updated *Table 17: Operation control register*, *Table 29: Stream mode definition register*, *Table 59: Timer and NFC interrupt register*, and *Table 115: SPI characteristics (5 MHz < 1 / TSCLK < 10 MHz)*. Added footnotes to *Table 79: External field detector activation threshold register*, and to *Table 82: External field detector deactivation threshold register*.
03-May-2022	4	Updated *Table 67: Number of transmitted bytes register 2*.
09-Nov-2022	5	Updated *Figure 1: Minimum system configuration - Single sided antenna driving*, *Figure 2: Minimum system configuration - Differential antenna driving*, and *Figure 4: ST25R3918 QFN32 pinout (top view)*. Updated *Table 1: ST25R3918 - VFQFPN32 pin assignment* and *Table 8: Serial data interface (4-wire interface) signal lines*. Minor text edits across the whole document.