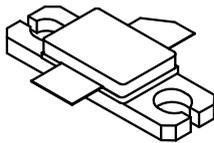
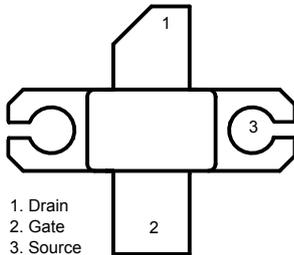


RF Power LDMOS transistor for frequencies up to 1.5 GHz



M243
Epoxy sealed



1. Drain
2. Gate
3. Source

GADG310120180952IG



Product status link

[ST50V10100](#)

Product summary

Order code	ST50V10100
Marking	ST50V10100
Package	M243
Packing	TBD

Features

Order code	F _{REQ}	V _{DD}	P _{OUT} (typ.)	Gain	N _D
ST50V10100	1000 MHz	50 V	100 W	18 dB	60%

- High efficiency and linear gain operations
- Integrated ESD protection
- Large positive and negative gate/source voltage range
- In compliance with the European Directive 2002/95/EC

Applications

- Industrial, scientific and medical from HF to 1.5 GHz
- Avionics

Description

The **ST50V10100** is a common source N-channel enhancement-mode lateral field effect RF power transistor designed for broadband commercial, Avionics and industrial applications at frequencies up to 1.5 GHz. It can be used in class A/AB and C for all typical modulation formats.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
BV_{DSS}	Drain-source voltage	110	V
V_{GS}	Gate-source voltage	-8 / +10	V
I_D	Drain current	18	A
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Junction temperature	+200	°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case, $T_{CASE} = +85\text{ °C}$, $P_{OUT}=100\text{ W}$	0.75	°C/W

Table 3. ESD protection

Symbol	Parameter	Class
HBM	Human body model (per JESD22-A114)	2

2 Electrical characteristics

($T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified).

Table 4. Static (per side)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 100\text{ }\mu\text{A}$	110			V
I_{DSS}	Zero-gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 50\text{ V}$			1	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = 6\text{ V}$			1	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = 50\text{ V}$, $I_D = 600\text{ }\mu\text{A}$	1	TBD	3	V
$V_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 5\text{ A}$			1.4	V
C_{iss}	Common source input capacitance	$V_{GS} = 0\text{ V}$, $V_{DD} = 50\text{ V}$, $f = 1\text{ MHz}$		118		pF
C_{oss}	Common source output capacitance			2		
C_{rss}	Common source feedback capacitance			44		

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
P_{OUT}	Output power	$V_{DD} = 28\text{ V}$, $I_{DQ} = 0.1\text{ A}$, $f = 915\text{ MHz}$	-	100	-	W
Gain	Power gain		-	18	-	dB
Efficiency	Drain efficiency		-	63	-	%
IMD3	3 rd order intermodulation		-	TBD	-	dBc
VSWR	Load mismatch	@ $P_{OUT} = 100\text{ W}$ all phases	-	10:1	-	

Table 6. Impedance data

Frequency (MHz)	Input impedance Z_{IN}	Drain load impedance Z_{DL}
100	TBD	TBD
250		
500		
750		
1000		
1250		
1500		

3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

3.1 M243 (0.230 x 0.360 2/L N/HERM W/FLG) package information

Figure 1. M243 (0.230 x 0.360 2/L N/HERM W/FLG) package outline

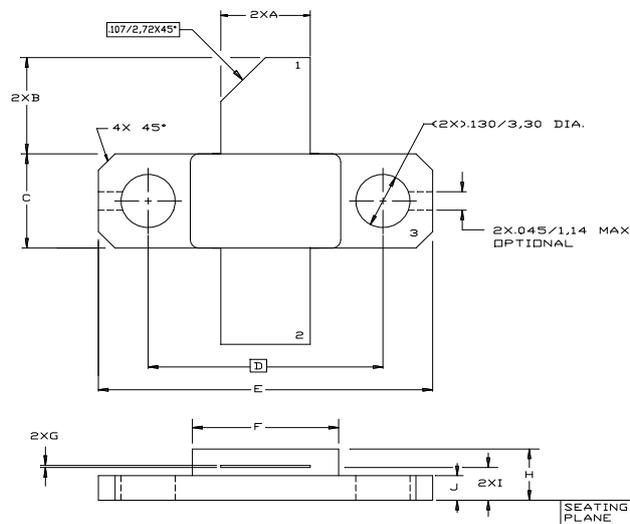


Table 7. M243 (0.230 x 0.360 2/L N/HERM W/FLG) package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	5.21		5.72
B	5.46		6.48
C	5.59		6.1
D		14.27	
E	20.07		20.57
F	8.89		9.4
G	0.1		0.15
H	3.18		4.45
I	1.83		2.24
J	1.27		1.78

Revision history

Table 8. Document revision history

Date	Version	Changes
11-Sep-2018	1	Initial release.
22-Mar-2019	2	Updated Table 1 and Table 4 .

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