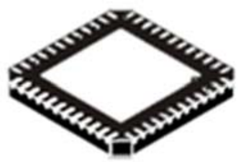
ST75MM

METERS AND MORE® compliant power line communication System on Chip

Datasheet - production data



VFQFPN 7 x 7 x 1.0 48L (pitch 0.50)

Features

- METERS AND MORE standard compliant power line communication System on Chip
- High-performing, configurable DSP core for flexible PHY layer processing:
  - Very robust B-PSK modulation with convolutional coding and Viterbi decoding compliant with METERS AND MORE specifications with 4.8 kbps data rate
  - Optional high speed modes with Q-PSK and 8-PSK modulations for increased data rates up to 28.8 kbps
  - Optional dual channel operation mode
  - Optional peak noise avoidance algorithm mode
  - Signal to noise ratio channel estimation
- 8-bit protocol engine embedding turnkey METERS AND MORE compliant data link layer
- Up to 57.6 kbps host controller UART interface
- Embedded AES-128 encryption engine for data authentication and confidentiality services
- Fully integrated analog front end:
  - ADC and DAC
  - Digital transmission level control
  - PGA with automatic gain control
  - High sensitivity receiver
- Fully integrated single-ended power amplifier for line driving
  - Up to 1 A rms, 14 V p-p output
  - Configurable active filtering topology
  - Very high linearity
  - Embedded temperature sensor
  - Current control feature
- 8 to 18 V power amplifier supply
- 3.3 V or 5 V digital i/o supply
- Embedded zero-crossing detection for line phase recognition
- Suitable for CENELEC EN50065, ARIB and FCC part 15 compliant applications
- Embedded access protocol suitable for EN50065 compliant applications in the 125- to 140-kHz frequency band
- Communication carrier frequency programmable up to 250 kHz
- VFQFPN48 7 x 7 exposed pad package
- -40 °C to +85 °C temperature range

Applications

- METERS AND MORE standard compliant advanced metering infrastructures (AMI)
- Sub-metering and Smart Grid applications
- Command and control networks
- Smart home applications

Description

The ST75MM is a flexible power line communication System on Chip combining a high-performing PHY processor and a protocol controller core, implementing the turnkey METERS AND MORE protocol standard along with the fully integrated analog front end (AFE) and line driver in a single chip, for future-proof, compact and cost effective Smart Grid solutions.

Table 1. Device summary

Order codes	Package	Packaging
ST75MM	VFQFPN48	Tube
ST75MMTR		Tape and reel

Contents

1 Device overview . . . 4

2 Pin connection . . . 6

Pin description . . . 6

3 Maximum ratings . . . 9

3.1 Absolute maximum ratings . . . 9

3.2 Thermal data . . . 9

4 Electrical characteristics . . . 10

5 Analog front end (AFE) . . . 16

5.1 Reception path . . . 16

5.2 Transmission path . . . 16

5.3 Power amplifier . . . 17

5.4 Current and voltage control . . . 17

5.5 Thermal shutdown and temperature control . . . 19

5.6 Zero-crossing comparator . . . 19

6 Power management . . . 20

Ground connections . . . 22

7 Clock management . . . 23

8 Functional overview . . . 24

8.1 Bootloader routine . . . 24

8.2 Start-up sequence . . . 24

8.3 PHY activity signaling . . . 25

9 Carrier sense multiple access algorithm . . . 26

10 PLC protocol 27

10.1 Introduction 27

10.2 Physical layer 27

10.3 Data link layer 27

11 Package information 28

11.1 VFQFPN48 (7 x 7 x 1.0 mm) package information 28

12 Revision history 30

1 Device overview

Based on the ST industrial STarGRID™ SoC platform, the ST75MM offers a “turnkey” power line communication solution compliant with the METERS AND MORE protocol stack, enabling field-proven, bidirectional data transfer for advanced metering infrastructures (AMI).

The METERS AND MORE protocol meets functionality, security and communication requirements defined by the OPEN meter project.

The METERS AND MORE protocol has been conceived and massively proven to ensure best communication efficiency, robustness and security in real field conditions, thanks to the following main protocol functionalities:

- Very short message exchanges, optimized for low data rate power line communications
- Robust narrow-band BPSK modulation with powerful correction coding allowing stable point to point communication link even in harsh noisy conditions
- Dynamic optimization of the communication paths for end-to-end reliable communication in real variable conditions
- Support of high level of encryption and authentication by the use of state-of-the-art 128-bit AES algorithm
- Automatic network configuration and management for plug-and-play systems
- Smart retransmission management for communication robustness and bandwidth maximization

According to a simplified ISO/OSI protocol architecture, the METERS AND MORE protocol specifies the physical layer (PHY), the data link layer and the application layer, including the METERS AND MORE specific metering data model.

Optionally, the METERS AND MORE protocol can support other metering application layers and related data models through dedicated convergence layers defined by the Association, such as for example the DLMS/COSEM application layer (IEC620956).

In order to provide a turnkey communication system, while assuring highest application flexibility, the ST75MM device embeds the METERS AND MORE PHY and data link layers, leaving the application layer and the metering data model to be managed by the external host controller.

The ST75MM also features a configurable CSMA algorithm, compatible with the channel access as specified by the EN50065-1 standard, which doesn't require the external host intervention after the initial configuration.

Made using a multi-power technology with state-of-the-art VLSI CMOS lithography, the ST75MM is based on a dual digital core architecture (a PHY processor engine and a protocol controller core) to guarantee outstanding communication performance.

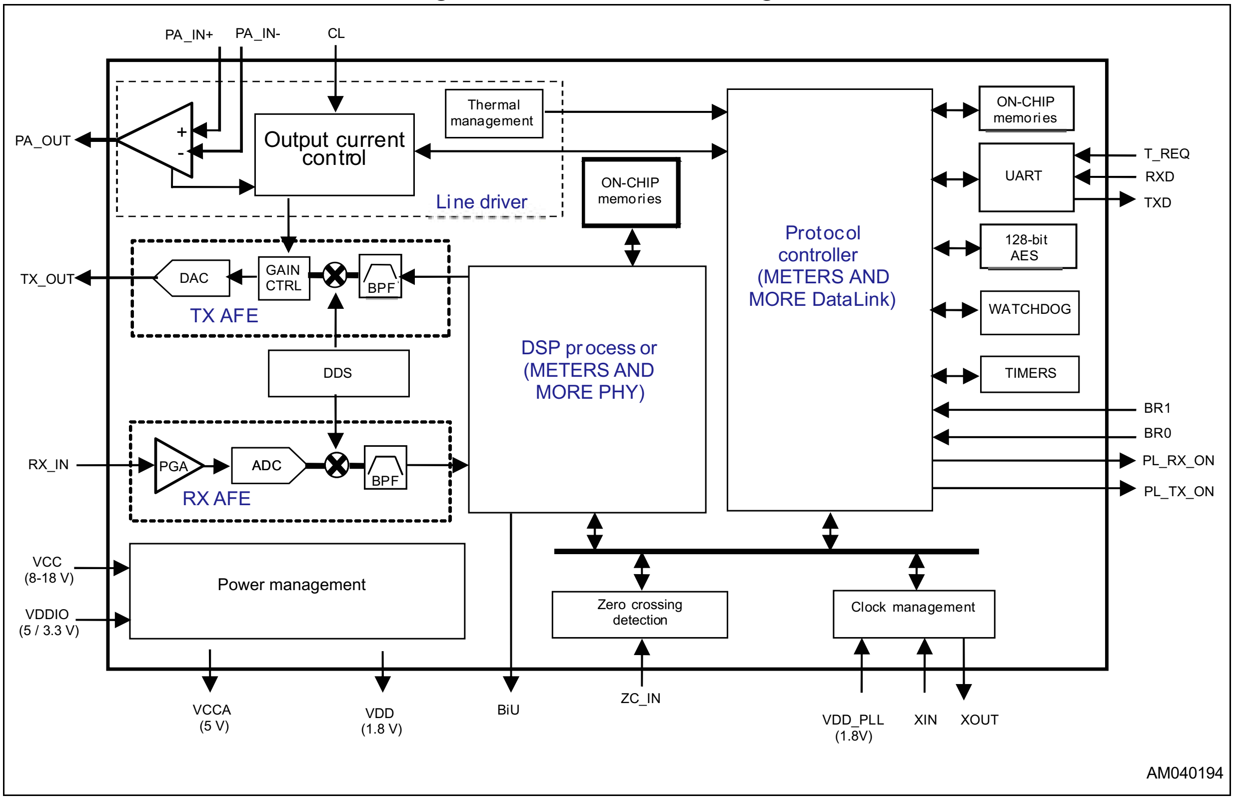
An HW 128-bit AES encryption block with customizable key management is available on-chip when secure communication is requested.

The on-chip analog front end, featuring analog-to-digital and digital-to-analog conversion plus automatic gain control, along with the integrated line driver delivering up to 1 A rms output current makes the ST75MM a unique System on Chip for power line communication.

Line coupling network design is also very simplified, leading to a very low BOM cost.

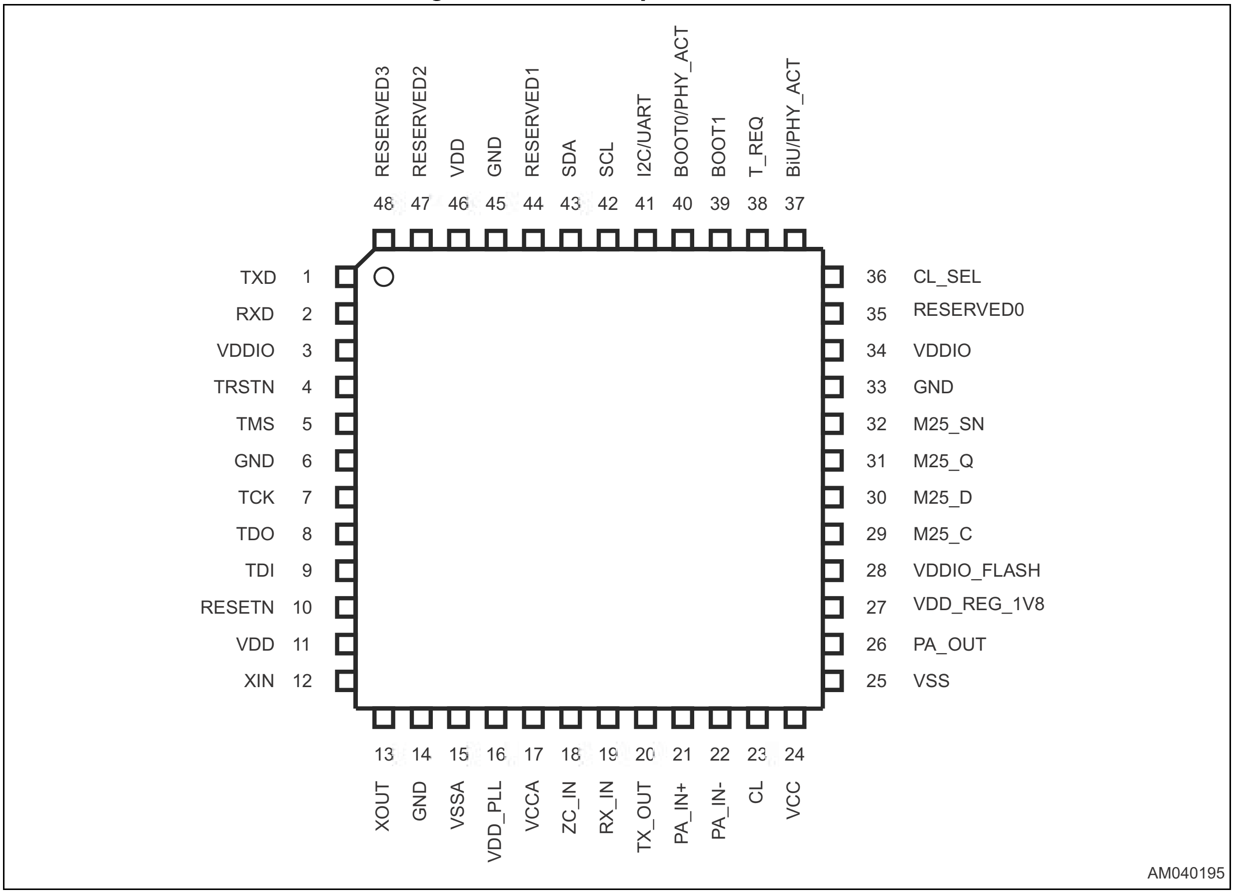
Safe and performing operations are guaranteed while keeping power consumption and signal distortion levels very low, thus making the ST75MM an ideal platform for the most stringent application requirements and regulatory standards compliance.

Figure 1. ST75MM block diagram



2 Pin connection

Figure 2. ST75MM pin connection



Pin description

Table 2. Pin description

Pin	Name	Type	Reset state	Internal pull-up	Description
1	TXD	Digital output	High Z	Disabled	UART data out external pull-up to VDDIO required
2	RXD	Digital input	High Z	Disabled	UART data in
3	VDDIO	Power	-	-	3.3 V - 5 V I/O supply
4	TRSTN	Digital input	Input	Enabled	System JTAG interface reset (active low)
5	TMS	Digital input	Input	Enabled	System JTAG interface mode select
6	GND	Power	-	-	Digital ground
7	TCK	Digital input	High Z	Disabled	System JTAG interface clock external pull-up to VDDIO required

Table 2. Pin description (continued)

Pin	Name	Type	Reset state	Internal pull-up	Description
8	TDO	Digital output	High Z	Disabled	System JTAG interface data out
9	TDI	Digital input	Input	Enabled	System JTAG interface data in
10	RESETN	Digital input	Input	Disabled	System reset (active low)
11	VDD	Power	-	-	1.8 V digital supply
12	XIN	Analog	-	-	Crystal oscillator input / external clock input
13	XOUT	Analog	-	-	Crystal oscillator output (if external clock supplied on XIN, XOUT must be left floating)
14	GND	Power	-	-	Digital ground
15	VSSA	Power	-	-	Analog ground
16	VDD_PLL	Power	-	-	1.8 V PLL supply voltage (connect to VDD)
17	VCCA	Power	-	-	5 V analog supply / internal regulator output
18	ZC_IN	Analog input	-	-	Zero-crossing input
19	RX_IN	Analog input	-	-	Reception analog input
20	TX_OUT	Analog output	-	-	Transmission analog output
21	PA_IN+	Analog input	-	-	Power amplifier non-inverting input
22	PA_IN-	Analog input	-	-	Power amplifier inverting input
23	CL	Analog input	-	-	Current limit sense input
24	VCC	Power	-	-	Power supply
25	VSS	Power	-	-	Power ground
26	PA_OUT	Analog output	-	-	Power amplifier output
27	VDD_REG_1V8	Power	-	-	1.8 V digital supply / internal regulator output externally accessible for filtering purposes only
28	VDDIO_FLASH	Power	-	-	3.3 V external Flash memory SPI interface supply. Connect to VDDIO if external Flash memory is not connected.
29	M25_C	Digital output	Output	Disabled	External Flash memory serial clock. Leave floating if external Flash memory is not connected.
30	M25_D	Digital output	Output	Disabled	External Flash memory serial data in. Leave floating if external Flash memory is not connected.
31	M25_Q	Digital input	Input	Disabled	External Flash memory serial data out. Pull-up to VDDIO if external Flash memory is not connected.
32	M25_SN	Digital output	Output	Disabled	External Flash memory chip select. Leave floating if external Flash memory is not connected.
33	GND	Power	-	-	Digital ground

Table 2. Pin description (continued)

Pin	Name	Type	Reset state	Internal pull-up	Description
34	VDDIO	Power	-	-	3.3 V - 5 V I/O supply
35	RESERVED0	-	-	-	Not used, connect to GND
36	CL_SEL	Digital output	High Z	Disabled	Current limit resistor selection output. Pull-up to VDDIO.
37	BiU/PHY_ACT	Digital output	High Z	High Z	Band-in-use detector output / PHY activity signal. Pull-up to VDDIO.
38	T_REQ	Digital I/O	High Z	Disabled	Host interface control line. Pull-up to VDDIO.
39	BOOT1	Digital I/O	High Z	Disabled	See *Section 8: Functional overview on page 24* for function during start-up and normal operation. Pull-up to VDDIO.
40	BOOT0/PHY_ACT	Digital I/O	High Z	Disabled	See *Section 8* for function during start-up and normal operation. Pull-up to VDDIO.
41	I2C/UART	Digital input	Input	Disabled	Host interface selection1 = I2C0 = UART
42	SCL	Digital I/O	High Z	Disabled	I^2C serial clock
43	SDA	Digital I/O	High Z	Disabled	I^2C data line
44	RESERVED1	-	-	-	Not used, pull-up to VDDIO
45	GND	Power	-	-	Digital ground
46	VDD	Power	-	-	1.8 V digital supply
47	RESERVED2	-	-	-	Not used, pull-up to VDDIO
48	RESERVED3 -	-	-	-	Not used, pull-up to VDDIO
-	Exposed pad	-	-	-	Electrically connected to VSSA. It must be thermally connected to a copper ground plane for enhanced electrical and thermal performance.

3 Maximum ratings

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		Min.	Max.	
VCC	Power supply voltage	-0.3	20	V
VSSA-GND	Voltage between VSSA and GND	-0.3	0.3	V
VDDIO	I/O supply voltage	-0.3	5.5	V
VDDIO_FLASH	External Flash interface supply voltage	-0.3	5.5	V
VI	Digital input voltage	GND -0.3	VDDIO+0.3	V
VO	Digital output voltage	GND -0.3	VDDIO+0.3	V
V(PA_IN)	PA inputs voltage range	VSS -0.3	VCC+0.3	V
V(PA_OUT)	PA_OUT voltage range	VSS -0.3	VCC+0.3	V
V(RX_IN)	RX_IN voltage range	- (VCCA +0.3)	VCC+0.3	V
V(ZC_IN)	ZC_IN voltage range	- (VCCA +0.3)	VCCA+0.3	V
V(TX_OUT, CL)	TX_OUT, CL voltage range	VSSA -0.3	VCCA +0.3	V
V(XIN)	XIN voltage range	GND -0.3	VDDIO +0.3	V
I(PA_OUT)	Power amplifier output non-repetitive peak current	-	5	A peak
I(PA_OUT)	Power amplifier output non-repetitive rms current	-	1.4	A rms
T_{amb}	Operating ambient temperature	-40	85	ºC
T_{stg}	Storage temperature	-50	150	ºC
V(ESD)	Maximum withstanding voltage range Test condition: CDF-AEC-Q100-002 “human body model” Acceptance criteria: “normal performance”	-2	+2	kV

3.2 Thermal data

Table 4. Thermal characteristics

Symbol	Parameter	Value	Unit
RthJA1	Maximum thermal resistance junction to ambient steady state(1)	50	°C/W
RthJA2	Maximum thermal resistance junction to ambient steady state(2)	42	°C/W

1. Mounted on a 2-side + vias PCB with a dissipating ground area on the bottom side.
2. Same conditions as in *1*, with maximum transmission duration limited to 100 s.

4 Electrical characteristics

TA = -40 to +85 °C, TJ < 125 °C, VCC = 18 V, unless otherwise specified.

Table 5. ST75MM electrical characteristics

Symbol	Parameter	Note	Min.	Typ.	Max.	Unit
Power supply						
VCC	Power supply voltage	-	8	13	18	V
I(VCC) RX	Power supply current - Rx mode	VCCA externally supplied	-	0.35	0.5	mA
I(VCC) TX	Power supply current - Tx mode, no load	VCCA externally supplied	-	22	30	mA
VCC UVLO_TL	VCC undervoltage lockout low threshold	-	6.1	6.5	6.95	V
VCC UVLO_TH	VCC undervoltage lockout high threshold	-	6.8	7.2	7.5	V
VCC UVLO_HYST	VCC undervoltage lockout hysteresis	-	250(1)	700	-	mV
I(VCCA) RX	Analog supply current - Rx mode	-	-	5	6	mA
I(VCCA) TX	Analog supply current - Tx mode	V(TX_OUT) = 5 V p-p, no load	-	8	10	mA
VDD	Digital core supply voltage	Externally supplied	-10%	1.8	+10%	V
I(VDD)	Digital core supply current	-	-	35	-	mA
I(VDD) RESET	Digital core supply current in RESET state	-	-	8	-	mA
VDD_PLL	PLL supply voltage	-	-	VDD	-	V
I(VDD_PLL)	PLL supply current	-	-	0.4	0.5	mA
VDDIO	Digital I/O supply voltage	Externally supplied	-10%	3.3 or 5	+10%	V
VDDIO_FLASH	External Flash memory interface supply voltage/ 1.8 V regulator input voltage	Flash memory connected	-10%	3.3	+10%	V
		1.8 V regulator input voltage only	-10%	3.3 or 5	+10%	V
VDDIO_FLASH UVLO_TL	1.8 V regulator undervoltage lockout low threshold	-	2.2	2.4	2.6	V
VDDIO_FLASH UVLO_TH	1.8 V regulator undervoltage lockout high threshold	-	2.45	2.65	2.85	V
VDDIO_FLASH UVLO_HYST	1.8 V regulator undervoltage lockout hysteresis	-	180	240	-	mV

Table 5. ST75MM electrical characteristics (continued)

Symbol	Parameter	Note	Min.	Typ.	Max.	Unit
Analog front end						
Power amplifier						
V(PA_OUT) BIAS	Power amplifier output bias voltage - Rx mode	-	-	VCC/2	-	V
GBWP	Power amplifier gain-bandwidth product	-	100	-	-	MHz
I(PA_OUT) MAX	Power amplifier maximum output current	-	-	-	1000	mA rms
V/PA_OUT) TOL	Power amplifier output tolerance(2)	VCC = 18 V, V(PA_OUT) = 14 V p-p (typ), V(PA_OUT) BIAS = VCC/2, RLOAD = 50 Ω See *Figure 3*	-3%	-	+3%	-
V(PA_OUT) HD2	Power amplifier output 2nd harmonic distortion	-	-	-70	-63	dBc
V(PA_OUT) HD3	Power amplifier output 3rd harmonic distortion	-	-	-66	-63	dBc
V(PA_OUT) THD	Power amplifier output total harmonic distortion	-	-	0.1	0.15	%
C(PA_IN)	Power amplifier input capacitance	PA_IN+ vs. VSS(3)	-	10	-	pF
		PA_IN- vs. VSS(3)	-	10	-	pF
PSRR	Power supply rejection ratio	50 Hz	-	100	-	dB
		1 kHz	-	93	-	dB
		100 kHz	-	70	-	dB
CL_TH	Current sense high threshold on CL pin	-	2.25	2.35	2.4	V
CL_RATIO	Ratio between PA_OUT and CL output current	-	-	80	-	-
Transmitter						
V(TX_OUT) BIAS	Transmitter output bias voltage - Rx mode	-	-	VCCA/2	-	V
V(TX_OUT) MAX	Transmitter output maximum voltage swing	TX GAIN = 31, no load	4.8	4.95	VCCA	V p-p
TX_GAIN	Transmitter output digital gain range	-	0	-	31	-
TX_GAIN TOL	Transmitter output digital gain tolerance	-	-0.35	-	0.35	dB
R(TX_OUT)	Transmitter output resistance	-	-	1	-	kΩ

Table 5. ST75MM electrical characteristics (continued)

Symbol	Parameter	Note	Min.	Typ.	Max.	Unit
V(TX_OUT) HD2	Transmitter output 2nd harmonic distortion	V(TX_OUT) = V(TX_OUT) MAX, no load	-	-72	-67	dBc
V(TX_OUT) HD3	Transmitter output 3rd harmonic distortion	-	-	-70	-55	dBc
V(TX_OUT) THD	Transmitter output total harmonic distortion	-	-	0.1	0.2	%
Receiver						
V(RX_IN) MAX	Receiver input maximum voltage	VCC = 18V	-	-	15	V p-p
V(RX_IN) BIAS	Receiver input bias voltage	-	-	VCCA/2	-	V
Z(RX_IN)	Receiver input impedance	-	-	10	-	-
V(RX_IN) MIN	Receiver input sensitivity	B-PSK coded mode, f = 86 kHz, BER = 10 - 3, SNR ≥ 20 dB(3)	-	36	-	dBμV RMS
		FSK mode, symbol rate = 2400, deviation = 1, f = 86 kHz, BER = 10 - 3, SNR ≥ 20 dB(3)	-	39	-	dBμV RMS
PGA_MIN	PGA minimum gain	-	-	-18	-	dB
PGA_MAX	PGA maximum gain	-	-	30	-	dB
Oscillator						
V(XIN)	Oscillator input voltage swing	Clock frequency supplied externally	-	1.8	VDDIO	V p-p
V(XIN) TH	Oscillator input voltage threshold	-	0.8	0.9	1	V
f(XIN)	Crystal oscillator frequency	-	-	8	-	MHz
f(XIN) TOL	External quartz crystal frequency tolerance	-	-150	-	+150	ppm
ESR	External quartz crystal ESR value	-	-	-	100	Ω
CL	External quartz crystal load capacitance	-	-	16	20	pF
fCLK_AFE	Internal frequency of the analog front end	-	-	8	-	MHz
fCLK_PROTOCOL	Internal frequency of the protocol controller core	-	-	28	-	MHz
fCLK_PHY	Internal frequency of the PHY processor	-	-	56	-	MHz

Table 5. ST75MM electrical characteristics (continued)

Symbol	Parameter	Note	Min.	Typ.	Max.	Unit
Temperature sensor						
T_TH1	Temperature threshold 1	(3)	63	70	77	°C
T_TH2	Temperature threshold 2	-	90	100	110	°C
T_TH3	Temperature threshold 3	-	112	125	138	°C
T_TH4	Temperature threshold 4	-	153	170	187	°C
Zero-crossing comparator						
V(ZC_IN) MAX	Zero-crossing detection input voltage range	-	-	-	10	V p-p
V(ZC_IN) TL	Zero-crossing detection input low threshold	-	-40	-30	-20	mV
V(ZC_IN) TH	Zero-crossing detection input high threshold	-	30	40	50	mV
V(ZC_IN) HYST	Zero-crossing detection input hysteresis	-	62	70	78	mV
V(ZC_IN) d.c.	Zero-crossing signal duty cycle	-	-	50%	-	-
Digital section						
Digital I/O						
$R_{PULL-UP}$	Internal pull-up resistors	VDDIO = 3.3 V	-	66	-	kΩ
		VDDIO = 5 V	-	41	-	kΩ
VIH	High logic level input voltage	-	0.65 * VDDIO	-	VDDIO +0.3	V
VIL	Low logic level input voltage	-	-0.3	-	0.35 * VDDIO	V
VOH	High logic level output voltage	IOH = -4 mA	VDDIO -0.4	-	-	V
VOL	Low logic level output voltage	IOL = 4 mA	-	-	0.4	V
UART interface						
Data Bits	-	-	-	8	-	Bits
Stop Bits	-	-	-	1	-	Bits
Parity Bits	-	-	-	0	-	Bits
Baud Rate	-	-	-1.5%	57600	+1.5%	BAUD
			-1.5%	38400	+1.5%	BAUD
			-1.5%	19200	+1.5%	BAUD
			-1.5%	9600	+1.5%	BAUD

Table 5. ST75MM electrical characteristics (continued)

Symbol	Parameter	Note	Min.	Typ.	Max.	Unit
I^2C interface						
Data speed	-	-	-	-	400	kbps
Address length	-	-	-	7	10	Bits
Reset and power-on						
t_{RESETN}	Minimum valid reset pulse duration	-	-	1	-	µs
$t_{STARTUP}$	Start-up time at power-on or after a reset event	-	-	60	-	ms

1. Referred to T_{AMB} = -40 °C.
2. This parameter does not include the tolerance of external components.
3. Guaranteed by design.

Figure 3. PA linearity test circuit

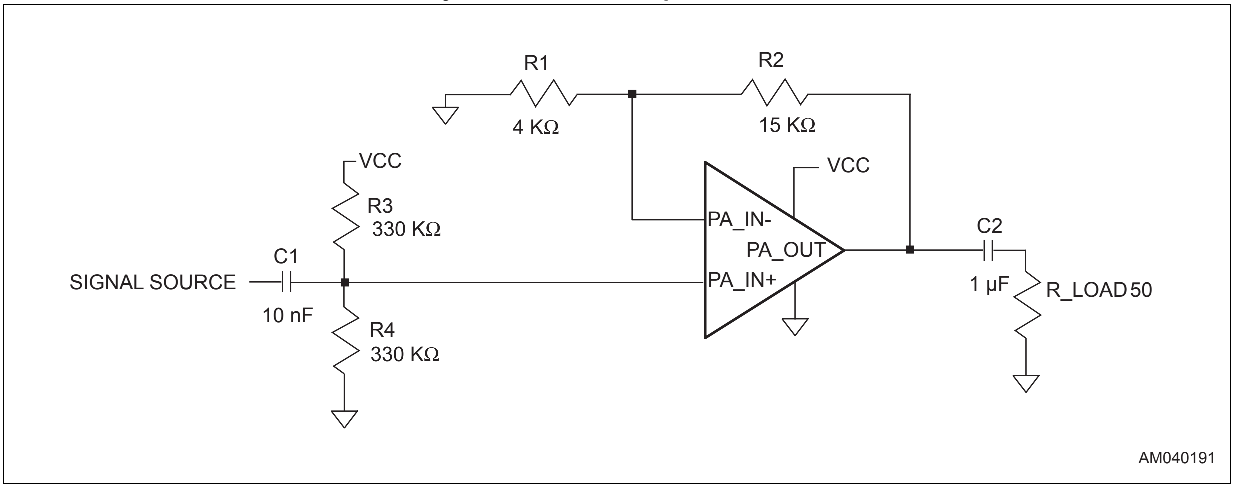
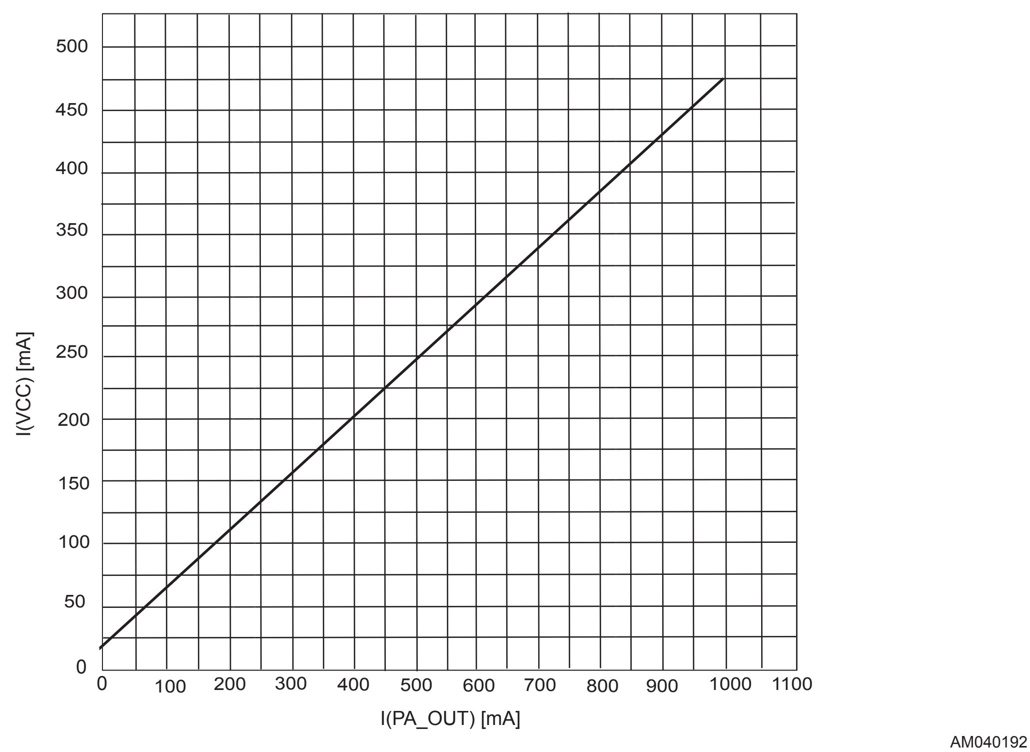


Figure 4. I(VCC) vs. I(PA_OUT) curve - typical values

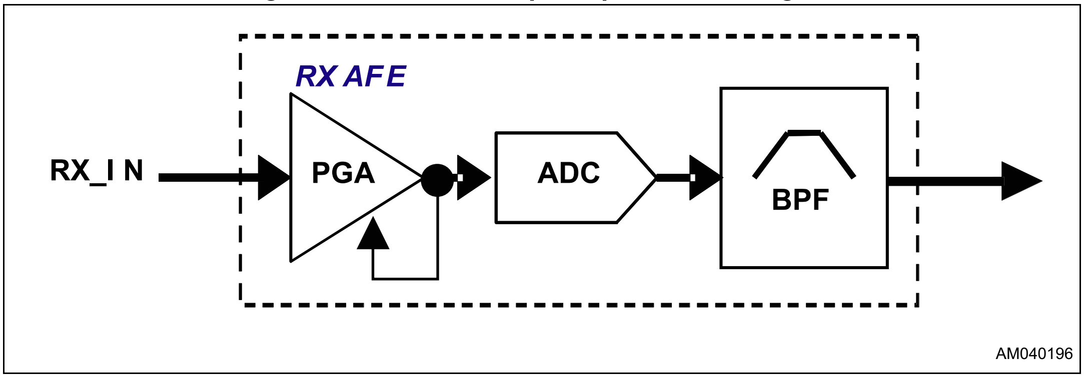


5 Analog front end (AFE)

5.1 Reception path

Figure 5 shows the block diagram of the ST75MM input receiving path. The main blocks are a wide input range analog programmable gain amplifier (PGA) and the analog-to-digital converter (ADC).

Figure 5. ST75MM reception path block diagram



The PGA is controlled by an embedded loop algorithm, adapting the PGA gain to amplify or attenuate the received signal according to the input voltage range for the ADC.

The PGA gain ranges from -18 dB up to 30 dB, with steps of 6 dB (typical), as described in *Table 6*.

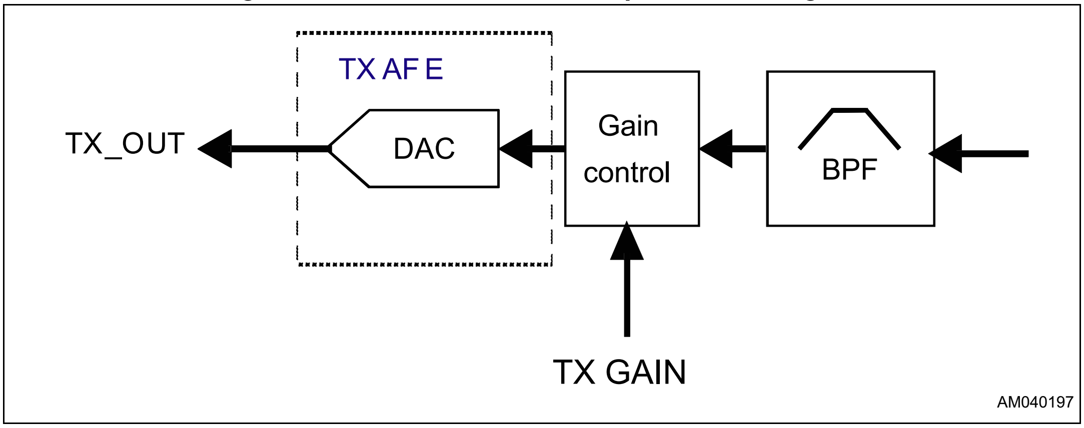
Table 6. PGA gain table

PGA code	PGA gain (typ) [dB]	RX_IN max. range [V p-p]
0	-18	V(RX_IN) MAX
1	-12	8
2	-6	4
3	0	2
4	6	1
5	12	0.500
6	18	0.250
7	24	0.125
8	30	0.0625

5.2 Transmission path

Figure 6 shows the transmission path block diagram. It is mainly based on a digital-to-analog converter (DAC), capable to generate a very linear signal up to its full scale output. The gain control block before the DAC gives the possibility to scale down the output signal to match the desired transmission level.

Figure 6. ST75MM transmission path block diagram



The amplitude of the transmitted signal can be set on a 32-step logarithmic scale through the TX_GAIN parameter, introducing an attenuation ranging from 0 dB (typ.), corresponding to the TX_OUT full range, down to -31 dB (typ.).

The attenuation set by the TX_GAIN parameter can be calculated as follows:

Equation 1: Output attenuation A [dB] vs. TX GAIN

$$A[dB] = (TX\_GAIN - 31) + TX\_GAIN_{TOL}$$

5.3 Power amplifier

The integrated power amplifier is characterized by very high linearity, required to comply with the different international regulations (CENELEC, FCC, etc.) limiting the spurious conducted emissions on the mains, and a current capability of I(PA_OUT) MAX that allows the amplifier driving even very low impedance points of the network.

All pins of the power amplifier are accessible, making it possible to build an active filter network to increase the linearity of the output signal.

5.4 Current and voltage control

The power amplifier output current sensing is performed by mirroring a fraction of the output current and making it flow through a resistor RCL connected between the CL pin and VSS. The following relationship can be established between V(CL) and I(PA_OUT):

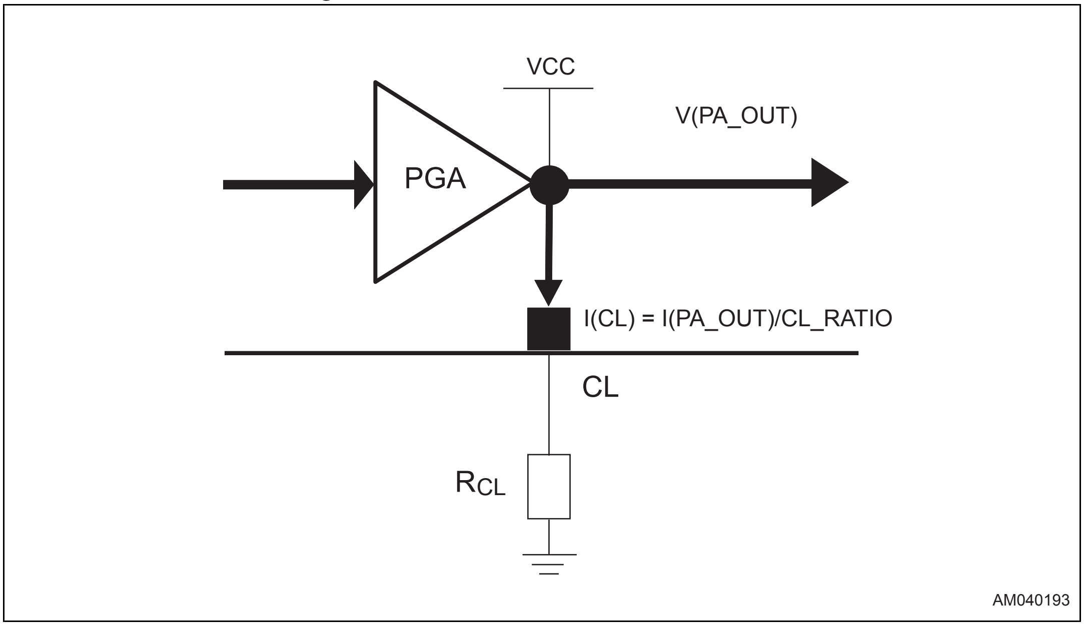
Equation 2: V(CL) vs. I(PA_OUT)

$$V(CL) = \frac{R_{CL} \cdot I(PA\_OUT)}{CL\_RATIO}$$

The voltage level V(CL) is compared with two internal thresholds CL_TL and CL_TH. When the V(CL) exceeds the CL_TH level, the V(TX_OUT) voltage is decreased by one TX_STEP at a time until V(CL) goes below the CL_TL threshold.

The current sense circuit is depicted in Figure 7.

Figure 7. PA_OUT current sense circuit



The RCL value to get the desired output current limit I(PA_OUT)LIM can be calculated as follows:

Equation 3: RCL calculation

$$R_{CL} = \frac{CL\_TH}{I(PA\_OUT)_{LIM} / CL\_RATIO}$$

Note that I(PA_OUT)LIM is expressed as the peak current, so the corresponding rms current shall be calculated according to the transmitted signal waveform. As FSK and PSK modulations have different crest factors, different RCL values are required for the two modulations.

The RCL values to get the 1 A rms output current limit, calculated with typical values for CL_TH and CL_RATIO parameters, are indicated in Table 7.

Table 7. CL resistor typical values

Parameter	Description	Value	Unit
R_{CL}	Resistor value for I(PA_OUT) MAX = 1 A rms = 1.41 A pk (FSK mode)	133	Ω
	Resistor value for I(PA_OUT) MAX = 1 A rms = 2 A pk (PSK mode)	94	Ω

The CL_SEL pin can be used to switch automatically the RCL resistor value according to the modulation used. If FSK is selected, CL_SEL is forced low, while if PSK is selected CL_SEL is in the high impedance state (pull-up to VDDIO required).

5.5 Thermal shutdown and temperature control

The ST75MM performs an automatic shutdown of the power amplifier circuitry when the internal temperature exceeds T_TH4. After a thermal shutdown event, the temperature must get below T_TH3 before the ST75MM power amplifier comes back to operation.

Moreover, a digital thermometer is embedded to identify the internal temperature in four zones, as indicated in *Table 8*.

Table 8. Temperature zones

Temperature zone	Temperature value
1	T < T_TH1
2	T_TH1 < T < T_TH2
3	T_TH2 < T < T_TH3
4	T > T_TH3

5.6 Zero-crossing comparator

The ST75MM embeds an analog comparator with hysteresis, used for optional zero-crossing detection and synchronization. It requires a bipolar (ac) analog input signal, synchronous to the mains voltage.

6 Power management

Figure 8 shows the power supply structure for the ST75MM. The ST75MM operates from three external supply voltages:

- VCC (8 to 18 V) for the power amplifier and the analog section
- VDDIO (3.3 or 5 V) for interface lines and digital blocks
- VDDIO_FLASH (3.3 V) for the external Flash memory SPI interface

If no external Flash memory is connected, VDDIO_FLASH must be connected to VDDIO.

Two internal linear regulators provide the remaining required voltages:

- 5 V analog front end supply: generated from the VCC voltage and connected to the VCCA pin
- 1.8 V digital core supply: generated from the VDDIO_FLASH voltage and connected to VDD_REG_1V8 (direct regulator output) and VDD pins

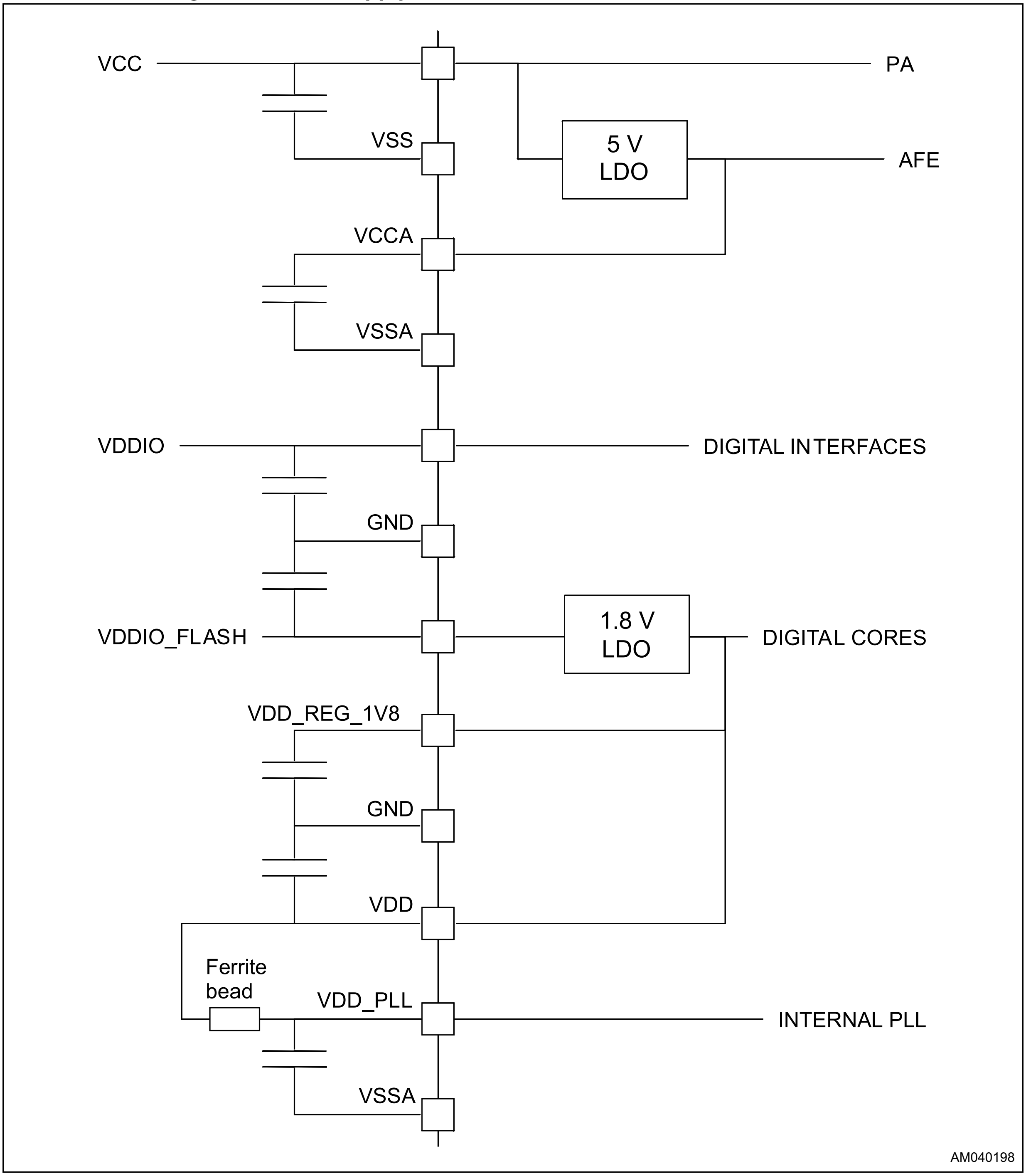
The VDD_PLL pin, supplying the internal clock PLL, must be externally connected to VDD through a ferrite bead for noise filtering purposes.

All supply voltages must be properly filtered to their respective ground, using external capacitors close to each supply pin, in accordance with the supply scheme depicted in *Figure 8*.

Note that the internal regulators connected to VDD_REG_1V8 and to VCCA are not designed to supply external circuitry; its output is externally accessible for the filtering purpose only.

External connections between all VDD pins are not required, since they are already internally connected.

Figure 8. Power supply internal scheme and external connections



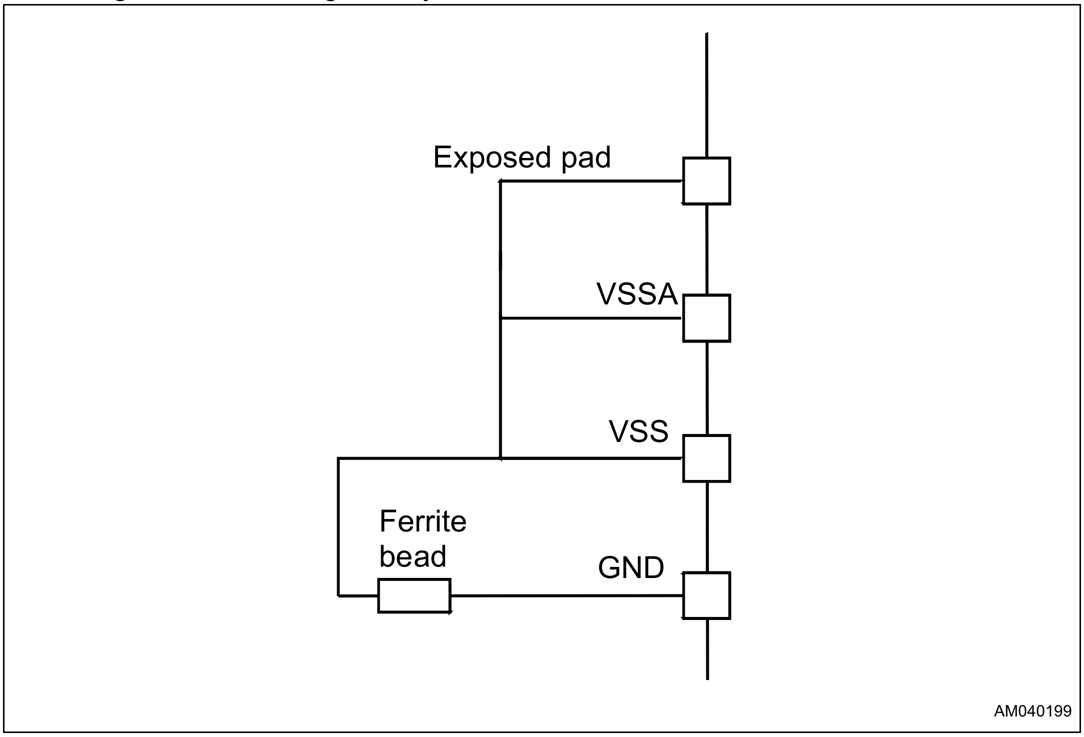
Ground connections

The ST75MM presents analog and digital ground connections. In particular, VSS is the power ground, VSSA is the analog ground, while GND pins refer to digital ground.

It is recommended to provide external connections among the ground pins as follows:

- GND pins 6, 14, 33 and 45 are connected together
- VSSA pins 15 and 35 are connected to the exposed pad
- VSS is also connected to the exposed pad
- Connection between VSSA and GND is provided through a ferrite bead

Figure 9. ST75MM ground pins and recommended external connections



7 Clock management

The main clock source is an 8-MHz crystal connected to the internal oscillator through XIN and XOUT pins. Both XIN and XOUT pins have a 32-pF integrated capacitor, in order to drive a crystal having a load capacitance of 16 pF with no additional components.

Alternatively, an 8-MHz external clock can be directly supplied to the XIN pin, leaving XOUT floating.

A PLL internally connected to the output of the oscillator generates the f_{CLK_PHY}, required by the PHY processor block engine. f_{CLK_PHY} is then divided by two to obtain $f_{CLK\_PROTOCOL}$, required by the protocol controller.

8 Functional overview

8.1 Bootloader routine

The ST75MM program ROM contains a bootloader routine, executed by the 8051 processor after any reset event.

8.2 Start-up sequence

During the start-up phase of the ST75MM (following a power-on, HW or SW reset event), the status of I^2C/UART, BOOT0/PHY_ACT and BOOT1 pins is checked, influencing the device behavior according to the following tables.

Note: The boot mode with BOOT0/PHY_ACT = 0 is required for standard use.

Table 9. Host interface selection

Line	Logical level	Host interface	Reference configuration
I^2C/UART	0	UART port selected as host interface	Connect to GND
	1	I^2C port selected as host interface	

Table 10. Boot memory selection

Line	Logical level	Boot source	Reference configuration
BOOT0/PHY_ACT	0	Boot from internal ROM	Connect to GND
	1	Boot from external Flash (ST RESERVED USE)	

Table 11. BOOT1 configuration

Line	Logical level	Boot sector	Reference configuration
BOOT1	x	No effect if BOOT0/PHY_ACT set to 0	Pull-up to VDDIO

The ST75MM device embeds a ROM memory containing the METERS AND MORE protocol stack for turnkey implementation of a METERS AND MORE compliant node.

An SPI dedicated interface is available for connecting an external Flash memory, for ST reserved use. It is not required to include it when designing an ST75MM application.

8.3 PHY activity signaling

After the start-up phase, the modem status will be signaled according to *Table 12*.

Table 12. PHY activity status

Signal	Logical level	Condition
BOOT1/TX_ON	1	No transmission ongoing
	0	Modem in transmission state
PHY_ACT	1	Modem in passive reception state
	0	Modem in active reception or transmission state

The PHY_ACT signal is available on one of the two pins BOOT0/PHY_ACT or BiU/PHY_ACT based on the host interface selection pin (I^2C/UART), according to *Table 13*.

Table 13. PHY_ACT pin selection

Line	Logical level	PHY_ACT mapping
I2C/UART	1	BOOT0/PHY_ACT pin is used to signal PHY activity
	0	BiU/PHY_ACT pin is used to signal PHY activity

The BiU/PHY_ACT pin has also the function to signal the band-in-use event, defined according to the EN 50065-1 specifications for the 125-kHz - 140-kHz (CENELEC-C) band, if the band-in-use detection is active and the signaling is enabled.

9 Carrier sense multiple access algorithm

The ST75MM power line modem implements the CENELEC access protocol (CSMA), as defined in the EN50065-1 regulation, making it the ideal choice for applications running in the 125-kHz to 140-kHz band (CENELEC-C sub-band).

The CSMA algorithm implemented in the ST75MM power line modem has a high degree of reconfigurability, among the other parameters it is possible to define:

- The source of band-in-use signal (either received signal strength or METERS AND MORE useful communication)
- The number of CSMA time slots
- The duration of each CSMA time slot.

10 PLC protocol

10.1 Introduction

The ST75MM implements the METERS AND MORE protocol over power line medium as it is specified by the METERS AND MORE Association A.I.S.B.L, relevant documentation can be found accessing the Association web site.

10.2 Physical layer

The ST75MM implements the METERS AND MORE physical layer services, further information can be found at the METERS AND MORE Association web site:

- www.metersandmore.com

10.3 Data link layer

The ST75MM implements the METERS AND MORE data link layer services, further information can be found at the METERS AND MORE Association web site:

- www.metersandmore.com.

11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

11.1 VFQFPN48 (7 x 7 x 1.0 mm) package information

The ST75MM is hosted in a 48-pin thermally enhanced, very thin, fine pitch quad flat package no lead (VFQFPN) with the exposed pad, which allows the device dissipating the heat that is generated by the operation of the two linear regulators and the power amplifier.

Figure 10. VFQFPN48 (7 x 7 x 1.0 mm) package outline

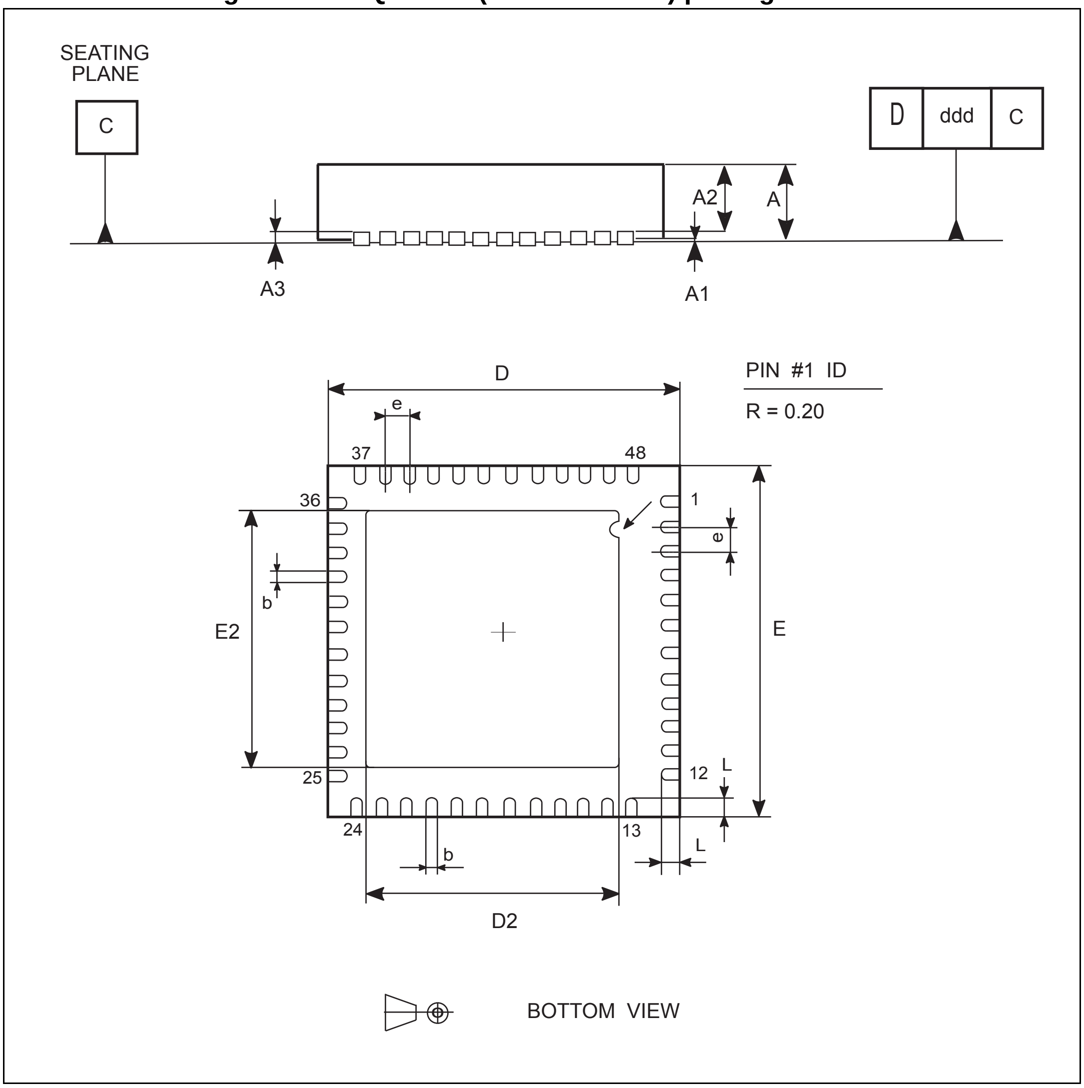


Table 14. VFQFPN48 (7 x 7 x 1.0 mm) package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	-	0.02	0.05
A2	-	0.65	1.00
A3	-	0.25	-
B	0.18	0.23	0.30
D	6.85	7.00	7.15
D2	4.95	5.10	5.25
E	6.85	7.00	7.15
E2	4.95	5.10	5.25
e	0.45	0.50	0.55
L	0.30	0.40	0.50
ddd	-	0.08	-

12 Revision history

Table 15. Document revision history

Date	Revision	Changes
18-Oct-2017	1	Initial release.