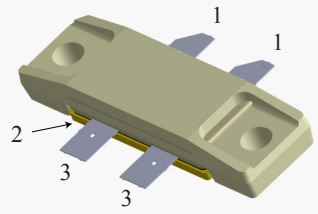
# STAC3932B

Datasheet

## HF/VHF/UHF RF power N-channel MOSFET




STAC780-4B

| Pin connection | |
|---|---|
| **Pin** | **Connection** |
| 1 | Drain |
| 2 | Source (bottom side) |
| 3 | Gate |

## Features

| Order code | Frequency | $V_{DD}$ | $P_{OUT}$ | Gain | Efficiency |
|---|---|---|---|---|---|
| STAC3932B | 123 MHz | 100 V | 580 W | 24.6 dB | 70 % |

- Excellent thermal stability
- Common source push-pull configuration
- $P_{OUT}$ = 580 W typ. with 24.6 dB gain at 123 MHz
- In compliance with the 2002/95/EC European directive
- ST air-cavity STAC packaging technology

## Description

The STAC3932B is an N-channel MOS field-effect RF power transistor. It is intended for use in 100 V DC large signal applications up to 250 MHz.

| Product status |
|---|
| STAC3932B |

| Product summary | |
|---|---|
| **Order code** | STAC3932B |
| **Marking** | STAC3932 |
| **Package** | STAC780-4B |
| **Packing** | Box |
| **Base / Bulk qty** | 20 / 80 |

# 1 Electrical data

## 1.1 Maximum ratings

**Table 1. Absolute maximum ratings ($T_{CASE}$ = 25 °C)**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{(BR)DSS}$ (1) | Drain source voltage | 250 | V |
| $V_{DGR}$ | Drain-gate voltage ($R_{GS}$ = 1 MΩ) | 250 | V |
| $V_{GS}$ | Gate-source voltage | ±20 | V |
| $I_D$ | Drain current | 20 | A |
| $P_{DISS}$ | Power dissipation | 625 | W |
| $T_J$ | Maximum operating junction temperature | 200 | °C |
| $T_{STG}$ | Storage temperature range | -65 to +150 | °C |

*1. $T_J$ = 150 °C*

## 1.2 Thermal data

**Table 2. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thJC}$ | Junction - case thermal resistance | 0.28 | °C/W |

## 1.3 ESD protection characteristics

**Table 3. ESD protection**

| Symbol | Test Methodology | Class |
|---|---|---|
| HBM | Human Body Model (per JESD22-A114) | 2 |

# 2 Electrical characteristics

$T_{CASE}$ = +25 °C (unless otherwise specified)

## 2.1 Static

**Table 4. Static**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain - Source Breakdown voltage | $V_{GS}$ = 0 V, $I_{DS}$ = 100 mA, $T_J$ = 150 °C | 250 | | | V |
| $I_{DSS}$ | Zero gate voltage drain leakage current | $V_{GS}$ = 0 V, $V_{DS}$ = 100 V | | | 1 | mA |
| $I_{GSS}$ | Gate - Source leakage current | $V_{GS}$ = 20 V, $V_{DS}$ = 0 V | | | 250 | nA |
| $V_{DS(ON)}$ | Drain - Source on voltage | $V_{GS}$ = 10 V, $I_D$ = 5 A | | 2.5 | 3.5 | V |
| $V_{TH}$ | Gate - Source threshold voltage | $I_{DS}$ = 250 mA | 2.0 | | 4.0 | V |
| $G_{FS}$ | Forward transconductance | $V_{DS}$ = 10 V, $I_D$ = 2.5 A | 3.0 | | 5.0 | S |
| $C_{ISS}$ | Input capacitance | $V_{GS}$ = 0 V, $V_{DS}$ = 100 V, f = 1 MHz | | 492 | | pF |
| $C_{OSS}$ | Ouput capacitance | | | 134 | | pF |
| $C_{RSS}$ | Reverse transfer capacitance | | | 5.2 | | pF |

## 2.2 Dynamic

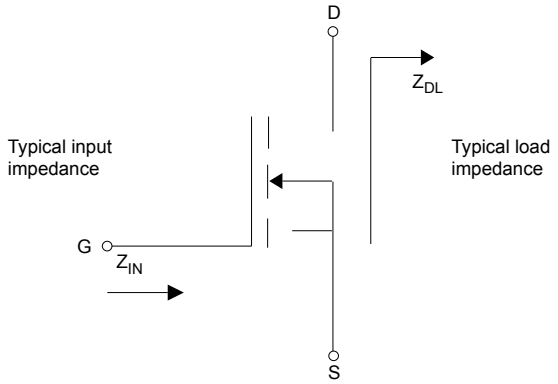
**Table 5. Dynamic (1)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $P_{OUT}$ | Output power | CW, $P_{IN}$ = 2 W | 450 | 580 | - | W |
| $P_{OUT}$ | Output power | Pulse PW = 1 ms, DC = 10 % , $P_{IN}$ = 8 W | | 900 | - | W |
| $\eta_D$ | Drain efficiency | CW, $P_{IN}$ = 2 W | | 70 | - | % |
| $\eta_D$ | Drain efficiency | Pulse PW = 1 ms, DC = 10 % , $P_{IN}$ = 8 W | | 65 | - | % |

1. *$V_{DD}$ = 100 V, $I_{DQ}$ = 2 x 250 mA, f = 123 MHz*

# 3 Impedances

**Figure 1. Impedance data**




*Note: Measured gate-to-gate and drain-to-drain, respectively (balanced configuration).*

**Table 6. Impedance data**

| Frequency | $Z_{IN}$ (Ω) | $Z_{DL}$(Ω) |
|---|---|---|
| 123 MHz (pulse) | 1.0 - j 4.80 | 6.3 + j 10.5 |
| 123 MHz (CW) | 0.8 - j 3.45 | 5.0 + j 13.0 |
| 64 MHz (pulse) | 1.4 - j 10.0 | 12.8 + j 14.0 |

# 4 Typical performance

**Figure 2. Capacitances vs drain supply voltage**

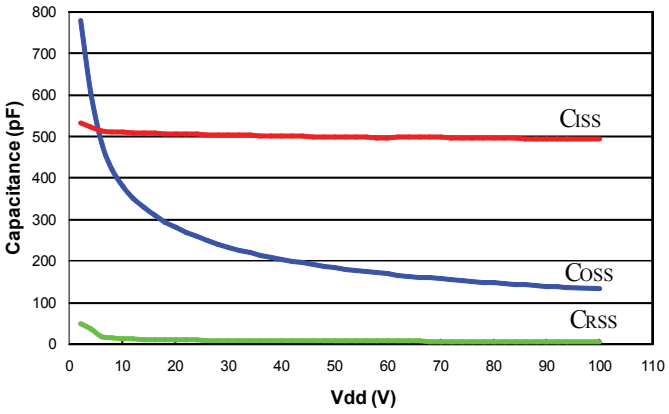



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**Figure 3. Safe operating area**

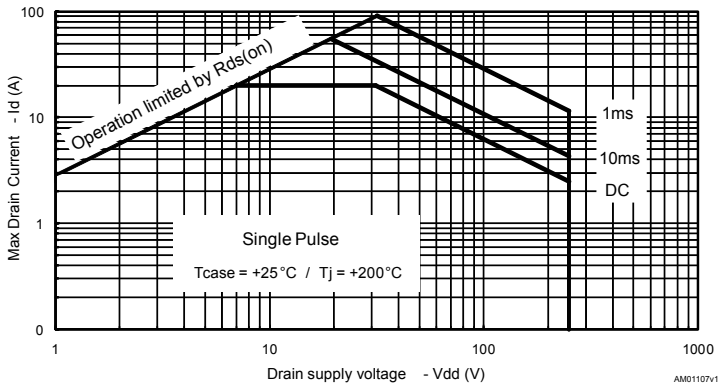

Figure 4. **Transient thermal impedance**

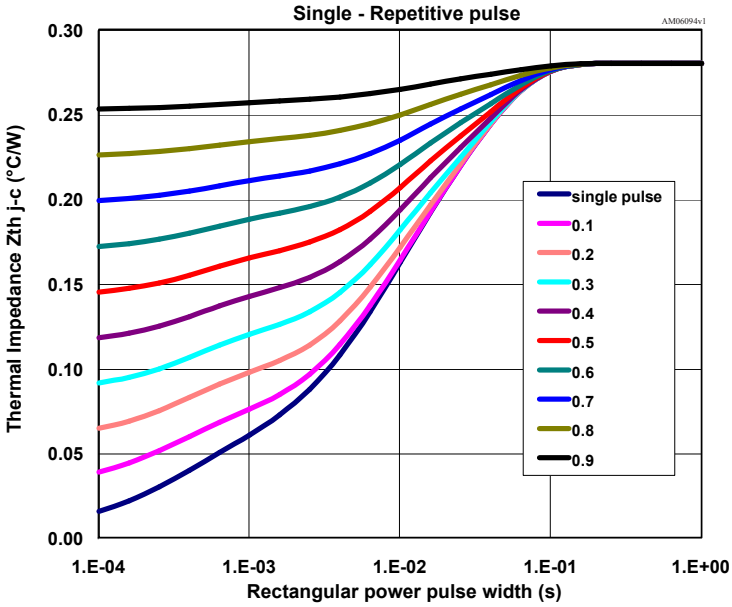


Figure 5. **Transient thermal model**

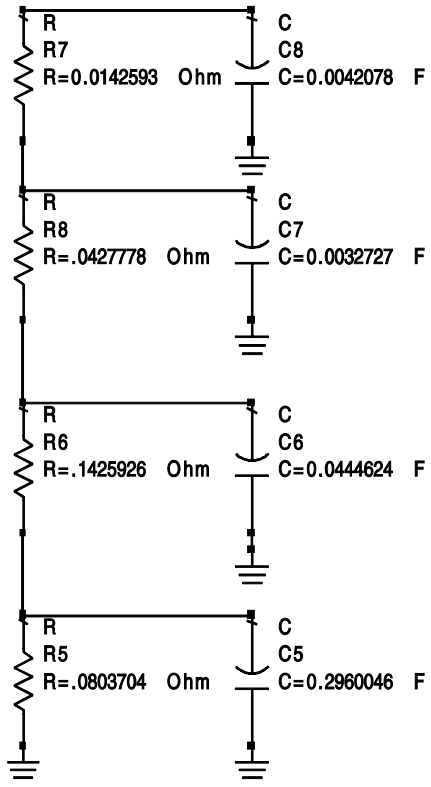


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Figure 6. **Zero temperature coefficient point**

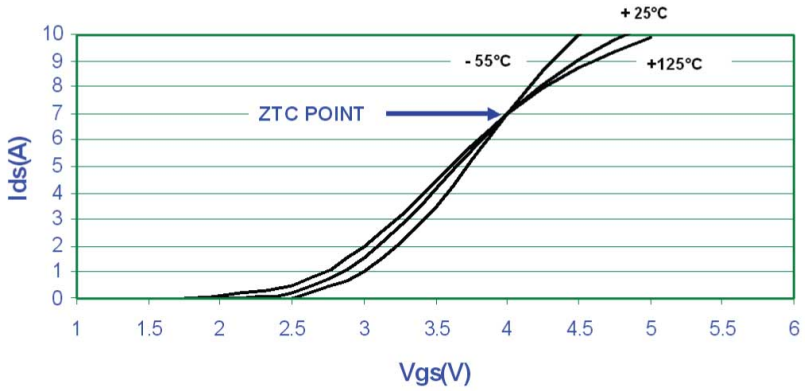


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Figure 7. **Output power and efficiency vs input power (CW)**

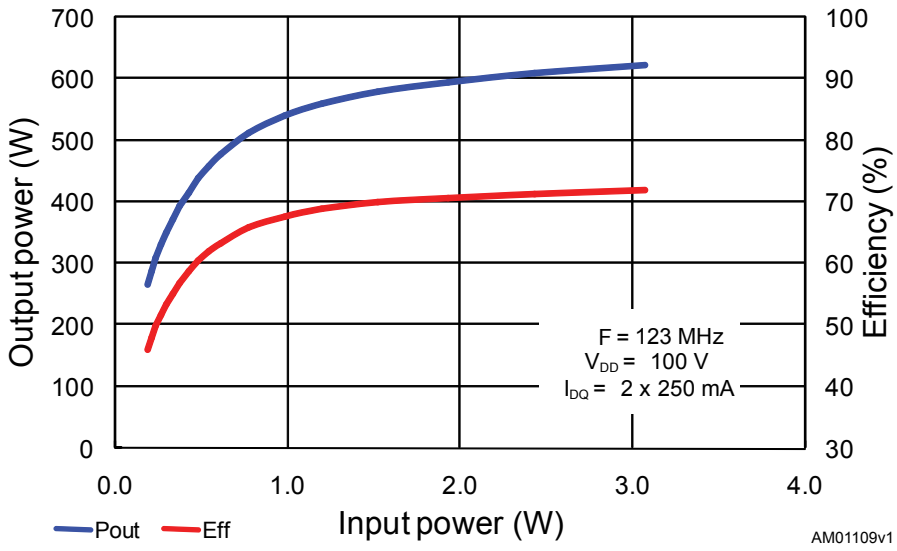


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Figure 8. **Gain vs output power (CW)**

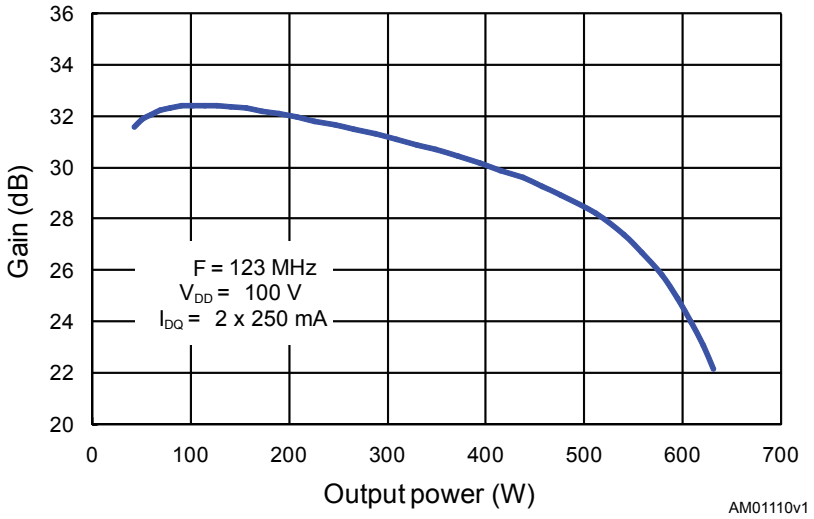
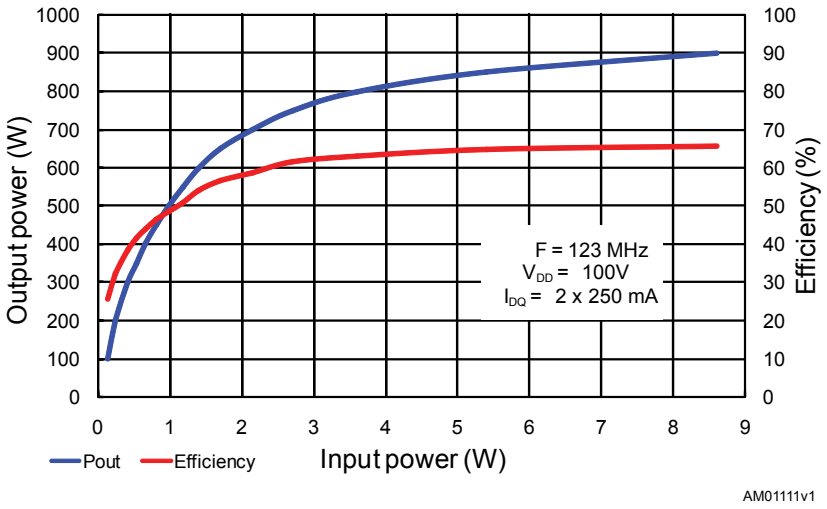



Figure 9. **Output power and efficiency vs input power (PW = 1 ms, DC = 10%)**



# 5 Test circuit

## 5.1 Electrical schematic and BOM

**Figure 10. Electrical schematic**

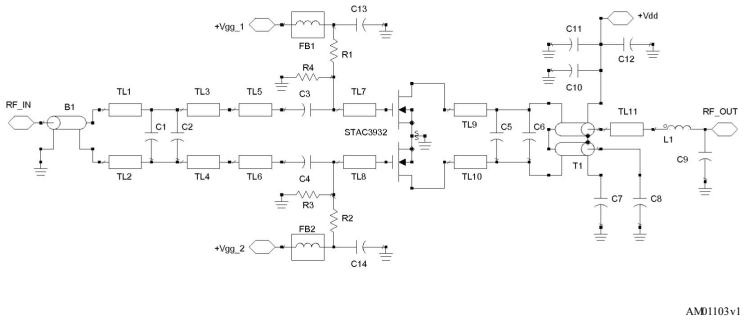



**Table 7. Bill of materials**

| Component | Description |
|---|---|
| C1 | 270 pF ATC 100B chip capacitor |
| C2 | 180 pF ATC 100B chip capacitor |
| C3, C4 | 750 pF ATC 700B chip capacitor |
| C5, C8 | 43 pF ATC 100B chip capacitor |
| C6 | 20 pF ATC 100B chip capacitor |
| C7 | 1000 pF ATC 100C chip capacitor |
| C9 | 5.6 pF ATC 100B chip capacitor |
| C10 | 2200 pF ATC 100C chip capacitor |
| C11 | 470 pF ATC 100B chip capacitor |
| C12 | 100 µF, 200 V electrolytic capacitor |
| C13, C14 | 1200 pF ATC 700B chip capacitor |
| R1, R2 | 15 Ω 1/4 W chip resistor |
| R3, R4 | 30 Ω 1/4 W axial lead resistor |
| L1 | 3 turns, 16 ga magnet wire, Id 3/8", .165" turn spacing, 78 nH |
| FB1, FB2 | ferrite bead, Fair-Rite # 2743019447 |
| B1 | 1/4 λ balun transformer, RG316-25 Ω ,16.5" |
| T1 | 20 ga teflon coated wire thru 4 copper tubes OD 1/8"x 1.5" |
| TL1, TL2 | 0.740" x 0.200" microstrip |
| TL3, TL4 | 0.360" x 0.200" microstrip |
| TL5, TL6 | 0.480" x 0.350" microstrip |
| TL7, TL8 | 0.220" x 0.350" microstrip |
| TL9, TL10 | 0.350" x 0.660" microstrip |
| TL11 | 0.415" x 0.200" microstrip |
| Board | 0.062" FR-4 |

## 5.2 Board and layout

Figure 11. **Test circuit PCB photo**

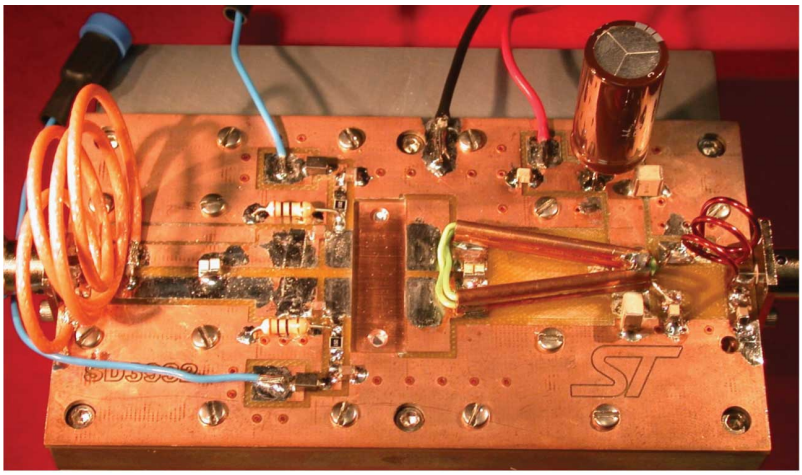


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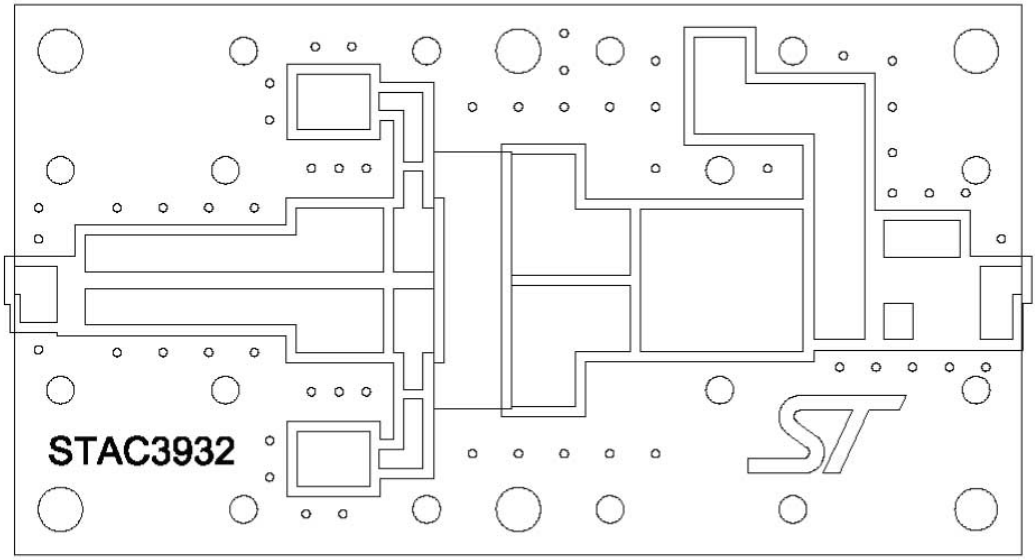
Figure 12. **Test circuit layout**

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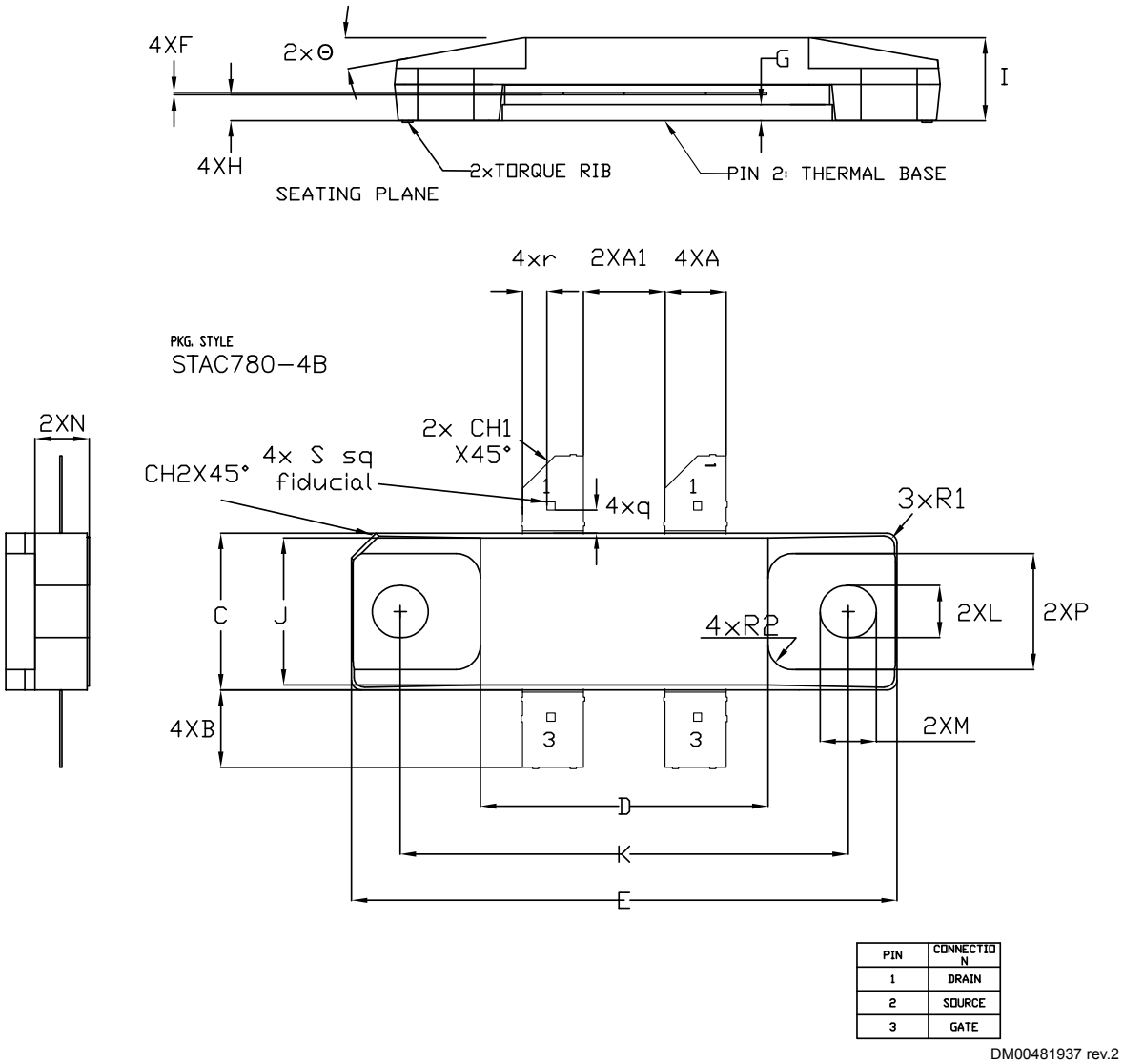
# 6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

## 6.1 STAC780-4B package information

Figure 13. **STAC780-4B package outline**



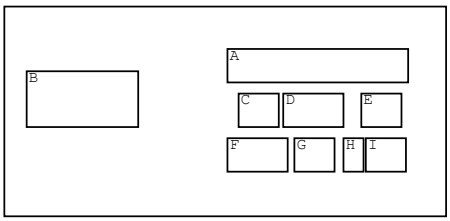

DM00481937 rev.2

Table 8. **STAC780-4B mechanical data**

| Symbol | Milimeters | | |
|---|---|---|---|
| | Min | Typ | Max |
| A | 3.76 | | 3.86 |
| A1 | 5.03 | | 5.13 |
| B | 4.57 | | 5.08 |
| C | 9.65 | | 9.91 |
| D | 17.78 | | 18.08 |
| E | 33.88 | | 34.19 |
| F | 0.13 | | 0.18 |
| G | 0.97 | | 1.14 |
| H | 1.52 | | 1.70 |
| I | 4.83 | | 5.33 |
| J | 9.52 | | 9.78 |
| K | 27.69 | | 28.19 |
| L | 3.20 | 3.25 | 3.30 |
| M | 3.43 | 3.51 | 3.58 |
| M | 3.30 | 3.38 | 3.45 |
| p | 7.14 | 7.21 | 7.29 |
| q | | 1.45 | |
| R1 | | 0.64 | |
| R2 | | 1.52 | |
| r | | 1.52 | |
| s | | 0.51 | |
| Θ | | 10° | |
| CH1 | | 2.03 | |
| CH2 | | 1.52 | |

## 6.2 Marking information

**PACKAGE FACE** : TOP




LEGEND

☐ Marking Composition Field

A - MARKING AREA
B - ST LOGO
C - Assy Plant
(PP)
D - BE Sequence
(LLL)
E - Diffusion Traceability Plant
(WX)
F - COUNTRY OF ORIGIN
(MAX CHAR ALLOWED = 3)
G - Test & Finishing Plant
(TF)
H - Assy Year
(Y)
I - Assy Week
(WW)

## Revision history

Table 9. **Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 06-Mar-2009 | 1 | First release. |
| 18-Feb-2010 | 2 | Updated description on cover page. |
| 16-Mar-2010 | 3 | Updated Figure 7: Maximum safe operating area.<br>Added Figure 8: Transient thermal impedance. and Figure 9: Transient thermal model. |
| 06-Jul-2011 | 4 | Updated Chapter 7: Package mechanical data.<br>Added Chapter 8: Marking, packing and shipping specifications. |
| 22-Sep-2011 | 5 | Update values for L and M in Table 9: STAC244B mechanical data. |
| 01-Jul-2013 | 6 | Modified pin labeling in Figure 1: Pin connection.<br>Minor text corrections throughout document. |
| 03-Apr-2020 | 7 | Updated package information. Added *Section 1.3 ESD protection characteristics*. |
| 14-Jul-2020 | 8 | Modified Table 4. Static. |

# Contents