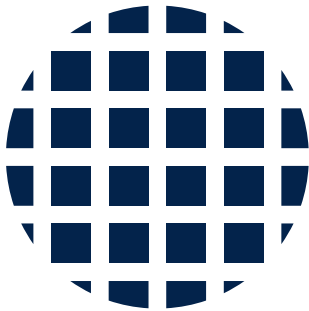


High voltage half-bridge gate driver for GaN transistors



Features

- dV/dt immunity ± 200 V/ns
- Driver current capability:
 - 1.3/2.4 A source/sink typ @ 25 °C, 6 V
 - 5.5/6 A source/sink typ @ 25 °C, 15 V
- Separated turn on and turn off gate driver pins
- 45 ns propagation delay with tight matching
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- Interlocking function
- UVLO on low-side and high-side sections
- Dedicated pin for shut down functionality
- Over temperature protection

Applications

- High-voltage PFC, DC-DC and DC-AC converters
- Switch-mode power supplies
- UPS systems
- Solar power
- Motor driver for home appliances, factory automation and industrial drives.

Product status link

STDRIVEG600W wafer

Description

The **STDRIVEG600W** is a single chip half-bridge gate driver for Enhancement mode GaN FETs or N-channel power MOSFET.

The high-side section is designed to stand a voltage up to 600 V and is suitable for designs with bus voltage up to 500 V.

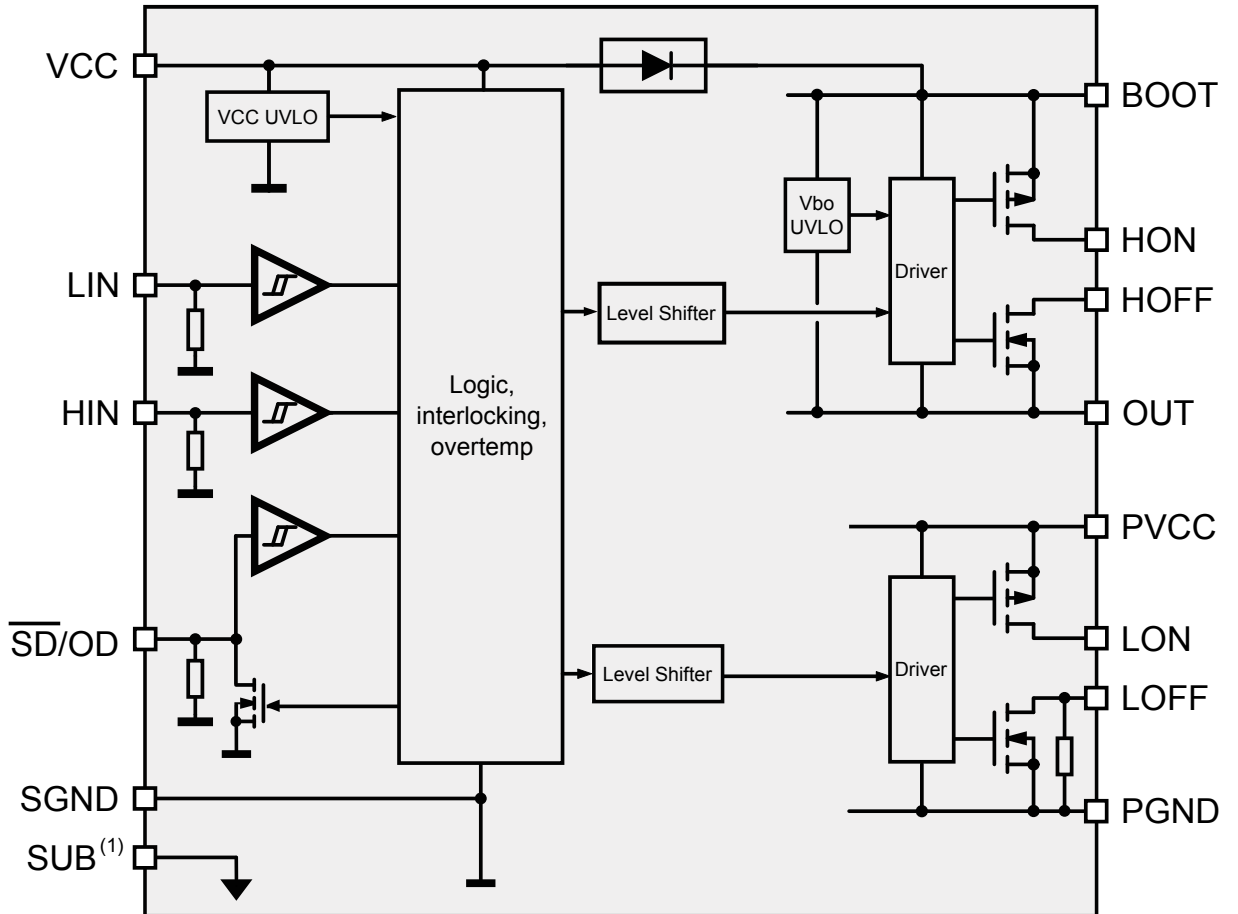
The device is designed for driving high-speed GaN and Si FETs thanks to high current capability, short propagation delay and operation with supply voltage down to 5 V.

The **STDRIVEG600W** features UVLO protection on both the lower and upper driving sections, preventing the power switches from operating in low efficiency or dangerous conditions, and the interlocking function avoids cross-conduction conditions.

The logic inputs are CMOS/TTL compatible down to 3.3 V for easy interfacing with microcontroller and DSP.

1 Block diagram

Figure 1. STDRIVEG600W block diagram



Note: SUB is die back side, it is not a PAD.

2 Pad description

Table 1. Pad description

Pad #	Pad Name	Type	Function
1	LIN	I	Low-side driver logic input (active high)
2	$\overline{\text{SD/OD}}$	I	Shut down logic input (active low); open-drain output signals overtemperature protection
3	HIN	I	High-side driver logic input (active high)
4	VCC	P	Logic supply voltage
5	PVCC	P	Low-side driver supply voltage
7	SGND	P	Signal ground
9	PGND	P	Low-side driver ground
10	LOFF	O	Low-side driver sink output
11	LON	O	Low-side driver source output
13	OUT	P	High-side (floating) common voltage
14	HOFF	O	High-side driver sink output
15	HON	O	High-side driver source output
16	BOOT	P	Bootstrap supply voltage
6, 8, 12	RES	-	Reserved. Do not connect, leave pad floating
-	SUB	P	Substrate (die back side). Die must be attached with a high electrically conductive glue on a frame tied to SGND.

Note: for more details refer to [Section 8 Pad position](#)

3 Electrical data

3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value ⁽¹⁾		Unit
		Min.	Max.	
VCC	Logic supply voltage	-0.3	21	V
V _{PG} ⁽²⁾	Low-side driver supply voltage	-0.3	21	V
VCC-PGND	Logic supply vs. Low-side driver ground	-0.3	21	V
PVCC	Low-side driver supply vs. logic ground	-0.3	21	V
PGND	Low-side driver ground vs. logic ground	-21	21	V
V _{BO} ⁽³⁾	High-side supply voltage	-0.3	21	V
BOOT	Bootstrap voltage	-0.3	620	V
V _{HS}	High-side gate output voltage (HON, HOFF)	OUT - 0.3	BOOT + 0.3	V
V _{LS}	Low-side gate output voltage (LON, LOFF)	PGND - 0.3	PVCC + 0.3	V
V _i	Logic input pins voltage (LIN, HIN, \overline{SD}/OD)	-0.3	21	V
dV _{OUT} /dt	Output slew rate ⁽⁴⁾	-	200	V/ns
T _J	Junction temperature	-40	150	°C
T _{stg}	Storage temperature	-55	150	°C

1. Each voltage referred to SGND unless otherwise specified
2. $V_{PG} = PVCC - PGND$
3. $V_{BO} = BOOT - OUT$
4. See [Figure 13](#) (characterization done on SO16 discrete package)

3.2 Recommended operating conditions

Table 3. Recommended operating conditions

Symbol	Pin	Parameter	Test conditions	Value ⁽¹⁾		Unit
				Min.	Max.	
VCC	4 vs. 7	Logic Supply voltage	-	4.75	20	V
V _{PG} ⁽²⁾	5 vs. 9	Low-side driver supply voltage	-	4.75	20	V
VCC-PGND	4 vs. 9	Logic supply vs. LS driver ground	-	0	20	V
VCC-PVCC	4 vs. 5	Logic supply vs. LS driver supply	-	-3	3	V
PVCC	5 vs. 7	Low-side supply pin	-	3	20	V
PGND	9 vs. 7	Low-side driver ground	-	-5	5	V
V _{BO} ⁽³⁾	16 vs. 13	Floating supply voltage	-	4.4	20	V
OUT	13 vs. 7	DC output voltage	-	-15 ⁽⁴⁾	520	V
BOOT	16 vs. 7	Bootstrap voltage	-	0 ⁽⁵⁾⁽⁶⁾	530	V
V _i	1,2,3	Logic input voltage	-	0	20	V
f _{sw}	-	Switching frequency ⁽⁷⁾	-	-	1	MHz
T _J	-	Junction temperature	-	-40	125	°C

1. Each voltage referred to SGND unless otherwise specified
2. $V_{PG} = PVCC - PGND$
3. $V_{BO} = BOOT - OUT$
4. $VCC = 5\text{ V}$, $V_{BO} = 20\text{ V}$
5. BOOT must be $\geq 5\text{ V}$ to propagate high-side commands. Refer to [Section 5.4.2](#)
6. Actual limit could be limited by bootstrap diode dissipation
7. Actual limit depends on power dissipation constraints.

4 Electrical characteristics

Test conditions:

 VCC = PVCC = 6 V, PGND = SGND, V_{BO} = 6 V; LON = LOFF, HON = HOFF; T_J = +25 °C, unless otherwise specified

Table 4. Electrical characteristics

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
Logic section supply							
VCC _{thON}	4	VCC UV turn ON threshold	-	4.2	4.5	4.75	V
VCC _{thOFF}		VCC UV turn OFF threshold	-	3.9	4.2	4.5	V
VCC _{hys}		VCC UV hysteresis	-	0.2	0.3	0.45	V
I _{QVCCU}		VCC Undervoltage quiescent supply current	VCC = PVCC = 3.8 V	-	320	410	μA
I _{QVCC}		VCC quiescent supply current	$\overline{SD}/OD = LIN = 5 V$; HIN = 0 V; OUT = 6 V	-	680	900	μA
I _{SVCC}		VCC switching supply current	$\overline{SD}/OD = 5 V$; f _{sw} = 500 kHz; LIN = not HIN; OUT = 6 V	-	800	-	μA
Low-side driver section supply ⁽¹⁾							
I _{QPCC}	5	PVCC quiescent current	$\overline{SD}/OD = LIN = 5 V$; HIN = 0 V	-	75	120	μA
I _{SPCC}		PVCC switching supply current	f _{sw} = 500kHz; No load ⁽²⁾	-	390	-	μA
High-side floating section supply ⁽³⁾							
V _{BOthON}	16 - 13	V _{BO} UV turn ON threshold	-	3.6	4.0	4.4	V
V _{BOthOFF}		V _{BO} UV turn OFF threshold	-	3.4	3.7	4.0	V
V _{BOhys}		V _{BO} UV hysteresis	-	0.1	0.3	0.5	V
I _{QBOU}		Undervoltage V _{BO} quiescent current	VCC = PVCC = V _{BO} = 3.4 V	-	140	200	μA
I _{QBO}	V _{BO} quiescent current	$\overline{SD}/OD = HIN = 5 V$; LIN = 0 V; OUT = 6 V	-	160	210	μA	
I _{SBO}	-	BOOT switching supply current	f _{sw} = 500 kHz; No load; OUT = 20 V ⁽²⁾	-	1100	-	μA
I _{LK}	13, 14 15, 16	High voltage leakage current	HON = HOFF = OUT = BOOT = 600 V; LIN = 0 V	-	-	11	μA
Bootstrap structure							
R _{Dboot}	4 - 16	Bootstrap diode on resistance	LIN = $\overline{SD}/OD = 5 V$; HIN = 0 V;	100	140	170	Ω

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
			OUT = BOOT = 5.5 V				
Output driving buffers							
I _{SO}	15, 11	High/low-side source short circuit current	V _{PG} = V _{BO} = 15 V ⁽²⁾	4	5.5	7.5	A
			V _{PG} = V _{BO} = 6 V ⁽²⁾	1	1.3	1.9	
			V _{PG} = V _{BO} = 6 V; T _J = -40 to +125°C ⁽²⁾	0.75	-	2.5	
I _{SI}	14, 10	High/low-side sink short circuit current	V _{PG} = V _{BO} = 15 V ⁽²⁾	4.5	6	8	A
			V _{PG} = V _{BO} = 6 V ⁽²⁾	1.9	2.4	3	
			V _{PG} = V _{BO} = 6 V; T _J = -40 to +125°C ⁽²⁾	1.4	-	3.7	
R _{DSonON}	15, 11	High/low-side source R _{DSon}	I = 10 mA; V _{PG} = V _{BO} = 15 V ⁽²⁾	0.9	1.25	1.7	Ω
			I = 10 mA; V _{PG} = V _{BO} = 6 V ⁽²⁾	1.3	2	2.4	
			I = 10 mA; V _{PG} = V _{BO} = 6 V; T _J = -40 to +125°C ⁽²⁾	1	-	3.4	
R _{DSonOFF}	14, 10	High/low-side sink R _{DSon}	I = 10 mA; V _{PG} = V _{BO} = 15 V ⁽²⁾	0.65	0.9	1.25	Ω
			I = 10 mA, V _{PG} = V _{BO} = 6 V ⁽²⁾	0.85	1.2	1.55	
			I = 10 mA; V _{PG} = V _{BO} = 6 V; T _J = -40 to +125°C ⁽²⁾	0.7	-	2.2	
R _{BLEED}	10, 9	LS gate bleeder resistor	-	75	100	125	kΩ
Logic inputs							
V _{ih}	1, 2, 3	High level logic threshold voltage	T _J = 25 °C	2	2.17	2.5	V
			T _J = -40 to +125°C ⁽²⁾	-	-	2.7	
V _{il}	1, 2, 3	Low level logic threshold voltage	T _J = 25 °C	1.1	1.31	1.45	V
			T _J = -40 to +125°C ⁽²⁾	0.8	-	-	
V _{hyst}		Logic input threshold hysteresis	-	0.7	0.86	1.2	V
I _{INh}	1, 3	LIN, HIN logic "1" input bias current	LIN = HIN = 5 V	23	33	55	μA
I _{INl}		LIN, HIN logic "0" input bias current	LIN = HIN = 0 V	-	-	1	μA
R _{PD_IN}		LIN, HIN pull-down resistor	-	90	150	220	kΩ
I _{SDh}	2	\overline{SD}/OD logic "1" input bias current	\overline{SD}/OD = 5 V	11	15	20	μA
I _{SDl}		\overline{SD}/OD logic "0" input bias current	\overline{SD}/OD = 0 V	-	-	1	μA
R _{PD_SD}		\overline{SD}/OD pull-down resistor	-	250	330	450	kΩ
V _{TSD}		Thermal shutdown unlatch threshold	T _J = 25 °C	0.5	0.75	1.0	V
R _{ON_OD}		\overline{SD}/OD on resistance	T _J = 25 °C;	8	10	18	Ω

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
I _{OL_OD}	2		$\overline{SD}/OD = 400 \text{ mV}$				
		\overline{SD}/OD low level sink current	T _J = 25 °C; $\overline{SD}/OD = 400 \text{ mV}$	22	40	50	mA
Over temperature protection							
T _{TSD}	-	Shutdown temperature	(2)	150	175	200	°C
T _{HYS}	-	Temperature hysteresis	(2)	17	20	23	°C
Dynamic characteristics (4)							
t _{on}	1, 3 vs. 10=11	High/low-side driver turn-on propagation delay	OUT = 0 V; LIN, HIN: 0 to 3.3 V;	30	45	60	ns
t _{off}	and 14=15	High/low-side driver turn-off propagation delay	Pulse width > 120 ns; No load	30	45	60	ns
t _r	10=11	Rise time	C _L = 1 nF	-	7	-	ns
t _f	14=15	Fall time		-	5	-	ns
MT	1, 3 vs. 10=11 and 14=15	Delay matching high/low-side turn-on/off ⁽⁵⁾	OUT = 0 V; LIN, HIN: 0 to 3.3 V; Pulse width > 120 ns; No load	-	0	10	ns
t _{SDon}	2 vs. 10=11	High/low-side driver turn-on propagation delay	OUT = 0 V; SD/OD: 0 to 3.3 V;	30	45	60	ns
t _{SDoff}	and 14=15	High/low-side driver turn-off propagation delay	Pulse width > 120 ns; No load	30	45	60	ns

1. V_{PG} = PVCC - PGND

2. Values by characterization data, not tested in production

3. V_{BO} = BOOT - OUT

4. See Figure 12

5. $MT = \max(|t_{on}(LON/LOFF) - t_{off}(LON/LOFF)|, |t_{on}(HON/HOFF) - t_{off}(HON/HOFF)|, |t_{off}(LON/LOFF) - t_{on}(HON/HOFF)|, |t_{off}(HON/HOFF) - t_{on}(LON/LOFF)|)$

5 Functional description

5.1 Logic inputs

The STDRIVEG600W is a half-bridge gate driver with three logic inputs to control the external high-side and low-side power transistors.

The device is controlled through following logic inputs:

- \overline{SD}/OD : Shut-down input, active low;
- LIN: low-side driver inputs, active high;
- HIN: high-side driver inputs, active high.

Table 5. Truth table (applicable when the device is not in UVLO)

Inputs			Outputs	
\overline{SD}/OD	LIN	HIN	LON = LOFF	HON = HOFF
L	X ⁽¹⁾	X ⁽¹⁾	L	L
H	L	L	L	L
H	L	H	L	H
H	H	L	H	L
H	H	H	L ⁽²⁾	L ⁽²⁾

1. X: Don't care.

2. Interlocking function

The logic inputs have internal pull-down resistors. The purpose of these resistors is to set a proper logic level in case, for example, there is an interruption in the logic lines or the controller outputs are in tri-state conditions. If logic inputs are left floating, the gate driver outputs are set to low level to turn-off the external power transistors. The recommended input pulse width to obtain undistorted output pulses (with MT as in Table 4) is 120 ns. Shorter pulses could be extended up to 120 ns or blanked, if shorter than 30 ns (typ). If all inputs are high, the interlocking function turns low both outputs.

5.2 Supply rails, UVLO protections

The device is supplied by three rails (VCC, PVCC and BOOT).

The VCC pin supplies current to the logic circuit, level-shifters in the low-side section and the integrated bootstrap diode.

The PVCC pin supplies low-side output buffer. The current used to provide gate charge to the low-side power switch flow through this pin.

The PVCC pin can be connected either to the same supply voltage of the VCC pin or to a separated voltage source. In case the same voltage source is used, it is suggested to connect VCC and PVCC pins by means of a small decoupling resistance.

The BOOT pin supplies high-side output buffer through a bootstrap capacitor connected to the OUT pin. The current used to provide gate charge to the high-side power switch flow through this pin.

The use of dedicated bypass ceramic capacitors located as close as possible to each supply pin is highly recommended.

The VCC and BOOT supplies are monitored by undervoltage lockout protection (UVLO) to prevent power switch conduction in dissipative condition due to low V_{GS} .

5.2.1 VCC UVLO protection

Undervoltage protection is available on VCC to GND supply pins, with dedicated circuitry. A hysteresis sets the respective turn-off threshold.

When VCC voltage falls below the $V_{CCthOFF}$ threshold, all the outputs are switched low, both LON/LOFF and HON/HOFF.

When VCC voltage reaches the V_{CCthON} threshold, the device returns to normal operation and sets:

- LON/LOFF output according to actual input pin status;
- HON/HOFF output according to actual input pin status if BOOT-OUT (V_{BO}) is not in UVLO.

Figure 3 shows device behavior while V_{BO} is not in UVLO.

Figure 2. VCC UVLO and LON, LOFF

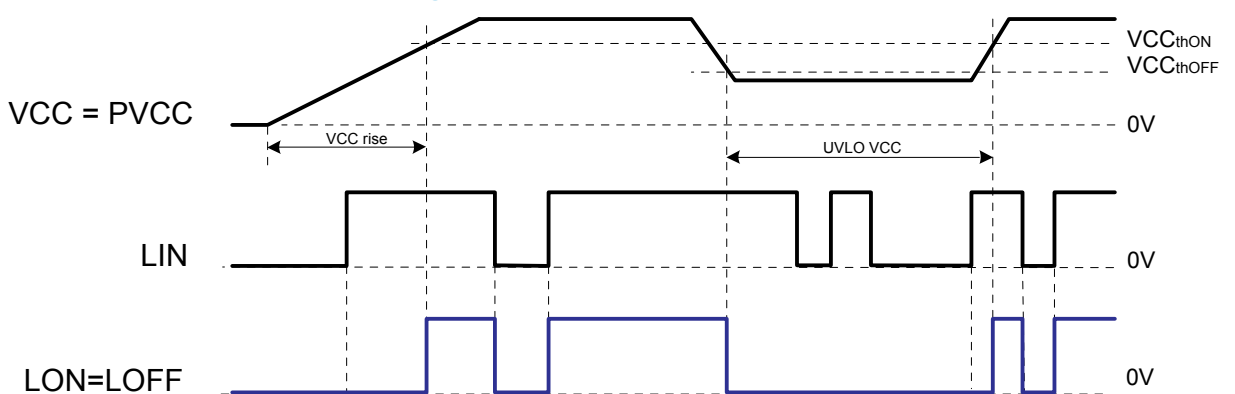
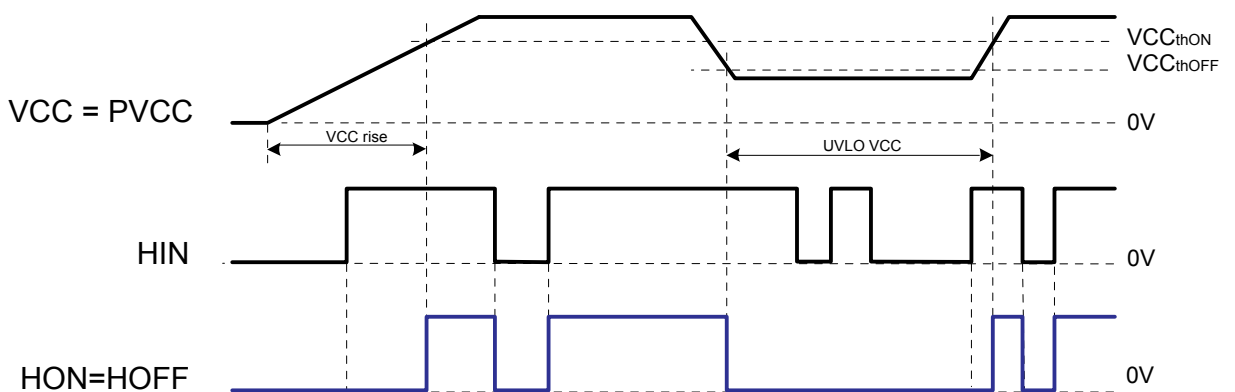


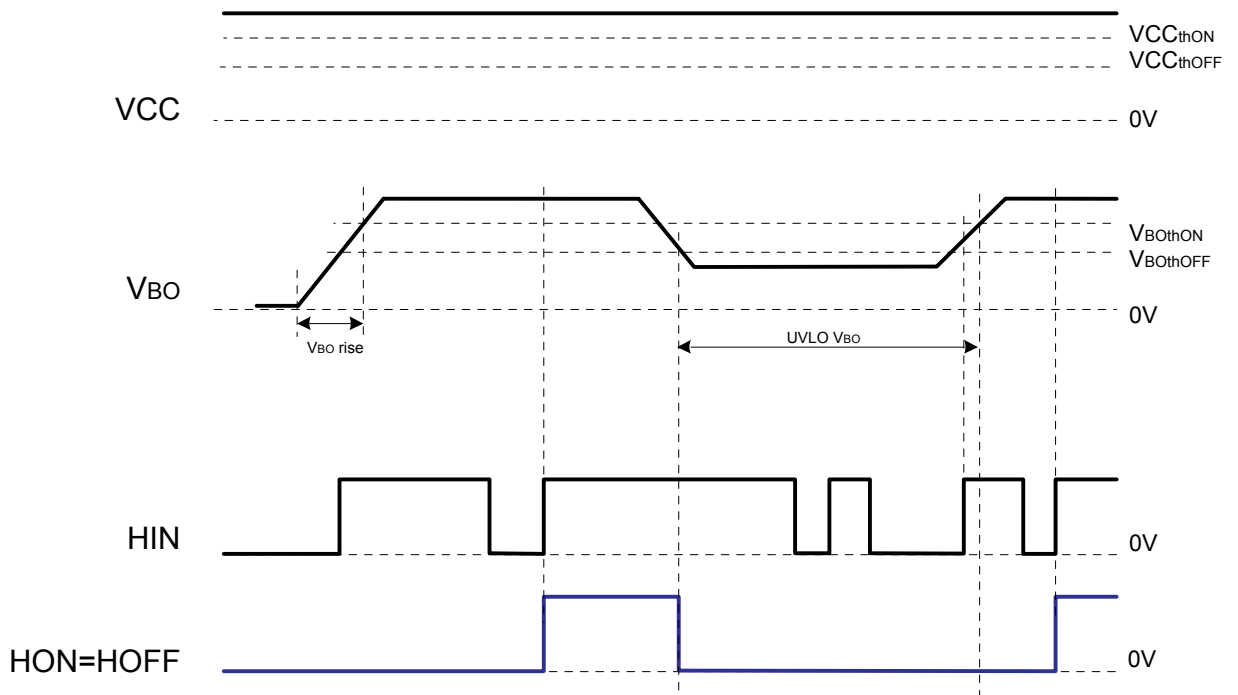
Figure 3. VCC UVLO and HON, HOFF



5.2.2 V_{BO} UVLO protection

Undervoltage protection is available on the bootstrap section between BOOT to OUT supply pins (V_{BO}). A hysteresis sets the turn-off threshold.

When V_{BO} voltage goes below $V_{BOthOFF}$ threshold, the HON/HOFF output is switched low. When V_{BO} voltage reaches the V_{BOthON} threshold, the device returns to normal operation and the output remains low until the next HIN input pin transition or VCC UVLO exit.

Figure 4. V_{BO} UVLO


5.3 Thermal shutdown

The STDRIVEG600W has a thermal shutdown protection feature.

When junction temperature reaches the T_{TSD} temperature threshold, the device turns low both driver outputs to leave the half-bridge in 3-state and signaling the state forcing $\overline{SD/OD}$ pin low.

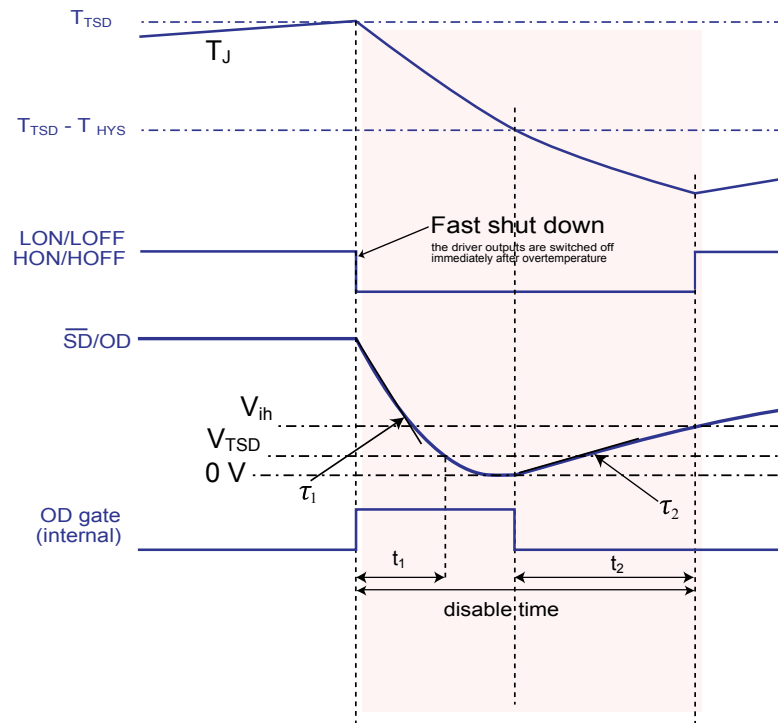
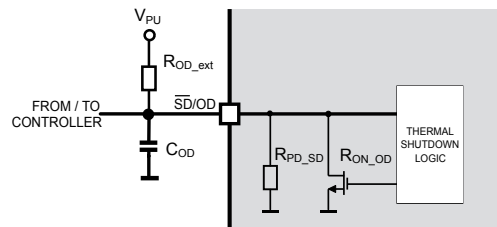
The $\overline{SD/OD}$ pin is released when junction temperature is below ' $T_{TSD}-T_{HYS}$ ' and $\overline{SD/OD}$ is below V_{TSD} .

The STDRIVEG600W driver outputs are driven again according to inputs when $\overline{SD/OD}$ rise above V_{ih} .

The thermal smart shutdown system gives the possibility to further increase the disable time after the overtemperature event adding the C_{OD} capacitor.

Adding C_{OD} enables to increase the disable time up to very large values without delaying the protection intervention time.

The RC time constant tuned by C_{OD} and R_{OD_ext} determine the additional disable time t_2 .

Figure 5. Thermal Shutdown timing waveform

THERMAL SHUTDOWN CIRCUIT


5.4 OUT below ground ruggedness and operation

The STDRIVEG600W is a half-bridge gate driver with a high current capability to target high frequency and high current applications.

Any half-bridge inverter inherently includes some inductive parasites in the power loop that generates positive and negative output voltage spikes during power switch commutations, due to di/dt .

These spikes could be detrimental for inverter EMI, efficiency, power switch operation and application design margin, so spikes shall be minimized to achieve best performance and inverter ruggedness.

Overall spike level is generally minimized first by carefully designing PCB and secondly by tuning switching speed.

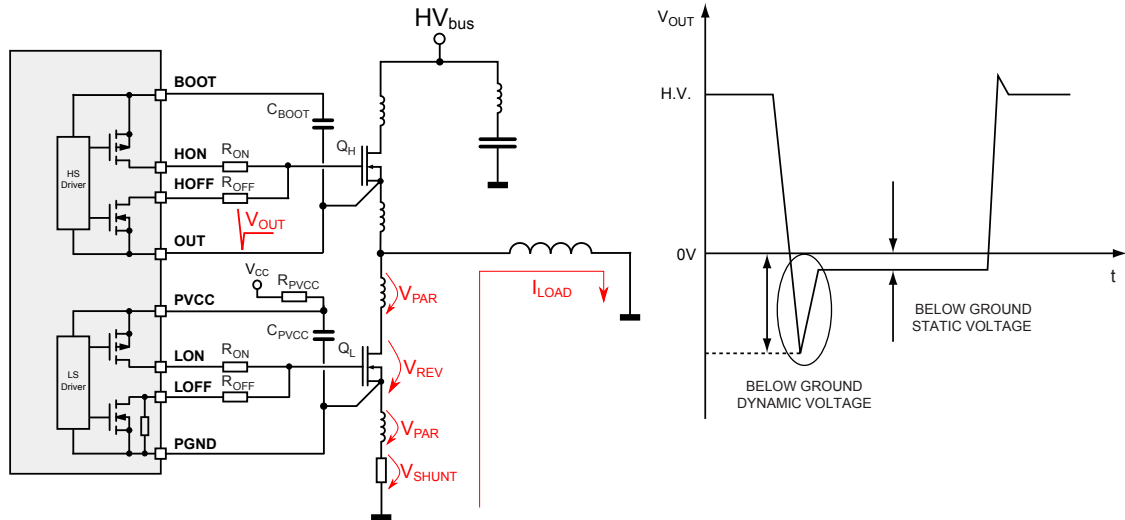
However, low switching speed generally decrease inverter efficiency: a tradeoff between EMI and efficiency is necessary, and some spikes could still be present.

A very common phenomenon observed and analyzed in the application is the OUT below-ground level which is composed by two contributes:

- Dynamic OUT below-GND, primarily due to parasitic inductance, secondary by power switch timing characteristics, with spiky shape.

- Static below-ground, due to low-side reverse conduction characteristics V_{REV} and shunt voltage drop V_{SHUNT} .

Figure 6. Dynamic and static OUT below ground



5.4.1 Dynamic OUT below-GND spike

The dynamic OUT below-ground spike is caused by parasitic inductance due to di/dt on low-side power switch while current start recirculating after high side Q_H hard turn-off.

Since the di/dt increases with the value of operating current, the below-GND spike amplitude is generally higher in overload or short-circuit conditions.

Other effects may contribute to the below-GND amplitude, such as for example the low-side MOSFET forward recovery or gate ringing in case of GaN FETs with not optimal gate loop.

The duration of the dynamic below-GND is very short, and for GaN devices usually limited to less than 10 ns.

The waveform [Figure 7](#) shows the STDRIVEG600W observed ruggedness in respect to OUT below-ground dynamic voltage spike obtained with the test setup in [Figure 8](#).

To purposely increase and test very deep OUT below-GND spike, an inductance has been intentionally placed in series to the low-side drain. The STDRIVEG600W operated even with -200 V and deeper spikes.

This deep spike is however unrealistic in properly designed applications and the waveform is reported as ruggedness example. It is always recommended to keep below ground spike small to minimize EMI and maximize application ruggedness.

Figure 7. Dynamic below-ground OUT voltage waveform with -210V peak

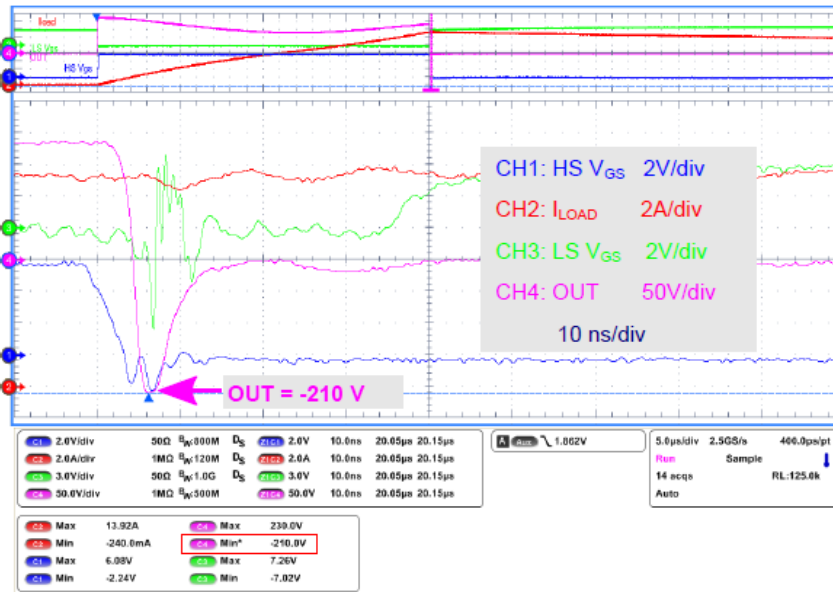
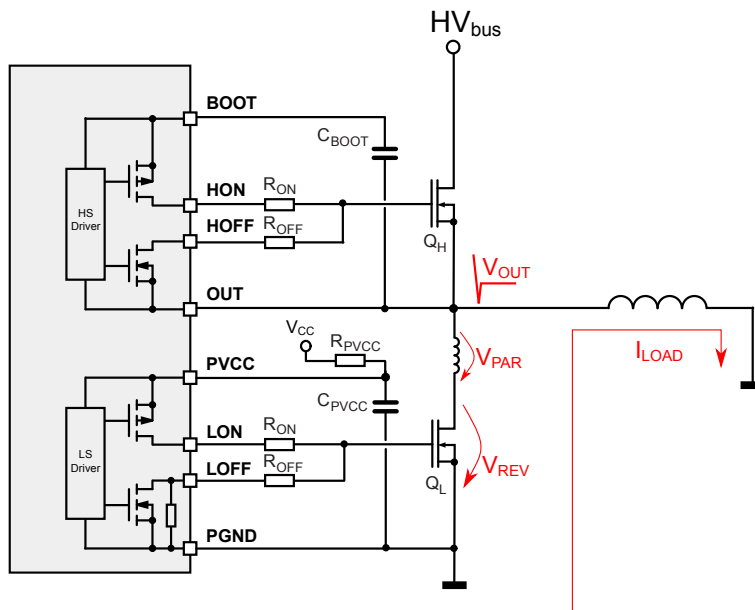


Figure 8. Dynamic below ground OUT voltage test setup



5.4.2 Static OUT below-GND and hard switching topologies

During the below-ground static voltage due to load current recirculation on low side switch Q_L , OUT negative voltage level is determined by low-side power switch reverse conduction drop V_{REV} and the shunt resistor voltage drop V_{SHUNT} (refer to Figure 6).

The voltage on BOOT pin follows OUT voltage with V_{BO} (BOOT-OUT, High-Side driver supply voltage) offset voltage:

Equation 1

(1)

$$BOOT = OUT + V_{BO}$$

For example, if $OUT = -1\text{ V}$, with a $V_{BO} = 6\text{ V}$ (which is a typical gate voltage for many GaN device), $BOOT$ is 5 V .

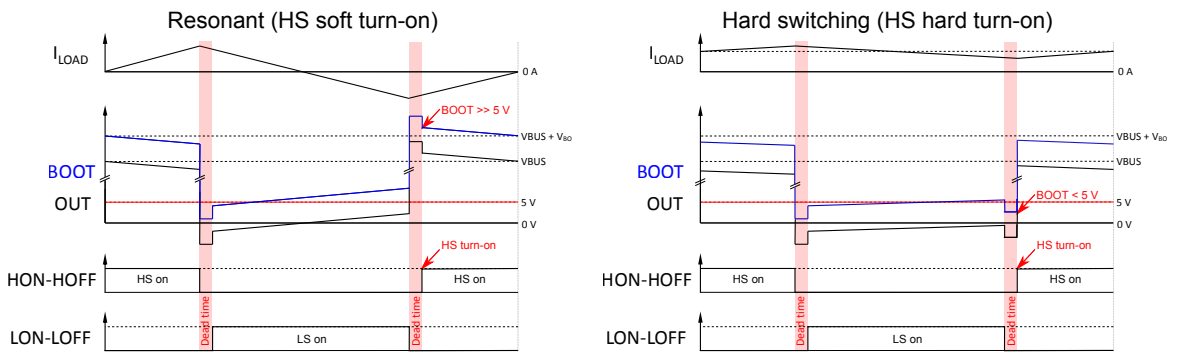
To achieve the driver propagation performance, $BOOT$ shall be $\geq 5\text{ V}$ (refer to Table 3).

GaN devices have several benefits compared to the Si MOSFET, one of them is the absence of body diode reverse recovery. On the other hand, GaN have worse reverse conduction characteristics.

During current recirculation on low-side while the GaN is off, OUT voltage is typically lower compared to Si MOSFET counterparts and $BOOT$ could be lower than 5 V during a high-side hard turn-on. In such a case, high-side turn-on propagation delay could be higher, or, at the highest current levels, turn-on command missed.

The following Figure 9 schematically shows typical voltages present on a GaN based half-bridge without additional recirculation diodes in parallel to GaN devices.

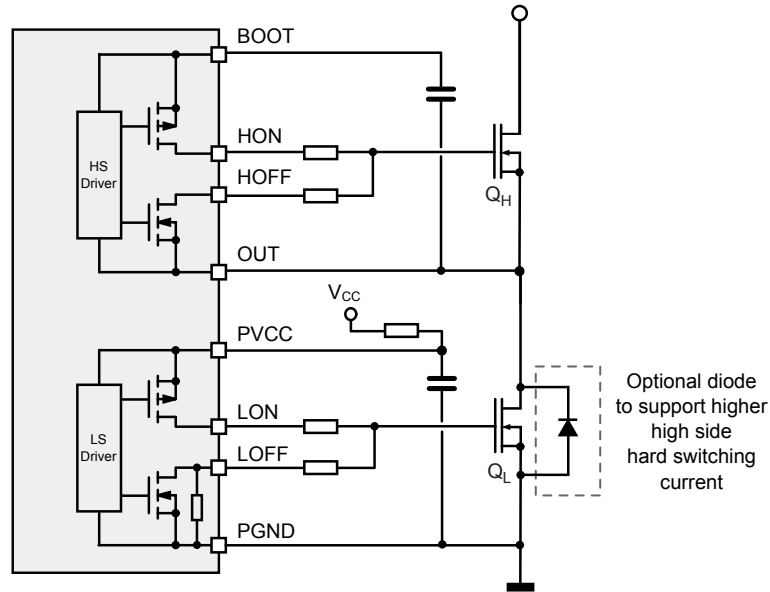
Figure 9. Resonant vs. Hard switching on GaN based half-bridge



In resonant topologies, high-side turn-on command is typically performed “soft” while OUT is already at BUS voltage, so $BOOT \gg 5\text{ V}$ within recommended conditions.

In hard switching topologies, if high-side turn-on command is performed “hard”, depending on load current, BOOT could be lower than 5 V in GaN based half-bridges. Adding a diode in parallel to low-side GaN can limit drop voltage enabling the use of the driver in those topologies also at high current as shown in Figure 10.

Figure 10. Hard switching topologies with optional diode to increase hard switching current



5.5 PGND and Kelvin source connection

The STDRIVEG600W natively supports source Kelvin connection on both high-side and low-side.

Source Kelvin connection is very beneficial for optimal gate driving, especially for GaN devices.

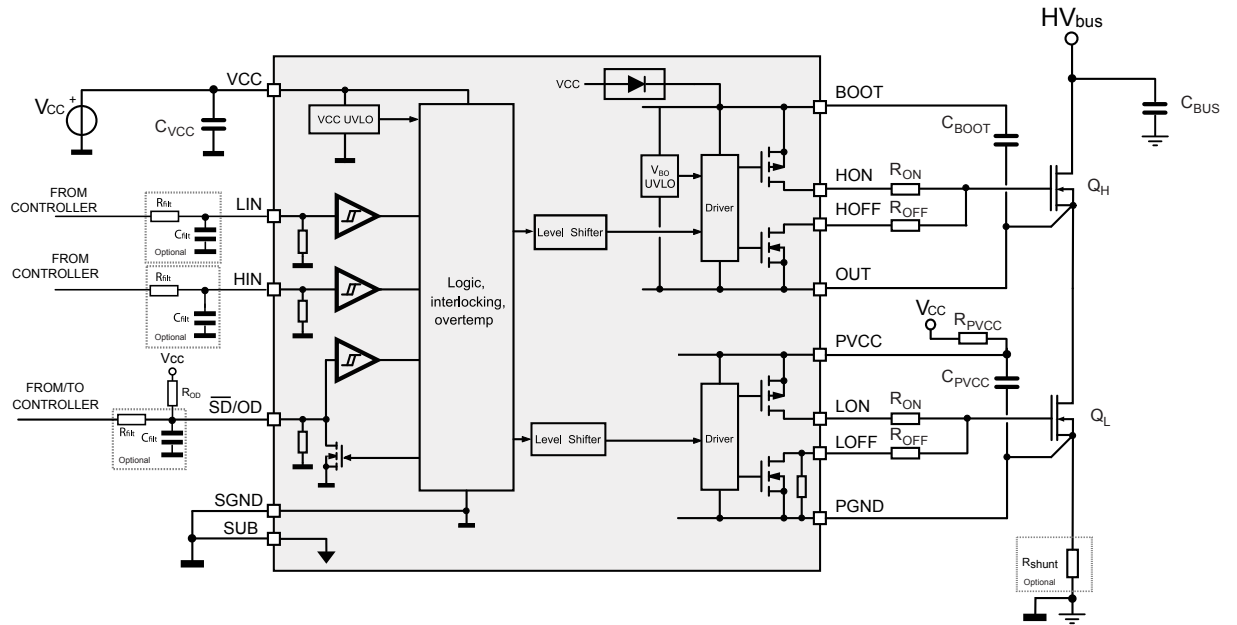
The dedicated PGND pin of the STDRIVEG600W enables to operate in presence of source bouncing due to the Kelvin connection.

The presence of the dedicated PGND and PVCC pins also enables the use of shunt resistors for load current sensing. This feature simplifies application schematic in GaN shunt-based applications without requiring input isolator or critical input filtering solutions, as suggested by some counterpart devices without dedicated PGND pin.

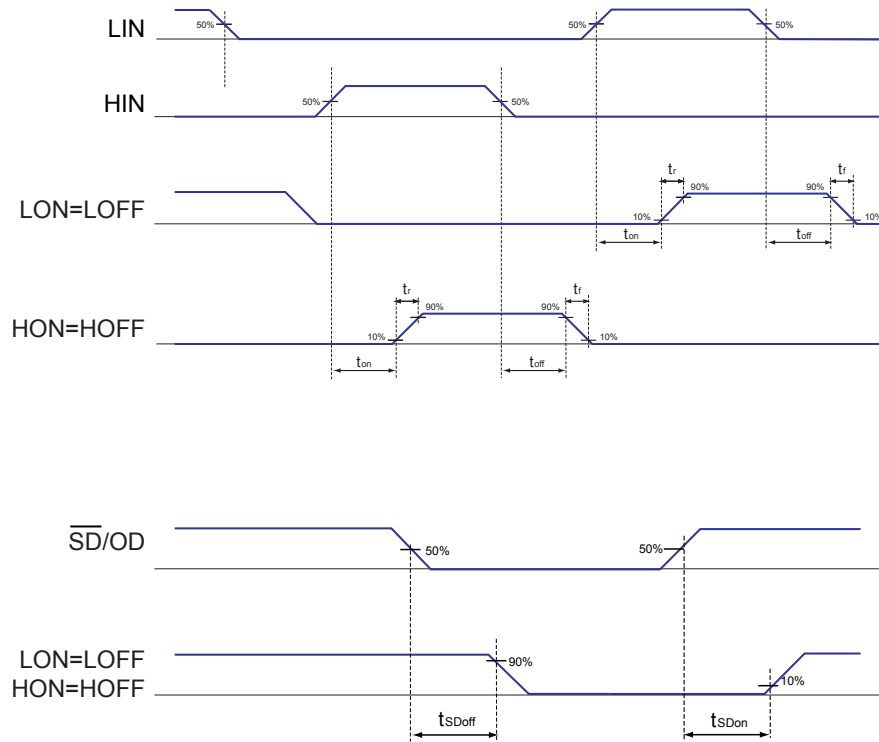
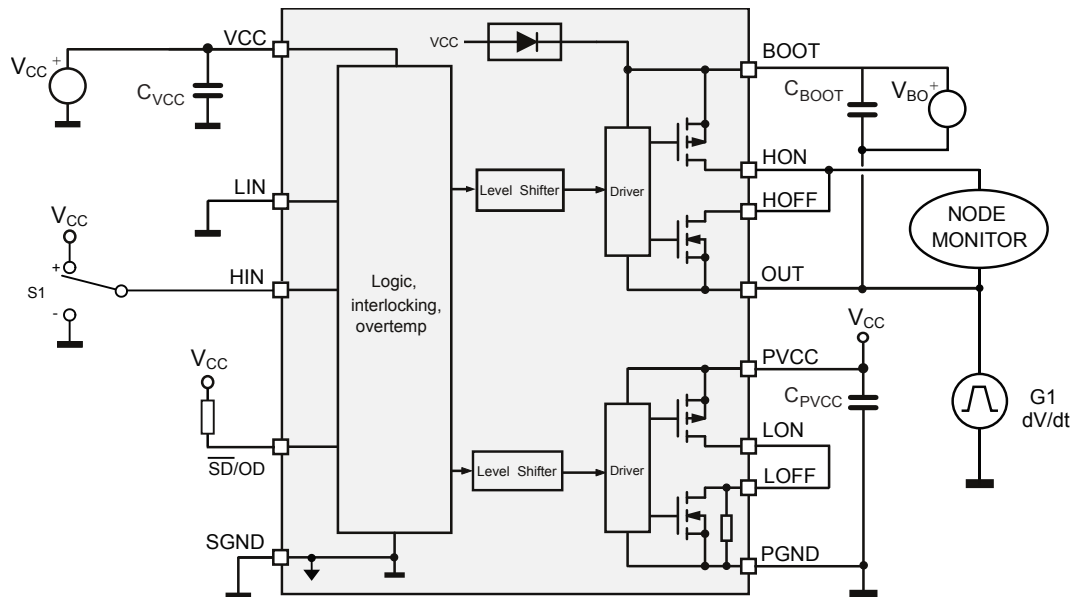
The driver PVCC can be supplied with a simple RC filter like the one shown in Figure 11.

6 Typical application diagram

Figure 11. Typical application diagram

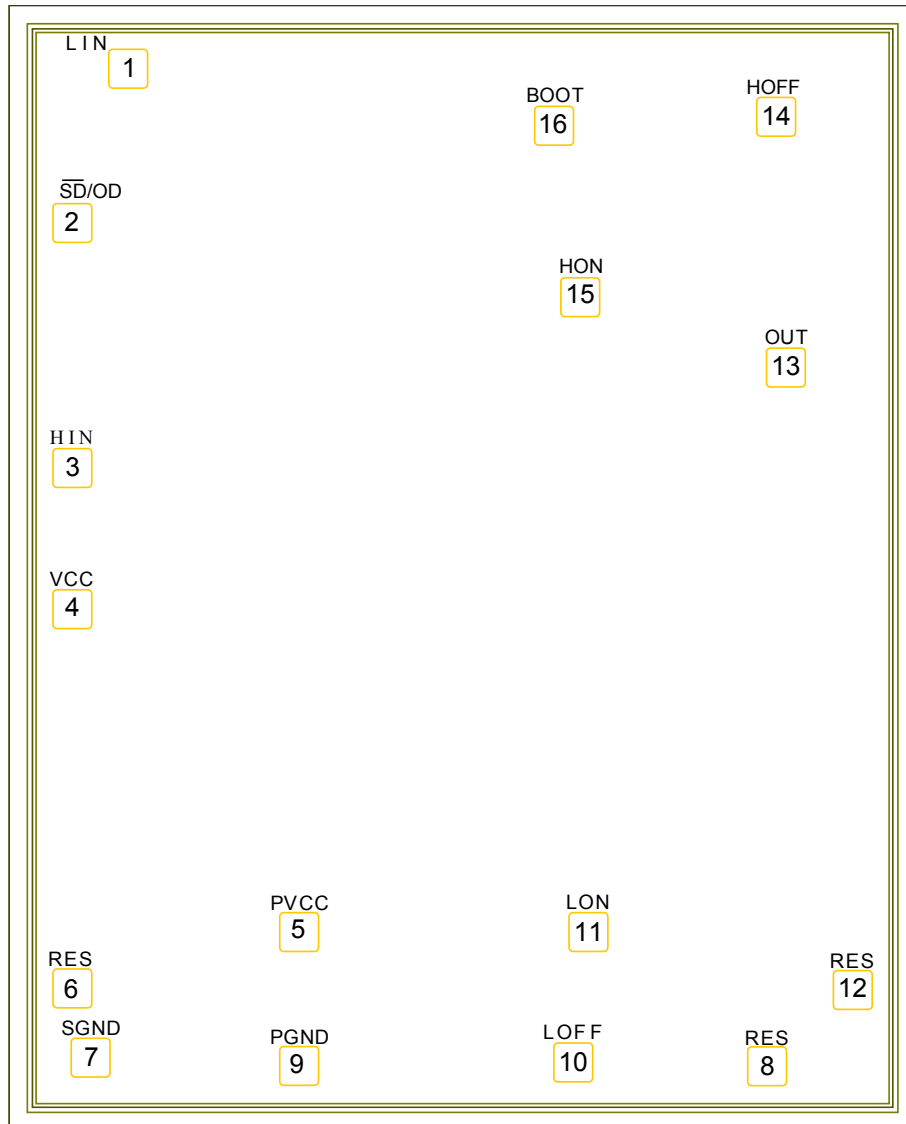


7 Testing and characterization information

Figure 12. Timing definition

Figure 13. CMTI characterization test setup


Note: characterization done on SO16 discrete package

8 Pad position

Figure 14. Pad position

Table 6. STDRIVEG600W mechanical parameters

Die size	2116.0 x 2622.0 μm (X x Y)
Die area	5.548 mm ²
Die thickness	280 \pm 20 μm
Back side type	Cr / NiV / Au

Table 7 shows pad coordinates: pad placement values correspond to each pad center coordinates; pad placement origin is the center of the die.

Table 7. STDRIVEG600W pad coordinates

Pad name	X position [mm]	Y position [mm]	X x Y pad dimension [mm x mm]
LIN	-776.18	1158.88	90.07 x 90.07
BOOT	212.29	1026.47	90.07 x 90.07
HON	273.01	628.66	90.07 x 90.07
HOFF	727.7	1047.31	90.07 x 90.07
OUT	750.24	465.4	90.07 x 90.07
RES	905.56	-979.18	90.07 x 90.07
RES	706.67	-1156.16	90.07 x 90.07
LON	292.03	-844.72	90.07 x 90.07
LOFF	256.84	-1147.31	90.07 x 90.07
PGND	-379.43	-1155.41	90.07 x 90.07
PVCC	-379.43	-844.72	90.07 x 90.07
SGND	-863.4	-1136.25	90.07 x 90.07
RES	-905.69	-975.48	90.07 x 90.07
VCC	-905.69	-95.45	90.07 x 90.07
HIN	-905.69	232.14	90.07 x 90.07
$\overline{\text{SD}}/\text{OD}$	-905.69	800.72	90.07 x 90.07

9 Ordering information

Table 8. Order codes

Order Code	Package
STDRIVEG600W	Wafer

Revision history

Table 9. Document revision history

Date	Version	Changes
06-Sep-2021	1	Initial release.

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