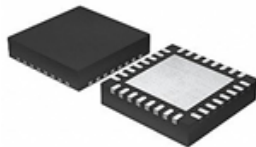


60 A electronic fuse for 12 V DC rail



VFQFPN (5x5x0.95) 32L

Features

- 60 A continuous current
- Input voltage range from 5 to 18 V
- Adjustable current limit
- Input undervoltage lockout
- Integrated 0.85 mΩ power MOSFET
- Enable/disable pin
- Programmable turn-on time
- Accurate current monitor signal
- Precise temperature monitor
- Overcurrent and fault status flags
- Internal MOSFET diagnostic
- Thermal protection
- Thermal latch (STEF12H60) or auto-retry versions (STEF12H60A)
- QFN32-5x5 package
- Temperature range: -40 °C to 125 °C

Applications

- Server main eFuse
- Hot-swap boards
- High power 12 V rail protection

Product status link

[STEF12H60](#)

Description

The **STEF12H60** is a 60 A integrated electronic fuse optimized for monitoring the output current and the input voltage, over the 12 V DC power lines.

When connected in series to the main power rail, it is able to detect and react to overcurrent conditions. When an overload condition occurs, the device limits the output current to a safe value defined by the user.

A precise current monitor signal provides continuous information about the load current to the system controller IC.

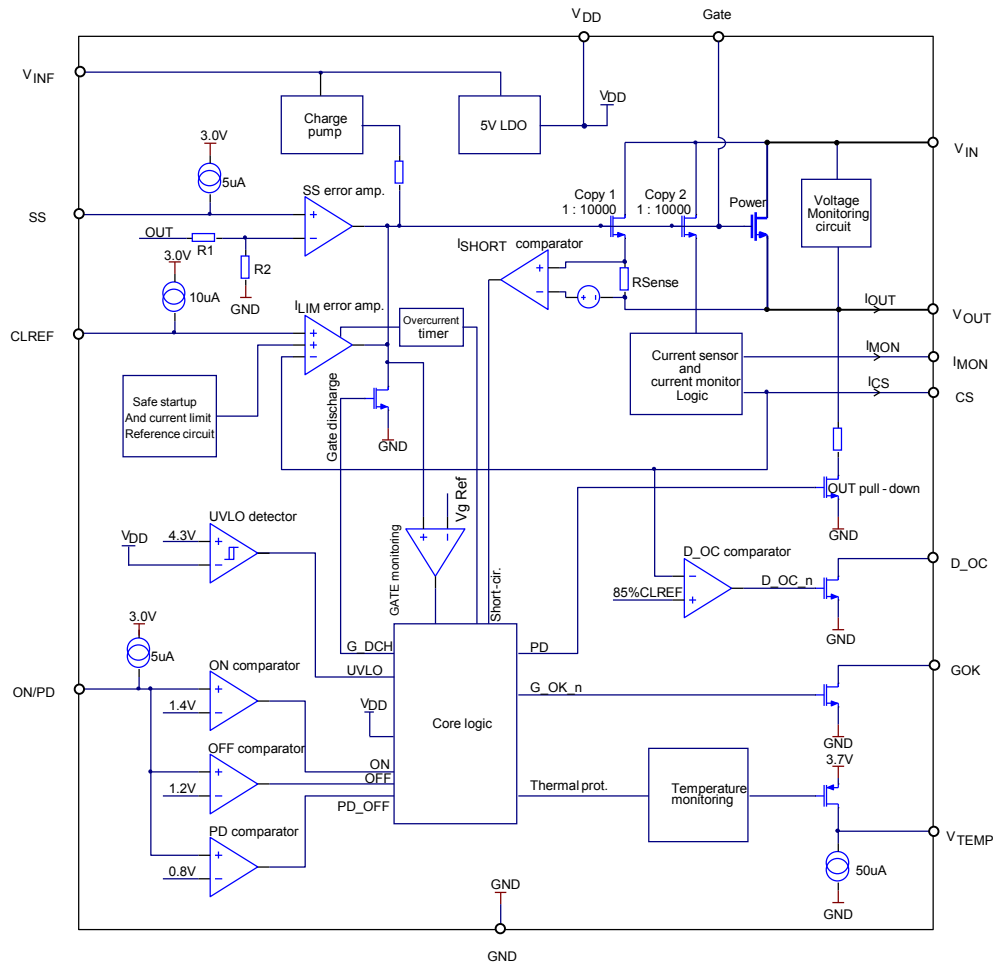
Similarly, a precise temperature sensor generates a monitor signal that permits the system controller to keep the device power dissipation under control.

Turn-on time is programmable, which helps control the inrush current during start-up operations.

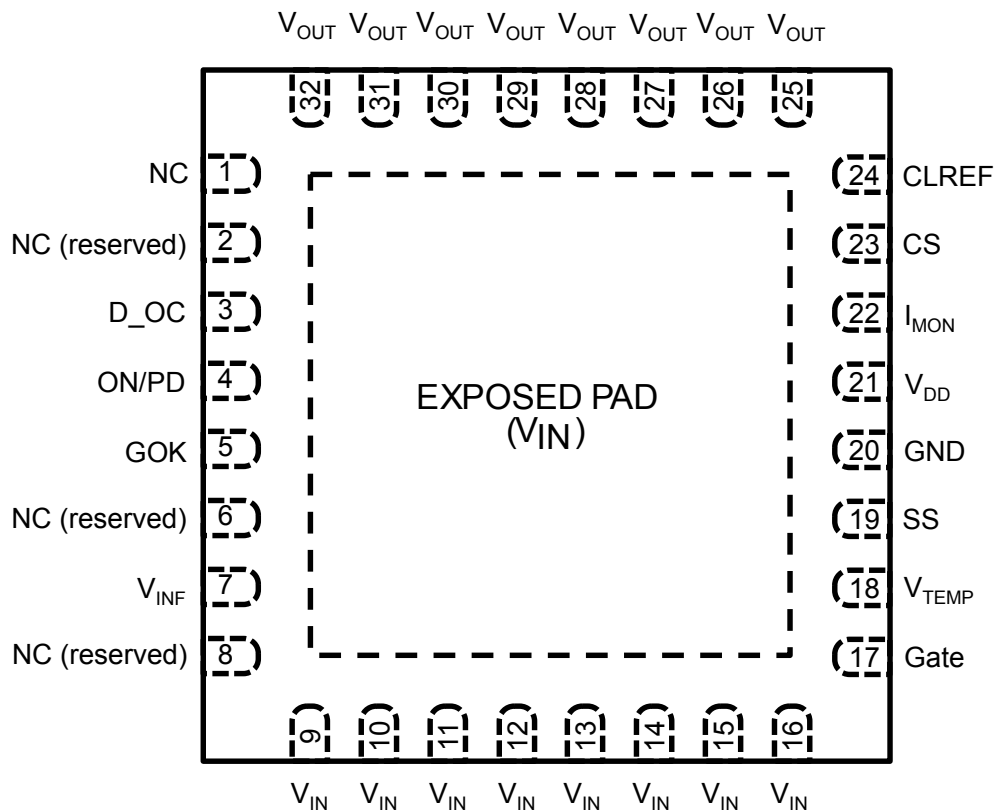
The device also embeds the undervoltage lock-out feature, self-diagnostic and absolute thermal protection.

1 Diagram

Figure 1. Block diagram



2 Pin configuration

Figure 2. Pin connection (top view)

Table 1. Pin configuration

| Pin # | Symbol | Function |
|-------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 25-32 | V_{OUT} | Output voltage of the eFuse. All pins must be connected together on the PCB |
| 3 | D_OC | Output pin, driven low if the current set-point is exceeded. It is a 5 V compliant open drain output |
| 4 | ON/PD | Enable/disable pin. This pin is internally pulled up. Pull this pin below the relevant threshold to shut down the chip. Pull it above threshold to enable the chip. This pin also commands the output pull-down resistance. A capacitor connected between this pin and GND can be used to increase the delay during startup. |
| 5 | GOK | Gate-OK output pin. It signals that a shutdown, which was not commanded by the enable pin, has happened. 5 V compliant open drain output, low when device is in a fault condition. |
| 1 | NC | Not internally connected. It can be connected to any potential. |
| 6, 8 | NC/reserved | These pins are reserved and must be left floating. |
| 2 | NC/reserved | This pin is reserved. If necessary, it can be connected to any potential up to V_{IN} . |
| 7 | V_{INF} | Input voltage for internal circuits. It is connected to V_{IN} through an R-C filter. |
| 9-16 | V_{IN} | Input voltage of the eFuse. All these pins must be connected together and to the exposed pad. |
| 17 | Gate | Gate pin of the internal MOSFET. This pin must be left floating or it can be bypassed to GND through an external R-C filter, to minimize the risk of oscillation in case of very small C_{OUT} or high input/output inductance. |

| Pin # | Symbol | Function |
|---------|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 18 | V _{TEMP} | Temperature monitor pin. Connect a 1 kohm resistor in parallel with a 0.1 μF capacitor between this pin and GND to ensure stability of the monitor signal. |
| 19 | SS | Soft-start pin. A capacitor connected between this pin and GND determines the soft-start time. If it is left floating the start-up time is about 300 μs. |
| 20 | GND | Analog device ground. |
| 21 | V _{DD} | Internal LDO output and compensation pin. It provides a regulated 5 V auxiliary output. This pin must be bypassed to GND via a 1 μF capacitor to ensure the correct functionality of the device. |
| 22 | I _{MON} | Current monitor pin. A resistor (R _{MON}) connected between this pin and GND generates a voltage proportional to the output current. A capacitor (C _{MON}) must be connected in parallel to R _{MON} to filter the monitor signal. |
| 23 | CS | Current feedback. A resistor (R _{CS}) connected between this pin and GND provides a feedback voltage for the current limit circuit and the overcurrent indicator (D_OC). Do not connect any capacitance to this pin. |
| 24 | CLREF | Current limit set-point pin. Connect a resistor to GND or force an external control voltage to define the current limit set-point. |
| EXP.PAD | VIN | Input voltage, internally connected to the power FET drain. |

3 Typical application circuit

Figure 3. Typical application diagram (external controller used for CLREF pin)

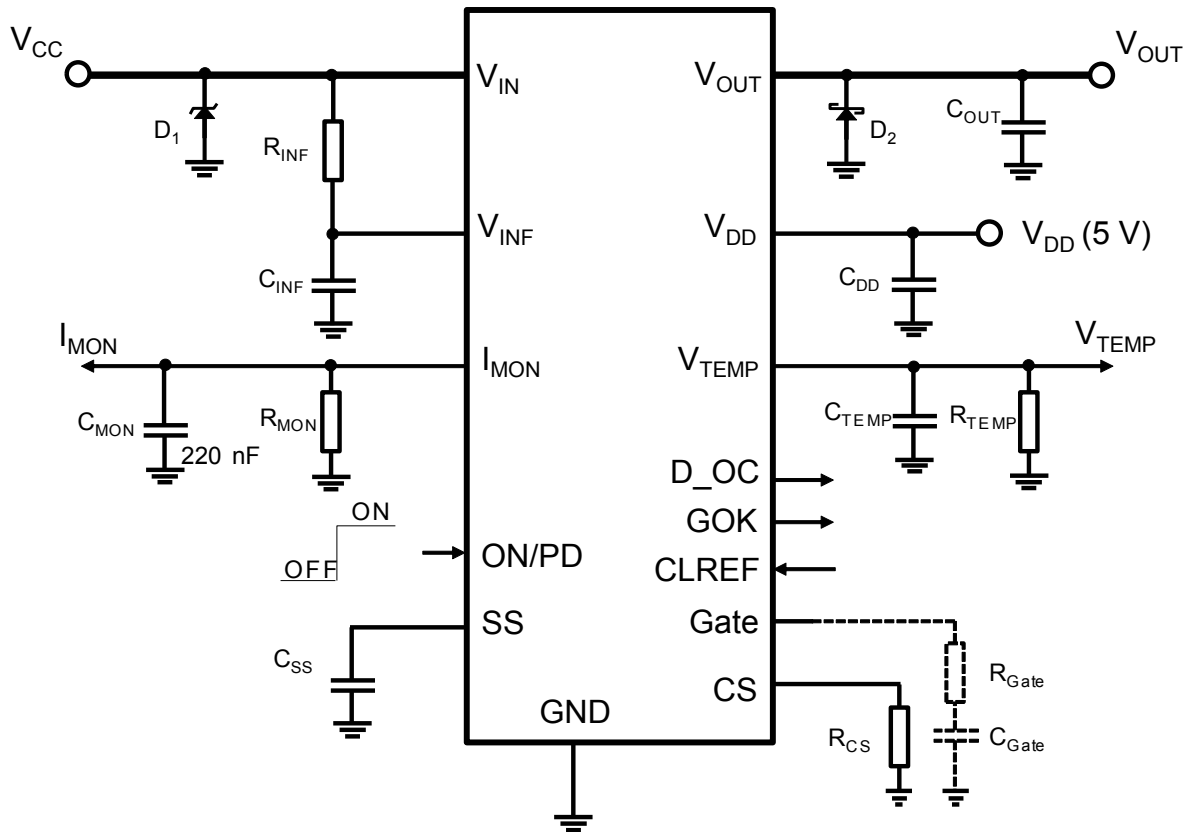
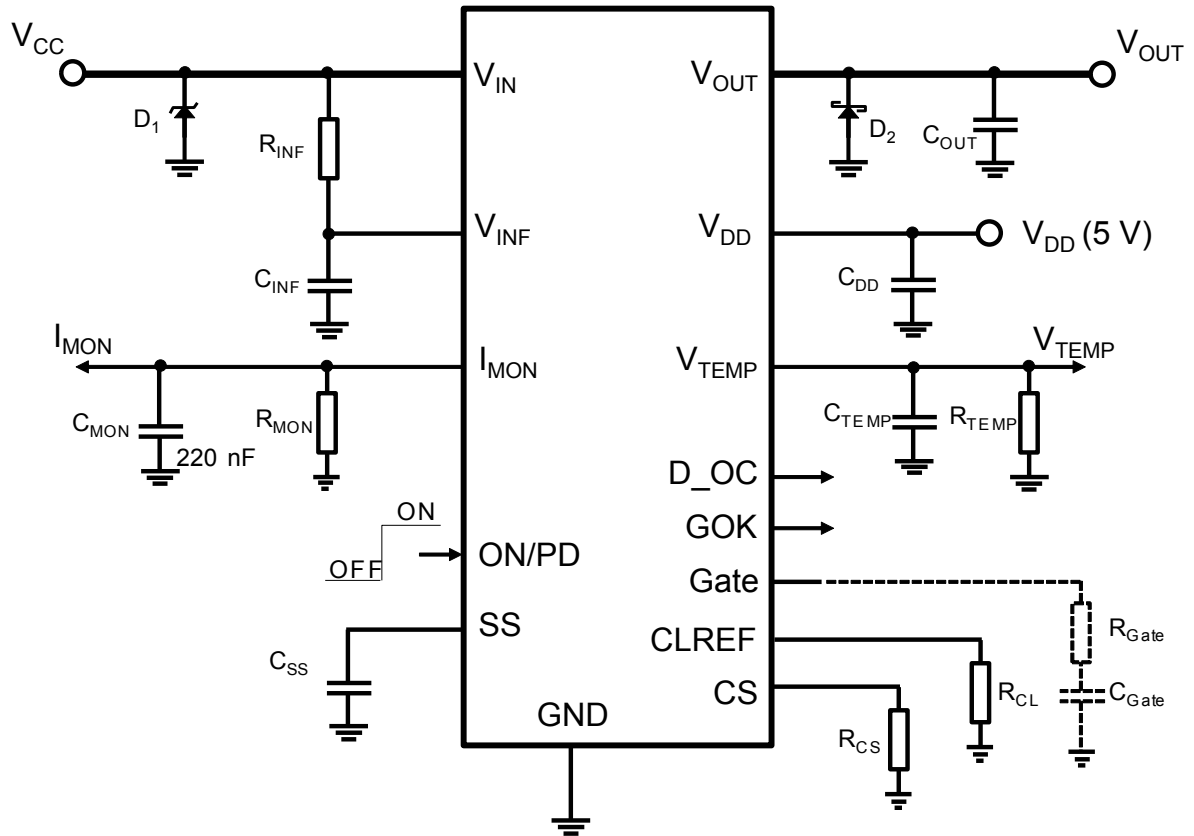


Figure 4. Typical application diagram (current limit fixed via R_{CL})



4 Absolute maximum ratings

Table 2. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|------------------|--------------------------------|------------------|------|
| V_{IN} | Input supply voltage | -0.3 to 20 | V |
| V_{INF} | Input supply voltage | -0.3 to V_{IN} | V |
| V_{OUT} | Output voltage | -0.3 to V_{IN} | V |
| V_{DD} | LDO output voltage | -0.3 to 7 | V |
| All other pins | Pin voltage | -0.3 to 6 | V |
| I_{OUT} | Continuous output current | 75 | A |
| I_{DD} | LDO continuous output current | 60 | mA |
| ESD | Charge device model | ± 500 | V |
| | Human body model | ± 2000 | |
| $T_{J-OP}^{(1)}$ | Operating junction temperature | -40 to 125 | °C |
| T_{J-MAX} | Maximum junction temperature | 150 | °C |
| T_{STG} | Storage temperature | -55 to 150 | °C |

1. The thermal limit is set above the maximum operating temperature. It is not recommended to operate the device at temperatures greater than the maximum ratings for extended periods of time.

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Exposure to absolute-maximum-rated conditions may affect device reliability.

Table 3. Thermal data

| Symbol | Parameter | Value | Unit |
|-------------|-----------------------------------------|-------------------|------|
| R_{thj-a} | Thermal resistance, junction-to-ambient | 26 ⁽¹⁾ | °C/W |
| | | 22 ⁽²⁾ | |

1. JEDEC still air natural convection test as per JESD 51-2 A, at ambient temperature of 25 °C by using JEDEC (JESD 51-7) 4L PCB FR4 board with using 1 sq-in pad, 1 oz Cu.

2. Forced moving air environment (100 LFM).

Table 4. Recommended operating conditions

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-------------|-----------------------------------------|--------------------------|------|------|------|---------------|
| V_{IN} | Input voltage | | 8 | 12 | 15 | V |
| I_{OUT} | Continuous output current | | | | 60 | A |
| I_{DD} | LDO continuous output current | $V_{INF} = 5.5\text{ V}$ | | | 50 | mA |
| R_{CS} | Current set resistor | | 1.8 | | 4 | k Ω |
| V_{CLREF} | Control voltage range | | 0.2 | | 1.4 | V |
| C_{OUT} | Output capacitance | | 47 | | | μF |
| t_{ss} | Soft-start duration | | 10 | 50 | 100 | ms |
| C_{DD} | V_{DD} capacitor value ⁽¹⁾ | | 1 | 2.2 | 10 | μF |

1. V_{DD} capacitor is mandatory to ensure the internal regulator stability and the device functionality .

Note: Functional operation beyond the recommended operating conditions is not implied.

5 Electrical characteristics

$T_J = -40\text{ °C}$ to $+125\text{ °C}$.

Typical values refer to $T_J = 25\text{ °C}$, $V_{IN} = V_{INF} = 12\text{ V}$, $V_{ON/PD} = \text{floating}$; $C_{OUT} = 100\text{ }\mu\text{F}$; unless otherwise specified.

Min. and max. values are guaranteed by design and characterization through statistical correlation.

Table 5. Electrical characteristics

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------------------------------------------|-------------------------------------------------------------------------------|-----------------------------------------------------------------------------|------|------|------|---------------------|
| Input section | | | | | | |
| V_{IN} | Operating input voltage | | 5 | 12 | 18 | V |
| I_q | Quiescent current | Device operating, no load ($V_{ON/PD} > 1.4\text{ V}$) | | 650 | 1000 | μA |
| | | Fault condition | | 250 | | |
| | | Off-state, $V_{ON/PD} = 0\text{ V}$, $V_{INF} = 16\text{ V}$ | | 200 | 400 | |
| LDO | | | | | | |
| V_{DD} | LDO output voltage | $I_{DD} = 1\text{ mA}$, $V_{INF} = 6\text{ V}$ | 4.6 | 4.9 | 5.2 | V |
| I_{DDmax} | LDO short-circuit current ⁽¹⁾ | $V_{DD} = 0\text{ V}$ | 60 | 120 | | mA |
| V_{DROP} | LDO dropout voltage | $I_{DD} = 30\text{ mA}$ | 66 | 100 | 160 | mV |
| V_{DD_ON} | UVLO rising threshold | | 4.1 | 4.3 | 4.6 | V |
| V_{DD_OFF} | UVLO falling threshold | | 3.8 | 4.0 | 4.2 | V |
| Startup | | | | | | |
| I_{SS} | Soft-start capacitor charging current | | 4.5 | 5.2 | 6 | μA |
| t_{SSMAX} | Soft-start max. time | if $V_{OUT} < 90\%$ of V_{IN} after t_{SSMAX} shutdown is forced | | 200 | | ms |
| A_S | Soft-start gain | Relation between internal soft-start signal ramp and V_{OUT} | | 10 | | V/V |
| Power MOSFET | | | | | | |
| $R_{DS(on)}$ | On-resistance | $T_J = 25\text{ °C}$ | | 0.85 | 1.1 | m Ω |
| I_L | Off-state leakage current | $V_{ON/PD} = 0\text{ V}$, $V_{IN} = 16\text{ V}$, $T_J = 25\text{ °C}$ | | | 1 | μA |
| Current limit and current monitor circuit | | | | | | |
| V_{CS_TH} | Current limit activation threshold ($V_{CS} = I_{RCS} \times R_{CS}$) | $V_{OUT} > 80\%$ of V_{IN} | 97 | 100 | 103 | % of V_{CLREF} |
| $V_{CL_MAX}^{(2)}$ | Maximum CL reference voltage | | 1.55 | 1.6 | 1.65 | V |

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------------------------|------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------------|
| V_{CL_FD} | Internal voltage reference for foldback current limit at startup | V_{OUT} is lower than 40% of V_{IN} | 130 | 150 | 170 | mV |
| V_{CL_ST} | Internal voltage reference for current limit at startup | V_{OUT} is between 40% and 80% of V_{IN} | 470 | 500 | 530 | mV |
| t_{CL} | Current limit response time ⁽³⁾ | from $V_{CS} > V_{CLREF}$ until current limit | | 100 | | μ s |
| I_{CL} | CLREF pin internal biasing current | From CLREF pin into 1 V source | 9.4 | 10 | 10.4 | μ A |
| V_{CL_MAX} | Maximum voltage of the CLREF pin internal biasing source | | | 3.0 | | V |
| I_{RCS}, I_{MON} | Current sense/monitor accuracy | $T_j = 25\text{ }^\circ\text{C}$, $5\text{ A} < I_{OUT} < 60\text{ A}$ ⁽³⁾ (4) | -3 | 1 | 3 | % |
| | | $T_j = 0\text{ to }85\text{ }^\circ\text{C}$, $5\text{ A} < I_{OUT} < 60\text{ A}$ (3) | -6 | | 6 | % |
| A_{CS}, A_{MON} | Current sense and current monitor gain | I_{RCS}/I_{OUT} , I_{MON}/I_{OUT} , $T_j = 0\text{ to }85\text{ }^\circ\text{C}$, $5\text{ A} < I_{OUT} < 60\text{ A}$ | 9.4 | 10 | 10.6 | μ A/A |
| t_{SH} | Shut-down timer ⁽³⁾ | From current limit detection to MOSFET turn-off | | 250 | | μ s |
| I_{SC} | Short-circuit current limit ⁽³⁾ | | | 100 | | A |
| T_{SC} | Short-circuit protection response time ⁽³⁾ | From $I_{OUT} > I_{SC}$ until MOSFET gate pull-down | | 500 | | ns |
| V_{MON_MAX} | Internal current source maximum voltage | Internal pull-up voltage on I_{MON} pin | | 3.0 | | V |
| ON/PD (chip-enable pin) | | | | | | |
| V_{OFF} | Low level input voltage | Output disabled/PD activated | 1.11 | 1.2 | 1.29 | V |
| V_{ON} | High level input voltage | Output enabled | 1.3 | 1.4 | 1.5 | V |
| V_{PD} | Pull-down de-activation threshold | Pull-down de-activated | 0.71 | 0.8 | 0.89 | V |
| t_{ON} | Initial delay time | From $V_{ON/PD} > V_{ON}$ to soft-start beginning | 0.8 | 1 | 1.2 | ms |
| $I_{ON/PD}$ | Enable pin bias current | | 4 | 5 | 6 | μ A |
| V_{ON/PD_MAX} | Internal current source maximum voltage | Internal pull-up voltage on ON/PD pin | | 3.0 | | V |
| R_{PD} | Output pull-down resistance | $V_{OUT} = 12\text{ V}$, pull-down activated | | 0.72 | | k Ω |

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|------------------------------------|--------------------------------------------------|-----------------------------------------------------------------------------------------------|------|------|------|------------------------|
| t_{PD} | Output pull-down delay timer | From $V_{OFF} < V_{ON/PD} < V_{PD}$ | | 2 | | ms |
| Temperature monitor | | | | | | |
| V_{TEMP} | V_{TEMP} voltage | $T = 25\text{ }^{\circ}\text{C}$ | | 450 | | mV |
| | Temp coefficient ⁽³⁾ | $T = 0\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$ | | 10 | | mV/ $^{\circ}\text{C}$ |
| | Load capability | Maximum current | | | 4 | mA |
| | Pull-down current | $T = 25\text{ }^{\circ}\text{C}$ | | 50 | | μA |
| Status line | | | | | | |
| GOK | Gate-OK output voltage | $I_{SINK} = 1\text{ mA}$ | | | 0.1 | V |
| | Leakage current | $V_{GOK} = 5\text{ V}$ | | | 1 | μA |
| V_{OC} | Overcurrent detection threshold | V_{CS} voltage threshold that triggers D_OC low | 83 | 85 | 87 | % V_{CLREF} |
| D_OC | Overcurrent monitor signal active low voltage | $I_{SINK} = 1\text{ mA}$, $V_{CS} > V_{OC}$ | | | 0.1 | V |
| | Leakage current | $V_{D_OC} = 5\text{ V}$, $V_{CS} < V_{OC}$ | | | 1 | μA |
| T_D | D_OC signal response time ⁽³⁾ | | | 1 | | μs |
| Thermal protection | | | | | | |
| TSD | Shutdown temperature ⁽³⁾ | GOK pulled low | | 140 | | $^{\circ}\text{C}$ |
| T_{Retry} | Autoretry delay time (only on the STEF12H60APUR) | From shutdown due to fault to automatic restart | | 1 | | s |
| Internal MOSFET diagnostics | | | | | | |
| V_{DS_TH} | Drain-source short detection threshold | If $V_{OUT} > V_{DS_TH}$ at startup, startup is postponed | | 90 | | % of V_{IN} |
| V_{DS_OK} | Drain-source voltage good detection threshold | If $V_{OUT} < V_{DS_OK}$ startup is resumed | | 70 | | % of V_{IN} |
| V_{OUT_LOW} | Low V_{OUT} detection threshold | After startup, if $V_{OUT} < V_{OUT_LOW}$, the device is turned off | | 90 | | % of V_{IN} |
| V_{DG_SH} | Gate-drain short detection voltage threshold | If $V_G > V_{DG_SH}$ after enable by ON pin, startup is postponed | | 3.1 | | V |
| V_{DG_OK} | Gate-drain voltage good detection threshold | If $V_G < V_{DG_OK}$ startup is resumed | | 3 | | V |
| V_{G_LOW} | Gate fault detection threshold | If $V_{GD} < V_{G_LOW}$ device is turned off | | 5.7 | | V |
| T_{G_LOW} | Get fault timer in normal operation | After T_{SSMAX} elapses, time from $V_{GD} < V_{G_LOW}$ transition to gate fault detection | | 200 | | ms |

1. Pulsed test. The internal LDO is not equipped with thermal protection. Short-circuit duration must not be longer than 1 ms to avoid damage.
2. If the voltage on CLREF pin is higher than V_{CL_MAX} internal reference, the current limit reference voltage is clamped to V_{CL_MAX} .
3. Guaranteed by design, but not tested in production.
4. MOSFET fully conducting, at minimum R_{ON} .

6 Device functional description

The STEF12H60 is a 12 V intelligent load switch, which is able to limit the current during fault events, such as: output overload or short-circuit.

The current limiting loop is also used during the start-up phase of the eFuse to avoid startups into faulty loads. During the normal operation, the eFuse works as a low-resistance power switch, therefore the output voltage follows the input one. In case of overcurrent event, the eFuse limits the V_{GS} of the internal MOSFET switch, in order to clamp the output current to a safe value.

If the fault persists, after a predefined safety timer, or in case the die temperature hits the thermal protection threshold, due to the increased power dissipation, the device goes into shutdown, the internal switch is turned-off and the load is disconnected from the power supply. The device is latched in this off-state until a power supply re-cycle is performed. The auto-retry version instead, is able to re-try starting the device after a fault event, with a typical delay of 1 ms.

The current limit and soft-start features are programmable by the users, by external components.

6.1 UVLO ON/PD function

The device is supplied through the V_{IN} pins, which carry the power directly to the internal power MOSFET drain connection, and the V_{INF} pin, which is the input of the internal regulator, used to supply the analog and logic circuits. This pin must be connected externally to V_{IN} through an R-C filter (see [Section 3 Typical application circuit](#)).

The UVLO (undervoltage lockout) monitors the voltage of the internally regulated V_{DD} node and turns on the device when $V_{DD} > V_{DD_ON}$ (typically 4.3 V). If V_{DD} falls below the UVLO hysteresis threshold ($V_{DD} < V_{DD_OFF}$), the device is turned off including the reset of fault state.

6.2 ON/PD function

During turn-on, provided that the UVLO rising threshold has been surpassed, the start-up procedure begins once the device is enabled via the ON/PD pin. The ON/PD is a logical input with a dual functionality, according to the following description:

1. *Enable/disable the device:* when $V_{ON/PD} > V_{ON}$, the device is enabled. If $V_{ON/PD}$ is pulled down to V_{OFF} or a lower voltage, the device is disabled and the output is shut down. In case the shutdown occurred due to a fault (thermal, overcurrent, failed startup), the device cannot be turned on again via the ON/PD pin. To reset the device from this latched status, a power supply re-cycle is necessary. Alternatively, a reset can be forced without turning off the power supply, by pulling V_{DD} pin below the UVLO voltage and then releasing it.
2. *Activate/deactivate the output discharge feature (PD – output pulldown):* if $V_{ON/PD}$ is kept between V_{PD} (typ. 0.8 V) and V_{OFF} (typ. 1.2 V) for at least 2 ms (t_{PD}), the integrated 0.77 k Ω R_{PD} discharging resistor is connected between V_{OUT} and GND.

The ON/PD pin has an internal pull-up current generator connected to the internal LDO therefore, if the pin is not connected to an external controller IC, it goes to the ON-state (device enabled).

The 5 μ A ON/PD bias current can be used to charge an external capacitor, in this manner prolonging the initial delay time, defined as the time interval between power supply reaching the UVLO threshold and the output voltage controlled ramp-up initialization.

6.3 Soft-start

The device provides monotonic, controlled start-up ramp, in order to keep the inrush current under control. The output voltage rise time can be set by an external C_{SS} , which is charged with a constant current during the start-up phase. The soft-start range is adjustable from 1 to 100 ms.

Given the required ramp-up time, the C_{SS} capacitance can be calculated according to the following equation:

$$C_{SS} = \frac{(t_{SS} \times I_{SS} \times 10)}{V_{IN}} \quad (1)$$

where V_{IN} is typically 12 V and t_{SS} is in the 10-100 ms range.

The table below shows typical values of soft-start duration calculated with standard capacitors and typical I_{SS} value.

Table 6. Output voltage rise time vs. C_{SS} value ($V_{IN} = 12\text{ V}$)

| Symbol | Value | | | | | | | |
|---------------|-------|------|------|------|------|------|------|-----|
| C_{SS} (nF) | 47 | 82 | 120 | 180 | 220 | 270 | 330 | 390 |
| T_{SS} (ms) | 10.8 | 18.9 | 27.7 | 41.5 | 50.8 | 62.3 | 76.2 | 90 |

Important: Soft-start capacitor must be always connected to ensure controlled operation during startup. In case of absence/bad connection of the C_{SS} , the start-up phase is short (300 μs). This might result in significantly high charging current, eventually leading to the device shutdown for overcurrent/overtemperature fault. To prevent the device from starting into faulty loads (such as: resistive load, or damaged bulk output capacitors) the following start-up control flow is applied:

- Start-up fold-back current limit: current limit value during start-up phase is dependent on the sensed output voltage. At the very beginning of startup, when the output voltage is close to zero, the current limit internal reference voltage is reduced to V_{CL_FD} . Any higher current limit value set by the user via the CLREF pin is overridden by the device
- Start-up current limit: during the ramp-up phase, the current limit internal reference voltage is reduced to V_{CL_ST} . Any higher current limit value, set by the user via the CLREF pin, is overridden by the device
- Maximum start-up time: start-up longer than 200 ms is always aborted by the device. If V_{OUT} does not reach 90% of V_{IN} in 200 ms, the device is turned off and the GOK fault indicator is asserted low

The CLREF normal functionality is resumed at the end of start-up phase ($V_{OUT} > 80\%$ of V_{IN}). Adding a capacitor in parallel to the ON/PD pin, the initial t_{ON} delay time between valid V_{IN} value and controlled output ramp-up start ($V_{OUT} = 1\text{ V}$) can be increased.

The default delay time without C_{ON} capacitor is typically 1.25 ms.

6.4 Normal operating conditions

Once the start-up phase ends, the STEF12H60 eFuse behaves like a mechanical fuse, supplying the load connected to its output with the same voltage shown at its input, minus the small voltage fall due to the N-channel MOSFET $R_{DS(on)}$. The status line open-drain indicators GOK and D_OC provide information about the status of the device.

6.5 Current sensing and current limit

When an overload event occurs, the current limiting circuit reduces the conductivity of the power MOSFET, in order to clamp the output current at the value defined by the user by the voltage set on CLREF pin. Current limit function consists of two sub-circuits:

- the **current sense (CS)** circuit, responsible for sensing the load current and providing a feedback signal to detect overcurrent. It relies on a small copy-MOSFET built into the integrated power MOSFET to generate a replica of the load current, proportional by $A_{CS} = I_{RCS}/I_{OUT} = 10\ \mu\text{A/A}$, into the external R_{CS} resistor attached to the eFuse

This current creates a variable V_{CS} voltage across the resistor, defining the eFuse working current CS, which is continuously compared to the current limit reference voltage present on the CLREF pin.

- the **current limit (CL)** circuit defines the reference threshold for the intervention of the current limitation function. This reference point is a voltage (V_{CLREF}) usually provided externally by the system control IC to the CLREF pin, and continuously compared internally to the feedback signal from CS circuit. In this manner, the current limit point can be throttled to satisfy the system power requirements during operation.

In simple standalone designs, such as the one shown in [Figure 4. Typical application diagram \(current limit fixed via \$R_{CL}\$ \)](#), where no control IC is present, the reference signal can be generated by connecting a resistor between CLREF pin and GND. An integrated bias generator sources 10 μ A of current to the R_{CL} resistor, generating a fixed V_{CLREF} , which sets the current limit thresholds.

To ensure reliability, the signal on CLREF is internally clamped to V_{CL_MAX} therefore, even in case of wrong signal provided externally on the pin, a safety current limit threshold is always present.

An overcurrent event is detected when the voltage on CS pin overcomes the V_{OC} threshold, which is typically 85% of the voltage at CLREF pin ($V_{CS} > V_{OC}$). In this case the status D_OC indicator is pulled down. If the load status reverts to normality (V_{CS} falls below 75% of V_{CLREF}), D_OC is released. Based on the value of R_{CS} resistor, the load current level for D_OC triggering can be evaluated by using the following equation:

$$I_{OUT} = \frac{V_{OC}}{R_{CS} \times A_{CS}} \quad (2)$$

In case of overcurrent detection, when V_{CS} surpasses V_{CLREF} , the V_{GS} of internal MOSFET is immediately modulated in order to clamp the load current to the I_{LIM} value defined by user via CLREF pin, according to the following:

$$I_{LIM} = \frac{V_{CLREF}}{R_{CS} \times A_{CS}} \quad (3)$$

During current limitation, additional protection features are activated, in order to keep the total power dissipation under control and protect the device and the system. In particular, a 250 μ s current limit timer (t_{SH}) starts after overload detection. Once timer elapses, the internal MOSFET is shut down and the GOK indicator is pulled to low status, to inform the system controller that a shutdown not due to ON/PD (fault) happened.

Moreover, due to high power dissipation in current limit condition, if the die temperature increases too much and hits the thermal protection threshold (140 $^{\circ}$ C typ.), the thermal protection intervenes, turning off the internal MOSFET and asserting GOK low.

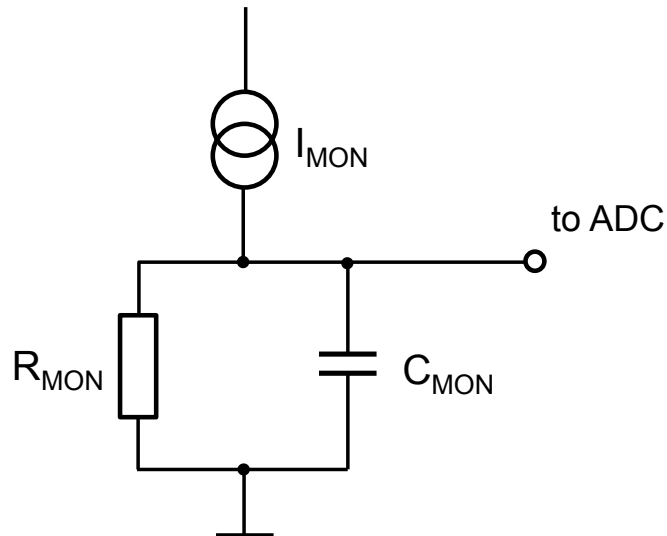
A second level current limit (I_{SC}) is quickly activated in case the load current overcomes 100 A.

This additional protection, fixed by design, is able to respond to short-circuit events on the output. In such occurrence the device is immediately shut down and the D_OC pin is asserted.

6.6 Current monitor

The device is equipped with a current monitoring capability that allows the system controller to read the current flowing through the fuse. An I_{MON} current proportional to the load current flowing through the eFuse is imposed on an external R_{MON} , converting the sensed current into a voltage for further processing by the ADC. The I_{MON} signal is the output of a chopper amplifier, therefore an external bypass capacitor is suggested to reduce the output ripple and to provide a smooth signal (see [Figure 6. Quiescent current vs. temperature](#)). The suggested minimum value for the filter capacitor is 3.9 nF. Lower values result in a worse ripple amplitude.

The current, monitoring amplifier gain and defined as $A_I = I_{MON} / I_{OUT}$, is typically 10 μ A/A.

Figure 5. Current monitor simplified circuit


6.7 Temperature monitor and thermal shutdown functions

The STEF12H60 embeds two thermal sensors, each one accomplishing a specific function:

- **Overtemperature sensor:** this is embedded into the power MOSFET. It monitors the power MOSFET temperature, which is subjected to very fast increases during overload events. If the device temperature exceeds the thermal threshold, typically 140 °C, the thermal shutdown circuit turns the power MOSFET off, thus disconnecting the load. The GOK pin is pulled down. The thermal shutdown protection is always active and overrides any other protection/control feature of the device.
- **Temperature sensor:** this consists of precise thermal sensors embedded in the controller die. The purpose is to statically monitor the overall device temperature, and generate a precise monitor signal (V_{TEMP}) accordingly. Overall typical accuracy is +/- 5 °C. To ensure a stable regulation of the temperature monitor signal, it is recommended to connect an R-C parallel network between this pin and GND, as shown in [Figure 3. Typical application diagram \(external controller used for CLREF pin\)](#) and [Figure 4. Typical application diagram \(current limit fixed via \$R_{CL}\$ \)](#). Recommended values are 1 kΩ for R_{TEMP} 0.1 μF for C_{TEMP} .

The device can be reset from a thermal shutdown condition by pulling the V_{DD} pin below the UVLO threshold or by re-cycling the supply voltage.

6.8 Status indicators and fault conditions

Two open-drain flags can be used to monitor the status of the eFuse, along with the current and temperature monitor signals.

- **D_OC - Overcurrent indicator:** in normal operation and during startup it is released. It is pulled down upon detection of an overload (see [Section 6.5 Current sensing and current limit](#))
- **GOK - gate ok indicator:** this indicator informs that there was a shutdown that was not commanded by the enable pin (ON/PD). In particular, this pin is pulled low when:
 - too low input voltage: V_{DD} lower than UVLO threshold
 - too long start-up time: V_{OUT} does not reach 90% of V_{IN} in 200 ms
 - too long current limit: a current limit event is longer than t_{SH} (250 μs typ.)

During the startup, GOK is released once UVLO is reached, therefore it cannot be used directly as a Power Good flag.

6.9 Diagnostic functions and protections

The STEF12H60 embeds several internal diagnostic features that prevent fault condition induced internally that may affect the application (refer to [Table 5. Electrical characteristics](#)):

- Power MOSFET gate leakage check during startup and normal operation ($V_{\text{Gate}} - V_{\text{IN}} < 5.6 \text{ V}$)
- Gate shorted-to- V_{IN}
- Drain to source short (disabled mode)
- V_{OUT} too low ($V_{\text{OUT}} < 90\%$ of V_{IN}) after soft-start
- V_{OUT} does not reach 90% of V_{IN} in 200 ms during startup
- Charge pump error
- Pull-down circuit error

In any case of fault GOK indicator is pulled down and the soft-start capacitor is discharged.

6.10 Latch (STEF12H60PUR) and auto-retry versions (STEF12H60APUR)

The STEF12H60 electronic fuse is offered in two variants that differ in how the device reacts after a fault condition (see [Section 6.8 Status indicators and fault conditions](#) and [Section 6.9 Diagnostic functions and protections](#)). In particular, the STEF12H60PUR latches off after a fault and can be reset by pulling the V_{DD} pin below the UVLO threshold or by re-cycling the supply voltage. The STEF12H60APUR instead stays in OFF mode for 1 s. (T_{Retry}) and after restarts automatically, initiating a soft-start cycle. The number of restart cycles is not internally limited.

7 Typical characteristics

($C_{IN} = 1 \mu F$; $C_{OUT} = 10 \mu F$, $T_J = 25^\circ C$ unless otherwise specified)

Figure 6. Quiescent current vs. temperature

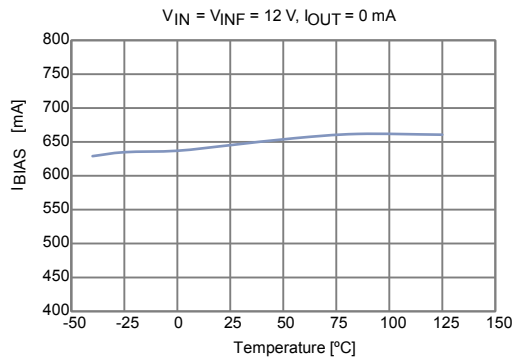


Figure 7. Shutdown current vs. temperature

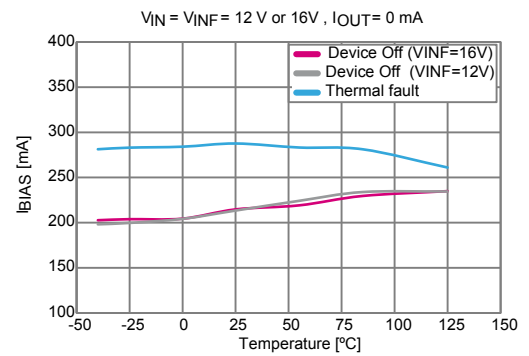


Figure 8. I_{MON} gain accuracy vs. load current and temperature

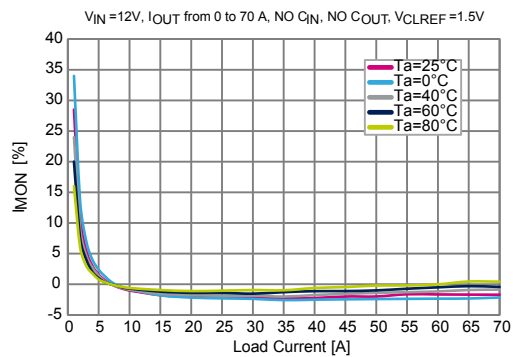


Figure 9. I_{MON} current vs. load current

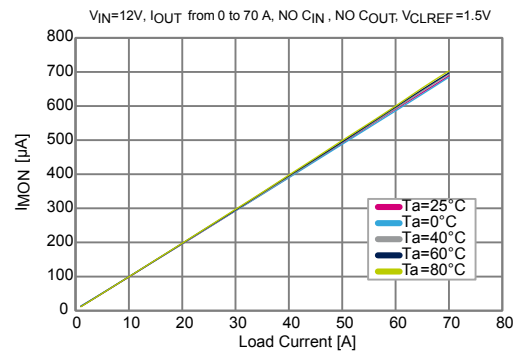


Figure 10. CS current vs. temperature

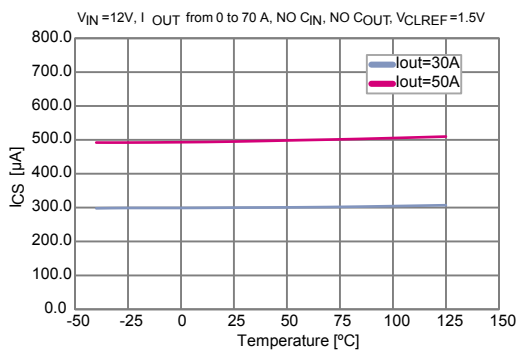


Figure 11. V_{CLREF} threshold vs. temperature

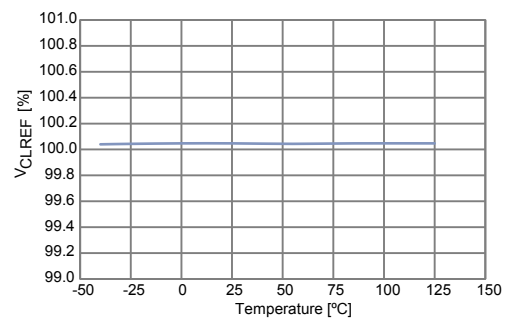


Figure 12. CLREF pin bias current vs. temperature

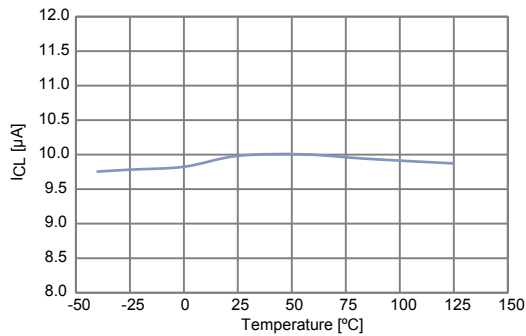


Figure 13. V_{DD} voltage vs. temperature

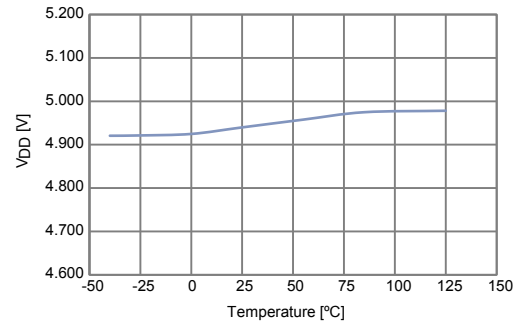


Figure 14. V_{TEMP} voltage vs. temperature

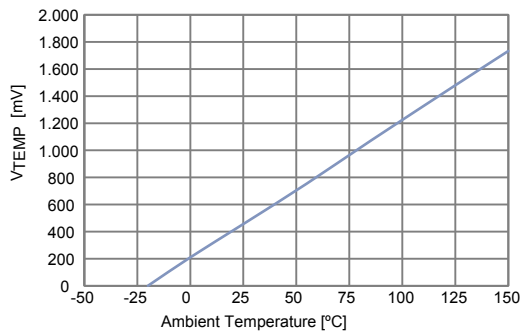


Figure 15. UVLO thresholds vs. temperature

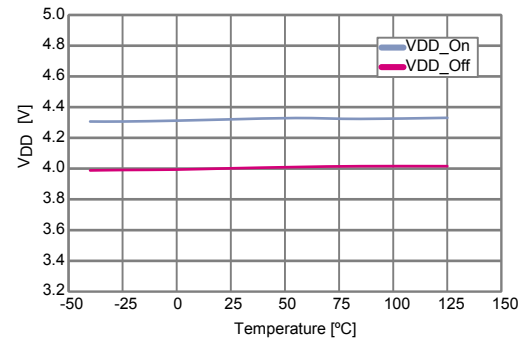


Figure 16. ON/PD thresholds vs. temperature

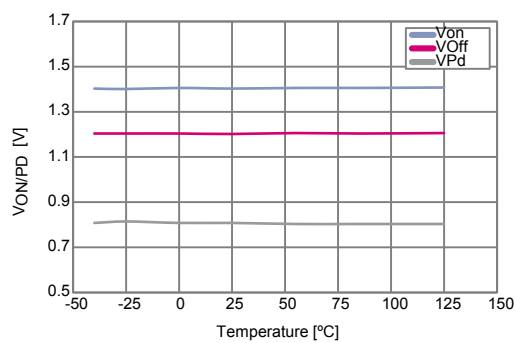


Figure 17. ON/PD pin current vs. temperature

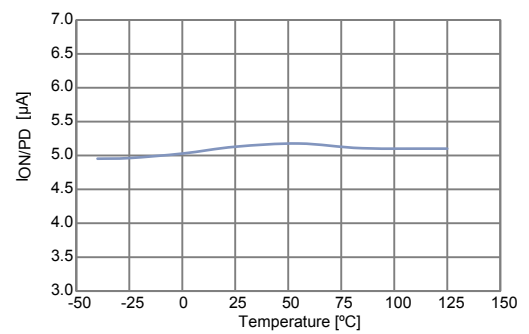


Figure 18. SS pin bias current vs. temperature

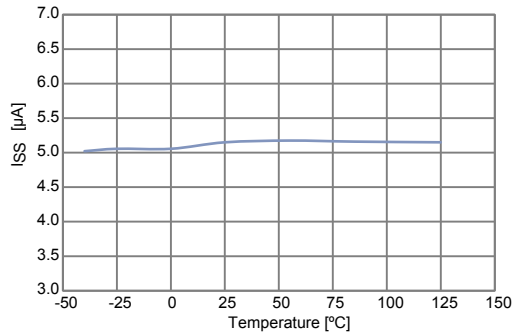


Figure 19. Turn-on initial delay vs. temperature

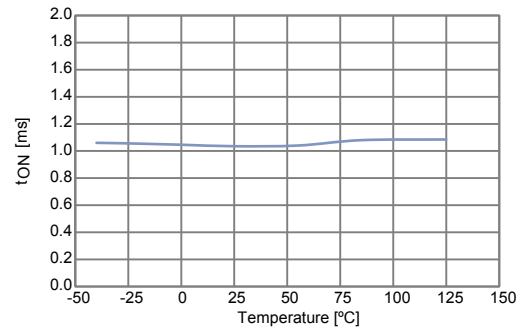


Figure 20. On-resistance vs. temperature

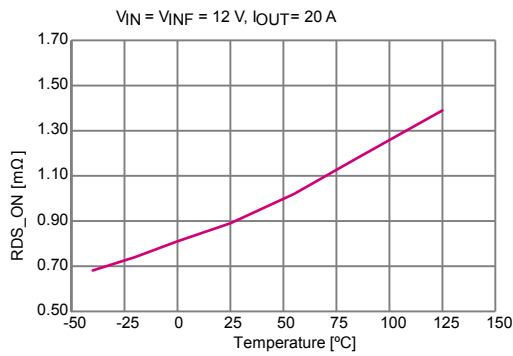


Figure 21. Off-state leakage current vs. temperature

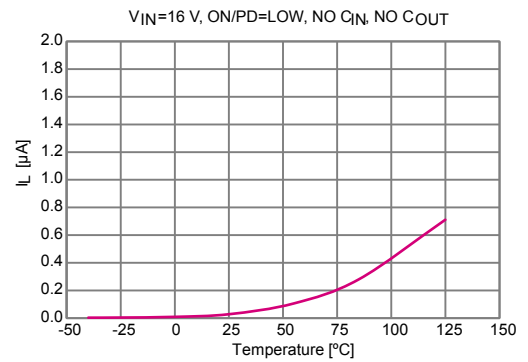


Figure 22. Startup by V_{IN} (no load)

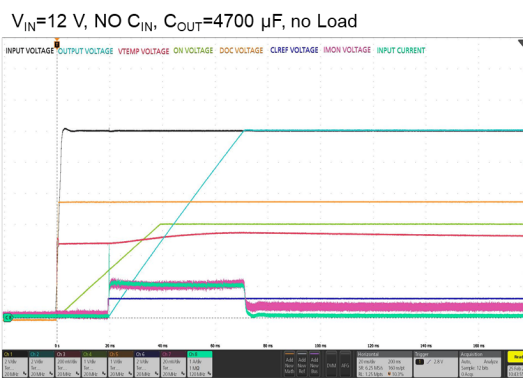


Figure 23. Shutdown by V_{IN} (no load)

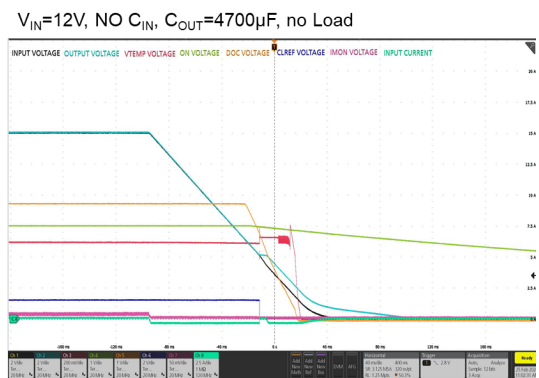


Figure 24. Startup by V_{IN} ($C_{OUT} = 6200 \mu\text{F}$, no load)

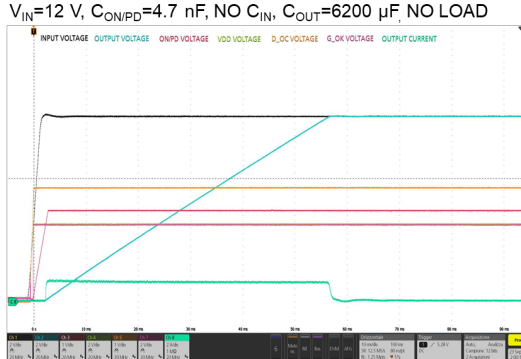


Figure 25. Startup by V_{IN} ($C_{OUT} = 6200 \mu\text{F}$, 15 A, res. load)

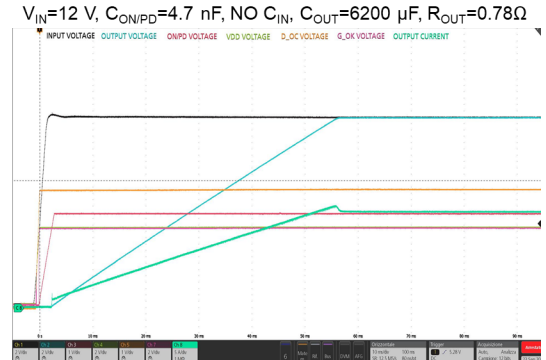


Figure 26. Startup by ON/PD (no load)

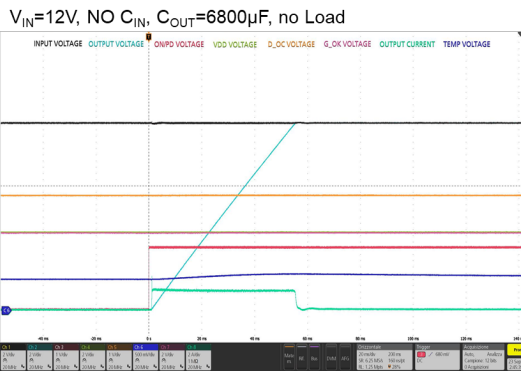


Figure 27. Shutdown by ON/PD (no load)

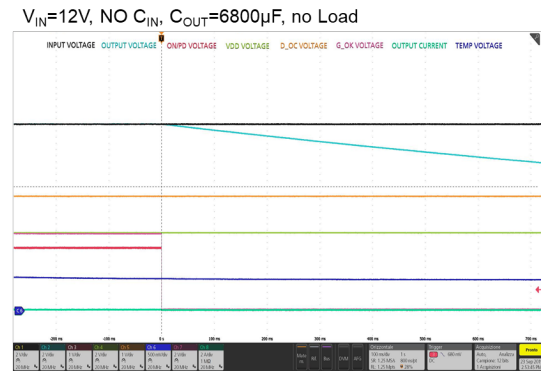


Figure 28. Start-up by ON/PD ($I_{OUT} = 15\text{ A}$, $C_{OUT} = 6800 \mu\text{F}$)

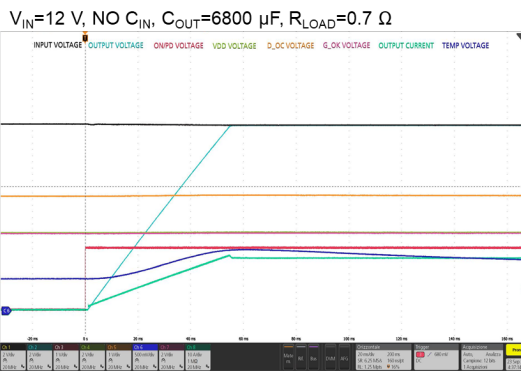


Figure 29. Shutdown by ON/PD ($I_{OUT} = 15\text{ A}$, $C_{OUT} = 6800 \mu\text{F}$)

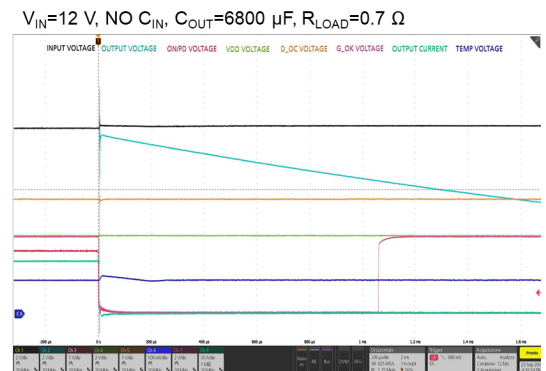


Figure 30. Start-up into output short-circuit

$V_{IN} = 12.5\text{ V}$, $C_{ON/PD} = 200\text{ nF}$, NO C_{IN} , NO C_{OUT} , $R_{LOAD} = 0\ \Omega$, $GOK = V_{DD}$

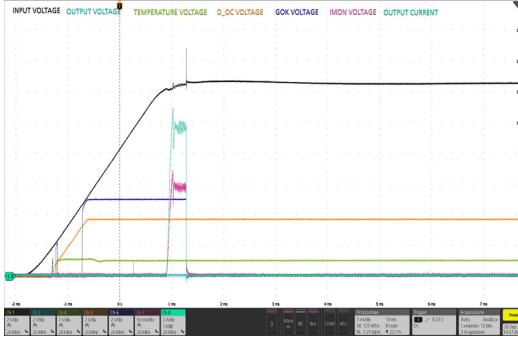
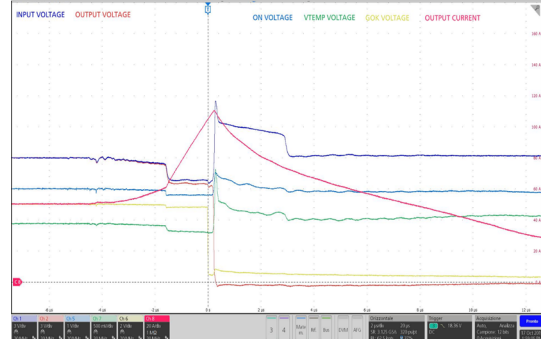


Figure 31. Output short-circuit during operation

$V_{IN} = 12\text{ V}$, $V_{OUT} = \text{from } 12\text{ V to } 0\text{ V}$, $GOK = 5\text{ V}$, $T_a = 70\text{ }^\circ\text{C}$



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 VFQFPN (5X5X0.95) 32L package information

Figure 32. VFQFPN (5X5X0.95) 32L package outline

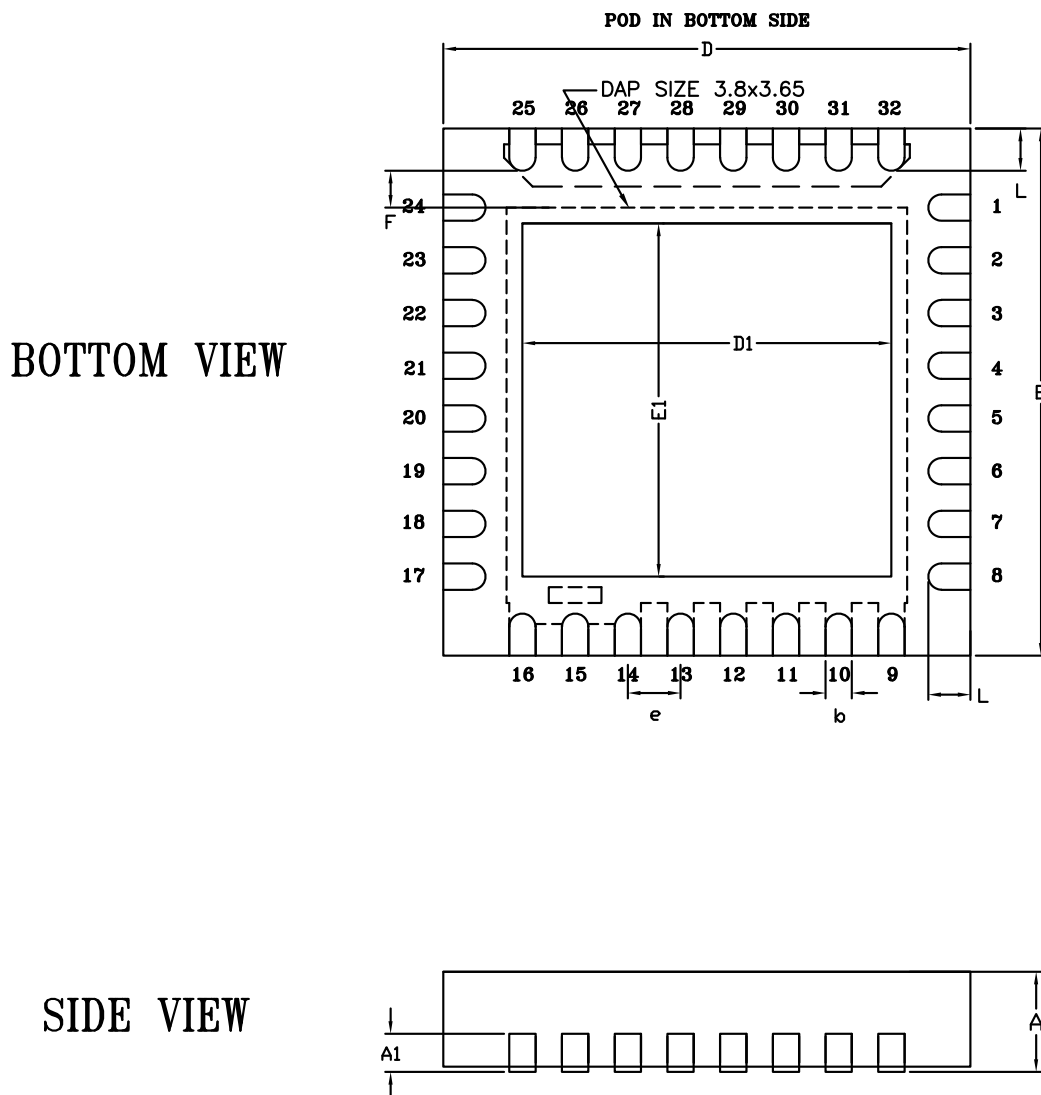
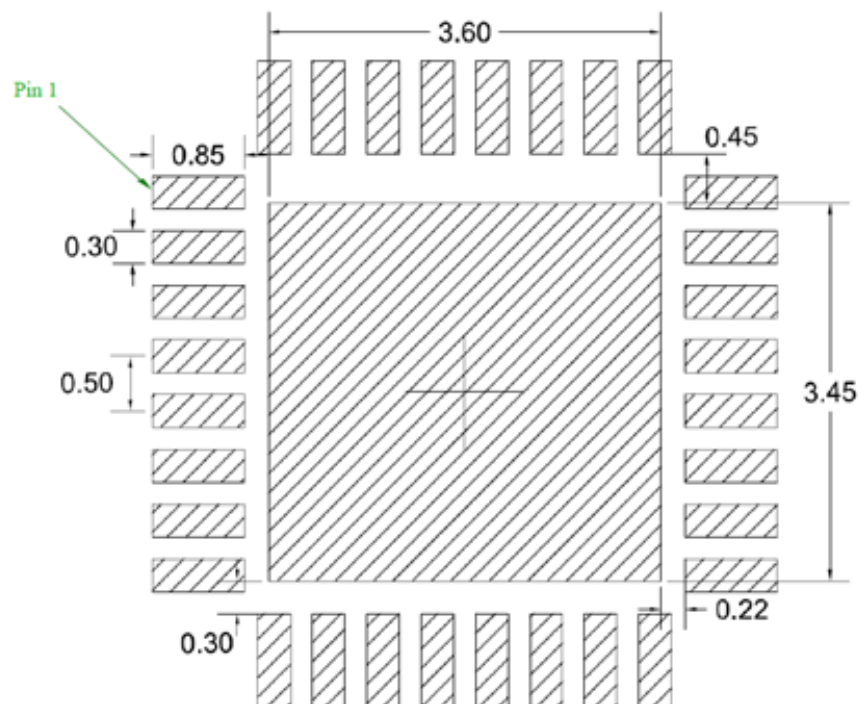


Table 7. VFQFPN (5X5X0.95) 32L package mechanical data

| Dim. | mm | | |
|------|------|------|------|
| | Min. | Typ. | Max. |
| A | 0.90 | 0.95 | 1 |
| A1 | | 0.20 | |
| D | 4.90 | 5.00 | 5.10 |
| D1 | 3.40 | 3.50 | 3.60 |
| E | 4.90 | 5.00 | 5.10 |
| E1 | 3.25 | 3.35 | 3.45 |
| e | | 0.50 | |
| F | | 0.35 | |
| b | 0.20 | 0.25 | 0.30 |
| L | 0.30 | 0.40 | 0.50 |

Figure 33. VFQFPN (5X5X0.95) 32L recommended footprint



8.2 VFQFPN (5X5X0.95) 32L packing information

Figure 34. Carrier tape

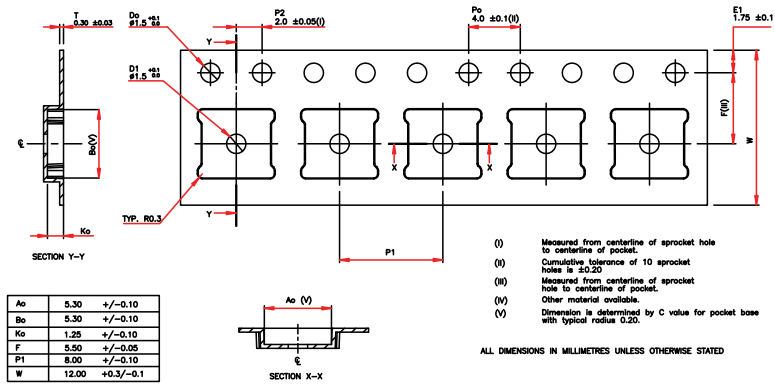


Figure 35. Pin 1 orientation in tape

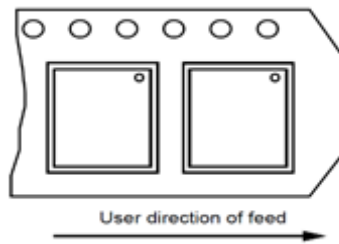


Figure 36. VFQFPN (5X5X0.95) reel outline

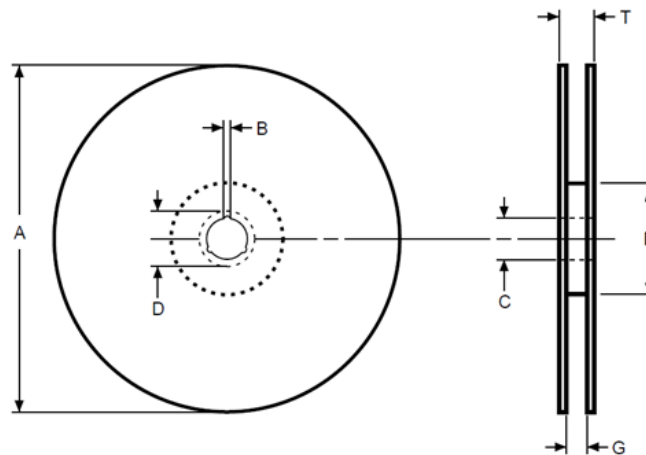


Table 8. VFQFPN (5X5X0.95) reel data

| Reel size | Tape width | A (max.) | B (min.) | C | D (min.) | G (max.) | N (min.) | T (max.) | Unit |
|-----------|------------|----------|----------|----------|----------|----------|----------|----------|------|
| 13" | 0.90 | 330 | 1.5 | 13 ± 0.2 | 20.2 | 12.6 | 100 | 18.4 | mm |

9 Ordering information

Table 9. Order codes

| Order code | Package | Shutdown mode (latch/auto-retry) | Marking |
|---------------|-----------------------|-------------------------------------|----------|
| STEF12H60PUR | VFQFPN (5X5X0.95) 32L | Latch | EF12H60 |
| STEF12H60APUR | VFQFPN (5X5X0.95) 32L | Auto-retry | EF12H60A |

Revision history

Table 10. Document revision history

| Date | Version | Changes |
|-------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 24-Feb-2020 | 1 | Initial release. |
| 08-May-2020 | 2 | Updated cover page, Table 1. Pin configuration, Table 2. Absolute maximum ratings, Table 4. Recommended operating conditions, Table 5. Electrical characteristics. Updated Section 6 Device functional description, Section 6.3 Soft-start, Section 6.5 Current sensing and current limit. |
| 12-May-2020 | 3 | First public release. Updated Figure 34. Carrier tape. |
| 03-Aug-2020 | 4 | Updated Table 1. Pin configuration. Updated Figure 3. Typical application diagram (external controller used for CLREF pin) and Figure 4. Typical application diagram (current limit fixed via R _{CL}). Updated Section 6.7 Temperature monitor and thermal shutdown functions. |

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