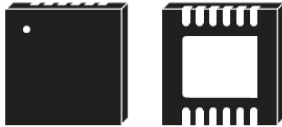


Electronic switch for 12 V, 5 V and 3.3 V buses



DFN12 3x3 mm

Features

- Power Input voltage from 0.5 V to 13.5 V
- Analog input voltage from 3.0 V to 13.5 V
- 17 A max DC output current
- Embedded 4.5 mΩ N-channel MOSFET
- Internal output discharge path
- Power Good
- Soft-start controlled with external capacitor
- Undervoltage lockout
- Short-circuit protection
- Thermal protection
- Operating junction temperature range: -40 °C to 125 °C

Application

- Bus protection
- Hot-swap and peripheral port protection
- Telecom, Networking and Industrial equipment
- Servers and Gateways

Maturity status link

[STEL12H24](#)

Description

The STEL12H24 is an integrated controlled inrush and overcurrent protection device optimized for power bus architectures.

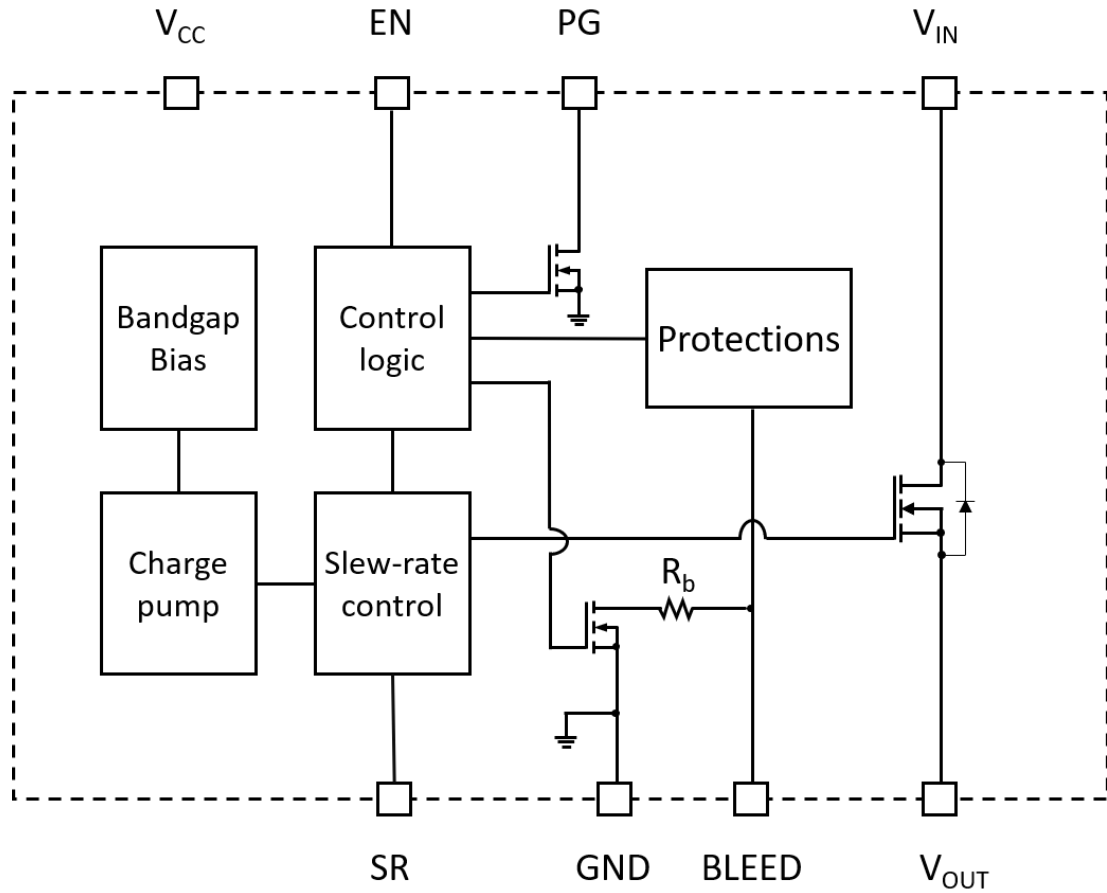
When connected to a 12 V, 5 V or 3.3 V power rail, it is able to limit the inrush current, detect input voltage faults and short-circuit conditions and signal these events via a Power Good output.

The low $R_{DS(ON)}$ value of the integrated MOSFET guarantees these conditions and low power dissipation during normal operation.

The device is available in a DFN12 leads 3 x 3 mm.

1 Diagram

Figure 1. Block diagram



2 Pin configuration

Figure 2. Pin connection (top view)

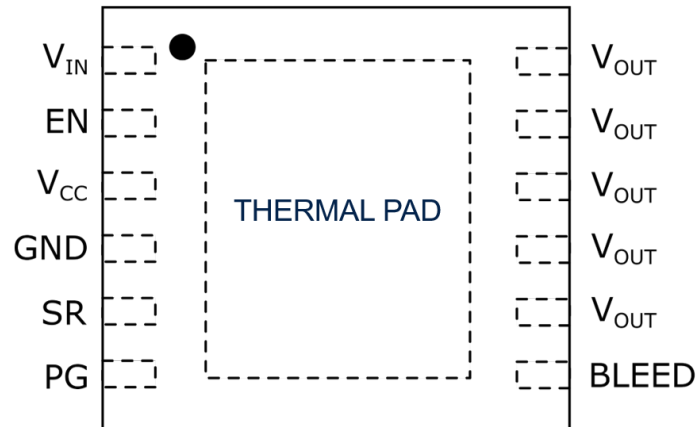
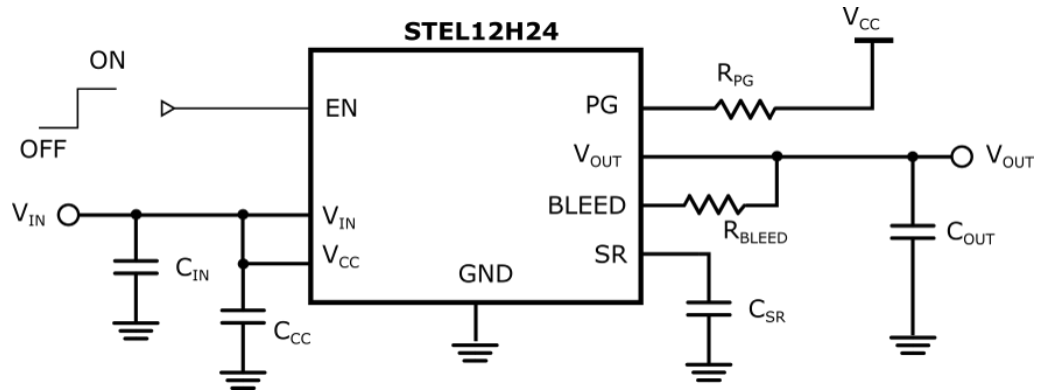


Table 1. Pin description

Pin #	Symbol	Function
1	V_{IN}	MOSFET drain, to be connected to the thermal pad.
2	EN	Enable pin. When High the MOSFET is turned on. This pin has internal pull down resistor to GND.
3	V_{CC}	Supply voltage for the control logic.
4	GND	Ground
5	SR	Slew rate control. Connect a capacitor with a nominal value between 100 nF and 1 μ F.
6	PG	Open drain Power Good pin. High when the MOSFET gate is fully charged.
7	BLEED	Load discharge connection. To be connected to V_{OUT} directly or through an external resistor.
8	V_{OUT}	Source of the MOSFET. To be connected to the load.
9		
10		
11		
12		
Thermal Pad	V_{IN}	MOSFET drain.

3 Typical application circuit

Figure 3. Typical application

Table 2. Typical application components

Symbol	Value		Description	Note
C_{IN}	0.1 μ F		Input capacitor	Higher value might be needed in case of noisy input voltage
C_{CC}	0.1 μ F		Control logic bypass capacitor	
R_{BLEED}	$V_{IN} = 12$ V	560 Ω	Minimum bleed resistor	
	$V_{IN} = 5$ V	200 Ω		
	$V_{IN} = 3.3$ V	100 Ω		
C_{SR}	100 nF		Slew rate capacitor	C_{SR} of 100 nF minimum nominal value must be always connected
R_{PG}	100 k Ω		Power Good pull-up resistor	
C_{OUT}	10 μ F		Output capacitor	

4 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	Input voltage	-0.3 to 20	V
$V_{OUT, BLEED}$	Output and bleed pin voltage	-0.3 to 20	V
P_{BLEED}	Maximum power on R_b internal resistance	160	mW
I_{BLEED}	Maximum sink current on R_b internal resistance	20	mA
V_{CC}	Supply voltage	-0.3 to 20	V
V_{EN}	Enable input voltage	-0.3 to $V_{CC} + 0.3$	V
V_{SR}	Slew rate pin voltage	-0.3 to 5	V
V_{PG}	Power Good pin Voltage	-0.3 to $V_{CC} + 0.3$	V
I_{OUT}	DC output current	17	A
T_{STG}	Storage temperature range	- 40 to 150	°C
T_{OP}	Operating junction temperature range	- 40 to 125	°C

Table 4. Thermal data

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal resistance junction-ambient	37	°C/W
$R_{\theta JC}$	Thermal resistance (top/bottom) junction-case	0.28	°C/W
$R_{\theta JB}$	Thermal resistance junction-board	11.2	°C/W
ψ_{JT}	Characterization parameter junction-top	0.63	°C/W
ψ_{JB}	Characterization parameter junction-board	11.2	°C/W

1. JEDEC still air natural convection test as per JESD 51-2 A, at ambient temperature of 25 °C by using JEDEC (JESD 51-7) 4L PCB FR4 board (with 2 PCB Thermal vias).

Table 5. ESD performance

Symbol	Parameter	Test conditions	Value	Unit
ESD	ESD protection voltage	HBM	2	kV
		CDM	500	V

1. Rating is for all pins except for V_{IN} and V_{OUT} which are tied to the internal MOSFET's Drain and Source. Typical MOSFET ESD performance for V_{IN} and V_{OUT} should be expected and these devices should be treated as ESD sensitive.

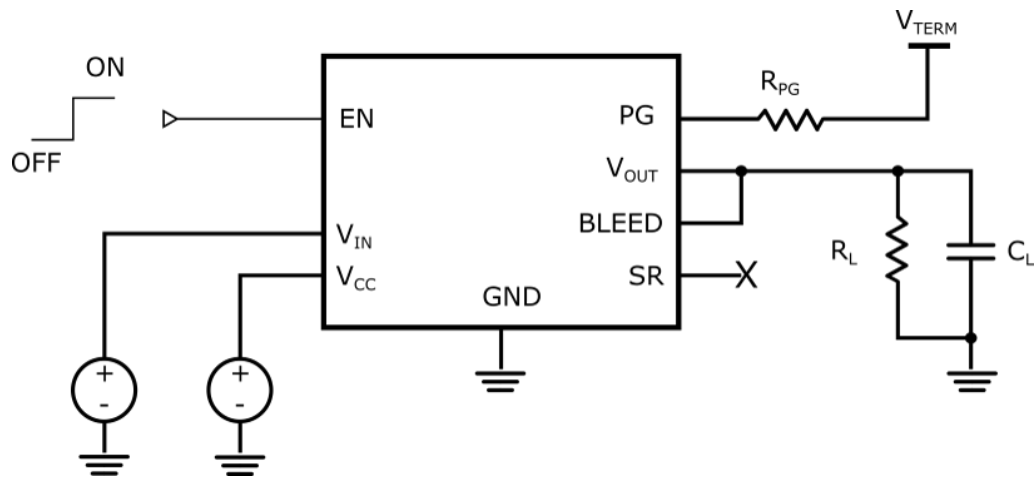
5 Electrical characteristics

$V_{CC} = 3.3\text{ V}$, $V_{IN} = 12\text{ V}$, $C_{IN} = 1\ \mu\text{F}$, $C_{OUT} = 10\ \mu\text{F}$, $V_{EN} = 3.3\text{ V}$, $R_{PG} = 100\ \text{k}\Omega$, $C_{SR} = 100\ \text{nF}$, $T_J = 25\ ^\circ\text{C}$ unless otherwise specified.

Table 6. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage	$-40\ ^\circ\text{C} \leq T_J \leq 125\ ^\circ\text{C}$	0.5		13.5	V
V_{CC}	Operating supply voltage	$-40\ ^\circ\text{C} \leq T_J \leq 125\ ^\circ\text{C}$	3		13.5	V
$V_{IN-UVLO}$	V_{IN} undervoltage lockout	V_{IN} rising	0.25	0.35	0.45	V
		Hysteresis	20	30	50	mV
$V_{CC-UVLO}$	V_{CC} undervoltage lockout	V_{CC} rising		2.6		V
		Hysteresis		160		mV
I_{STBY}	Standby supply current	$V_{EN} = 0$; $V_{CC} = 3\text{ V}$		3	5	μA
		$V_{EN} = 0$; $V_{CC} = 5\text{ V}$		6	8	
		$V_{EN} = 0$; $V_{CC} = 12\text{ V}$		8	10	
I_{OP}	Operating supply current	$V_{EN} = V_{CC} = 3\text{ V}$; $V_{IN} = 12\text{ V}$		80	200	μA
		$V_{EN} = V_{CC} = 5.5\text{ V}$; $V_{IN} = 1.8\text{ V}$		200	300	
		$V_{EN} = V_{CC} = 12\text{ V}$; $V_{IN} = 1.8\text{ V}$		300	400	
R_{ON}	On-resistance	$V_{CC} = 3.3\text{ V}$; $V_{IN} = 1.8\text{ V}$		5	6.5	m Ω
		$V_{CC} = 3.3\text{ V}$; $V_{IN} = 5\text{ V}$		4.5	6	
		$V_{CC} = 3.3\text{ V}$; $V_{IN} = 12\text{ V}$		4.5	6	
		$V_{CC} = V_{IN} = 3.3\text{ V}$		5	6.5	
		$V_{CC} = V_{IN} = 5.0\text{ V}$		4.5	6	
		$V_{CC} = V_{IN} = 12\text{ V}$		4.5	6	
I_{LEAK}	MOSFET leakage current	$V_{EN} = 0$; $V_{IN} = 13.5\text{ V}$		0.1	1	μA
R_b	Bleed resistance	$V_{EN} = 0$; $V_{CC} = 3\text{ V}$; $V_{IN} = 0.5\text{ V}$	80	95	110	Ω
		$V_{EN} = 0$; $V_{CC} = 5\text{ V}$; $V_{IN} = 1\text{ V}$	80	95	110	
		$V_{EN} = 0$; $V_{CC} = 12\text{ V}$; $V_{IN} = 2\text{ V}$	80	95	110	
I_{BLEED}	Bleed pin leakage current	$V_{EN} = V_{CC} = 3\text{ V}$; $V_{IN} = 1.8\text{ V}$		6	8	μA
		$V_{EN} = V_{CC} = 3\text{ V}$; $V_{IN} = 12\text{ V}$		40	52	
V_{IH}	EN input high voltage	$V_{CC} = 3\text{ to }12\text{ V}$	2.0			V
V_{IL}	EN input low voltage	$V_{CC} = 3\text{ to }12\text{ V}$			0.4	V
I_{IL}	EN input leakage current	$V_{EN} = 0\text{ V}$		10	100	nA
R_{PD}	EN pull down resistance	$V_{CC} = 3.3\text{ V}$, $V_{IN} = 3.3\text{ V}$	100	130	160	k Ω
V_{OL}	PG low voltage level	$V_{CC} = 3\text{ V}$; $I_{SINK} = 5\text{ mA}$			0.2	V
I_{OH}	PG leakage current	$V_{CC} = 3\text{ V}$; $V_{TERM} = 3.3\text{ V}$ (see Figure 4)		10	100	nA
K_{SR}	Slew rate constant	$V_{CC} = 3\text{ V}$	21	30	40	μA
		$V_{CC} = 12\text{ V}$	28	36	44	

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SC}	Short-circuit protection threshold	$V_{CC} = 3\text{ V}; V_{IN} = 0.5\text{ V}$	240	260	280	mV
		$V_{CC} = 3\text{ V}; V_{IN} = 13.5\text{ V}$	240	260	280	
OVP	Overshoot protection threshold		17	17.5		V
T_{SHDN}	Thermal shutdown			145		°C
	Hysteresis			18		

Figure 4. Switching characteristics test circuit

Table 7. Switching characteristics table

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
SR	Output slew rate	$V_{CC} = 3.3\text{ V}; V_{IN} = 1.8\text{ V}$		2.94		kV/s
		$V_{CC} = 5.0\text{ V}; V_{IN} = 1.8\text{ V}$		2.9		
		$V_{CC} = 3.3\text{ V}; V_{IN} = 12\text{ V}$		3		
		$V_{CC} = 5.0\text{ V}; V_{IN} = 12\text{ V}$		3.2		
		$V_{CC} = V_{IN} = 3.3\text{ V}$		2.9		
		$V_{CC} = V_{IN} = 5.0\text{ V}$		3.2		
		$V_{CC} = V_{IN} = 12\text{ V}$		3.6		
T_{ON}	Turn-on delay	$V_{CC} = 3.3\text{ V}; V_{IN} = 1.8\text{ V}$		1.5		ms
		$V_{CC} = 5.0\text{ V}; V_{IN} = 1.8\text{ V}$		1.7		
		$V_{CC} = 3.3\text{ V}; V_{IN} = 12\text{ V}$		1.7		
		$V_{CC} = 5.0\text{ V}; V_{IN} = 12\text{ V}$		1.93		
		$V_{CC} = V_{IN} = 3.3\text{ V}$		1.5		
		$V_{CC} = V_{IN} = 5.0\text{ V}$		1.8		
		$V_{CC} = V_{IN} = 12\text{ V}$		1.8		
T_{OFF}	Turn-off delay	$V_{CC} = 3.3\text{ V}; V_{IN} = 1.8\text{ V}$		100		µs
		$V_{CC} = 5.0\text{ V}; V_{IN} = 1.8\text{ V}$		100		

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T _{OFF}	Turn-off delay	V _{CC} = 3.3 V; V _{IN} = 12 V		110		μs
		V _{CC} = 5.0 V; V _{IN} = 12 V		100		
		V _{CC} = V _{IN} = 3.3 V		100		
		V _{CC} = V _{IN} = 5.0 V		100		
		V _{CC} = V _{IN} = 12 V		100		
T _{PG-ON}	Power Good turn-on time	V _{CC} = 3.3 V; V _{IN} = 1.8 V		2.5		ms
		V _{CC} = 5.0 V; V _{IN} = 1.8 V		3		
		V _{CC} = 3.3 V; V _{IN} = 12 V		6		
		V _{CC} = 5.0 V; V _{IN} = 12 V		6		
		V _{CC} = V _{IN} = 3.3 V		3		
		V _{CC} = V _{IN} = 5.0 V		3		
		V _{CC} = V _{IN} = 12 V		5		
T _{PG-OFF}	Power Good turn-off time	V _{CC} = 3.3 V; V _{IN} = 1.8 V		2.6		μs
		V _{CC} = 5.0 V; V _{IN} = 1.8 V		3		
		V _{CC} = 3.3 V; V _{IN} = 12 V		2.56		
		V _{CC} = 5.0 V; V _{IN} = 12 V		3		
		V _{CC} = V _{IN} = 3.3 V		2.5		
		V _{CC} = V _{IN} = 5.0 V		3		
		V _{CC} = V _{IN} = 12 V		2.5		
T _{SC-OFF}	Short-circuit delay time	V _{CC} = 3.3 V; V _{IN} = 1.8 V		500		ns
		V _{CC} = 5.0 V; V _{IN} = 1.8 V		500		
		V _{CC} = 3.3 V; V _{IN} = 12 V		500		
		V _{CC} = 5.0 V; V _{IN} = 12 V		500		
		V _{CC} = V _{IN} = 3.3 V		500		
		V _{CC} = V _{IN} = 5.0 V		500		
		V _{CC} = V _{IN} = 12 V		500		

Figure 5. Switching characteristics timing

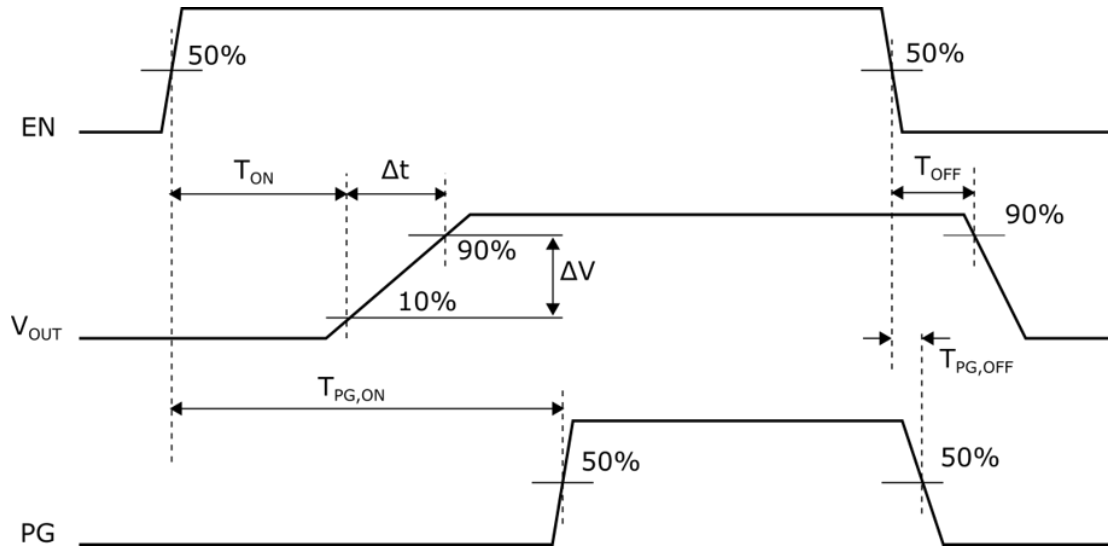
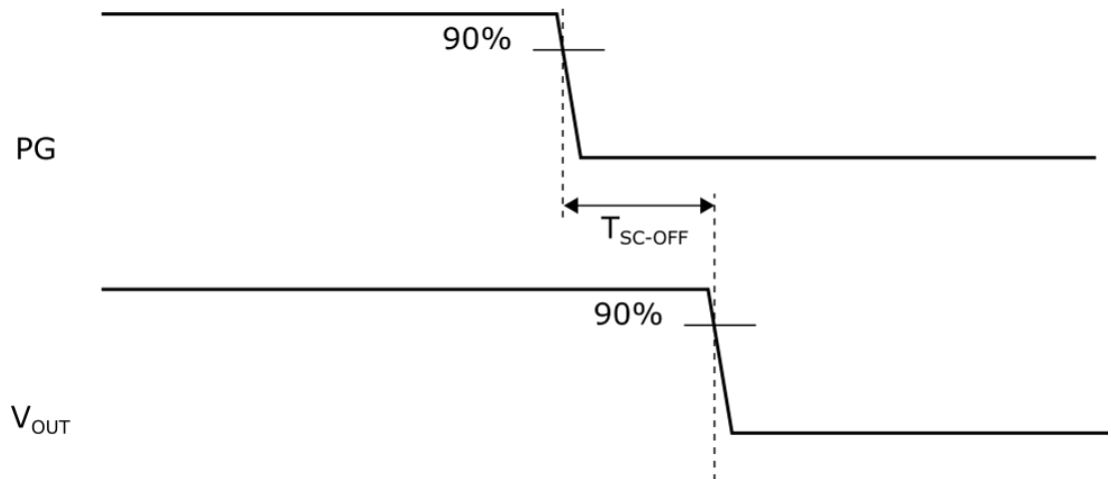


Figure 6. Short-circuit timing



6 Application information

6.1 Enable pin

If the V_{CC} is inside its operating range, the STEL12H24 is enabled by driving the EN pin above the V_{IH} threshold. When the V_{IH} threshold is crossed, the internal blocks are turned on and, after T_{ON} time, the soft-start procedure to activate the MOSFET starts.

6.2 Undervoltage lockout

The STEL12H24 has two UVLO circuits: one on the V_{CC} pin and another on V_{IN} pin.

When the undervoltage lockout threshold $V_{CC-UVLO}$ is crossed (V_{CC} rising), the STEL12H24 enables a timer of 1.2 ms, which activates a discharge circuit for the soft-start cap. This avoids inrush current if the soft-start capacitor remained charged before the $V_{CC-UVLO}$ threshold was crossed.

The $V_{IN-UVLO}$ acts on the V_{IN} pin. If the voltage on the V_{IN} pin is below $V_{IN-UVLO}$ threshold, the MOSFET is OFF and the discharge circuit is activated.

Both the UVLO circuits are disabled when EN pin is low.

6.3 Quick discharge

The STEL12H24 has an internal discharge switch and resistor connected between BLEED pin and GND which allows discharging the load capacitor when the MOSFET is turned off (please refer to [Figure 1](#)). The discharge switch and the MOSFET work always in an opposite manner, when one is ON the other is OFF and vice versa.

The BLEED pin must be connected to V_{OUT} through an external series resistor R_{BLEED} . The series resistor minimum value must be calculated in order to limit the power dissipation on the internal R_b below 160 mW and to limit its current to 20 mA maximum.

The minimum R_{BLEED} can be calculated using the following formula:

$$R_{BLEED} [k\Omega] = V_{IN} / 20 - R_b (\text{min}).$$

6.4 Power Good

The Power Good (PG) pin provides the information about the gate of the MOSFET. It is an open-drain output that goes high when the gate of the MOSFET is fully charged thus giving indication about the operation of the STEL12H24. For whatever reason the MOSFET is turned off (Enable, Thermal protection, UVLO, OVP or short-circuit) the PG pin is pulled low. It is recommended to connect a pull-up resistor greater than 1 k Ω between PG pin and any supply voltage in the system lower than PG pin AMR.

6.5 Short-circuit protection

The STEL12H24 is protected against short-circuit condition at the output. An internal comparator monitors the voltage difference between V_{IN} and BLEED pins. When this voltage exceeds the V_{SC} threshold, the MOSFET is turned off and the discharge switch is activated. The device restarts automatically with a controlled soft-start.

The short-circuit trigger point can be reduced by connecting an external resistor between BLEED and V_{OUT} . The leakage current flowing into the BLEED pin increases the voltage drop monitored by the internal comparator thus triggering a lower short-circuit current protection.

6.6 Slew rate control

One of the key features of the STEL12H24 is the controlled ramp-up of the MOSFET current during turn-on. This feature allows to limit the inrush current in hot swap applications.

The gate voltage of the MOSFET is increased linearly by mirroring the voltage ramp on the internal soft-start capacitor which provides a default value for the ramp-up time. This time can be increased by connecting a capacitor to C_{SR} pin. The C_{SR} pin is charged with a constant current of K_{SR} so the slew rate is given by the formula:

$$SR_{EXT} = 8 \times \frac{K_{SR}}{C_{SR}} \left[V/s \right] \quad (1)$$

Where C_{SR} is the capacitor connected to SR pin.

This capacitor should have a minimum nominal value of 100 nF and cannot exceed the value of 1 μ F.

6.7 Overvoltage protection

When the input voltage reaches the OVP threshold, the MOSFET is turned off. The STEL12H24 automatically keeps monitoring the V_{IN} voltage and reactivates the MOSFET in a controlled manner when V_{IN} falls below the OVP value. An internal hysteresis avoids oscillations when V_{IN} is close to the OVP value.

6.8 Thermal shutdown

The Thermal protection acts when the junction temperature reaches the T_{SHDN} value. At this point, the MOSFET is shut down and the discharge switch is activated. As soon as the junction temperature falls below the thermal hysteresis value, the device starts again with a soft-start cycle, given that the EN stays high.

7 Typical characteristics

EN = 2 V; $C_{IN} = 1 \mu\text{F}$; $C_{OUT} = 10 \mu\text{F}$; $T_J = 25 \text{ }^\circ\text{C}$ unless otherwise specified.

Figure 7. R_{ON} vs. V_{IN}

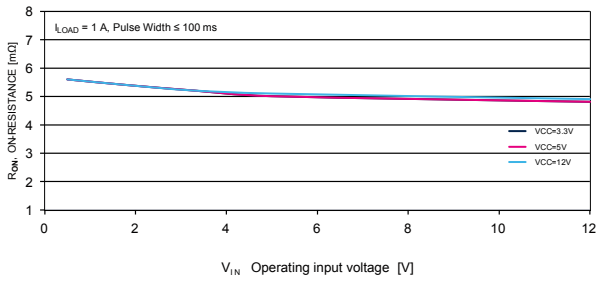


Figure 8. R_{ON} vs. temperature

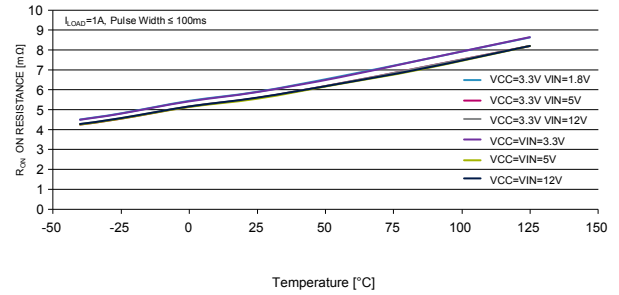


Figure 9. Standby current vs. V_{CC}

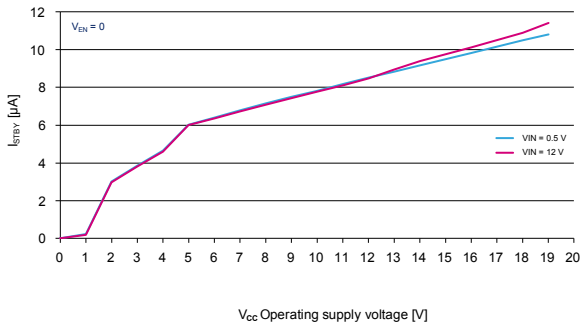


Figure 10. Standby current vs. temperature

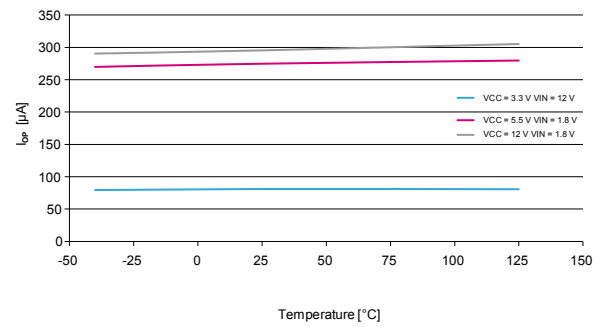


Figure 11. Supply current vs. V_{IN}

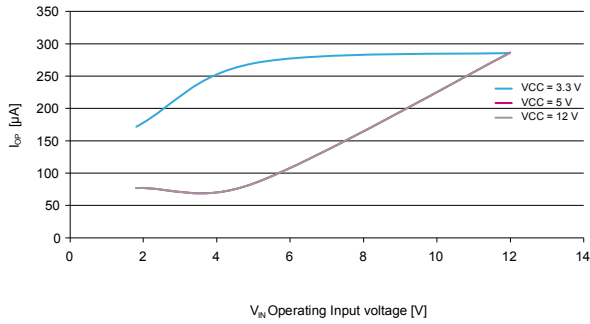


Figure 12. Supply current vs. V_{CC}

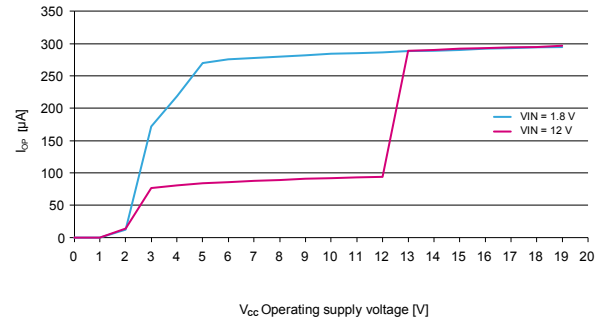


Figure 13. Supply current vs. temperature

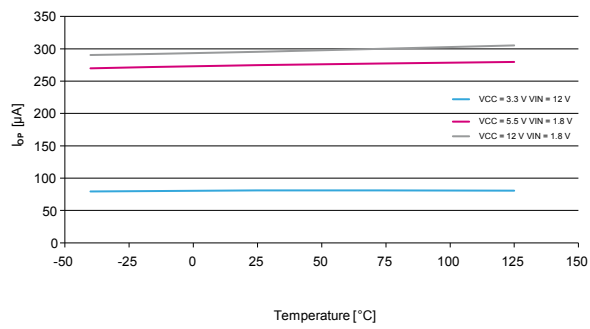


Figure 14. R_B vs. temperature

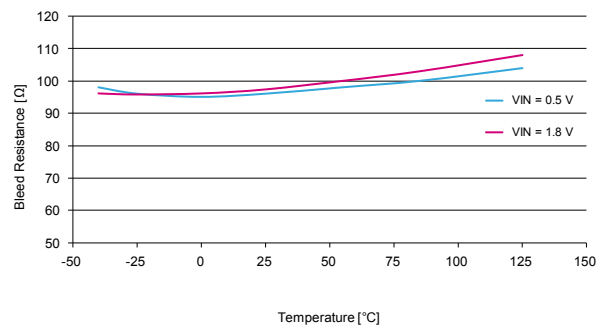


Figure 15. BLEED leakage current vs. temperature

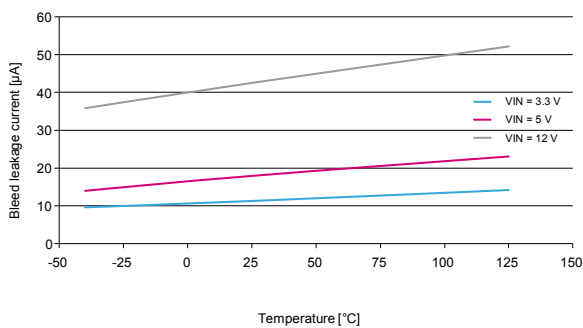


Figure 16. BLEED leakage current vs. V_{IN}

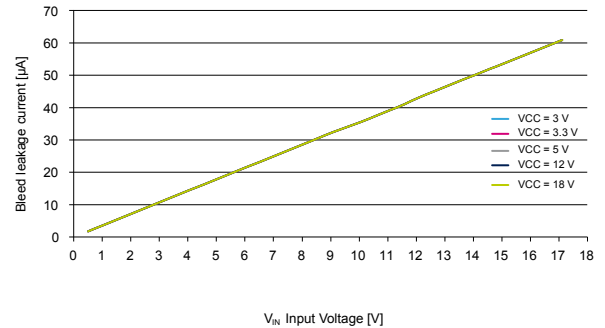


Figure 17. EN Input High/Low voltage vs. temperature

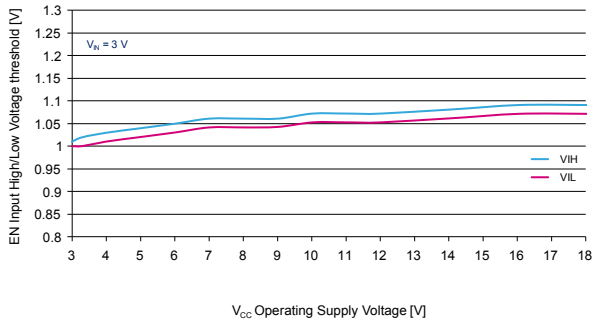


Figure 18. EN Pull-down resistance vs. temperature

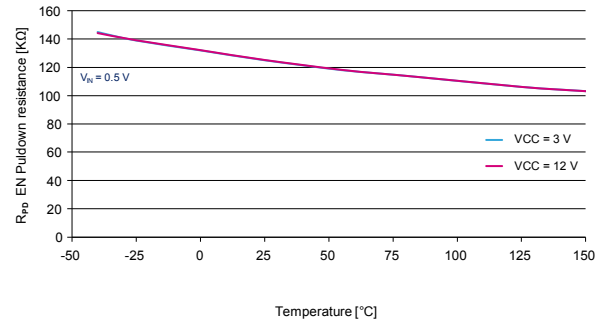


Figure 19. PG output low voltage vs. Vcc

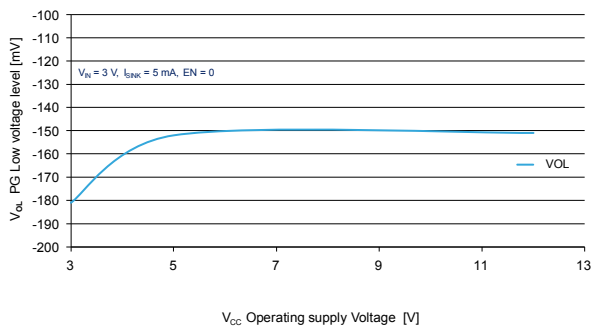


Figure 20. PG output low voltage vs. temperature

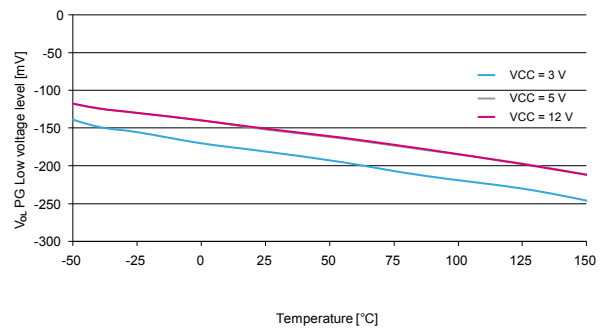


Figure 21. KSR vs. VIN

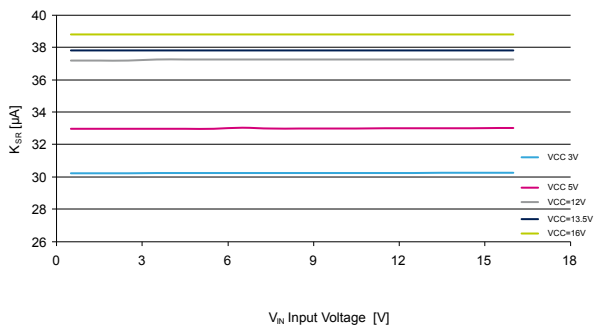


Figure 22. KSR vs. Vcc

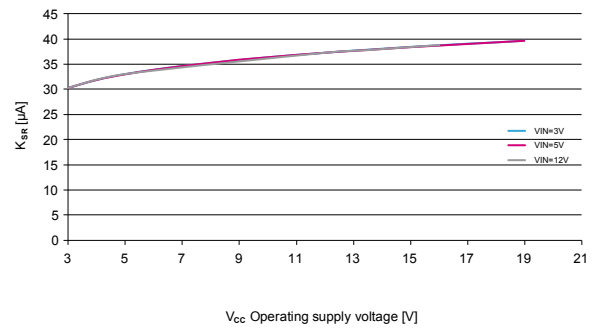


Figure 23. K_{SR} vs. temperature

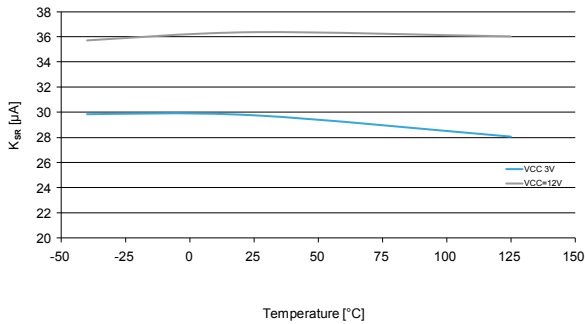


Figure 24. S_R vs. V_{CC}

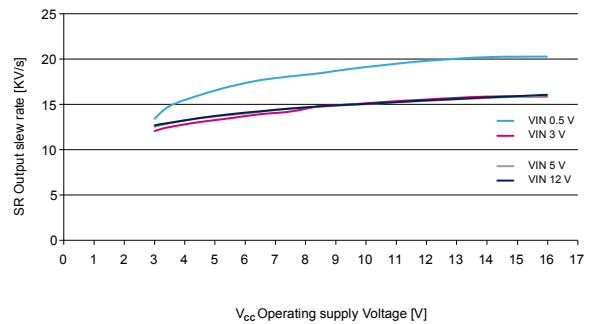


Figure 25. V_{SC} vs. V_{IN}

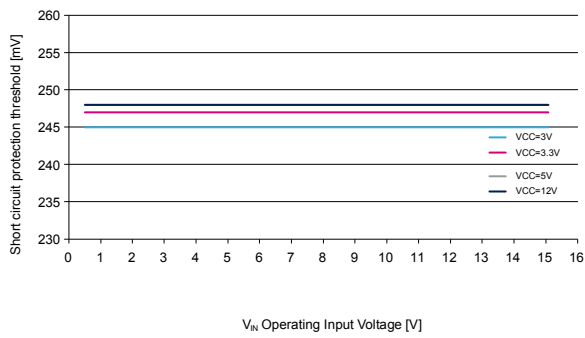


Figure 26. T_{ON} vs. V_{IN}

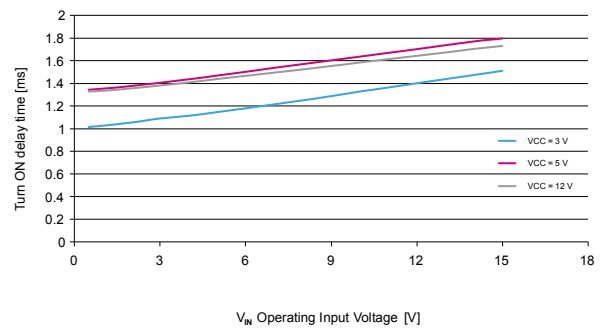


Figure 27. T_{PG-OFF} vs. V_{IN}

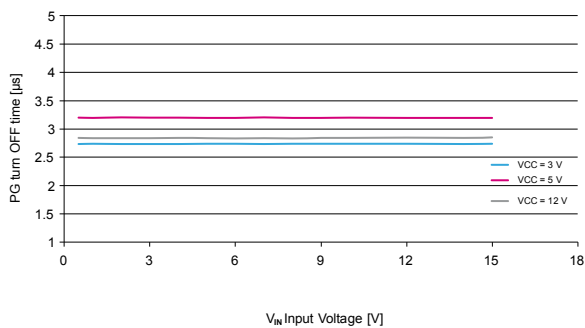


Figure 28. T_{OFF} vs. V_{IN}

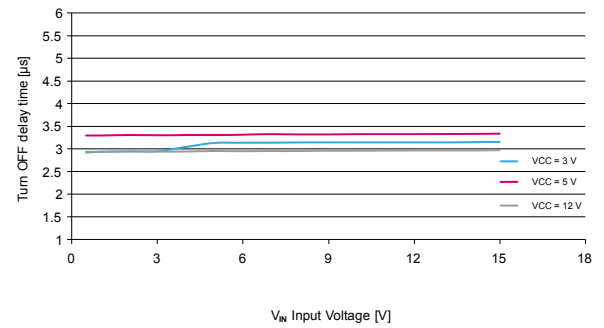


Figure 29. Mosfet leakage current vs. temperature

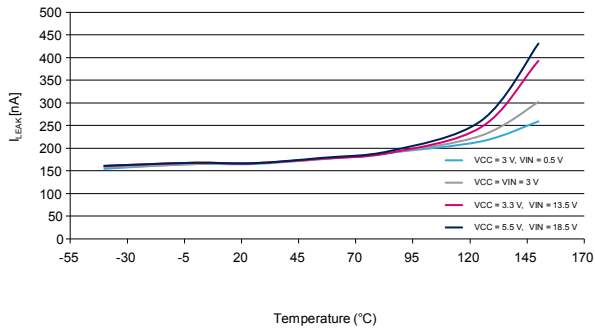


Figure 30. T_{PG-ON} vs. V_{IN}

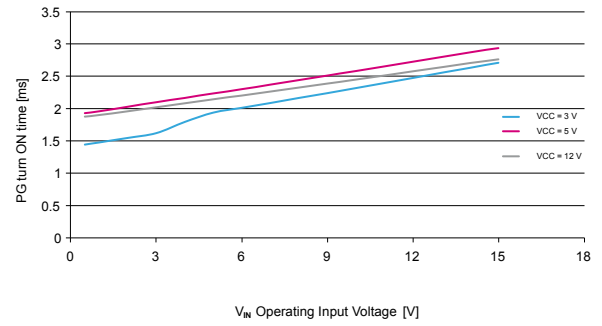


Figure 31. PG leakage current vs. V_{CC}

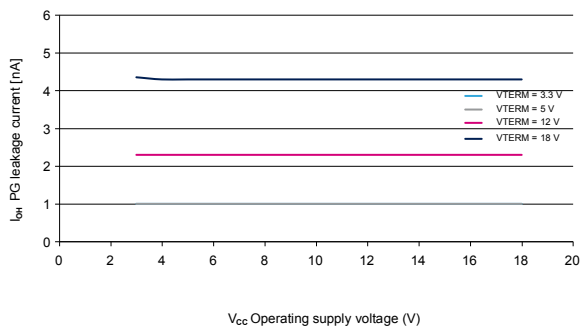
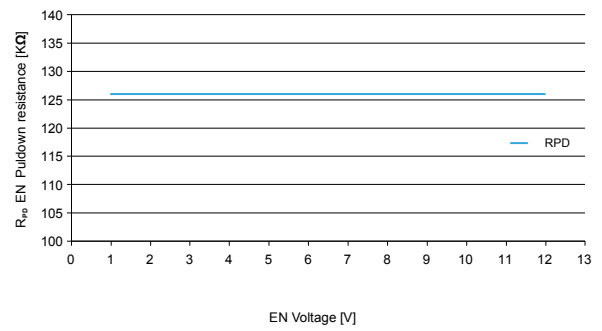


Figure 32. EN pulldown resistance vs. EN voltage



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 DFN12 (3 x 3 mm) package information

Figure 33. DFN12 (3 x 3 mm) package outline

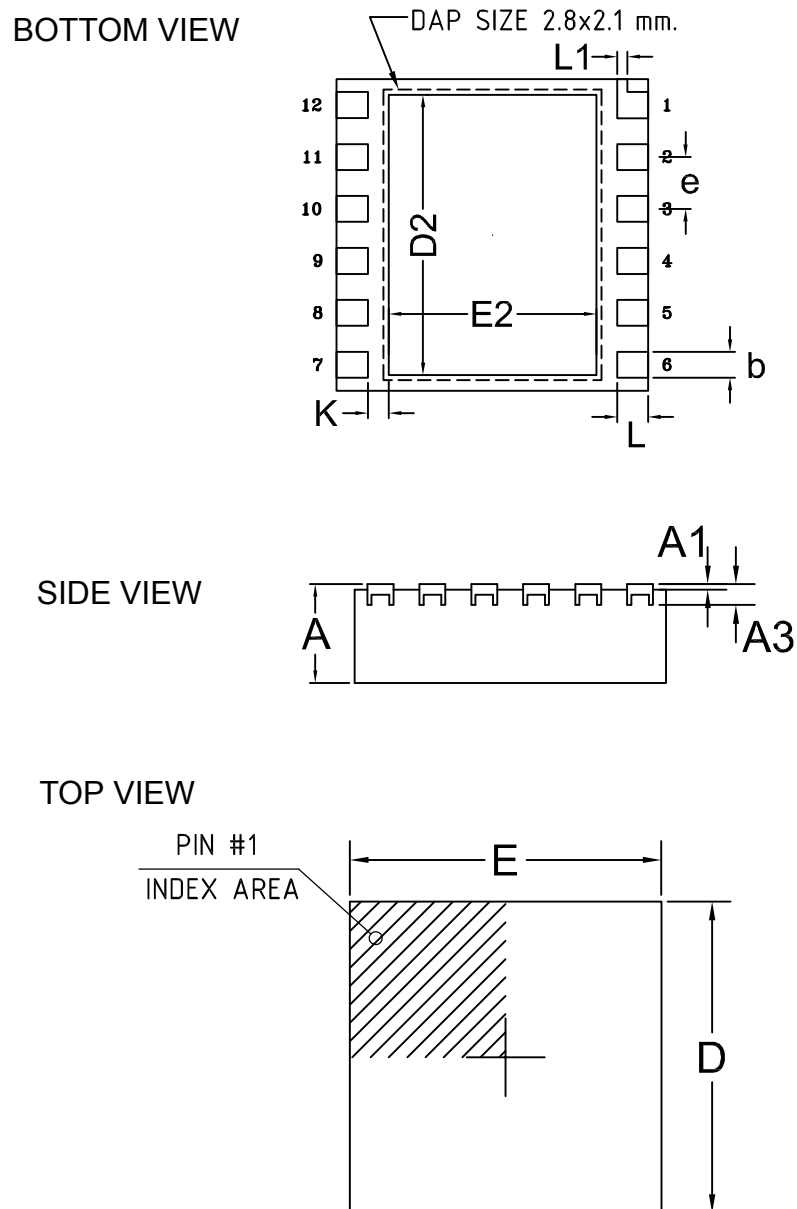
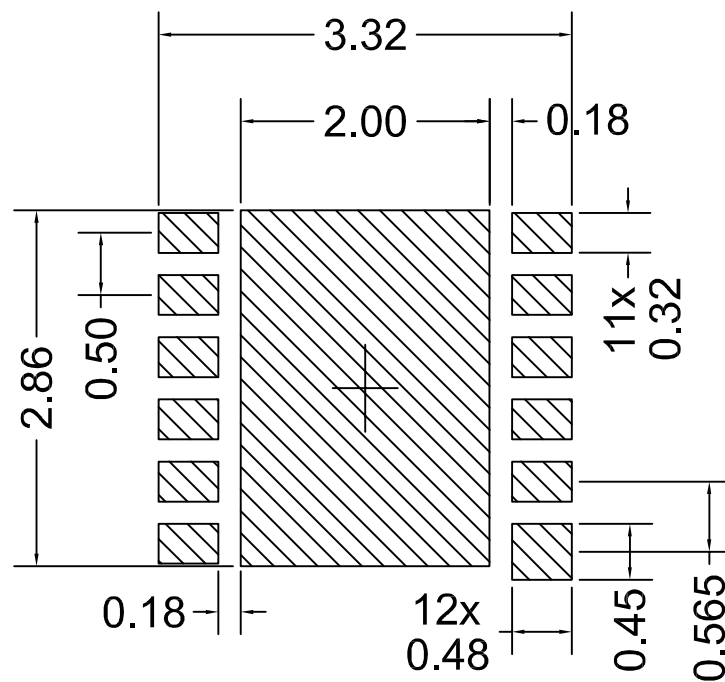


Table 8. DFN12 (3 x 3 mm) mechanical data

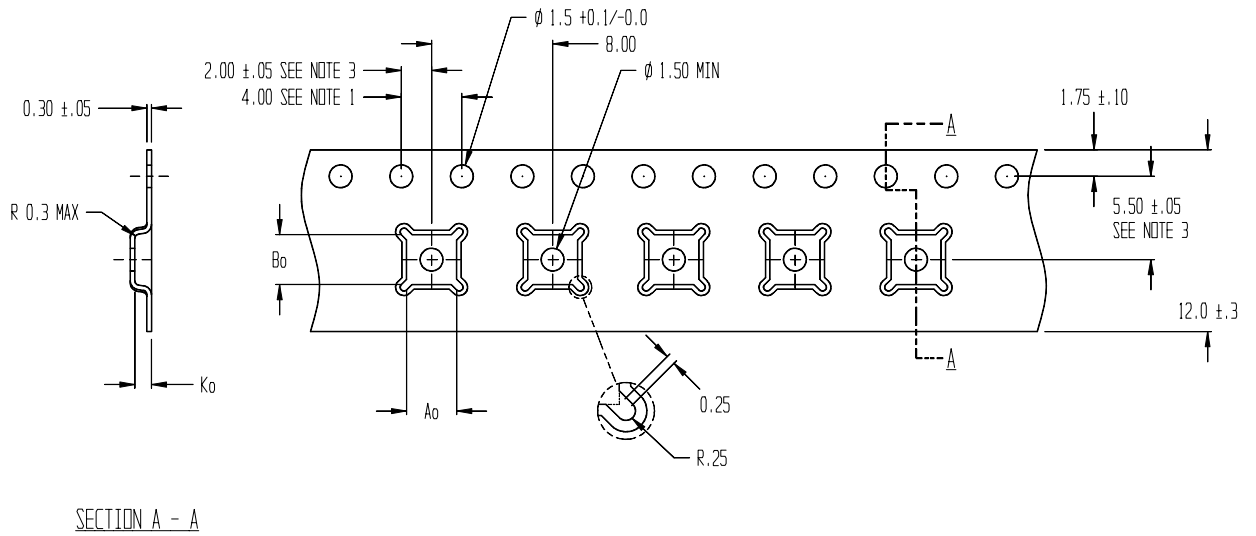
Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.85	0.90
A1	0.0	-	0.05
A3	0.203 Ref.		
b	0.20	0.25	0.30
D	2.95	3.00	3.05
D2	2.60	2.70	2.80
e	0.50 BSC		
E	2.95	3.00	3.05
E2	1.90	2.00	2.10
L	0.20	0.30	0.40
L1	0.10 Ref.		
K	0.20 Ref.		
K1	0.450 Ref.		
N	12		
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		

Figure 34. DFN12 (3 x 3 mm) recommended footprint



8.2 DFN12 (3 x 3 mm) packing information

Figure 35. DFN12 (3 x 3 mm) tape drawing



SECTION A - A

NOTES:

1. TO SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ± 0.2
2. CAMBER IN COMPLIANCE WITH EIA 481
3. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE

$A_0 = 3.30$
 $B_0 = 3.30$
 $K_0 = 1.10$

Figure 36. DFN12 (3 x 3 mm) reel oriented

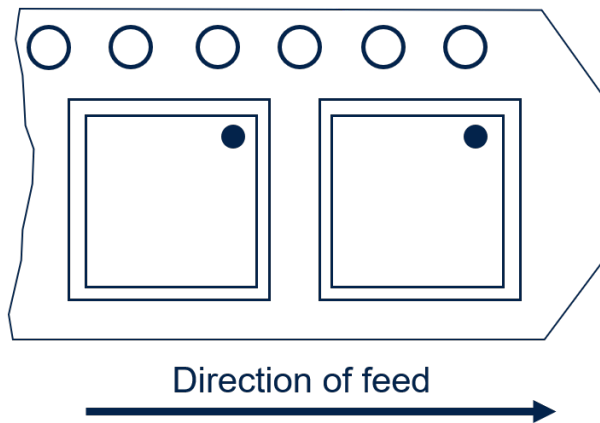
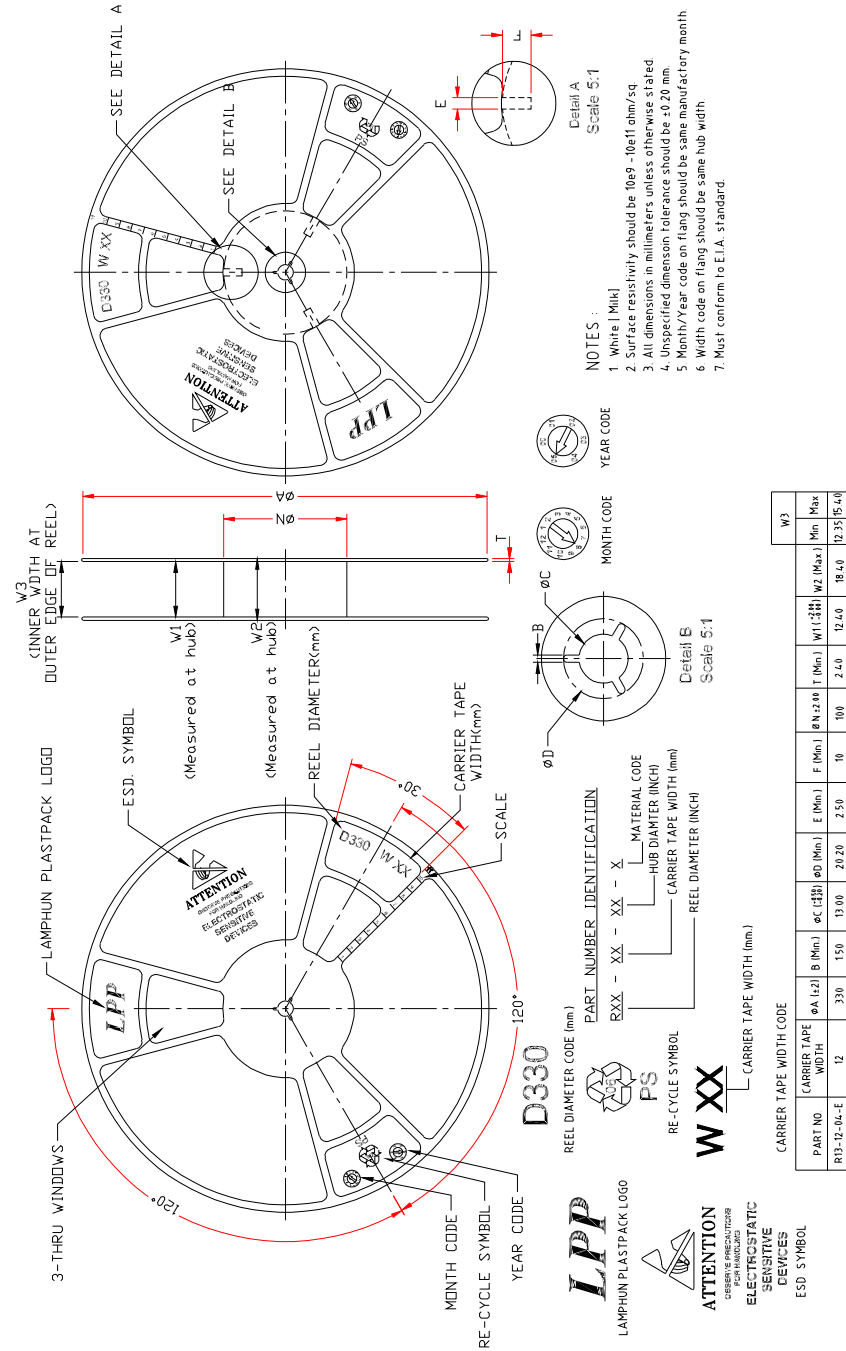


Figure 37. DFN12 (3 x 3 mm) reel dimensions



9 Ordering information

Table 9. Order codes

Order code	Package	Marking
STEL12H24PUR	DFN12 (3 x 3 mm)	EL24H

Revision history

Table 10. Document revision history

Date	Revision	Changes
13-Oct-2021	1	Initial release.

Contents

1	Diagram	2
2	Pin configuration	3
3	Typical application circuit	4
4	Maximum ratings	5
5	Electrical characteristics	6
6	Application information	10
6.1	Enable pin	10
6.2	Undervoltage lockout	10
6.3	Quick discharge	10
6.4	Power Good	10
6.5	Short-circuit protection	10
6.6	Slew rate control	10
6.7	Overvoltage protection	11
6.8	Thermal shutdown	11
7	Typical characteristics	12
8	Package information	17
8.1	DFN12 (3 x 3 mm) package information	17
8.2	DFN12 (3 x 3 mm) packing information	19
9	Ordering information	21
	Revision history	22

List of tables

Table 1.	Pin description	3
Table 2.	Typical application components	4
Table 3.	Absolute maximum ratings	5
Table 4.	Thermal data	5
Table 5.	ESD performance	5
Table 6.	Electrical characteristics	6
Table 7.	Switching characteristics table	7
Table 8.	DFN12 (3 x 3 mm) mechanical data	18
Table 9.	Order codes	21
Table 10.	Document revision history	22

List of figures

Figure 1.	Block diagram	2
Figure 2.	Pin connection (top view)	3
Figure 3.	Typical application.	4
Figure 4.	Switching characteristics test circuit.	7
Figure 5.	Switching characteristics timing	9
Figure 6.	Short-circuit timing	9
Figure 7.	R_{ON} vs. V_{IN}	12
Figure 8.	R_{ON} vs. temperature	12
Figure 9.	Standby current vs. V_{CC}	12
Figure 10.	Standby current vs. temperature	12
Figure 11.	Supply current vs. V_{IN}	13
Figure 12.	Supply current vs. V_{CC}	13
Figure 13.	Supply current vs. temperature	13
Figure 14.	R_p vs. temperature	13
Figure 15.	BLEED leakage current vs. temperature	13
Figure 16.	BLEED leakage current vs. V_{IN}	13
Figure 17.	EN Input High/Low voltage vs. temperature	14
Figure 18.	EN Pull-down resistance vs. temperature	14
Figure 19.	PG output low voltage vs. V_{CC}	14
Figure 20.	PG output low voltage vs. temperature	14
Figure 21.	K_{SR} vs. V_{IN}	14
Figure 22.	K_{SR} vs. V_{CC}	14
Figure 23.	K_{SR} vs. temperature	15
Figure 24.	S_R vs. V_{CC}	15
Figure 25.	V_{SC} vs. V_{IN}	15
Figure 26.	T_{ON} vs. V_{IN}	15
Figure 27.	T_{PG-OFF} vs. V_{IN}	15
Figure 28.	T_{OFF} vs. V_{IN}	15
Figure 29.	Mosfet leakage current vs. temperature	16
Figure 30.	T_{PG-ON} vs. V_{IN}	16
Figure 31.	PG leakage current vs. V_{CC}	16
Figure 32.	EN pulldown resistance vs. EN voltage	16
Figure 33.	DFN12 (3 x 3 mm) package outline	17
Figure 34.	DFN12 (3 x 3 mm) recommended footprint.	18
Figure 35.	DFN12 (3 x 3 mm) tape drawing	19
Figure 36.	DFN12 (3 x 3 mm) reel oriented	19
Figure 37.	DFN12 (3 x 3 mm) reel dimensions	20