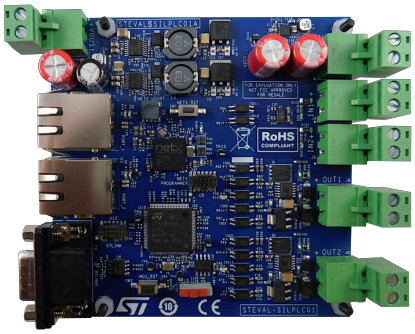
STEVAL-SILPLC01

Data brief

Safety-ready industrial PLC evaluation board



Product summary	
Safety-ready industrial PLC evaluation board	STEVAL-SILPLC01
Firmware for the STEVAL-SILPLC01	STSW-SILPLC
High-performance and DSP with DP-FPU	STM32H723VGT6
Self-powered digital input current limiter	CLT03-2Q3
Single channel high-side switches	IPS160HF
61 V 2 A asynchronous step-down switching regulator	L7987L
100 V, 3 A SOD128Flat Power Schottky rectifier	STPS3H100AF
Functional safety package for STM32 microcontrollers	X-CUBE-STL
Applications	Programmable Logic Controllers (PLC)

Features

- Built around the following ICs for the industrial market:
  - STM32H723VG: Arm® Cortex®-M7 32-bit RISC core operating at up to 550 MHz
  - CLT03-2Q3: self-powered digital input current limiter
  - IPS160HF: Single channel high-side switch
  - L7987L: 61 V 2 A asynchronous step-down switching regulator
  - ISOSD61: 16-bit isolated sigma-delta modulator, single-ended and LVDS interfaces
- Main supply voltage: 24÷36 V (max 60 V)
- Power management circuit for digital circuits voltage reference generation
- Designed to meet IEC61508 SIL 2 level
- Hardware assessed by TÜV Italia (TÜV SUD Group)
- Inductive load demagnetization and direct output diagnostics available on board
- X-CUBE-STL self test library certified by TÜV Rheinland
- Real-time communication with EtherCAT
- RS485 PHY
- Six-layer stack-up to improve immunity on real-time communication
- RoHS

Description

The STEVAL-SILPC01 is a PLC solution with a 1oo2 architecture, featuring the CLT03-2Q3dual channel digital input and the IPS160HF single channel digital output.

The hardware is designed to meet the SIL level. It has been officially assessed by TÜV Italia (TÜV SUD Group) in compliance with SIL 2 / PL d requirements: random failure rates, systematic capability (for the hardware), architectural constraints in accordance with IEC 61508, EN 62061, EN ISO 13849-1, and EN ISO 13849-2 standards.

The system is built around the STM32H723VG microcontroller. It is able to manage connectivity, load actuation and system diagnostic check for power management, digital input/output ICs, and temperature monitoring at the same time.

The solution integrates DC-DC converters in a buck configuration powered by the L7987L and L7983. The switching converters have been designed to provide 3.5 V on the user side and 6 V on the isolated side. With dedicated post regulation circuits, these voltage levels are stepped down to 3.3 V for the MCU, connectivity, and temperature sensor (available on the isolated side) and 5 V for the signal delta isolator (also available on the isolated side).

The CLT03-2Q3 input can detect a fixed DC voltage via a 0-36 V or 4-20 mA sensor, whereas the two IPS160HF allow load driving with a 2.5 A current capability for each output.

Several diagnostic and protection circuits are available on the board to ensure the system proper functionality and meet the IEC61508-2 requirements.

The hardware is supported by STSW-SILPLC firmware package, based on the STM32Cube architecture. It consists of an application layer, a drivers layer with BSP/CMSIS and HAL library, and a middleware layer.

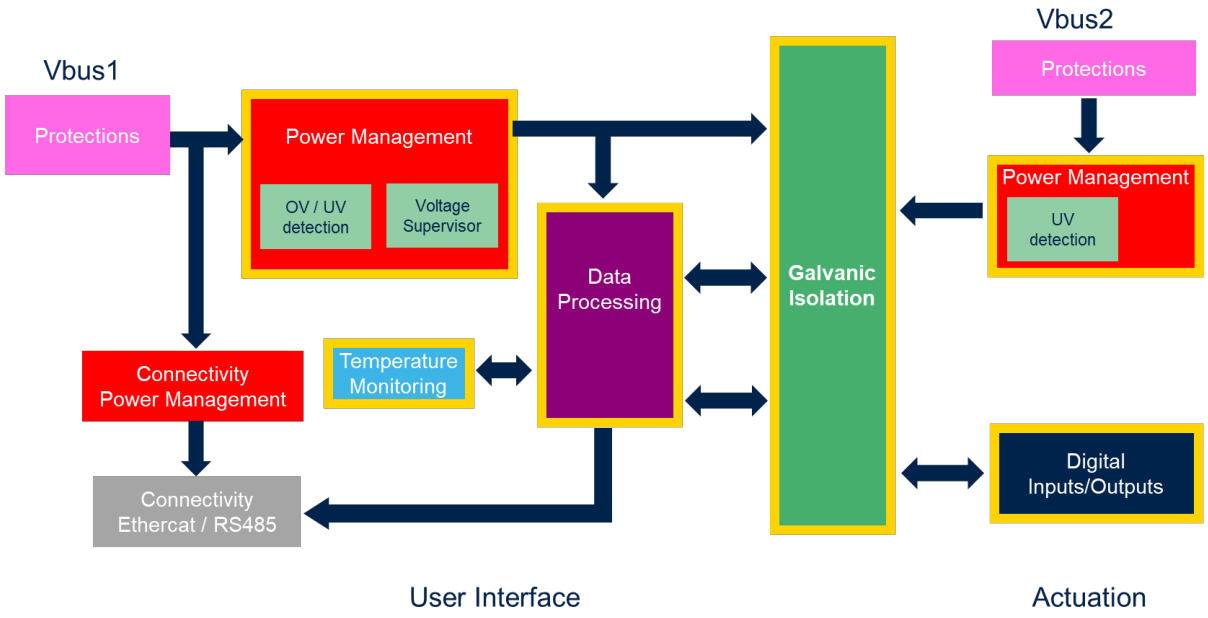
The firmware solution embeds the EtherCAT protocol stack V5.0.8 and X-CUBE-STL-H7 v1.2.0 certified by TÜV Rheinland. The stack library provides dedicated APIs to handle the data packet exchange between the master and the slave. Data consist of a set of commands to drive the load through the on-board IPS on board and manage system diagnostic using dedicated signals. These data types are exchanged using the process data channel of the protocol stack.

A daisy-chain configuration can be implemented to connect more than one sensor node to the same network. In this case, the master generates a common frame with the data to be addressed to all EtherCAT slaves (ECS). Each node identifies its own frame by verifying only the MAC address reported in the frame.

Dedicated documentation related to TÜV assessment on the hardware, such as TN1395 "Analysis of hardware systematic failures and techniques for on-chip redundancy", FMEDA, Assessment on hardware Report TI 722260614 Rev. 0, and the industrialization package, are available on demand, by signing a specific NDA.

1 Solution overview

Figure 1. **STEVAL-SILPLC01 functional block diagram**



The STEVAL-SILPLC01 architecture above shows only the logical function of each block, without references to the IC, to highlight the system mission profile.

The hardware includes the following sections: power management, connectivity, opto-isolation, and digital input outputs circuits. It has been designed to meet the IEC61508 standard, other functional safety standards (EN 62061, EN/ISO 13849-1, EN ISO 13849-2), and the IEC61000 standard about the EMC robustness.

To meet the requirements, different power management circuits have been designed for the safe I/O side and for the connectivity with a voltage supervisor that has a watchdog functionality to reduce the risk of data loss if the power supply falls. At firmware level, a data processing unit implements a set of safety functions to detect a failure event of the MCU (the firmware package is not included in the TÜV Italia (TÜV SUD Group)).

The application firmware has been developed to implement an application example and demonstrate the capability of the solution to meet the IEC61508 standard with a dedicated API for load driving, diagnostic monitoring, and board safe state driving in case of a fault event. At the application level, the firmware package assessment (not included in the TÜV Italia (TÜV SUD Group)) supports the X-CUBE-STL package certified by TÜV Rheinland.

Note: The STM32 self-test library (X-CUBE-STL) is supported by the application firmware. Contact your ST representative and sign a NDA to access the X-CUBE-STL package.

Note: Vbus1 is the operating supply voltage (24 - 36 V) for the user interface block, while Vbus2 is the operating supply voltage (24 - 36 V) for the actuation block.

2 Schematic diagrams

Figure 2. **STEVAL-SILPLC01 circuit schematic (1 of 9)**

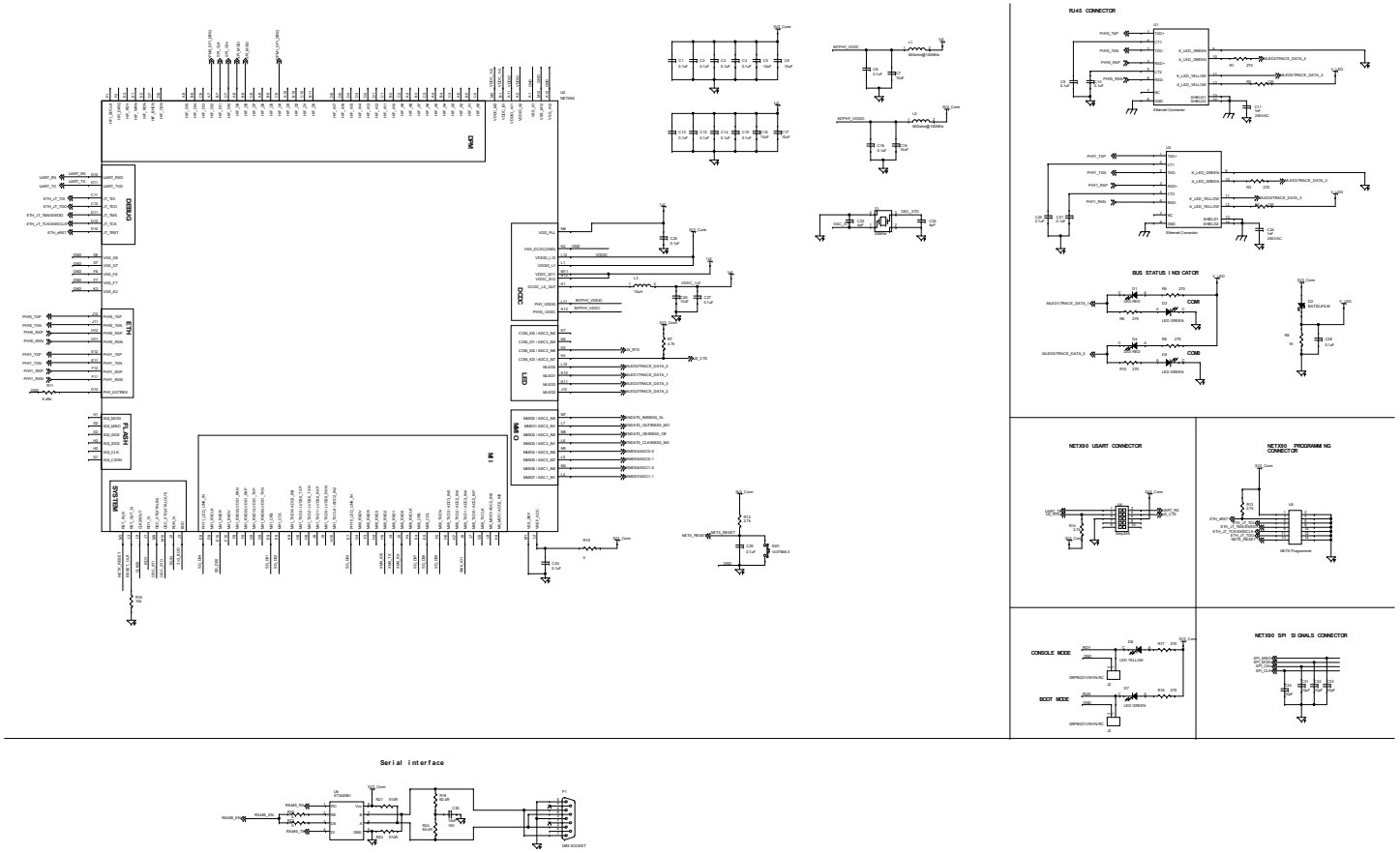


Figure 3. STEVAL-SILPLC01 circuit schematic (2 of 9)

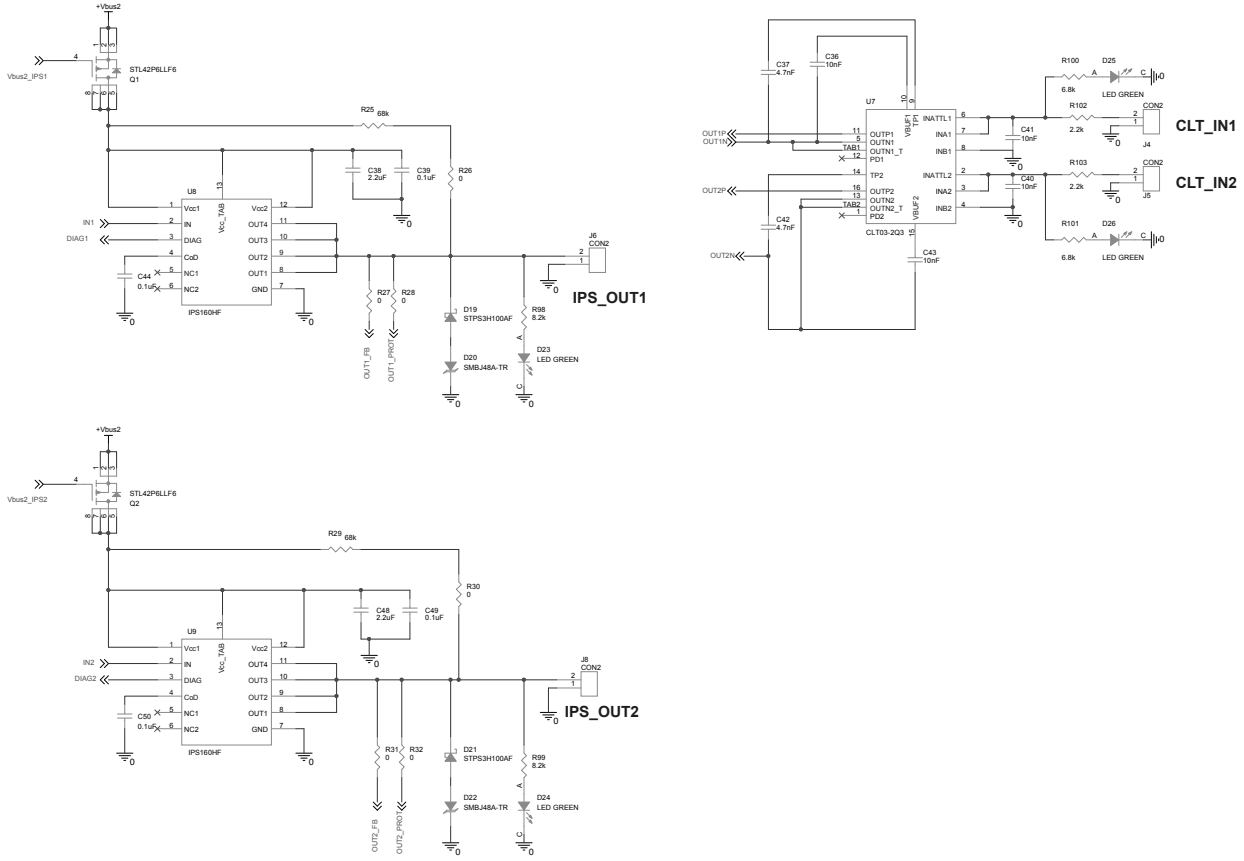


Figure 4. STEVAL-SILPLC01 circuit schematic (3 of 9)

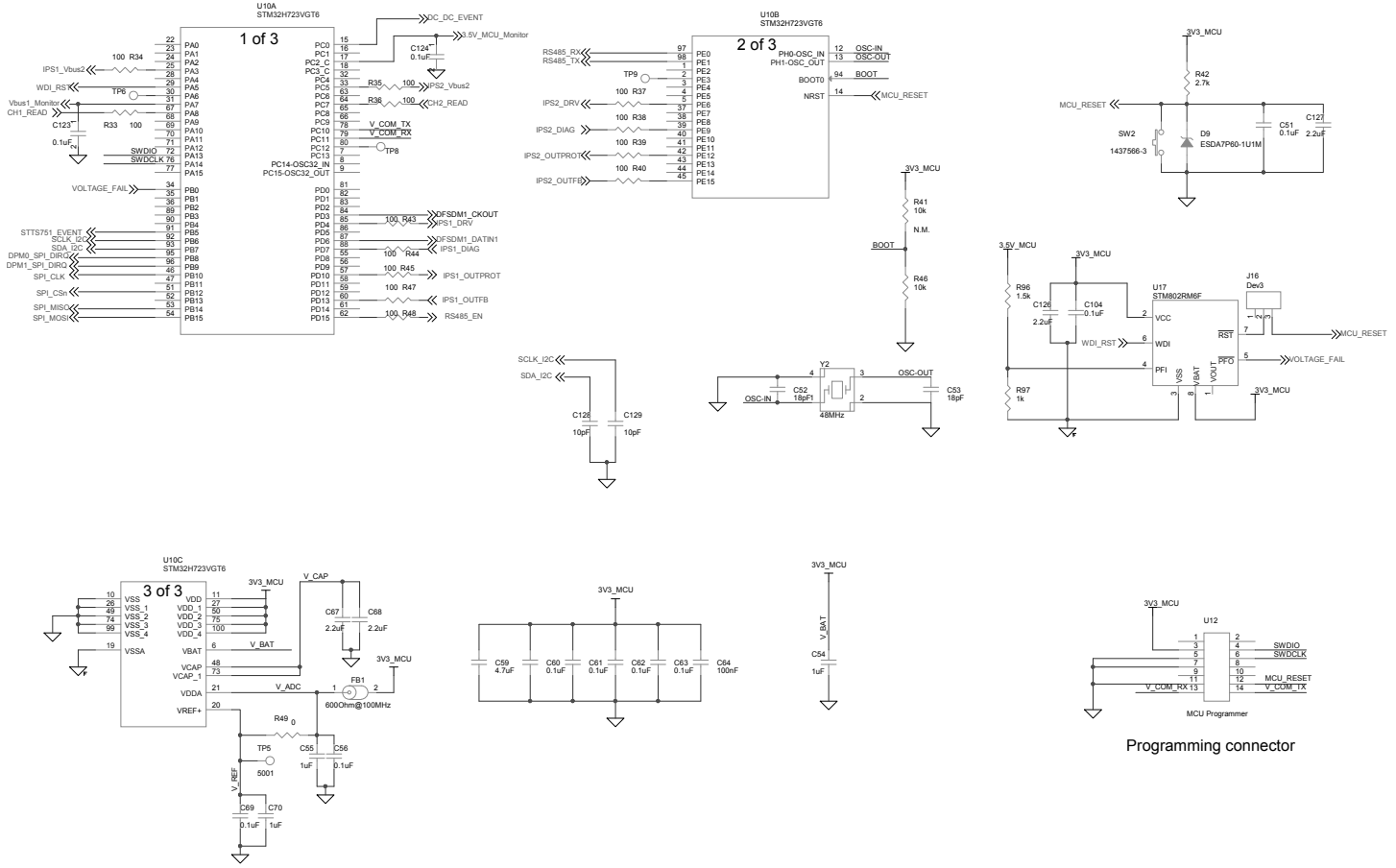


Figure 5. STEVAL-SILPLC01 circuit schematic (4 of 9)

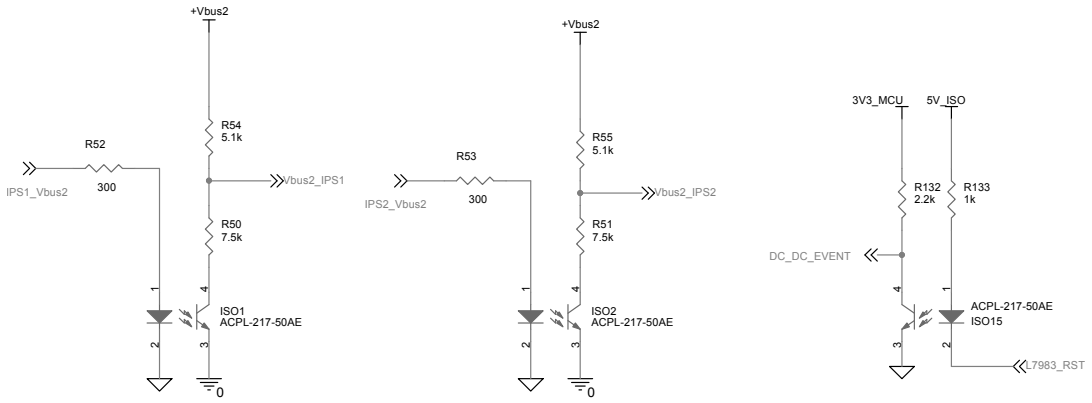


Figure 6. STEVAL-SILPLC01 circuit schematic (5 of 9)

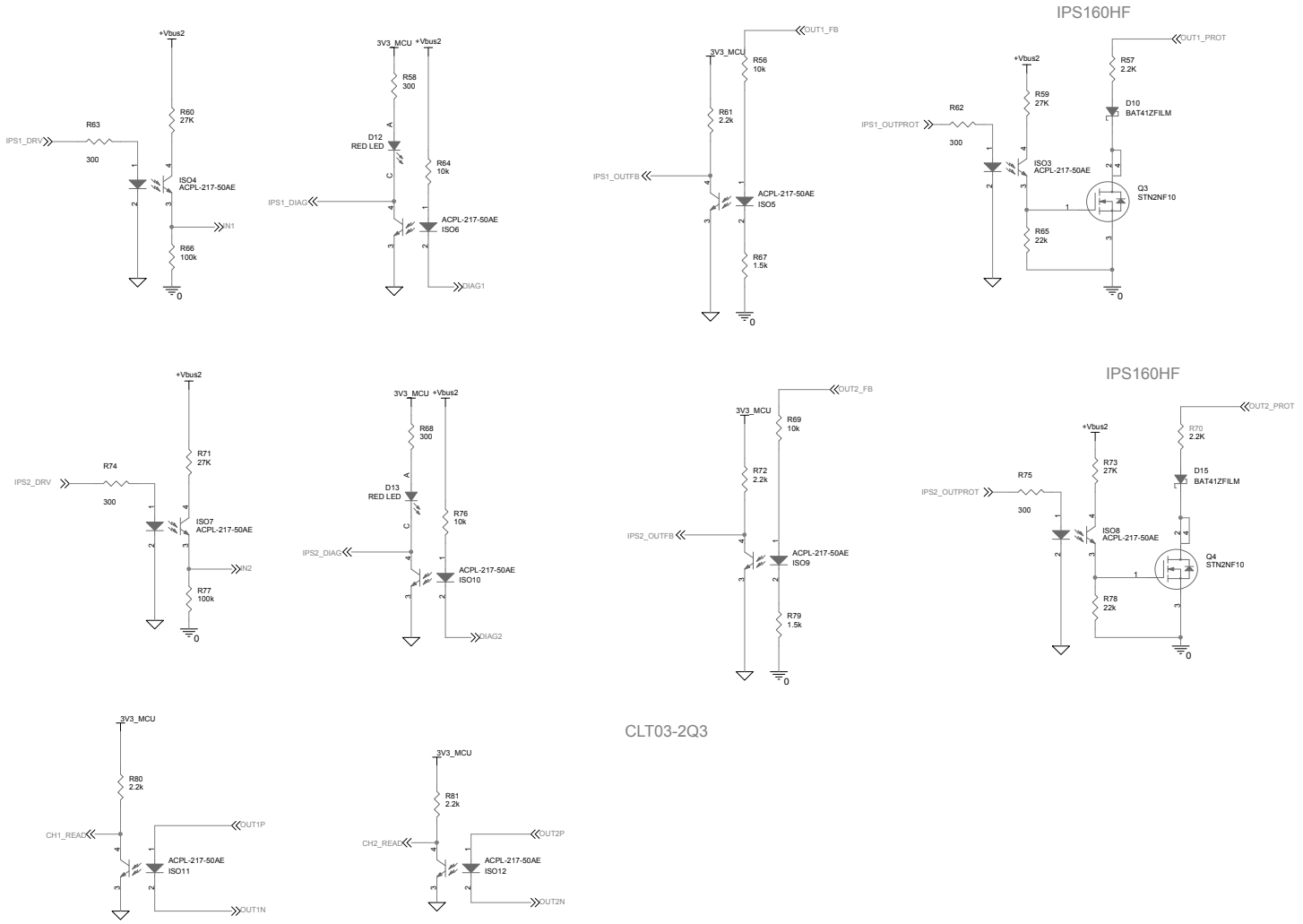


Figure 7. STEVAL-SILPLC01 circuit schematic (6 of 9)

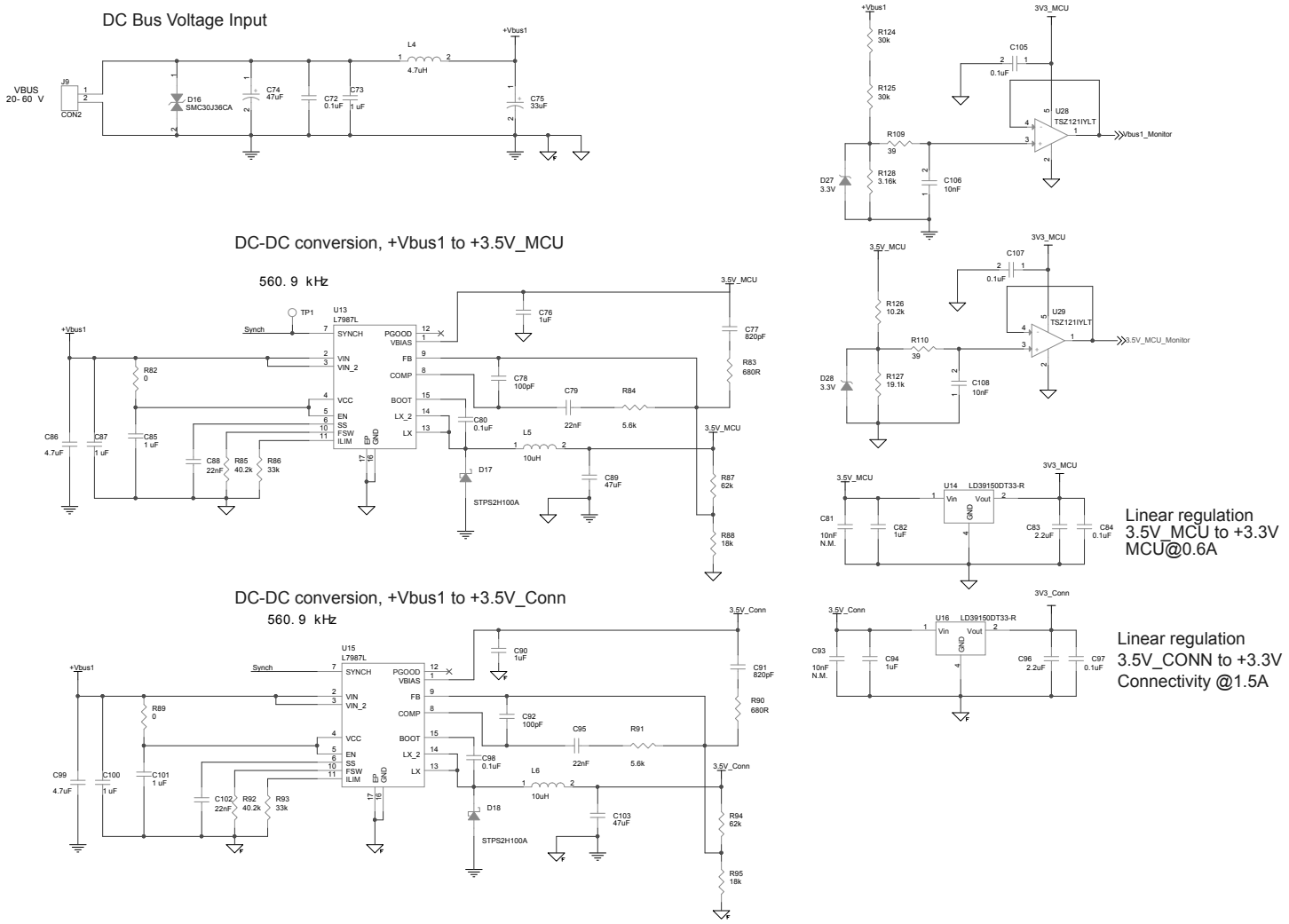


Figure 8. STEVAL-SILPLC01 circuit schematic (7 of 9)

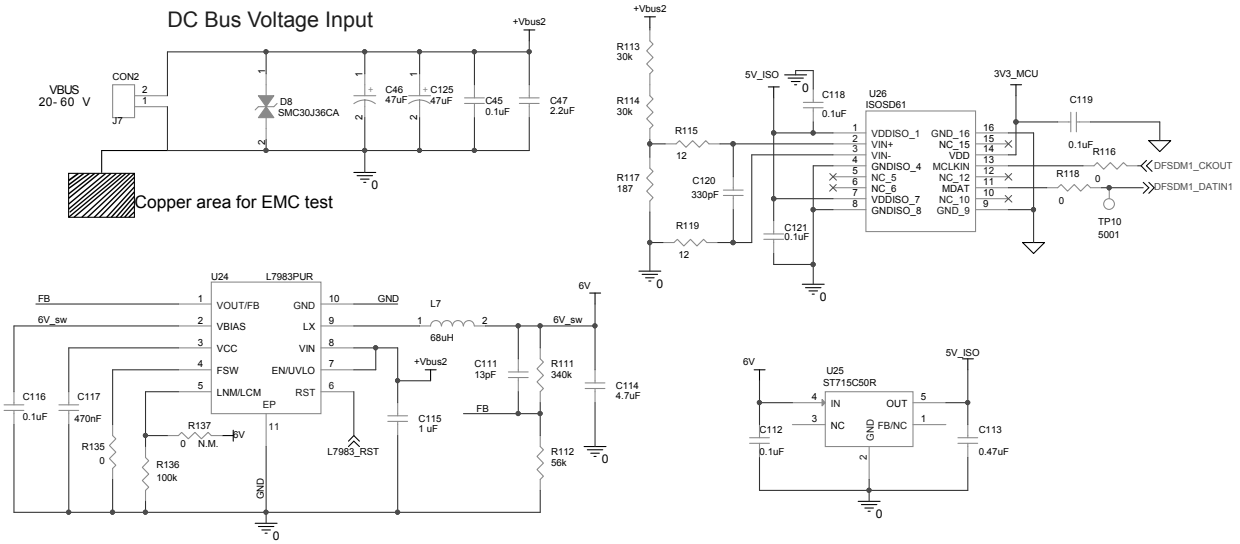


Figure 9. STEVAL-SILPLC01 circuit schematic (8 of 9)

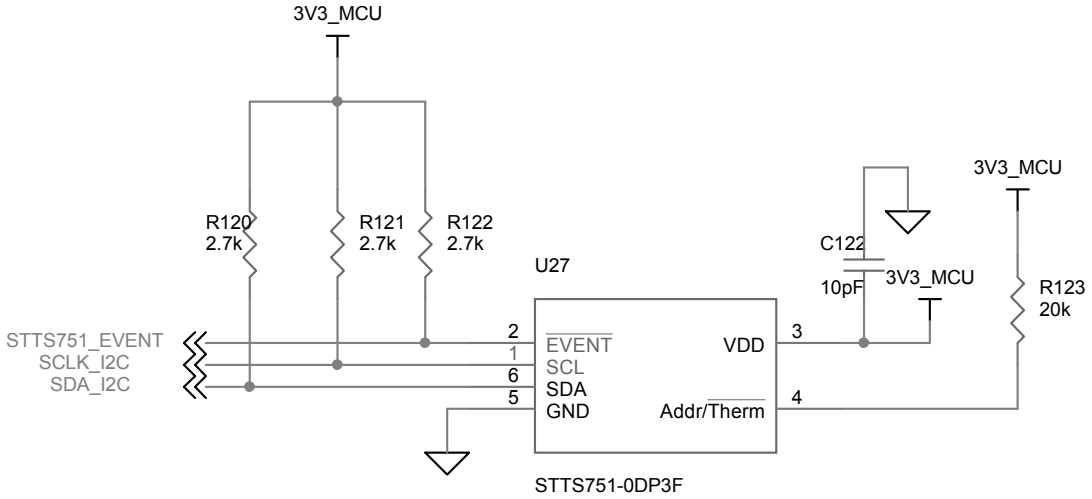


Figure 10. STEVAL-SILPLC01 circuit schematic (9 of 9)

3 Board versions

Table 1. STEVAL-SILPLC01 versions

Finished good	Schematic diagrams	Bill of materials
STEVAL$SILPLC01A (1)	STEVAL$SILPLC01A schematic diagrams	STEVAL$SILPLC01A bill of materials

1. *This code identifies the STEVAL-SILPLC01 evaluation board first version.*

Revision history

Table 2. **Document revision history**

Date	Revision	Changes
19-Oct-2022	1	Initial release.
25-Oct-2022	2	Updated cover page description.