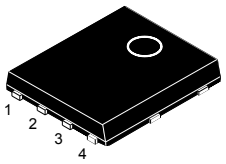
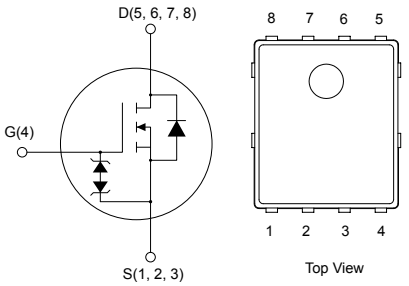
N-channel 600 V, 0.390 Ω typ., 7 A MDmesh™ M2 EP Power MOSFET in a PowerFLAT™ 5x6 HV package



PowerFLAT™ 5x6 HV



Features

Order code	V_{DS} @ T_{Jmax}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STL15N60M2-EP	650 V	0.418 Ω	7 A	55 W

- Extremely low gate charge
- Excellent output capacitance (C_{OSS}) profile
- Very low turn-off switching losses
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications
- Tailored for very high frequency converters (f > 150 kHz)

Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 enhanced performance (EP) technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance, optimized switching characteristics with very low turn-off switching losses, rendering it suitable for the most demanding very high frequency converters.

Product status
STL15N60M2-EP

Product summary	
Order code	STL15N60M2-EP
Marking	15N60M2E
Package	PowerFLAT™ 5x6 HV
Packing	Tape and Reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_{case} = 25 °C	7	A
	Drain current (continuous) at T_{case} = 100 °C	4.6	
I_{DM} (1)	Drain current (pulsed)	28	A
P_{TOT}	Total dissipation at T_{case} = 25 °C	55	W
I_{AR} (2)	Avalanche current, repetitive or not repetitive	1.5	A
E_{AS} (3)	Single pulse avalanche energy	110	mJ
dv/dt(4)	Peak diode recovery voltage slope	15	V/ns
dv/dt(5)	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		

1. *Pulse width is limited by safe operating area.*
2. *Pulse width limited by T_{jmax}.*
3. *starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V.*
4. *I_{SD} ≤ 7 A, di/dt = 400 A/µs; V_{DS} peak < $V_{(BR)DSS}$, V_{DD} = 400 V.*
5. *V_{DS} ≤ 480 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	2.27	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	59	

1. *When mounted on a 1-inch² FR-4, 2 Oz copper board.*

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 3. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_{case} = 125 °C (1)			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3.25	4	4.75	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 4.5 A		0.390	0.418	Ω

1. *Defined by design, not subject to production test.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	590	-	pF
C_{oss}	Output capacitance		-	30	-	
C_{rss}	Reverse transfer capacitance		-	1.1	-	
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0 V	-	148	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	7	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 11 A, V_{GS} = 0 to 10 V (see Figure 15. Test circuit for gate charge behavior)	-	17	-	nC
Q_{gs}	Gate-source charge		-	3.1	-	
Q_{gd}	Gate-drain charge		-	7.3	-	

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 5. Switching energy

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
E_{OFF}	Turn-off energy (from 90% V_{GS} to 0% I_D)	V_{DD} = 400 V, I_D = 1.5 A, R_G = 4.7 Ω, V_{GS} = 10 V	–	4.7	-	µJ
		V_{DD} = 400 V, I_D = 3.5 A, R_G = 4.7 Ω, V_{GS} = 10 V	–	5.2	-	

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 5.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	11	-	ns
t_r	Rise time		-	10	-	
$t_{d(off)}$	Turn-off delay time		-	40	-	
t_f	Fall time		-	15	-	

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		7	A
I_{SDM} (1)	Source-drain current (pulsed)		-		28	A
V_{SD} (2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 7 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 11 A, di/dt = 100 A/µs, V_{DD} = 60 V (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	280		ns
Q_{rr}	Reverse recovery charge		-	2.7		µC
I_{RRM}	Reverse recovery current		-	19.5		A
t_{rr}	Reverse recovery time	I_{SD} = 11 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	400		ns
Q_{rr}	Reverse recovery charge		-	3.8		µC
I_{RRM}	Reverse recovery current		-	19		A

1. *Pulse width is limited by safe operating area.*
2. *Pulse test: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

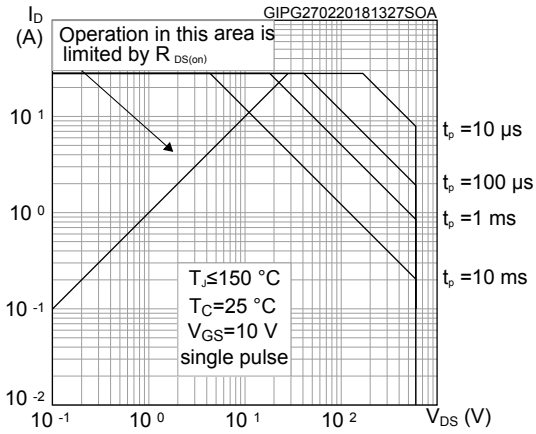


Figure 2. Thermal impedance

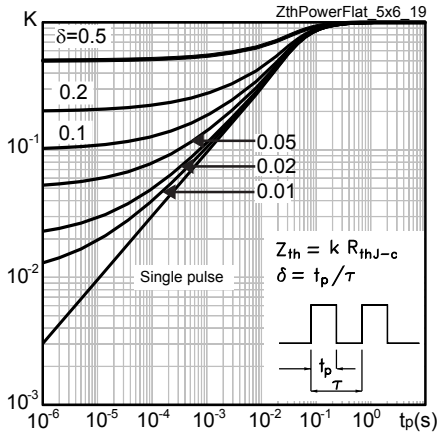


Figure 3. Output characteristics

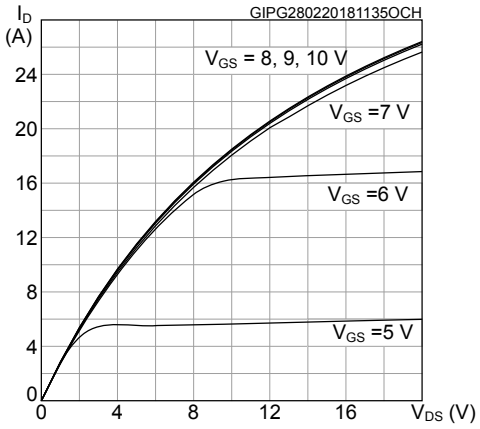


Figure 4. Transfer characteristics

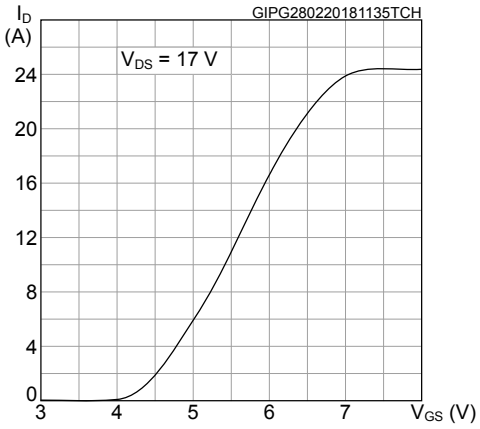


Figure 5. Gate charge vs gate-source voltage

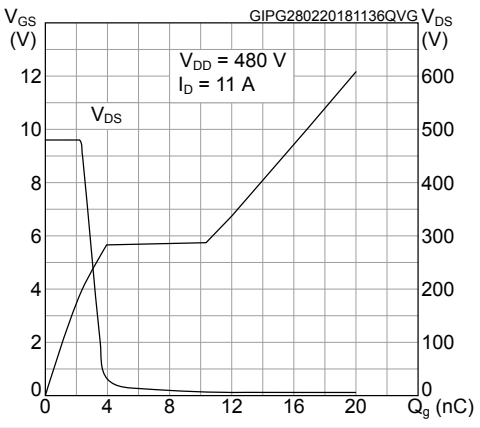


Figure 6. Static drain-source on-resistance

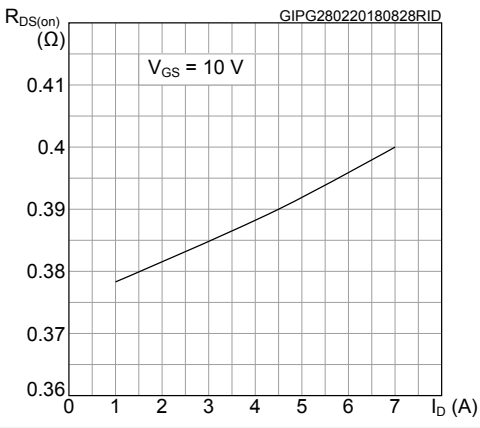


Figure 7. Capacitance variations

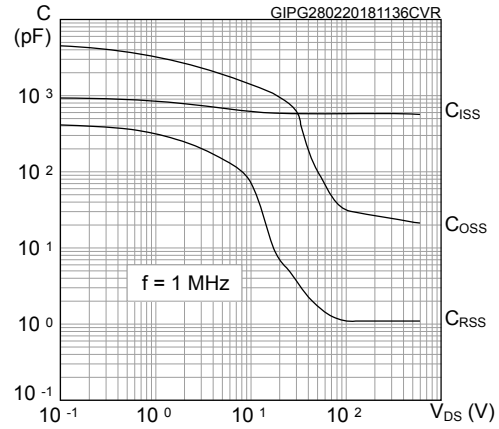


Figure 8. Output capacitance stored energy

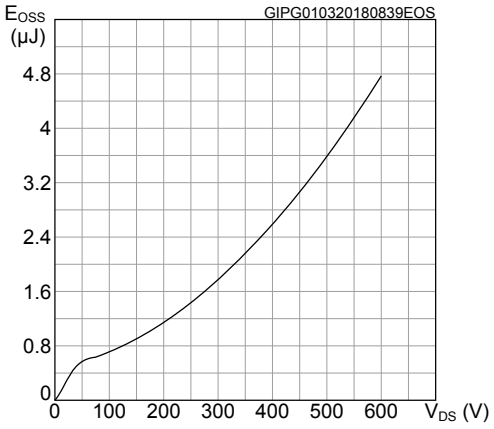


Figure 9. Normalized gate threshold voltage vs temperature

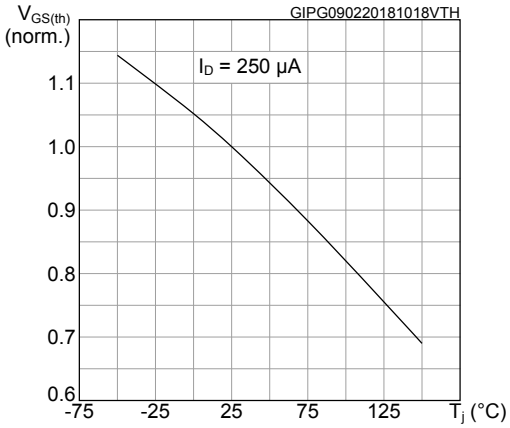


Figure 10. Normalized on-resistance vs temperature

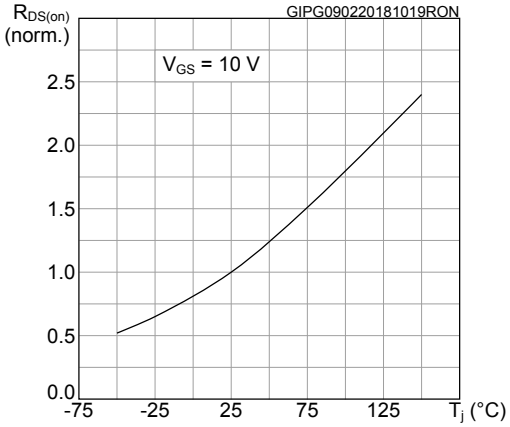


Figure 11. Normalized $V_{(BR)DSS}$ vs temperature

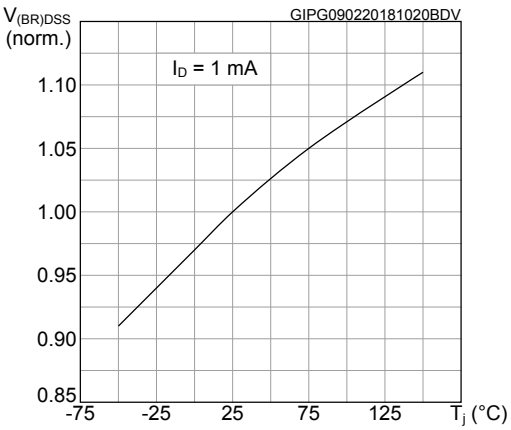


Figure 12. Turn-off switching energy vs drain current

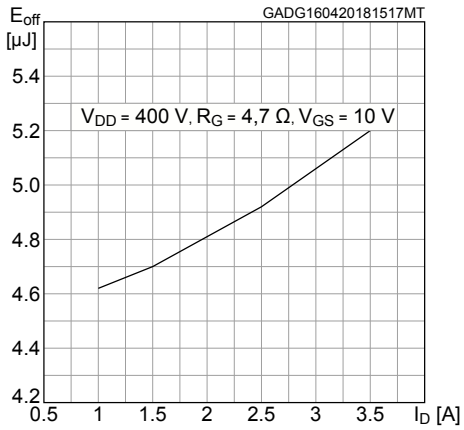
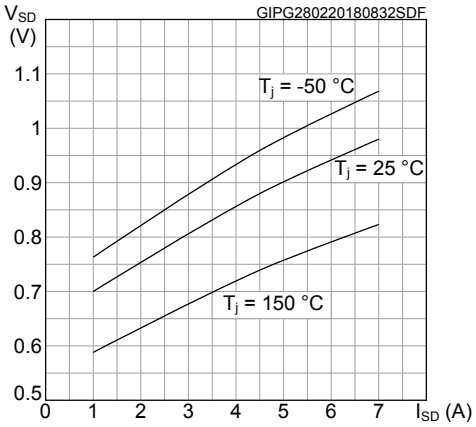


Figure 13. Source-drain diode forward characteristics



3 Test circuits

Figure 14. Test circuit for resistive load switching times

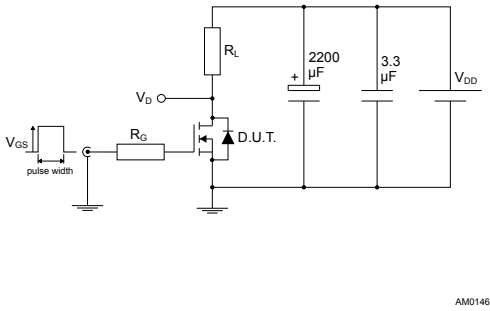


Figure 15. Test circuit for gate charge behavior

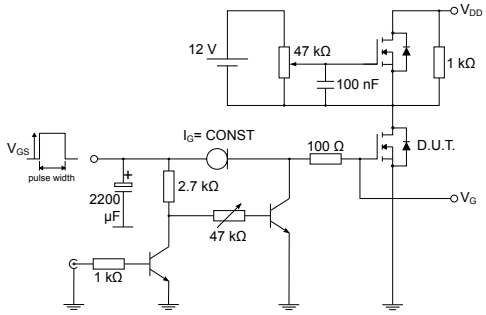


Figure 16. Test circuit for inductive load switching and diode recovery times

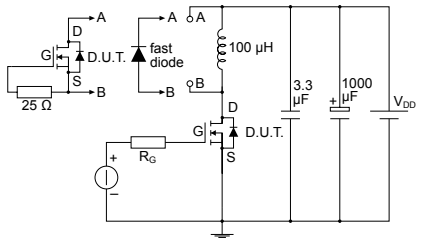


Figure 17. Unclamped inductive load test circuit

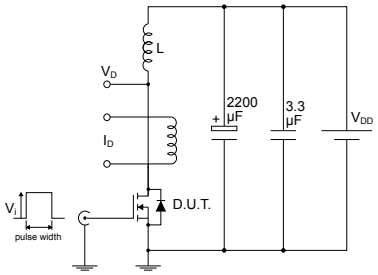


Figure 18. Unclamped inductive waveform

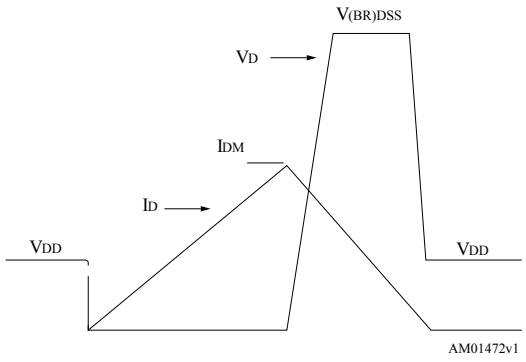
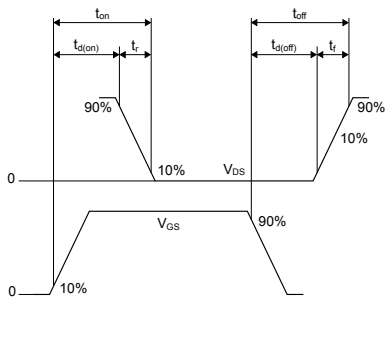


Figure 19. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 HV package information

Figure 20. **PowerFLAT™ 5x6 HV package outline**

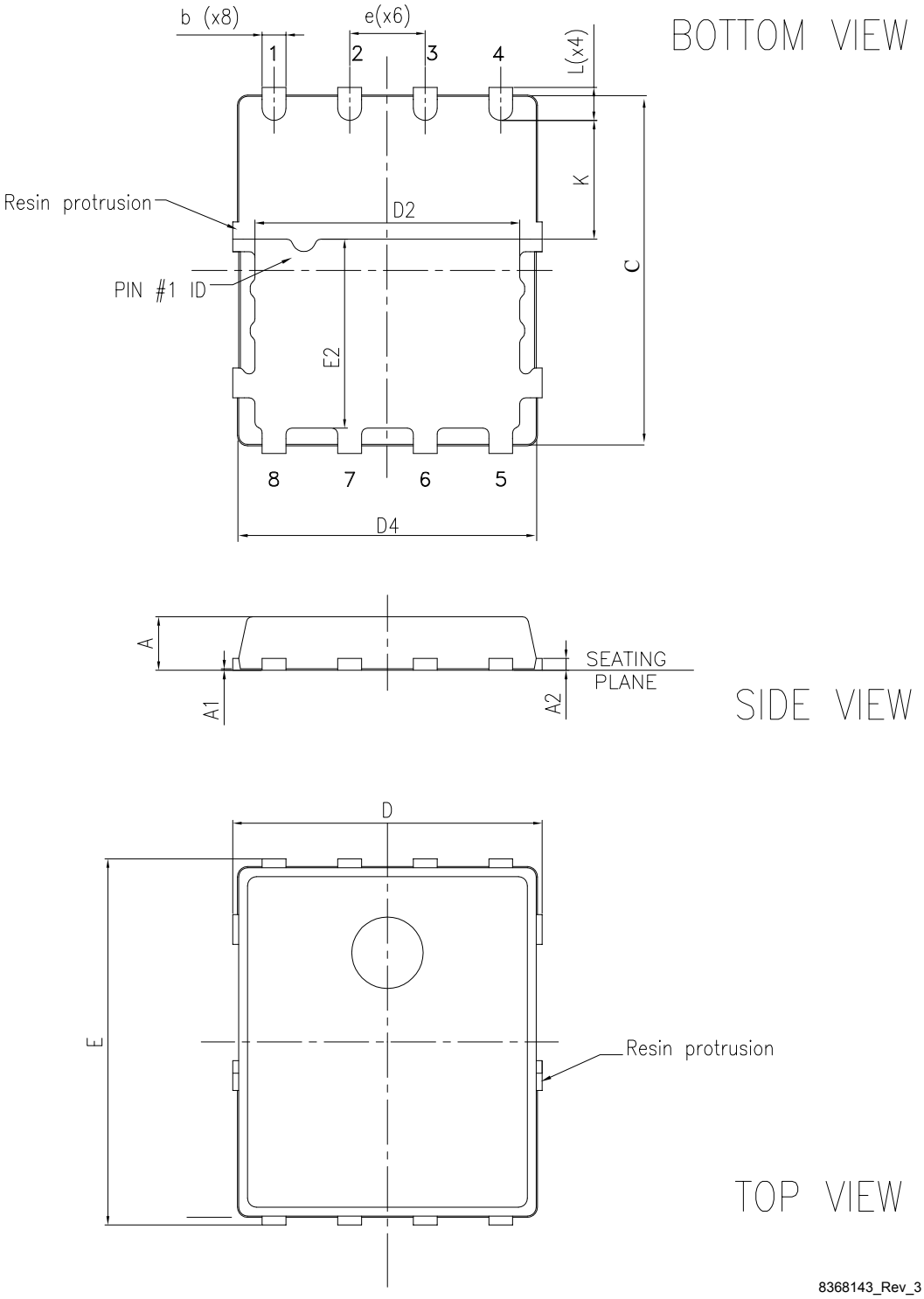
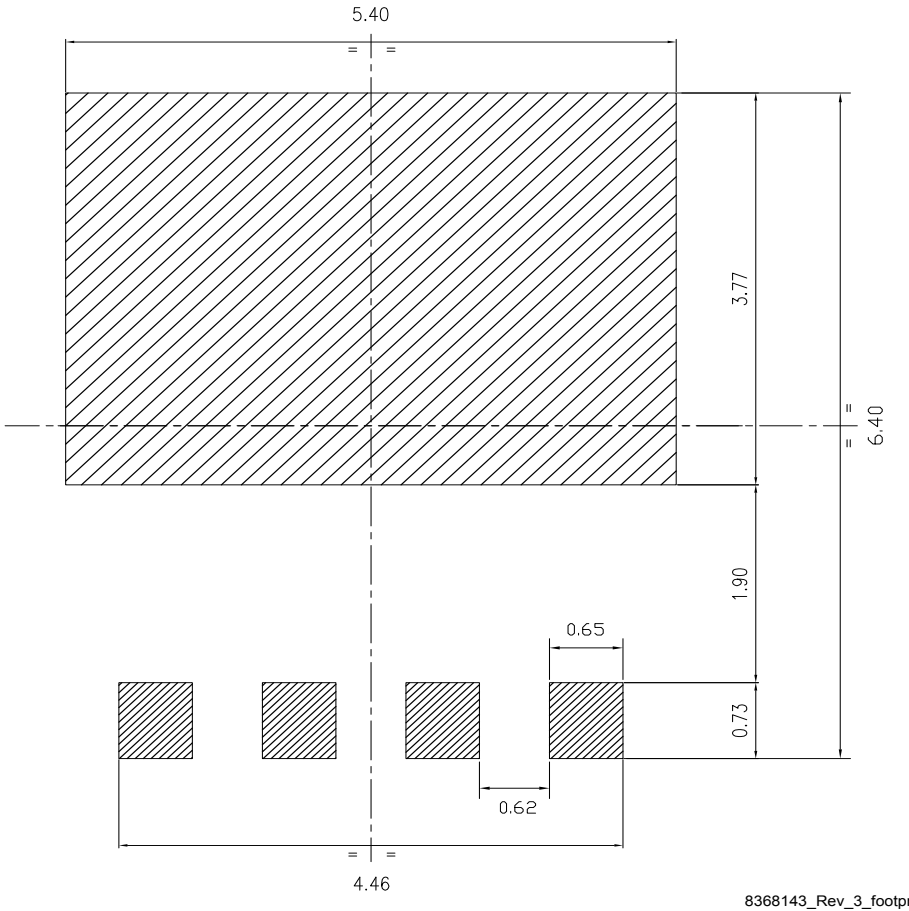


Table 8. **PowerFLAT™ 5x6 HV mechanical data**

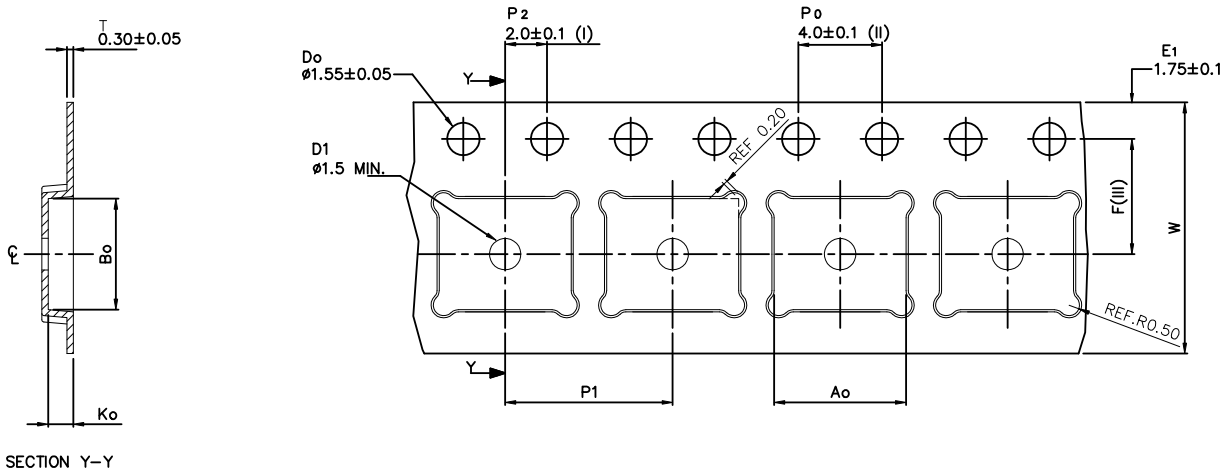
Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.8	6	6.1
D	5.10	5.20	5.30
E	6.05	6.15	6.25
E2	3.10	3.20	3.30
D2	4.30	4.40	4.50
D4	4.8	5	5.1
e		1.27	
L	0.50	0.55	0.60
K	1.90	2.00	2.10

Figure 21. **PowerFLAT™ 5x6 HV recommended footprint (dimensions are in mm)**



4.2 PowerFLAT™ 5x6 packing information

Figure 22. **PowerFLAT™ 5x6 tape (dimensions are in mm)**



Ao	6.30 +/– 0.1
Bo	5.30 +/– 0.1
Ko	1.20 +/– 0.1
F	5.50 +/– 0.1
P1	8.00 +/– 0.1
W	12.00 +/– 0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.

(II) Cumulative tolerance of 10 sprocket holes is ±0.20.

(III) Measured from centreline of sprocket hole to centreline of pocket

Base and bulk quantity 3000 pcs
All dimensions are in millimeters

8234350_Tape_rev_C

Figure 23. **PowerFLAT™ 5x6 package orientation in carrier tape**

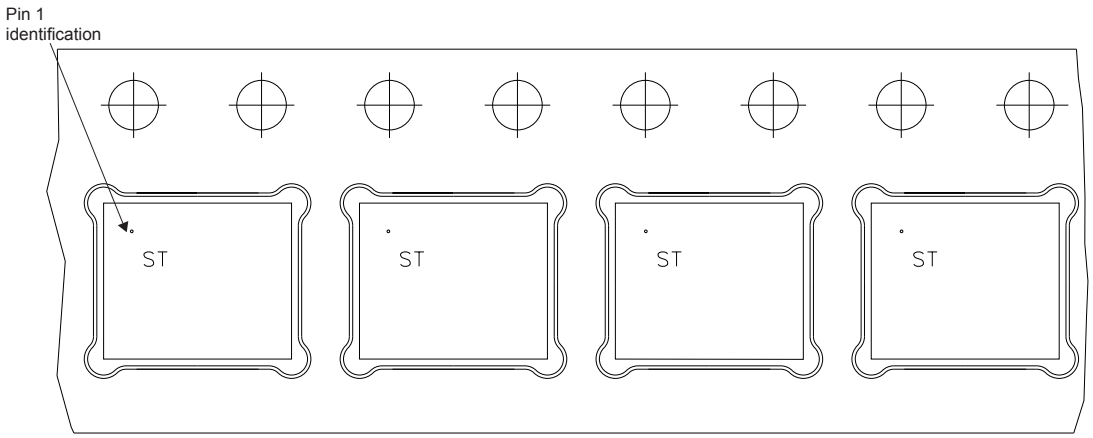
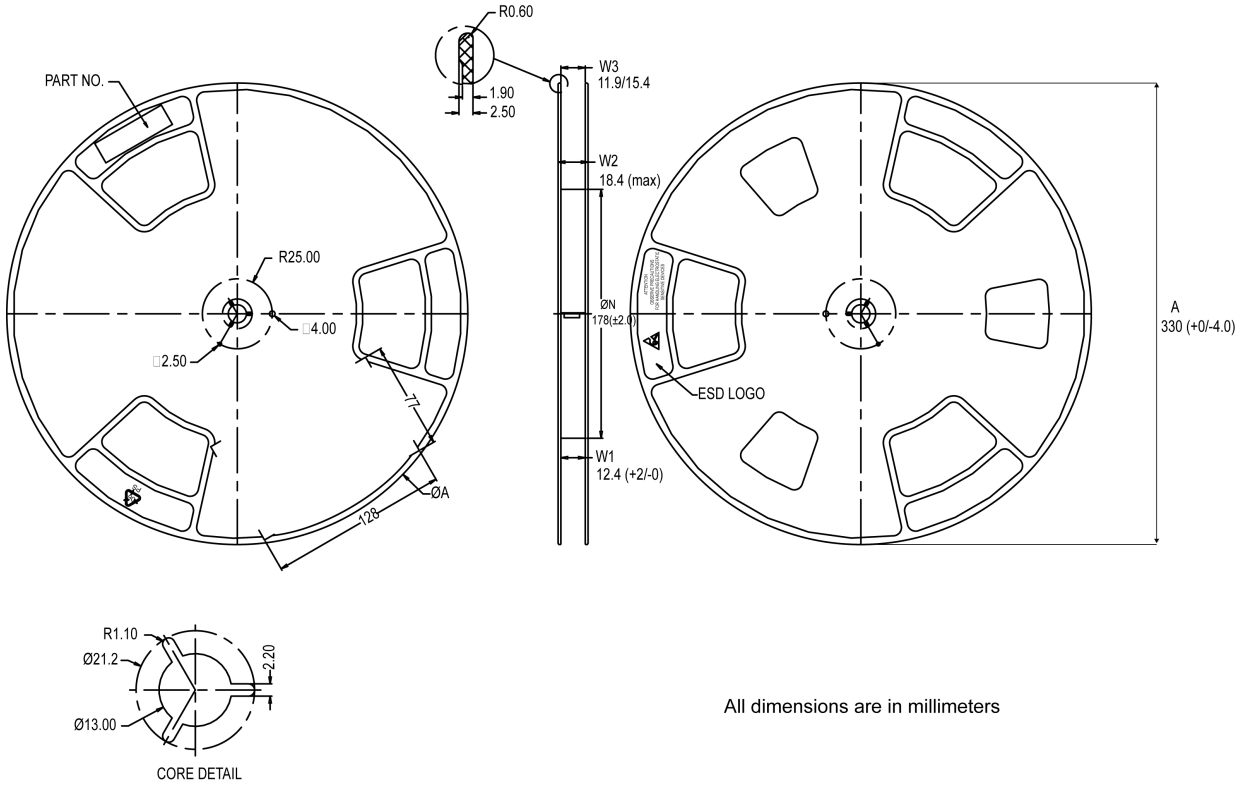


Figure 24. **PowerFLAT™ 5x6 reel**



All dimensions are in millimeters

8234350_Reel_rev_C

Revision history

Table 9. Document revision history

Date	Revision	Changes
15-Jun-2015	1	First release.
06-Mar-2018	2	Removed maturity status indication from cover page. The document status is production data. Modified *Table 3. Static.* Modified the entire *Section 2.1 Electrical characteristics (curves).* Minor text changes.
15-May-2018	3	Added note in Table 4. Dynamic. Updated Table 5. Switching energy and Figure 12. Turn-off switching energy vs drain current . Minor text changes.

Contents