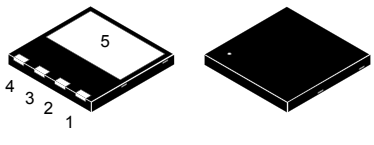
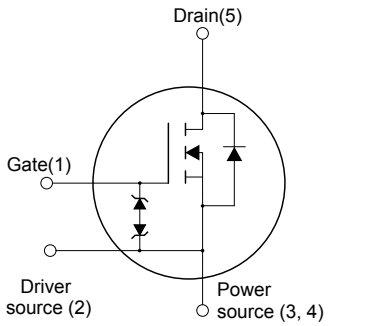
# N-channel 600 V, 0.115 Ω typ., 21 A MDmesh™ M6 Power MOSFET in a PowerFLAT™ 8x8 HV package




**PowerFLAT™ 8x8 HV**




| Product status link |
|---|
| STL33N60M6 |

| Product summary | |
|---|---|
| **Order code** | STL33N60M6 |
| **Marking** | 33N60M6 |
| **Package** | PowerFLAT™ 8x8 HV |
| **Packing** | Tape and reel |

## Features

| Order code | $V_{DS}$ | $R_{DS(on)}$ max. | $I_D$ |
|---|---|---|---|
| STL33N60M6 | 600 V | 137 mΩ | 21 A |

- Reduced switching losses
- Lower $R_{DS(on)}$ per area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

## Applications

- Switching applications
- LLC converters
- Boost PFC converters

## Description

The new MDmesh™ M6 technology incorporates the most recent advancements to the well-known and consolidated MDmesh family of SJ MOSFETs.
STMicroelectronics builds on the previous generation of MDmesh devices through its new M6 technology, which combines excellent $R_{DS(on)}$ per area improvement with one of the most effective switching behaviors available, as well as a user-friendly experience for maximum end-application efficiency.

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{GS}$ | Gate-source voltage | ±25 | V |
| $I_D$ | Drain current (continuous) at $T_{case}$ = 25 °C | 21 | A |
| | Drain current (continuous) at $T_{case}$ = 100 °C | 13 | |
| $I_{DM}$(1) | Drain current (pulsed) | 78 | A |
| $P_{TOT}$ | Total dissipation at $T_{case}$ = 25 °C | 150 | W |
| dv/dt(2) | Peak diode recovery voltage slope | 15 | V/ns |
| dv/dt(3) | MOSFET dv/dt ruggedness | 50 | |
| $T_{stg}$ | Storage temperature range | -55 to 150 | °C |
| $T_j$ | Operating junction temperature range | | |

1. *Pulse width is limited by safe operating area.*
2. *$I_{SD}$ ≤ 21 A, di/dt = 400 A/µs, $V_{DS}$ < $V_{(BR)DSS}$, $V_{DD}$ = 400 V*
3. *$V_{DS}$ ≤ 480 V*

**Table 2. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj\text{-}case}$ | Thermal resistance junction-case | 0.83 | °C/W |
| $R_{thj\text{-}pcb}$ (1) | Thermal resistance junction-pcb | 45 | °C/W |

1. *When mounted on FR-4 board of inch², 2oz Cu.*

**Table 3. Avalanche characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $I_{AR}$ | Avalanche current, repetitive or non-repetitive (pulse width limited by $T_{Jmax}$) | 4 | A |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_j$ = 25 °C, $I_D$ = $I_{AR}$, $V_{DD}$ = 50 V) | 500 | mJ |

# 2 Electrical characteristics

($T_{case}$ = 25 °C unless otherwise specified).

**Table 4. On/off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS}$ = 0 V, $I_D$ = 1 mA | 600 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current | $V_{GS}$ = 0 V, $V_{DS}$ = 600 V | | | 1 | µA |
| | | $V_{GS}$ = 0 V, $V_{DS}$ = 600 V, $T_{case}$ = 125 °C(1) | | | 100 | |
| $I_{GSS}$ | Gate-body leakage current | $V_{DS}$ = 0 V, $V_{GS}$ = ±25 V | | | ±5 | µA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 3.25 | 4 | 4.75 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS}$ = 10 V, $I_D$ = 10.5 A | | 0.115 | 0.137 | Ω |

1. *Defined by design, not subject to production test.*

**Table 5. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{DS}$ = 100 V, f = 1 MHz, $V_{GS}$ = 0 V | - | 1515 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 128 | - | |
| $C_{rss}$ | Reverse transfer capacitance | | - | 4.2 | - | |
| $C_{oss\ eq.}$(1) | Equivalent output capacitance | $V_{DS}$ = 0 to 480 V, $V_{GS}$ = 0 V | - | 269 | - | pF |
| $R_G$ | Intrinsic gate resistance | f = 1 MHz, $I_D$ = 0 A | - | 1.5 | - | Ω |
| $Q_g$ | Total gate charge | $V_{DD}$ = 480 V, $I_D$ = 25 A, $V_{GS}$ = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior) | - | 33.4 | - | nC |
| $Q_{gs}$ | Gate-source charge | | - | 7.2 | - | |
| $Q_{gd}$ | Gate-drain charge | | - | 16.3 | - | |

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$.*

**Table 6. Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}$ = 300 V, $I_D$ = 12.5 A, $R_G$ = 4.7 Ω, $V_{GS}$ = 10 V (see Figure 13. Switching times test circuit for resistive load and Figure 18. Switching time waveform) | - | 19.5 | - | ns |
| $t_r$ | Rise time | | - | 33 | - | |
| $t_{d(off)}$ | Turn-off delay time | | - | 38.5 | - | |
| $t_f$ | Fall time | | - | 7.5 | - | |

**Table 7. Source-drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | | - | | 21 | A |
| $I_{SDM}$ (1) | Source-drain current (pulsed) | | - | | 78 | A |
| $V_{SD}$ (2) | Forward on voltage | $I_{SD}$ = 21 A, $V_{GS}$ = 0 V | - | | 1.6 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 25 A, di/dt = 100 A/µs, $V_{DD}$ = 60 V (see Figure 15. Test circuit for inductive load switching and diode recovery times) | - | 265 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 3.07 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 23.2 | | A |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 25 A, di/dt = 100 A/µs, $V_{DD}$ = 60 V, $T_j$ = 150 °C (see Figure 15. Test circuit for inductive load switching and diode recovery times) | - | 374 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 5.78 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 30.9 | | A |

1. *Pulse width is limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%*

## 2.1 Electrical characteristics (curves)

**Figure 1. Safe operating area**

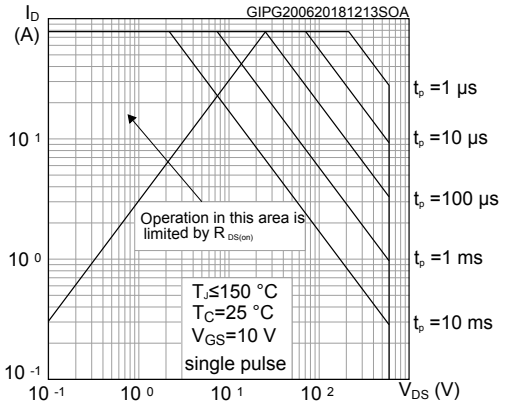



**Figure 2. Thermal impedance**

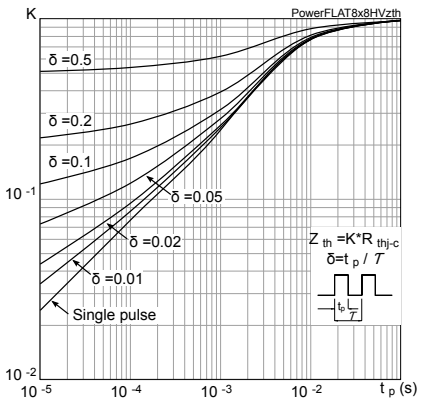



**Figure 3. Output characteristics**

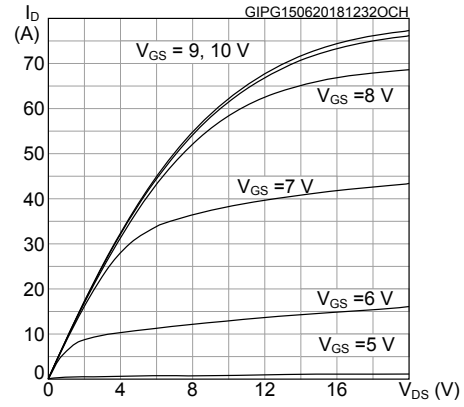



**Figure 4. Transfer characteristics**

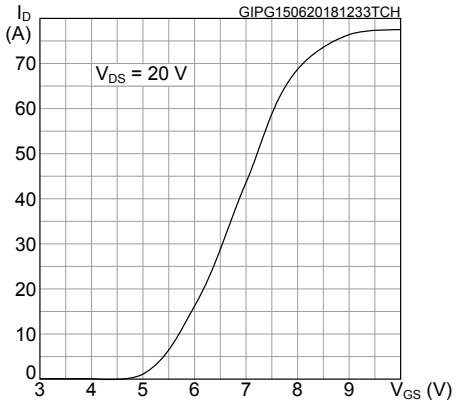



**Figure 5. Gate charge vs gate-source voltage**

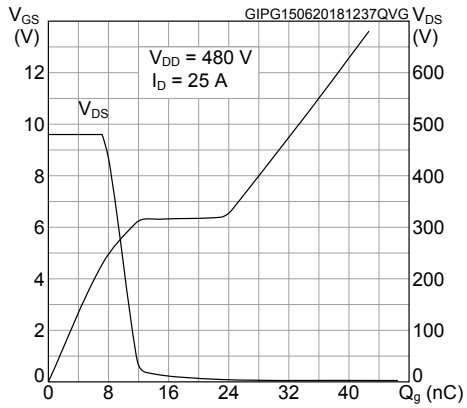



**Figure 6. Static drain-source on-resistance**

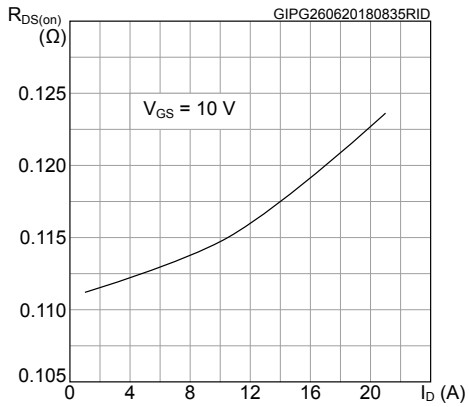


**Figure 7. Capacitance variations**

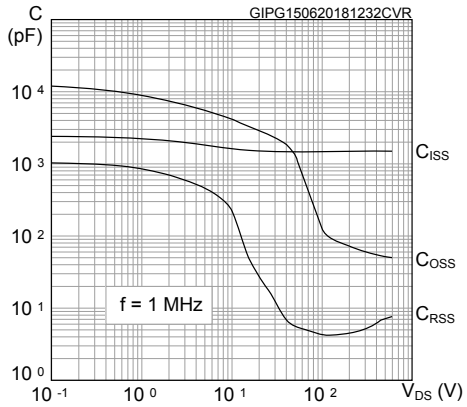



**Figure 8. Normalized gate threshold voltage vs temperature**

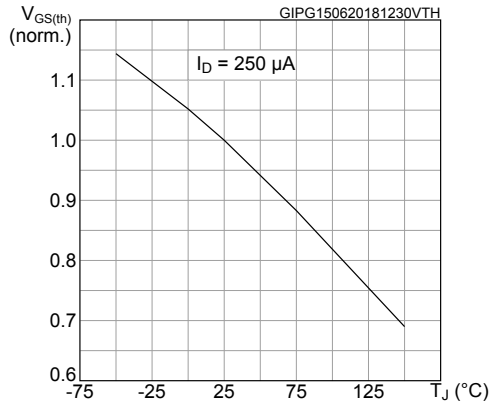



**Figure 9. Normalized on-resistance vs temperature**

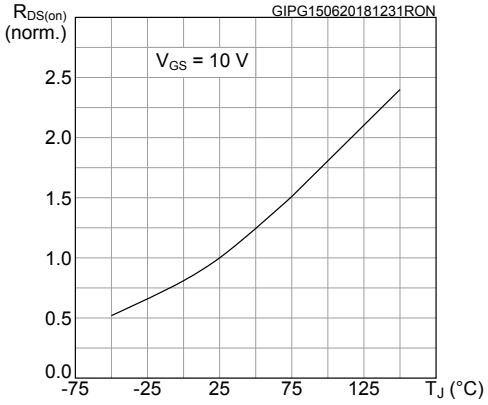



**Figure 10. Normalized $V_{(BR)DSS}$ vs temperature**

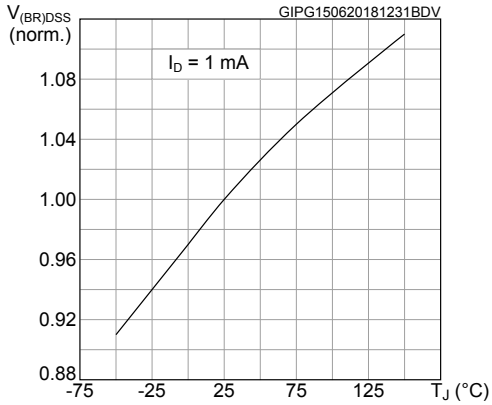



**Figure 11. Output capacitance stored energy**

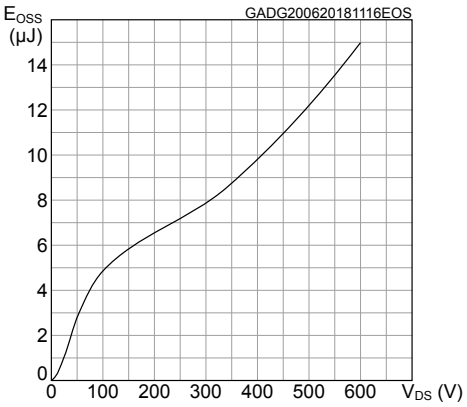
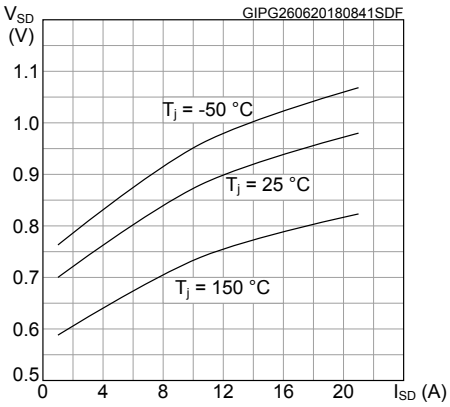



**Figure 12. Source-drain diode forward characteristics**



# 3 Test circuits

**Figure 13. Switching times test circuit for resistive load**

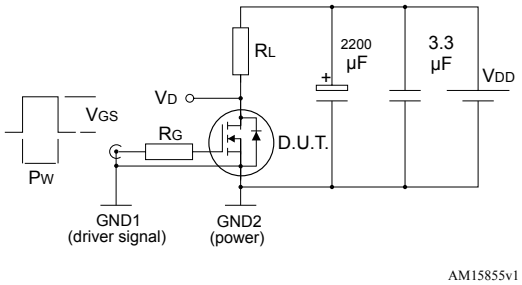



**Figure 14. Test circuit for gate charge behavior**

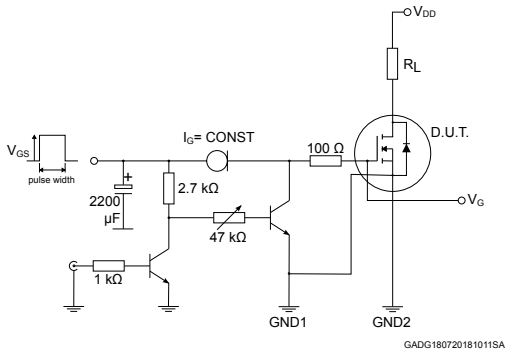



**Figure 15. Test circuit for inductive load switching and diode recovery times**

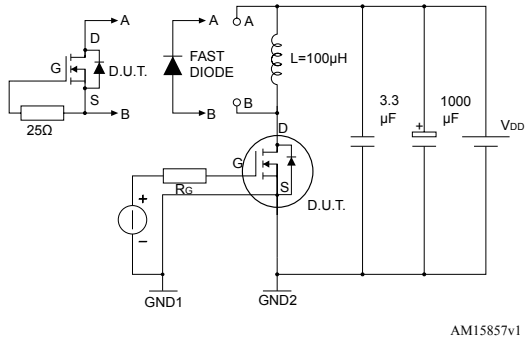



**Figure 16. Unclamped inductive load test circuit**

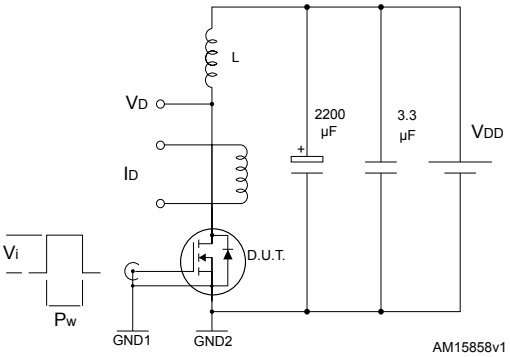



**Figure 17. Unclamped inductive waveform**

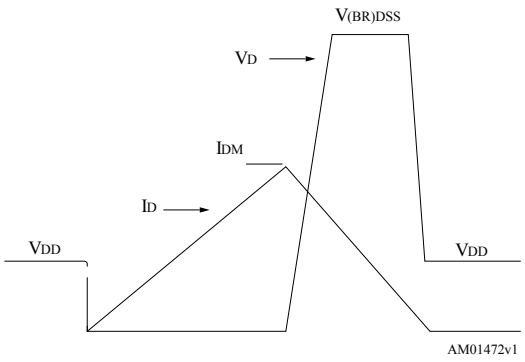
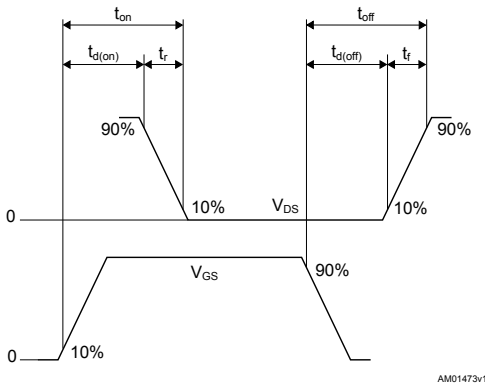



**Figure 18. Switching time waveform**



# 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

## 4.1 PowerFLAT™ 8x8 HV package information

Figure 19. **PowerFLAT™ 8x8 HV package outline**

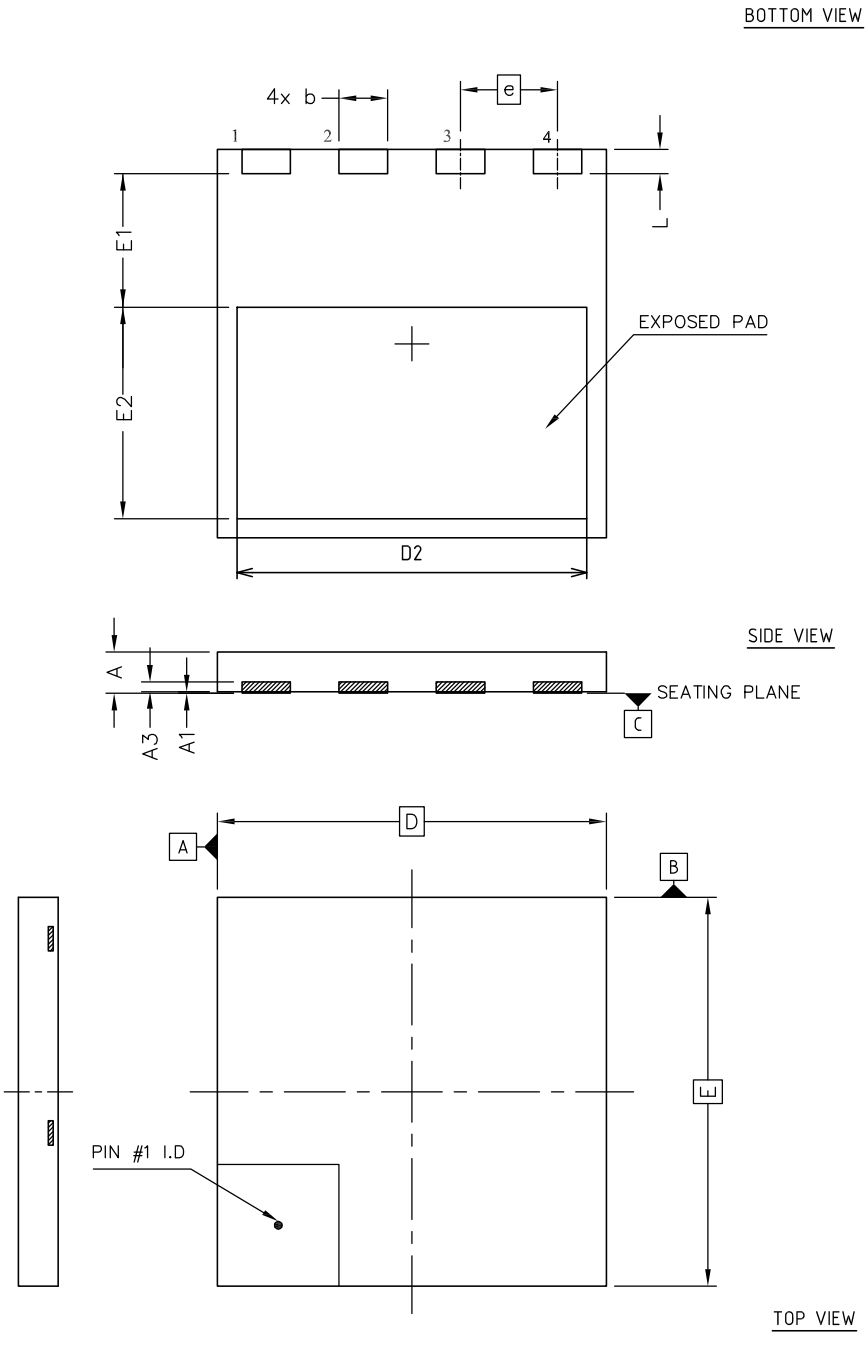
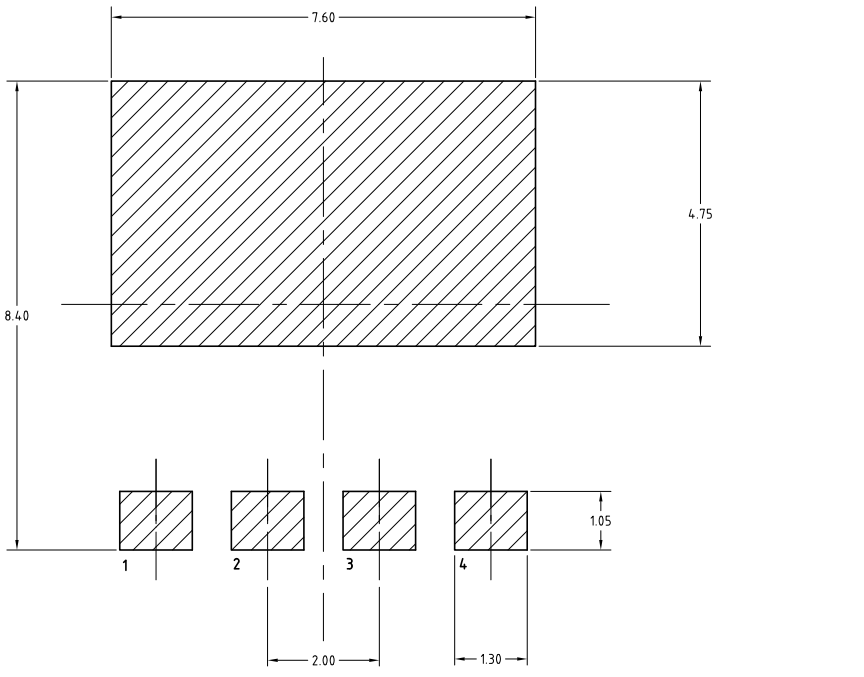


**Table 8. PowerFLAT™ 8x8 HV mechanical data**

| Ref. | Dimensions (in mm) | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 0.75 | 0.85 | 0.95 |
| A1 | 0.00 | | 0.05 |
| A3 | 0.10 | 0.20 | 0.30 |
| b | 0.90 | 1.00 | 1.10 |
| D | 7.90 | 8.00 | 8.10 |
| E | 7.90 | 8.00 | 8.10 |
| D2 | 7.10 | 7.20 | 7.30 |
| E1 | 2.65 | 2.75 | 2.85 |
| E2 | 4.25 | 4.35 | 4.45 |
| e | | 2.00 BSC | |
| L | 0.40 | 0.50 | 0.60 |

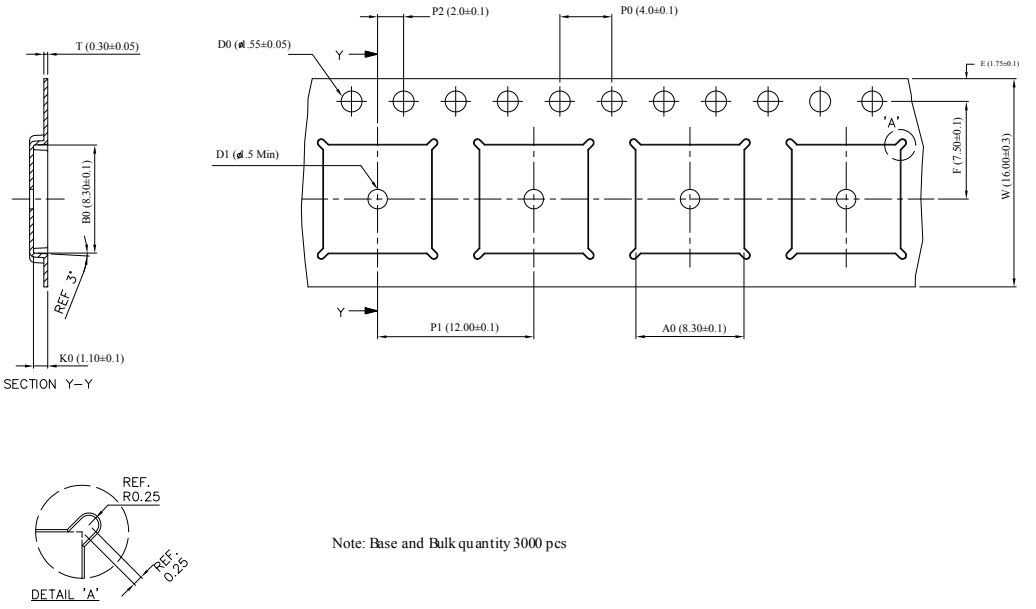
**Figure 20. PowerFLAT™ 8x8 HV footprint**




*Note: All dimensions are in millimeters.*

## 4.2 PowerFLAT™ 8x8 HV packing information

**Figure 21. PowerFLAT™ 8x8 HV tape**




*Note: All dimensions are in millimeters.*

**Figure 22. PowerFLAT™ 8x8 HV package orientation in carrier tape**

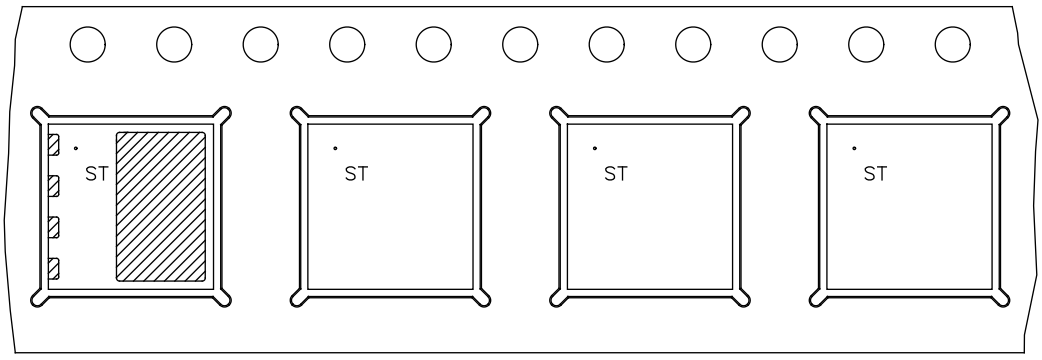
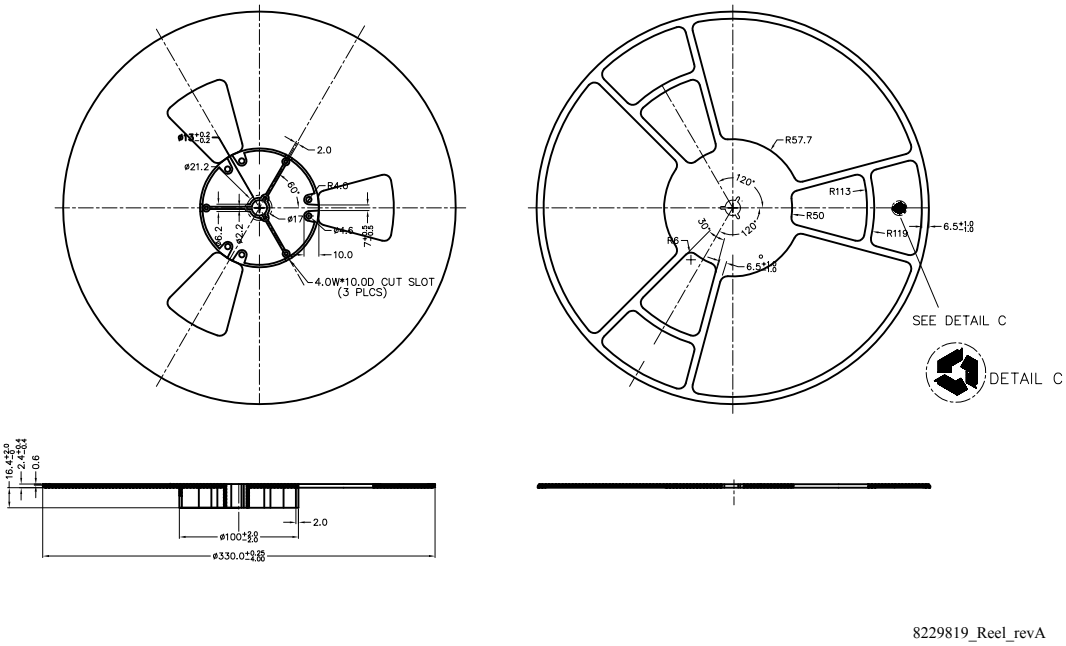


Figure 23. **PowerFLAT™ 8x8 HV reel**




*Note: All dimensions are in millimeters.*

## Revision history

Table 9. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 02-Jul-2018 | 1 | Initial release. |
| 18-Jul-2018 | 2 | Modified Section 3 Test circuits.<br>Minor text changes. |
| 02-Aug-2018 | 3 | Updated features in cover page. |

# Contents