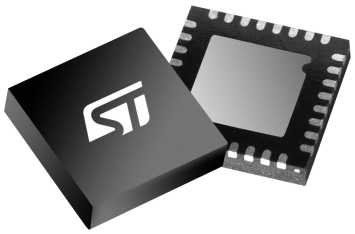
STPM801

Datasheet

Automotive high voltage hot swap, soft start and oring



VFQFN-32 (5x5 mm)

Features

- AEC-Q100 qualified
- Single channel
- Wide input voltage range: 4 V to 65 V
- Reverse input protection -65 V
- 2 external N-channel MOSFET pre-drivers
  - One soft start feature
  - One oring feature
- Quiescent current < 50 µA if WAKE low
- Integrated charge pump
- Input overvoltage protection
- Input undervoltage protection
- Output overcurrent protection
- Complies with the 16750 AC ripple test requirements (50 Hz - 25 kHz)
- Adjustable soft start with external capacitor
- Developed according to ISO 26262 to support ASIL D application

Product status link
STPM801

Product summary		
Order code	Package	Packing
STPM801	VFQFN-32	Tray
STPM801-TR		Tape and Reel

Description

STPM801 offers integrated hot swap, soft start and oring protections. It protects loads from high voltage transients, limiting and regulating the output during an overvoltage event, such as load dump, by controlling the voltage drop across an external N-channel MOSFET.

The STPM801 also monitors the input supply to protect in case of overvoltage (OV) and undervoltage (UV) conditions.

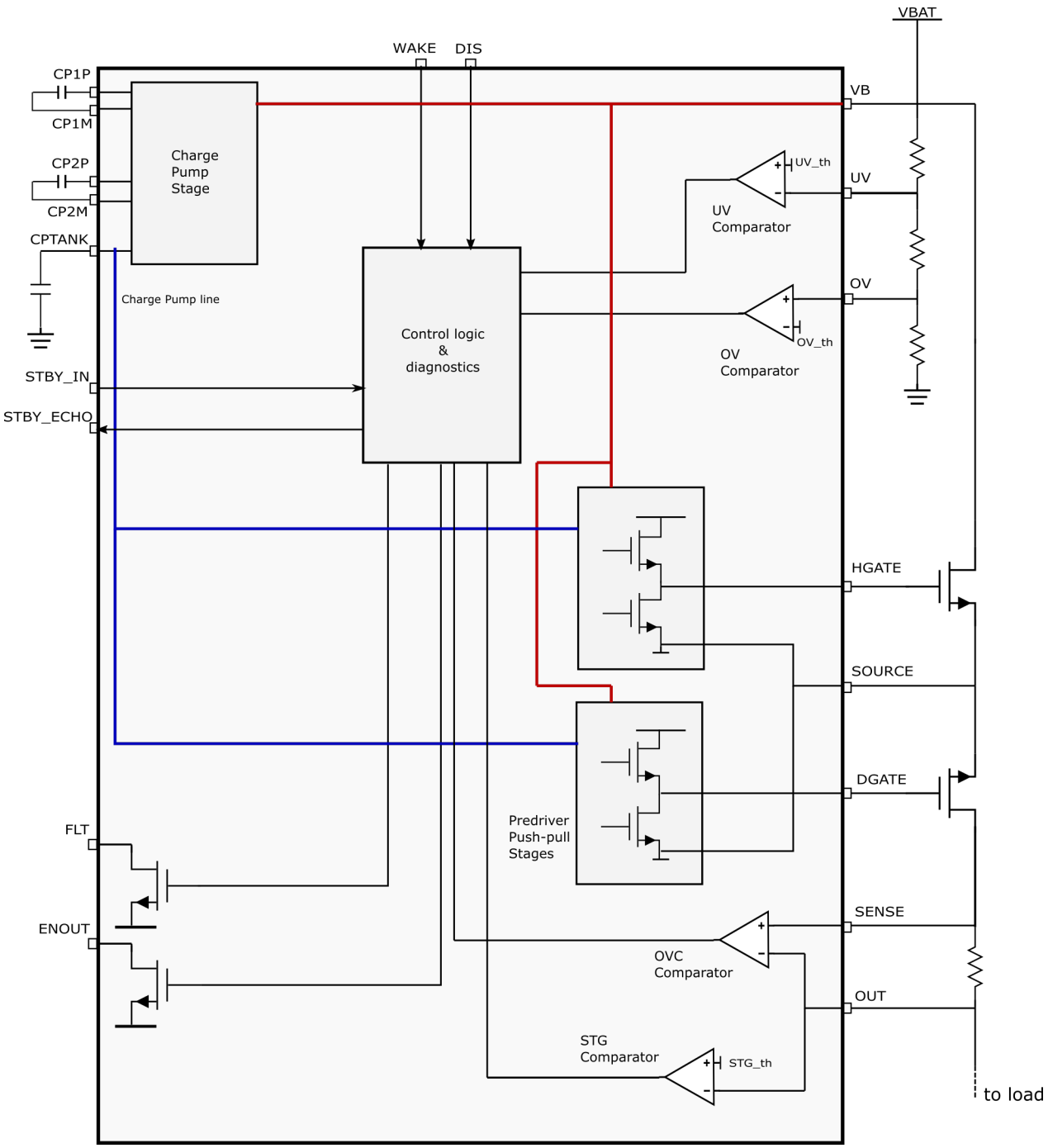
An integrated ideal diode controller drives a second MOSFET (the oring) to replace a Schottky diode for reverse input protection and output voltage holdup. The STPM801 controls the forward voltage drop across the MOSFET and minimizes reverse current transients in case of fault like power source failure, brownout or input short.

STPM801 offers a set of features to support applications that need to fulfill functional safety requirements as defined by automotive Safety Integrity Level (ASIL) A-B-C-D depending on application TSR.

1 Block diagram and pin description

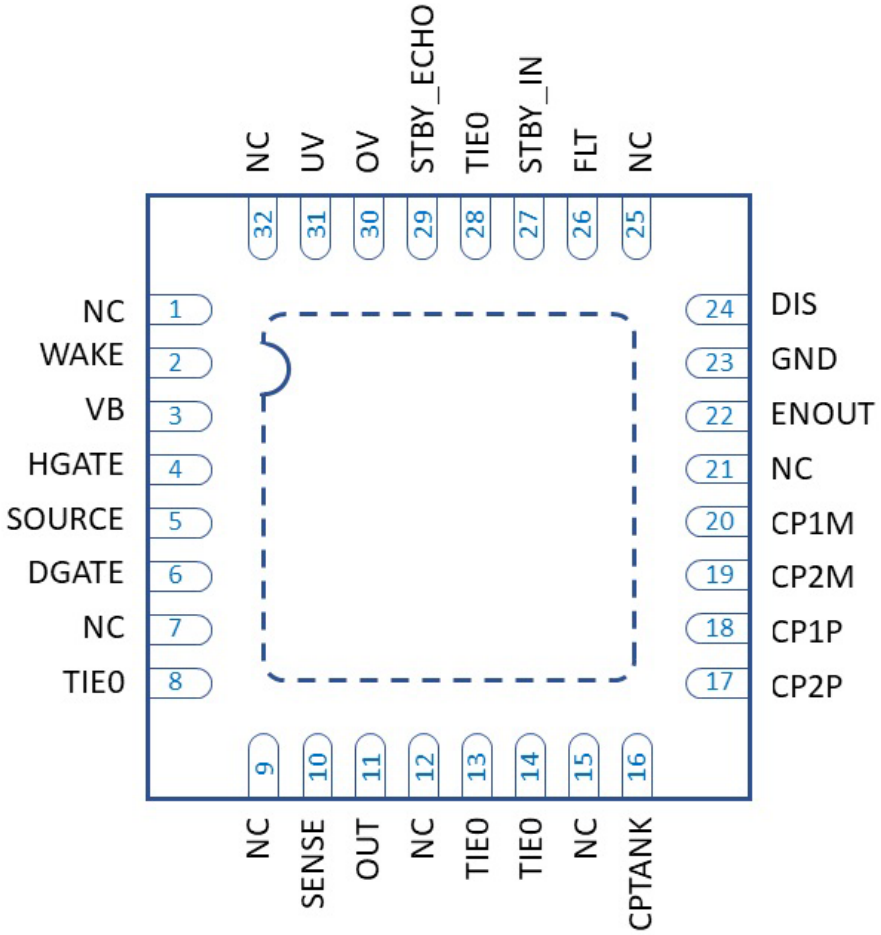
1.1 Block diagram

Figure 1. **STPM801 Block diagram**



1.2 Pin description

Figure 2. **Pin out (top view)**



Note: Exposed pad not electrically connected to the internal substrate.

STPM801 VFQFN32 package is equipped with corner pins, which are electrically floating; it is in any case recommended to solder them towards GND in order to guarantee mechanical robustness.

Table 1. Pin functions and description

No.	Name	Type	Description
1	NC	-	Connect directly to GND
2	WAKE	I	Shutdown control
3	VB	SUPPLY	Input voltage
4	HGATE	I/O	Gate drive output of hot swap MOS
5	SOURCE	I/O	Common source input and gate drive return
6	DGATE	I/O	Diode controller gate drive output enabling oring function
7	NC	-	Connect directly to GND
8	TIE0	-	Connect directly to GND
9	NC	-	Connect directly to GND
10	SENSE	I	External resistor current sense
11	OUT	I	External MOS drain voltage sense
12	NC	-	Connect directly to GND
13	TIE0	-	Connect directly to GND
14	TIE0	-	Connect directly to GND
15	NC	-	Connect directly to GND
16	CPTANK	O	Charge pump output. Connect a capacitor to ground. Typical value 220 nF.
17	CP2P	I/O	Charge pump pin for capacitor 2, positive side
18	CP1P	I/O	Charge pump pin for capacitor 1, positive side
19	CP2M	I/O	Charge pump pin for capacitor 2, negative side
20	CP1M	I/O	Charge pump pin for capacitor 1, negative side
21	NC	-	Connect directly to GND
22	ENOUT	O	Output enable when external MOS are fully on. Internal pulldown works as open drain output and external resistor pulls up the output. Typical 4.7 kW for 5 V IO line.
23	GND	Ground	Ground
24	DIS	I	Disable
25	NC	-	Connect directly to GND
26	FLT	O	FLT output signal when a fault is present. Internal pulldown works as open drain output and external resistor pulls up the output. Typical 4.7 kW for 5 V IO line.
27	STBY_IN	I	Connect directly to GND if standby mode is not used or drive it according to standby chapter
28	TIE0	-	Connect directly to GND
29	STBY_ECHO	O	Connect directly to GND if standby mode is not used or read it according to standby chapter
30	OV	I	Input overvoltage protection. Overvoltage comparator input.
31	UV	I	Input undervoltage protection. Undervoltage comparator input.
32	NC	-	Connect directly to GND

2 Product features

STPM801 is a controller which operates with external back-to-back connected N-channel power MOSFETs, realizing a connection between the input voltage supply line, connected to VB, and the output supply line OUT. STPM801 makes, therefore, available, on OUT, a voltage supply protected against high voltage transients and high load currents. The product can be used either for 12 V or 24 V supply rails.

The two N-channel transistors driven by the device are, respectively, the hot swap and the oring MOSFETs. The first is used as a normal power switch; the soft Start function helps to limit the inrush current during the device power-up. The oring MOSFET is mainly used as ideal diode, but it helps also blocking the current conduction in case of reverse battery detection.

External capacitor connected to HGATE is used to define soft start time, together with HGATE current provided by the device.

The device regulates the forward voltage drop across the oring MOSFET, used as ideal diode (by modulating DGATE voltage), in order to ensure smooth current transfer from one supply to the other, without oscillations. The ideal diode turns on quickly to reduce load voltage drop during supply switch over. Reverse current transients are minimized by means of the reverse battery detection.

Pre-driver acting on DGATE performs fast turn on/turn off, in order to withstand with fast transients pulses of ISO 16750 standard. For driving external MOSFETS with proper timings, a charge pump with external flying and tank capacitors is realized.

A current sense amplifier translates the voltage drop across a shunt resistor to an internal overcurrent flag.

Undervoltage (UV) and overvoltage (OV) on diagnosis on VB are present. Detection thresholds are defined by means of an external voltage divider.

Short to GND (STG) detection on VOUT is present.

VDS comparators are present on both soft start and oring MOSFETs.

ENOUT and FLT are open drain outputs. ENOUT is activated at the startup if VB-VOUT voltage drop is lower than VFULL_ON. FLT is asserted whenever an internal fault is detected.

A standby mode is also available, with device operating at reduced functionality, but allowing a reduction on power dissipation.

3 Maximum ratings

3.1 Operating range

Within the operating range, the part operates as specified and without parameter deviations. The device may not properly operate if maximum operating conditions are exceeded.

Whenever the device comes back into the operating range, after being taken outside it (but without exceeding the Absolute maximum ratings), the part will recover with no damage or degradation.

Additional supply voltage and temperature conditions are given separately at the beginning of each electrical specification table.

All the voltages are referred to the substrate ground if not otherwise specified.

3.2 Absolute maximum ratings and operating voltage

Table 2. Absolute maximum ratings

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Note
WAKE	-	VB = WAKE, all pin GND	-65	-	65	V	-
VB	GLOBAL	All pin GND	-65	-	65	V	-
HGATE	-	HGATE = DGATE = CPTANK, VB = CP1P = CP2P = CP1M = CP2M = SOURCE = SENSE = OUT = 65 V, All pin GND	-65	-	75	V	-
SOURCE	-	-	-65	-	65	V	-
DGATE	-	-	-65	-	75	V	-
TIE0	-	-	-0.3	-	5	V	-
SENSE	-	-0.3 V DC testing condition. SENSE pin can sustain a negative voltage respect GND. SENSE and OUT can drop maximum 3.6 V below GND for maximum 100 µs and 4.6 V below GND for maximum 10 µs	-0.3	-	65	V	-
OUT	-	-0.3 V DC testing condition. OUT pin can sustain a negative voltage respect GND. SENSE and OUT can drop maximum 3.6 V below GND for maximum 100 µs and 4.6 V below GND for maximum 10 µs	-0.3	-	65	V	-
CPTANK	-	-	-0.3	-	75	V	Not usable as external supply
C2P	-	-	-0.3	-	75	V	-
C1P	-	-	-0.3	-	75	V	-
C2M	-	-	-0.3	-	65	V	-
C1M	-	-	-0.3	-	65	V	-
ENOUT	-	-	-0.3	-	65	V	No back-feed in case of supply fault
GND	-	-	-0.3	-	0.3	V	-
DIS	-	-	-0.3	-	65	V	-
FLT	-	-	-0.3	-	65	V	No back-feed in case of supply fault
STBY_IN	-	-	-0.3	-	40	V	-

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Note
STBY_ECHO	-	-	-0.3	-	5	V	-
OV	-	-	-65	-	65	V	-
UV	-	-	-65	-	65	V	-

Table 3. Relative absolute maximum ratings

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Note
CTANK-VB	-	-	-3	-	15	V	
C2P-C2M	-	-	-0.3	-	65	V	
C1P-C1M	-	-	-0.3	-	65	V	
VB-HGATE	-	-	-15	-	65	V	
HGATE-SOURCE	-	-	-0.3	-	15	V	No external DC forced
DGATE-SOURCE	-	-	-0.3	-	12	V	No external DC forced
VB-WAKE	-	-	-0.3	-	65	V	
VB-SOURCE	-	-	-2	-	65	V	
SOURCE-SENSE/OUT	-	-	-65	-	2	V	
SENSE-OUT	-	-	-1	-	1	V	

Charge pump can sustain maximum 105 V with respect to VB during test pulse 1 for short time (less than 100 µs, with CPTANK = +40 V e VBP = -65 V).

SENSE and OUT pins can sustain a negative voltage with respect to GND. SENSE and OUT can drop up to 3.6 V below GND for maximum 100 µs, and up to 4.6 V below GND for maximum 10 µs. This event is sustainable for a limited number in the life of the device, maximum 10 times.

In case of hot swap turning off, due to High load present, VB line can increase very fast. In this case, the maximum rating is 70 V for maximum 100 µs. In this condition CPTANK pin can sustain 77 V for less than 100 µs.

Table 4. Maximum operating voltage

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
WAKE	-	-	-0.3	-	40	V	-
VB	GLOBAL	-	-0.3	-	40	V	-
HGATE	-	-	-0.3	-	50	V	-
SOURCE	-	-	-0.3	-	40	V	-
DGATE	-	-	-0.3	-	40	V	-
SENSE	-	-	-0.3	-	40	V	-
OUT	-	-	-0.3	-	40	V	-
CPTANK	-	-	-0.3	-	50	V	-
CP2P	-	-	-0.3	-	50	V	-
CP1P	-	-	-0.3	-	50	V	-
CP2M	-	-	-0.3	-	40	V	-
CP1M	-	-	-0.3	-	40	V	-
ENOUT	-	-	-0.3	-	40	V	-
GND	-	-	-0.3	-	0.3	V	-
DIS	-	-	-0.3	-	40	V	-

Symbol	Parameter	Condition	Min	Typ	Max	Unit	Pin
FLT	-	-	-0.3	-	40	V	-
STBY_IN	-	-	-0.3	-	5	V	-
STBY_ECHO	-	-	-0.3	-	3.6	V	-
OV	-	-	-0.3	-	40	V	-
UV	-	-	-0.3	-	40	V	-

3.3 ESD data

Table 5. ESD data

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit	Notes
HBM_ ESD	HBM(1)	All pins(2)	-2	-	2	kV	Class 2
CDM _ESD	CDM(1)	All pins	-500	-	500	V	Class C3
CDM_COR_ESD	CDM(1)	Corner pins	-750	-	750	V	Class C4
LUT	Latch up(3)	All pins	-100	-	100	mA	-

1. *According to AEC-Q100-011.*
2. *Pins are all GND connected.*
3. *According to AEC-Q100-004.*

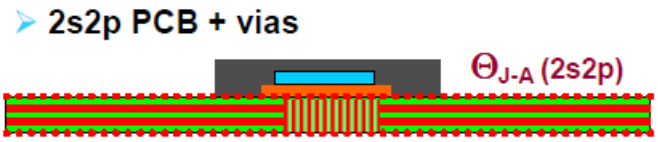
3.4 Temperature range and thermal data

Table 6. Temperature range and thermal data

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
Tamb	Operating temperature (ECU environment)	-	-40	-	125	°C	-
Tj(1)	Operating junction temperature	-	-40	-	150	°C	-
Tj	Extended operating junction temperature	-	-40	-	175	°C	12000 h over life time
Tsto	Storage temperature	-	-55	-	150	°C	
Rth_{J-A}(2)	Thermal resistance junction-to-ambient	-	-	35	-	°C/W	Homogeneous internal power distribution(3)
Rth_{j-cb}(2)	Thermal resistance junction-to-case-bottom	-	-	4	-	°C/W	Homogeneous internal power distribution

1. *All parameters are guaranteed, and tested, in the temperature range -40 ≤ Tj ≤ 150 °C unless otherwise specified. The device is still operative and functional at higher temperatures (up to Tj 175 °C). Device functionality at high temperature is guaranteed by bench validation, electrical parameters are guaranteed by correlation with ATE tests at reduced temperature and adjusted limits (if needed).*
2. *Not subject to production test, guaranteed by design.*
3. *Rth_{J-A} value is retrieved according to Jedec JESD51-2, -5, -7 guideline with a 2s2p board.*

Figure 3. **2s2p PCB with thermal vias**



Note: In "2s2p", the "s" suffix stands for "signal" and the number before indicates how many PCB layers are dedicated to signal wires. The "p" suffix stands for "power" and the number before indicates how many PCB layers are dedicated to power planes.

3.4.1 Thermal protection

Table 7. **Temperature thresholds**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Note
T_{SD_TH}	Thermal shutdown	-	165	175	185	° C	-
T_{SD_hys}	-	Hysteresis	-	10	-	° C	-
TSD_filter	Thermal filter time	Guaranteed by scan	8	10	12	µs	-

4 Functional description

4.1 Functional behavior in detail

In the next paragraphs all device functions, related to device power supply and the pre-drivers, are described in detail.

4.1.1 VB power supply

VB power supply is the main power input of STPM801. VB battery line starts the power-up and the power-down sequences by feeding the subsequent internal purpose circuitries (that is, bandgaps, monitoring units and internal regulators control loops).

VB is compatible to 12 V and 24 V systems. The supply input ranges from 4 V to 65 V. Full functionality and electrical parameters are guaranteed for VB in the range 4 V to 40 V; from 40 V to 60 V full functionality only. Reverse input voltage protection is -65 V.

Device can withstand with 1a, 1b, 2a, 2b, 3a, 3b test pulse of ISO-7637 standards, provided that an appropriate TVS protection is connected on the input battery line.

Once all internal supplies can release POR for the logic section, first of all the trimming parameters are downloaded from OTP memory; after that all the necessary internal checks are performed (analog comparators, clock monitor, safety off path self tests).

If at least one of these internal integrity checks is failing, pre-drivers are disabled and FLT output is asserted low,

If the results of previous checks are fine and no faults are detected, when charge pump is out of undervoltage, the drivers are finally switched on, and FLT output goes high. When device power-up and drivers turn on are completed, ENOUT pin is also released.

Whenever a fault is detected, the drivers are switched off, and FLT pin is asserted low. Fault and clearing methods are reported in Table 18.

Table 8. Power supply parameters

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Pin
VB, range1	Wide range AMR	Full function	4(1)	14	65	V	-
VB, range2	Operating range	Full parameters	4(1)	-	40	V	-
VB, min	Mininum VB to turn on device	-	6	-	-	V	-
ION	Supply current at T = 25 °C	VB = 14 V, device enable VOUT = VSENSE = VSOURCE, HGATE ON, DGATE regulation If VB is not present, or lower than OUT, current is sunk from OUT.		-	14	mA	-
ION_hot	Supply current at T = 150 °C	VB = 14 V, device enable VOUT = VSENSE = VSOURCE, HGATE ON, DGATE regulation If VB is not present, or lower than OUT, current is sunk from OUT.	-	-	16	mA	-
Isd_hot	Supply current in shutdown at VB = 14 V, T = 150 °C	VB = 14 V, device disabled	-	-	50	µA	VB
Isd	Supply current in shutdown at VB = 14 V, T = 25 °C	VB = 14 V, device disabled	-	-	25	µA	VB

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Pin
Isdtot_hot	Supply current in VB, UV, OV, WAKE pin during device shutdown at 14 V, T = 150 °C	Guaranteed by design	-	-	55	µA	VB, UV, OV, WAKE
Isdtot	Supply current in VB, UV, OV, WAKE pin during device shutdown at 12 V, T = 25 °C	Guaranteed by design	-	-	30	µA	VB, UV, OV, WAKE
VB_Slope_fast	maximum rise slew rate of VB line	Device OFF	-	-	1	V/µs	VB
VB_Slope_fast_ON		Device ON, driver OFF, VB > 8 V	-	-	5	V/µs	VB
		Device ON, driver ON.	-	-	0.2	V/µs	VB
VB_Slope_slow (rising and falling)	Minimum slew rate on VB line		0.5	-	-	V/s	VB

1. *Cranking scenario. PWR_UP occurs at VB ≥ VB_min.*

4.1.2 WAKE

A key pin (WAKE) acts as control input. Pulling WAKE pin below Turn_OFF threshold triggers the power down sequence. At first, both hot swap and oring pre-driver outputs are turned OFF, by triggering the internal active pull-down, for typically 1 ms power down_dly timing. After that, the device is turned off, with consequent reduction of current absorption from VB pin. Pulling this pin above Turn_ON threshold allows the internal startup circuits to turn the device again. A 1 ms filter time is applied on WAKE pin, on both rising and falling edges, in order to prevent device from turning on and off in a wrong way, due to disturbances present on WAKE pin.

When the device is off (without VB or WAKE LOW), HGATE AND DGATE are kept in high impedance (turn OFF guaranteed by the external passive components).

If VB rises up, starting from 0 V, and OUT is higher than STG threshold, VDS comparators could be set, depending on the timing of starting profile.

Table 9. WAKE input parameters

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Pin
WAKE_high_th	WAKE turn ON threshold	-	2.1	-	2.7	V	WAKE
WAKE_low_th	WAKE turn OFF threshold	-	1.4	-	2	V	WAKE
WAKE_hys	WAKE hysteresis	-	0.5	-	1	V	WAKE
WAKE_pd	WAKE leakage	WAKE < WAKE_high_th -200 mV	0.4	-	10	µA	WAKE
WAKE,ft	WAKE filter time	Guaranteed by scan	0.9	1	1.1	ms	-
Powerdown_dly	Power down delay time	Guaranteed by scan	0.9	1	1.1	ms	-

4.1.3 UV and OV detection

An external voltage divider is present on VB pin. UV and OV pins of the device are connected to this voltage divider. UV and OV voltages are compared with a fraction of internal bandgap reference.

When the UV pin falls below its 1 V threshold, HGATE and DGATE pins are pulled down. When the UV pin rises above 1.2 V HGATE and DGATE pins are pulled up.

When OV is above its 1.2 V threshold, both HGATE and DGATE are turned OFF. When OV falls below 1 V, both HGATE and DGATE pins are allowed to turn on again if there are no other faults. At power-up, an OV voltage higher than threshold blocks turn-on of the external drivers controlled by HGATE and DGATE pins.

See also Table 18 for details.

Figure 4. **Under voltage and over voltage detection**

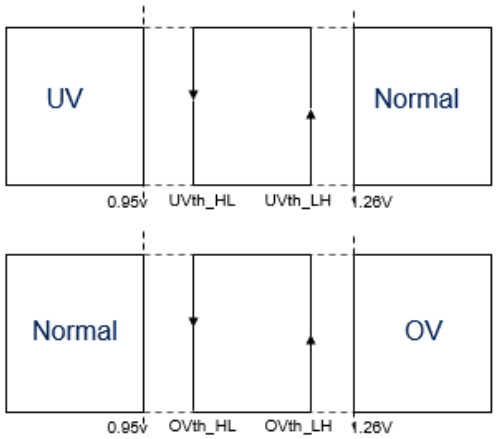
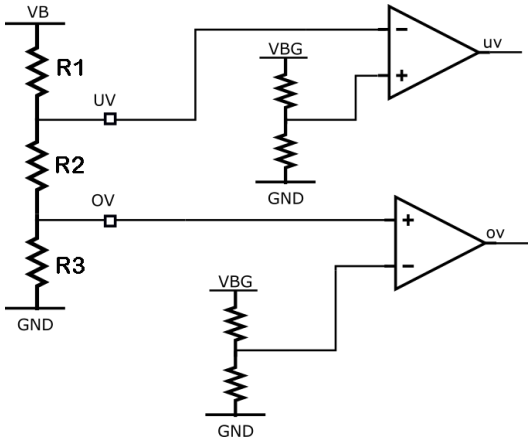


Table 10. **Under voltage and over voltage parameters**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Note
UVth,hl	Undervoltage threshold	-	0.95	1	1.05	V	UV
UVth,lh	Undervoltage threshold	-	1.14	1.2	1.26	V	UV
UV,flt	UV filter time	Guaranteed by scan	-	-	100	µs	-
OVth,lh	Overvoltage threshold	-	1.14	1.2	1.26	V	OV
OVth,hl	Overvoltage threshold	-	0.95	1	1.05	V	OV
OV,flt	OV filter time	Guaranteed by scan	-	-	10	µs	-
UV,leak	UV leakage	-	-	-	1	µA	UV
OV,leak	OV leakage	-	-	-	1	µA	OV

Figure 5. **OV and UV - VB diagnostic simplified block diagram**



User needs to size R1, R2, R3 in order to define proper detection values on VB (depending on, most of all, if 12 V or 24 V systems are used), considering that internal circuitry detects undervoltage or overvoltage conditions, when correspondent pins are equal to the threshold values summarized in Table 10.

4.1.4 OVC and STG

Overcurrent protections act sensing the voltage drop across an external shunt resistance, connected between SENSE and OUT pin.

The OVC thresholds and related filter time depend on the status of the output voltage, if a short to GND condition is also detected or not.

- In case of no short to ground detected on the output voltage
  - the OVC threshold voltage is OC_HV_th and the OVC filter time is OC_HV_flt.
  - during overcurrent detection, while the filter time OC_HV_flt is applied, shall the current increase and the voltage across the shunt go above the threshold OC_HV_fast_th, the filter time is shortened to the value OC_HV_fast_flt.
- In case of short to ground detected on the output voltage:
  - the OVC threshold voltage is OC_LV_th and the OVC filter time is OC_LV_flt.
  - during overcurrent detection, while the filter time OC_LV_flt is applied, shall the current increase and the voltage across the shunt go above the threshold OC_LV_fast_th, the filter time is shorted to the value OC_HV_fast_flt.

This architecture provides additional protection in case of output shorted to GND, lowering the threshold value. Moreover, if a strong overcurrent condition is detected (current exceeding the HV_fast or LV_fast thresholds), the filter time is also shortened in order to limit as much as possible high current levels through external FETs (see Figure 6). When overcurrent detection time is expired, the HGATE and DGATE external FET are driven OFF by the internal pulldown. Auto-retry function is present, and it is described in Section 4.2.2 Overcurrent auto retry.

Figure 6. Overcurrent digital architecture

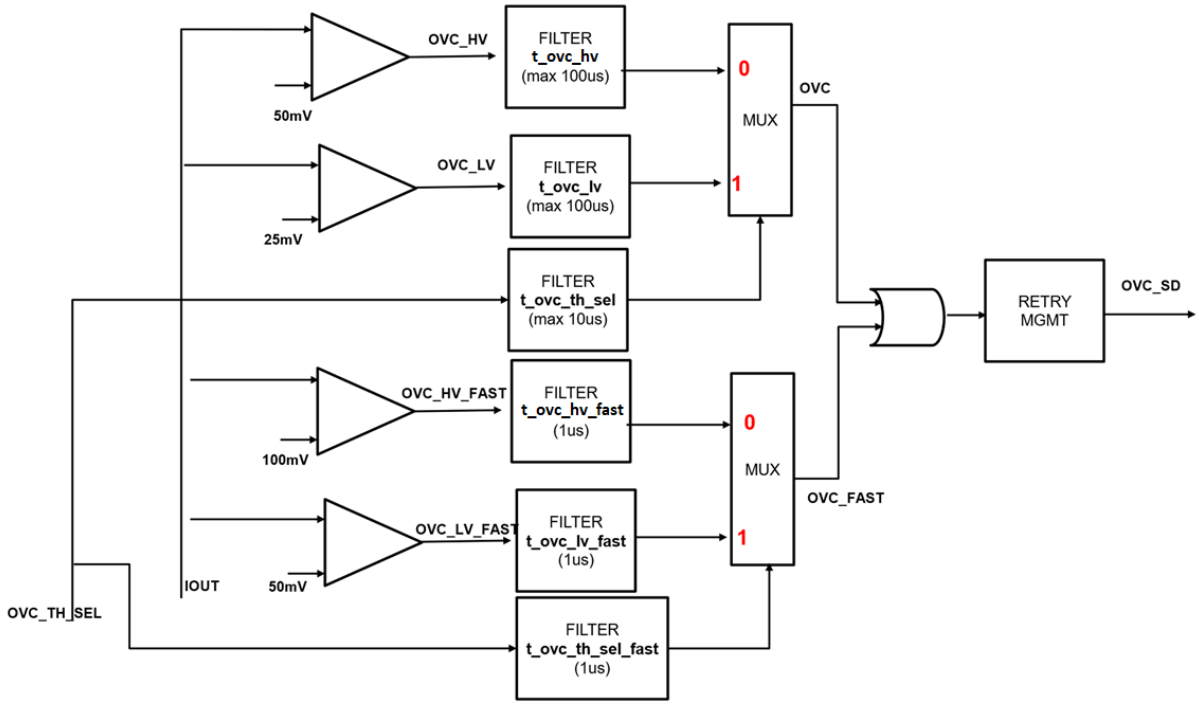
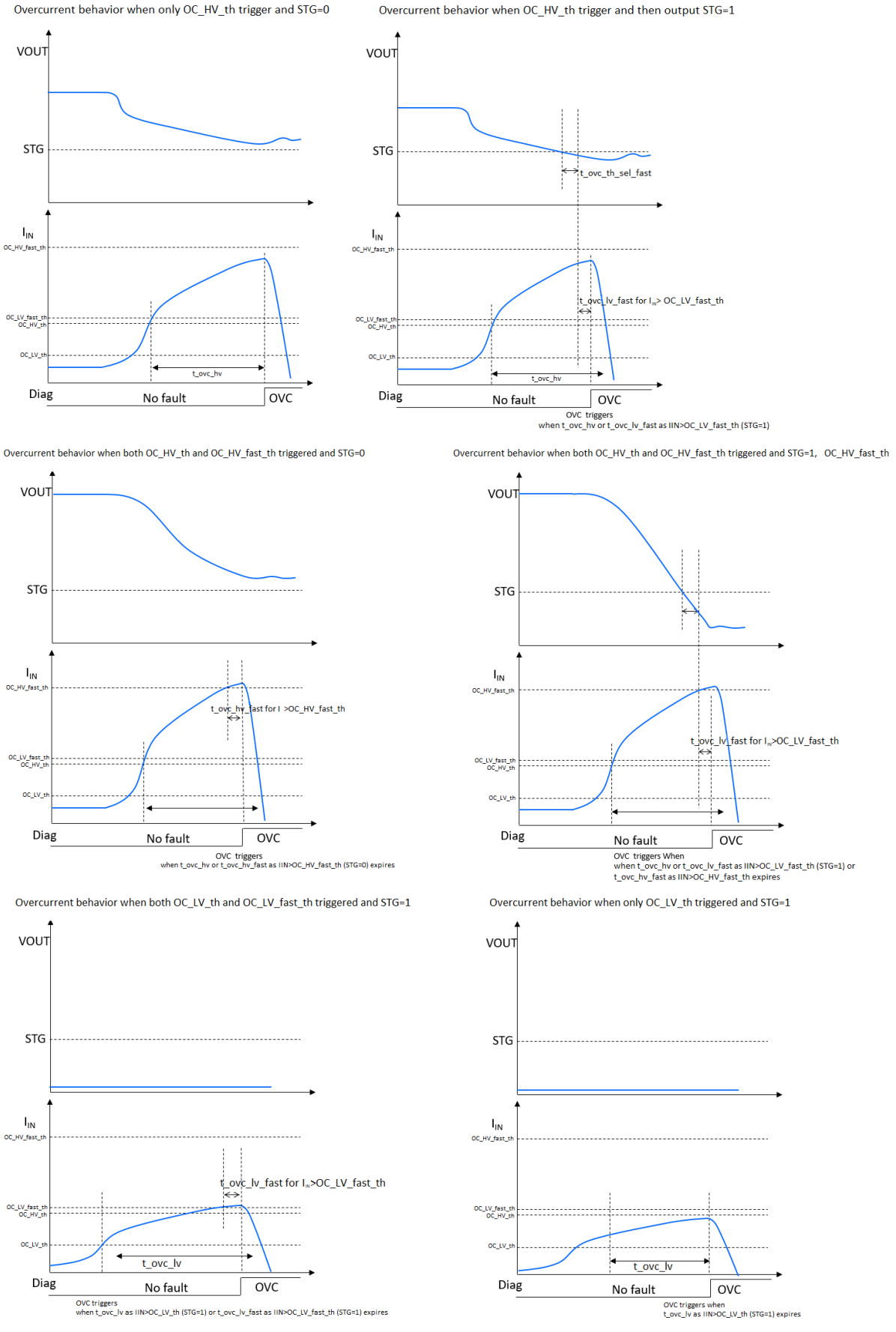


Figure 7. OVC timing and thresholds



STG detection is present on VOUT pin with a filter time *STG.flt*. When short is detected, the FLT pin is asserted low, while MOSFET driving signals HGATE/DGATE depend on the presence of other fault events at the same time.

During device power-up, with VOUT externally shorted, blanking time STG_blank is active, STG comparator is masked and has no impact on FLT pin. However, external MOSFET are protected by overcurrent protection features.

Table 11. Over current and short to GND parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Note
OC_HV_th	Overcurrent threshold (VSENSE - VOUT), VOUT > STG threshold	-	50	55	62.5	mV	SENSE, OUT
OC_LV_th	Overcurrent threshold (VSENSE - VOUT), VOUT < STG threshold	-	19	25	32	mV	SENSE, OUT
OC_HV_fast_th	Overcurrent threshold (VSENSE - VOUT), VOUT > STG threshold	-	90	100	110	mV	SENSE, OUT
OC_LV_fast_th	Overcurrent threshold (VSENSE- VOUT), VOUT< STG threshold	-	38	50	62	mV	SENSE, OUT
OC_HV_flt	Overcurrent filter time	STG = 0, guaranteed by scan	80	-	100	µs	-
OC_LV_flt	Overcurrent filter time	STG = 1, guaranteed by scan	80	-	100	µs	-
OC_HV_fast_flt	Overcurrent filter time	STG = 0, guaranteed by scan and design	1	-	2.2	µs	-
OC_LV_fast_flt	Overcurrent filter time	STG = 1, guaranteed by scan and design	1	-	2.2	µs	-
STG_th	OUT short to ground threshold	-	2.5	3.2	3.9	V	OUT
STG_flt	Short to ground filter time	Guaranteed by scan	-	-	10	µs	-
STG_blank	Blanking time from driver turning on command	Guaranteed by scan	80	-	100	ms	-

4.1.5 ENOUT

ENOUT is an open-drain output, going in high impedance when the voltage at the OUT pin is above (VB - VFULL_ON), indicating that the external MOSFETs are fully on. ENOUT pin cannot be asserted if WAKE pin voltage is below turn off threshold.

Table 12. ENOUT parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Note
ENOUT_OD_LL	ENOUT_OD low level	Pull-up current = 1 mA	-	-	0.4	V	ENOUT
ENOUT_Leakage	ENOUT_OD leakage	Apply 5 V to FLT, output buffer off	-	-	10	µA	ENOUT
VFULL_ON	VB-VOUT difference for releasing ENOUT	-	0.5	0.8	1.1	V	-
FULL_ON_flt	Filter time to activate ENOUT	Guaranteed by scan	-	-	100	µs	-

4.1.6 FLT

FLT is an open-drain output that is asserted low when a fault is detected, after that a proper filter time is elapsed (depending on the fault type). Fault pin cannot be asserted if WAKE pin voltage is below turn off threshold.

Table 13. FLT parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Note
FLT_OD_LL	FLT_OD low level	Pull-up current = 1 mA	-	-	0.4	V	FLT
FLT_OD_Leakage	FLT_OD leakage	Apply 5 V to FLT, output buffer off	-	-	10	µA	FLT

4.1.7 Charge pump

The charge pump supplies the voltage necessary to drive the external N-channel MOSFETs. Average current capability for the charge pump can guarantee proper turn on and turn off timings for oring MOSFET also in case of AC ripple on the supply line (standard ISO 16750).

The charge pump is enabled immediately at the device power-up, once the battery level is higher than under-voltage threshold, and WAKE input is high.

In case of under voltage on the charge pump (CP_UV), it is not possible to drive in the proper way the external MOSFETs; the pre-drivers are therefore switched OFF and FLT pin is asserted low.

The same check on CP voltage is done during the power-up. Once CP_UV is released, device can complete the power-up sequence. If CP_UV is not released by CP_UV_TIMEOUT expiration, drivers are turned off and FLT is asserted.

Figure 8. Charge pump configuration simplified block diagram

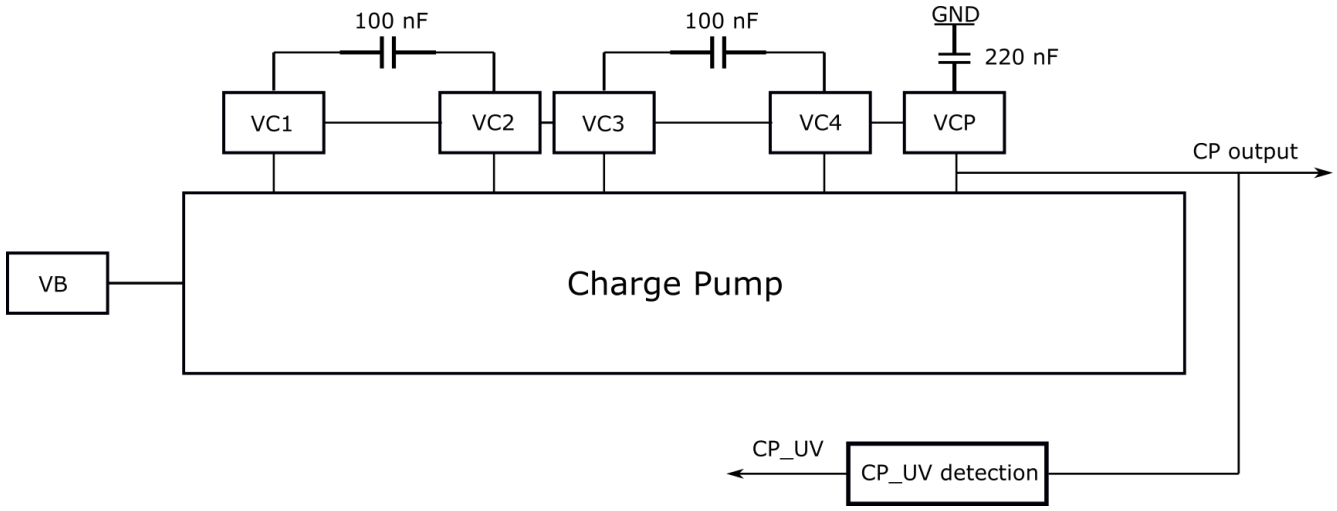


Table 14. Charge pump parameters

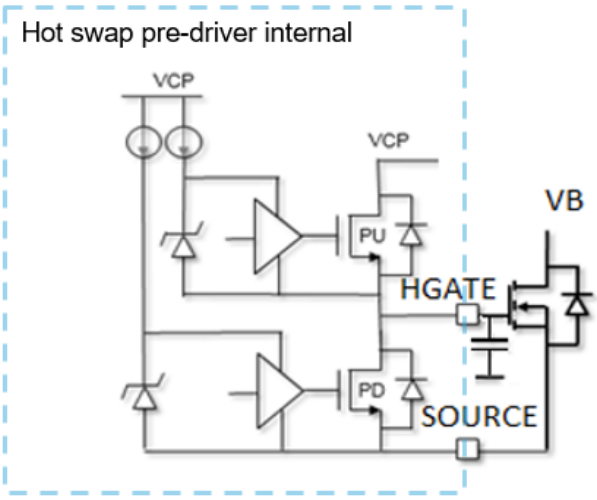
Symbol	Parameter	Test condition	Min	Typ	Max	Unit	PIN
VCP	Charge pump voltage	VB = 14 V, value referred to VB (voltage above VB)	9	11.8	15	V	CPTANK
VCP_low	Charge pump voltage	VB = 4.5 V, value referred to VB (voltage above VB)	5	-	-	V	CPTANK
CP_UV_L	Charge pump Undervoltage_L	CPTANK pin falls from VB + 11 V to VB + 0, Value referred to VB (voltage above VB)	4	-	5	V	CPTANK
CP_UV_H	Charge pump Undervoltage_H	CPTANK pin rises from VB + 0 to VB + 11 V, Value referred to VB (voltage above VB)	4.5	-	5.5	V	CPTANK

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	PIN
CP_UV_flt	Charge pump undervoltage filter time	Guaranteed by SCAN	7	10	12	µs	-
Fs	CP switching frequency	-	-	385	-	kHz	-
Cfly	C1 and C2 flying capacitor	-	80	100	120	nF	-
CPTANK	Tank output capacitor	-	176	220	264	nF	CPTANK
CP_UV_TIMEOUT	Charge pump undervoltage timeout	Guaranteed by SCAN	1.8	-	2.2	s	-
CPRegulation_OVmode	Charge pump regulation in OV condition	Put OV pin higher than 1.26 V and measure CP regulation	8.5	-	10.5	V	CPTANK

4.1.8 Hot swap pre-driver and soft start

An internal pre-driver, supplied by charge pump, can drive HGATE at a voltage that typically is clamped ΔV_{HG1_12V} above battery line, completely turning ON hot swap MOSFET.

Figure 9. Hot swap pre-driver simplified structure

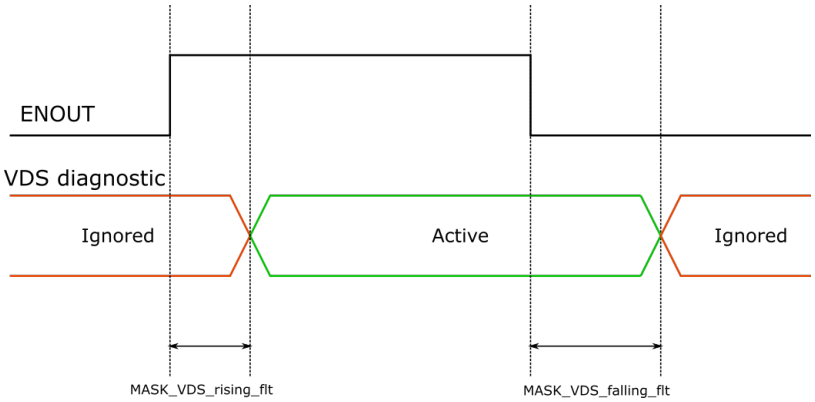


The pre-driver is floating with respect to the substrate and directly referred to the external FET gate-source terminals, allowing a better driving also during fast transient commutations, and can sustain, without being damaged, deep negative pulses.

A capacitor (maximum value 100 nF) is connected on HGATE pin, allowing the control of soft start timing during hot swap switching ON. This turn-on transient is, in fact, controlled by the charge at constant current I_{HG_PU} (gate pull-up current) of this capacitor. The more soft start timing is increased, the more the inrush current during the power-up is reduced. On the other hand, the switching OFF is realized with a strong pull-down current.

When ENOUT is de-asserted, hot swap VDS comparator is ignored. When the full on condition (OUT > VB - VFULL_ON, ENOUT asserted) is reached, the VDS comparator is enabled after MASK_VDS_rising_flt masking time. Indeed, when ENOUT is de-asserted again, the VDS comparator is ignored after MASK_VDS_falling_flt masking time. The behavior of VDS diagnostics is shown in Figure 10.

Figure 10. **VDS diagnostic enabling signal**



Every time hot swap driver is turned ON, the VDS comparator is masked until Hotswap_VDS mask_soft_start_flt is expired (and the other masking conditions disappear).

Table 15. **Hot swap and pre-driver parameters**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Hotswap_ΔV_{HG1_4V}	HGATE gate drive, (VHGATE − VSOURCE)	Drive voltage at VB = 4.5 V CP = VB + 5.3, VB + 6	5	-	-	V
Hotswap_ΔV_{HG1_12V}	HGATE gate drive, (VHGATE − VSOURCE)	Drive voltage at VB = 14 V, CP = VB + 15, VB + 9	9	-	13	V
Hotswap_$I_{HG,PU}$	GATE pull-up Current	-	20	37	55	µA
Hotswap_$I_{HG,PD}$	GATE pull-down Current	-	50	80	120	mA
Hotswap_VDS	VDS on soft start MOS. A fault is generated if detection happens after ENOUT set	-	0.8	1	1.2	V
Hotswap_VDS_flt	VDS detection filter time	Guaranteed by scan	0.8	0.9	1	ms
MASK_VDS_rising_flt	Masking diag on filter time after ENOUTrising edge	Guaranteed by scan	80	100	120	µs
MASK_VDS_falling_flt	Masking diag on filter time after ENOUTfalling edge	Guaranteed by scan	1	1.2	1.4	ms
Hotswap_VDS_mask_soft_start_flt	Soft start blanking time	Guaranteed by scan	80	90	100	ms

4.1.9 Oring pre-driver

The pre-driver for Oring MOSFET is an ideal diode regulator. When the load current creates more than Oring_Full_ON of drop across the MOSFET (Oring_Full_ON comparator), the DGATE pin is pulled high by an internal charge pump current source and clamped to Oring_ΔV_{DG2_12V} above the SOURCE pin.

When the load current is small enough, the DGATE pin is actively driven to maintain Oring_VREG across the MOSFET by actively regulating DGATE, thus implementing ideal diode function. In case of reverse voltage of more than Oring_VREV across the MOSFET (SOURCE - VSENSE voltage drop), the oring MOSFET is turned off, thus preventing reverse current from flowing from OUT to VB.

During normal operating condition, VGS of oring external FET is driven to allow the correct current load (VSense - VSource = Oring_VREG). For fast turning on and off condition, (when Vsense - Vsource > Oring_Full_ON) an internal comparator activates a strong pullup current on DGATE pin.

Oring reverse and full on comparators are also used to quickly turn on and off the oring MOSFET, in order to withstand with AC ripple disturbances (standard ISO 16750) and preventing AC noise from being transferred on VOUT line.

This pre-driver implements same diagnosis and masking of hot swap pre-driver, such as VDS detection, shown in Figure 10.

The VDS comparator of oring is also masked until the full on condition (OUT > VB - VFULL_ON) is reached.
Every time the oring pre-driver is turned ON, the VDS comparator is masked until a Oring_VDS_mask_soft_start_flt is expired (and the other masking conditions disappear).

Table 16. Oring pre-driver parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Oring_ΔV_{DG2_4V}	DGATE gate drive, (VDGATE - VSOURCE)	Drive voltage at VB = 4.5 V CP = VB + 5.3, VB + 6	4.5	-	-	V
Oring_ΔV_{DG2_12V}	DGATE gate drive, (VDGATE - VSOURCE)	Drive voltage at VB = 14 V, CP = VB + 11, VB + 9	6	-	8	V
Oring_V_{DG_12V}	DGATE gate driver, upper limit respect charge pump value	Drive voltage at VB = 14 V, CP = VB + 11 V, guaranteed by design	-	-	CP-1	V
Oring_$I_{DGATE(UP)}$	DGATE oring pull-up Current, peak	Peak current guaranteed by design, switch on time < 2 µs, 15 nF from 0 V to 4.5 V at VB 14 V	55	-	180	mA
Oring_$I_{DGATE(UP)_VBmin}$	DGATE oring pull-up Current, peak at VB min	Peak current guaranteed by design, switch on time < 3 µs, 15 nF from 0 V to 4.5 V at VB 4.5 V	45	-	130	mA
Oring_$I_{DGATE(DN)}$	DGATE oring pull-down Current, peak	Peak current guaranteed by design, switch off time < 1.5 µs, 15 nF from regulated to 1.5 V	100	-	300	mA
Oring_$I_{DGATE(DN)_VBmin}$	DGATE oring pull-down Current, peak	Peak current guaranteed by design, switch off time < 1.5 µs, 15 nF from regulated to 1.5 V	90	-	250	mA
Oring_VREG	Ideal diode regulation voltage, (VSOURCE - VSENSE)	-	15	30	47	mV
Oring_Fullon	(VSOURCE - VSENSE) for fast turn ON activation	-	60	80	130	mV
Oring_VREV	Reverse voltage shut off (VSOURCE - VSENSE)	-	-20	-10	-4	mV
Oring_Turnoff_delay	DGATE turn-off propagation delay	Guaranteed by design	-	-	0.6	us
Oring_VDS	VDS on oring MOS.generates FLT if detection happens	-	270	300	330	mV
Oring_VDS_flt	Short detection filter time	Guaranteed by scan	0.8	0.9	1	ms
Oring_VDS_mask_soft_start_flt	Soft Start blanking time	Guaranteed by scan	80	90	100	ms
Source_Rev_Leakage	Source input leakage	VB floating < OUT = SENSE = 14 V, Force SOURCE pin 5 V measure sinked current	-	-	4	mA

4.1.10 DISABLE

When DIS pin is driven at high logic level, the device turns off HGATE and DGATE with internal pulldown. Differently from WAKE, DIS assertion turns off the pre-drivers only, but the device remains supplied. When DIS pin is driven at low logic level, the device turns on HGATE and DGATE with internal pullup.

For internal pulldown and pullup specification, refer to Section 4.1.9 Oring pre-driver.

Table 17. DISABLE parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
DIS_in_hl_th	High input voltage range	-	2	-	-	V

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
DIS_in_ll_th	Low input voltage range	-	-	-	0.8	V
DIS_in_pd	Internal pull down current	Pin = 3.3 V	20	40	60	µA
DIS_flt	Disable pin filter time	Guaranteed by scan	1.6	-	3	us

4.2 Fault management

In the next paragraphs all device functions related to faults handing are described.

4.2.1 Fault table

In the following table all the faults causing an alarm on FLT pin, with proper filter time, are listed.

To clear a latched fault, the WAKE pin has to be set low for its filter time (1 ms) and then set again to high for its filter time; after that a new power-up sequence can start.

Table 18. Fault table

Event	Filter time	HGATE	DGATE	FLT	Latched	Action for coming back to operating	Scenario
OV	10 µs	Low	Low	Active	Not	OV disappears and no other faults present	Input overvoltage starting from device ON condition
UV	100 µs	Low	Low	Active	Not	UV disappears	Input undervoltage starting from device ON condition
HOTSWAP VDS detection	1 ms	Low	Low	Active	Yes	Toggling WAKE	After softstart finish, M1 is open
ORING VDS detection	1 ms	Low	Low	Active	Yes	Toggling WAKE	M2 VDS short
Overcurrent	1/100 µs	Low	Low	Active	Latched after 32 retries	Toggling WAKE	Output overcurrent
STG	10 µs	No effect	No effect	Active	Not	N.A.	Output short to a lower fixed voltage level
VB < VOUT	10 µs	High (VDS masked)	Low (VDS masked)	Not active	Not	Reverse battery condition VB<VOUT disappear	Reverse current VBAT < Vout
CP_UV	10 µs	Low	Low	Active	Not	If CP_UV disappears	UV on charge pump - VGS on MOSFETs cannot be guaranteed
OT	10 µs	Low	Low	Active	Not	If OT disappears	Over-temperature detected
DIS	3 µs Max	Low	Low	Active	Not	If DIS is not active	DIS pin is not asserted
SAFETY_FAULT	100 µs fault detection	Low	Low	Active	Yes	Toggling WAKE	Selftest fail or clock monitor error or OTP CRC fail

If a reverse condition (VB < VOUT) is detected, VDS comparators of Oring and hot swap are both masked to avoid false detection.

Pre-driver VDS diagnostic is implemented and optimized to work with a recommended bill of material (see Table 24).

4.2.2 Overcurrent auto retry

When an overcurrent condition is detected, the device turns off HGATE and DGATE.

After retrying cooling down, the device tries again to switch them ON (auto retry function) for Tretry_attempt.

In case, after the auto retry attempt, the device recognizes OVC again, the turn OFF procedure of the drivers is triggered again.

Maximum number of retries is retry#: once this counter is expired, if the OVC is still present, the fault is latched and HGATE and DGATE are permanently switched off.

A toggling on WAKE input is, therefore, necessary to re-engage the device and unlatch the fault.

If one of the retry attempts is successfully concluded, the counter of the retry is reset (see Figure 11).

Figure 11. Auto retry mechanism

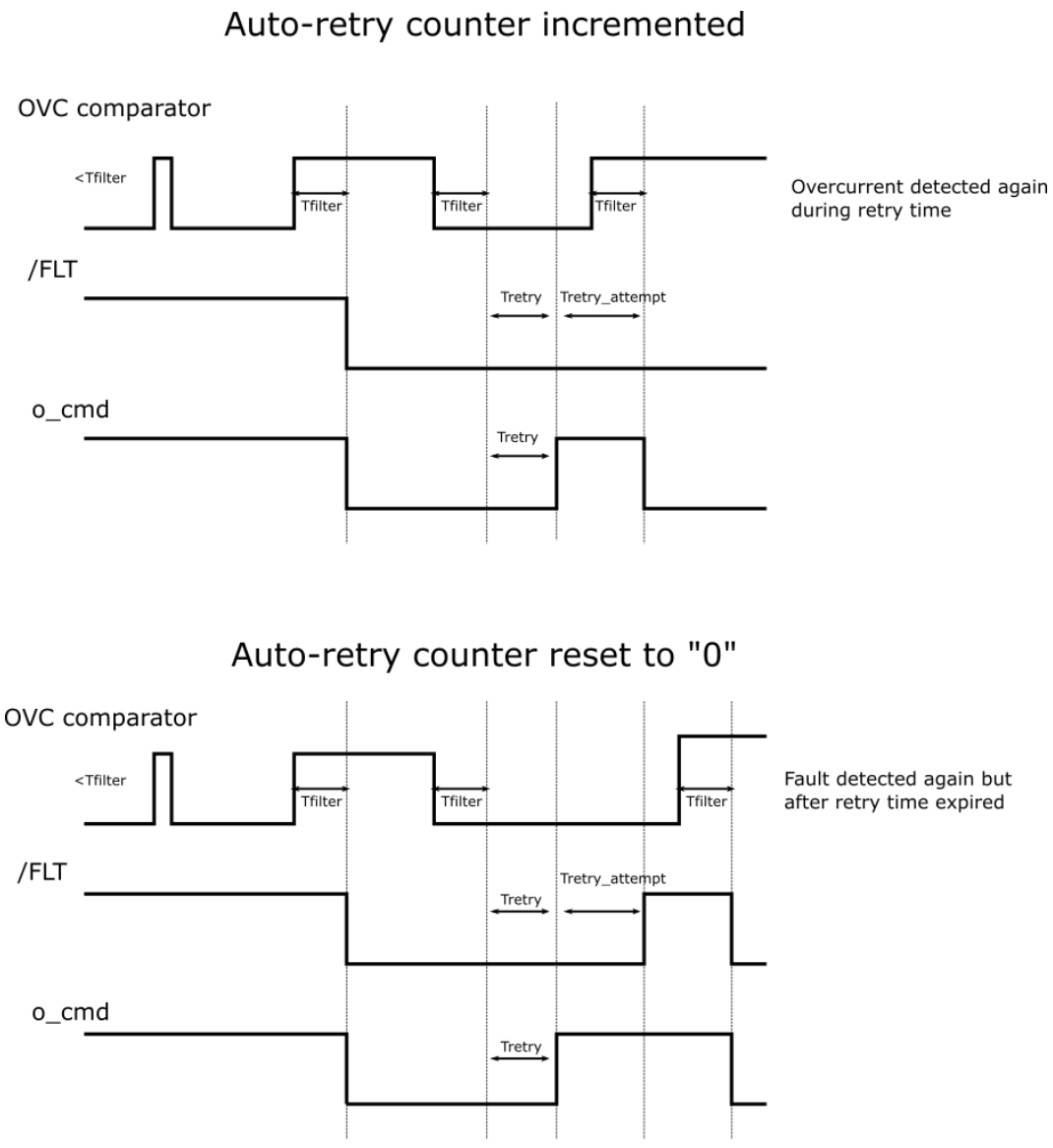


Table 19. **Auto retry parameters**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Tretry	Auto retry time after fault detection	-	105	-	130	ms
Tretry_attempt	Auto retry attempt duration	-	230	250	270	ms
Retry#	Max number of retry attempts	-	-	-	32	-

5 STAND-BY mode feature

5.1 STAND-BY behavior in detail

In the next paragraphs all device features in STAND-BY mode are presented in detail, putting in evidence the functional differences from normal operation mode, and describing the way to enter (exit) to (from) it.

5.1.1 STAND-BY mode feature description

STPM801 can enter in a hybrid configuration to reduce current consumption, disabling some diagnostics, and reducing safety and accuracy of some features. Basically, the device keeps the hotswap and oring functionality, with ideal diode regulation provided with a lower accuracy, and without fast pullup feature. Current consumption values in standby are shown in Table 20.

In standby mode all diagnostics are disabled, to save current consumption, except CP_UV and OVC feature, that are kept ON avoiding damage of external MOSFETs. OVC keeps the HV comparator with half threshold in typical condition, and STG comparator switches off hotswap and Oring, with a specified filter time (see Figure 12).

The device always starts in normal mode after it powers up; the standby condition can be reached by applying a dedicated pattern on STBY_IN pin. Once in standby mode, the IC can be brought back in normal mode by a rising pulse of STBY_IN lasting 1 ms at least. Device status either.

Normal or stand-by is echoed on the pin STBY_ECHO.

Standby mode access is denied when the device is in fault condition.

DIS pin is ignored in stand-by. Vice versa, if DIS pin is High during normal state, the stand-by pattern is ignored. If DIS pin is High in stand-by, the device can return to normal state, and, after the filter time of DIS pin expired, the drivers are turned off.

VB operative range in stand-by is between 4.5 V and 28 V: operation outside this specific range can lead to degraded performances; the IC integrity is by the way granted up to the specified AMR.

Table 20. Supply current in standby mode

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
ION_STAND-BY	Supply current in standby mode	VB = 14 V, device enable VOUT = VSENSE = VSOURCE, HGATE ON, DGATE regulation	5	-	9	mA

5.1.2 Oring driver in STAND-BY

The pre-driver for oring MOSFET is an ideal diode regulator. VDS detection is not present in standby mode. Neither the fast turn on comparator nor the related fast pull-up are present in standby mode. The other parameters related to oring driver have no change in standby mode.

5.1.3 Hot swap driver in STAND-BY

The pre-driver for hot swap MOSFET, in standby mode, has the same pull-up current (during turn-on) and pull-down current (at the switch off), as in normal mode. VDS diagnostics are disabled in stand-by. The other parameters are aligned with the specification in normal state, with the only exception reported in Table 21. Since the charge pump regulation, in standby mode, is lower, the minimum VGS guaranteed for the hot swap is also lower.

Table 21. Hot swap driver in standby

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
$\Delta V_{HG1\_12V\_STAND-BY}$	HGATE gate Drive_STAND-BY, (VHGATE - VSOURCE)	Drive voltage at VB = 14 V, CP = VB + 15, VB + 9	8	-	11	V

5.1.4 Diagnostic in STAND-BY

STG detection is also present in standby mode, with a different filter time. When a short is detected, the FLT pin is asserted low and the MOSFET driving signal HGATE/DGATE are turned off.

OVC diagnostic is also present in standby mode, but only HV comparators work and without retry function. When OVC is detected the FLT pin is asserted low and the MOSFET driving signals HGATE/DGATE are turned off.

OVC and STG diagnostics work in OR condition, as shown in Figure 12.

Figure 12. Overcurrent and short to GND during standby

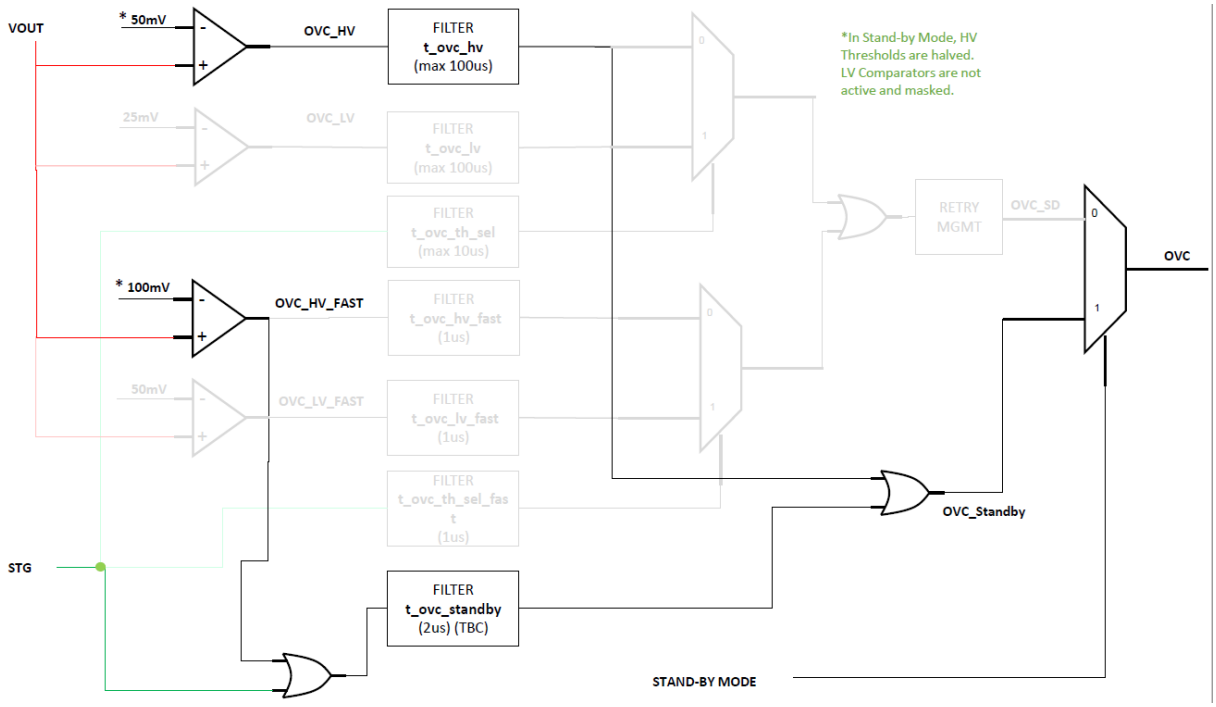


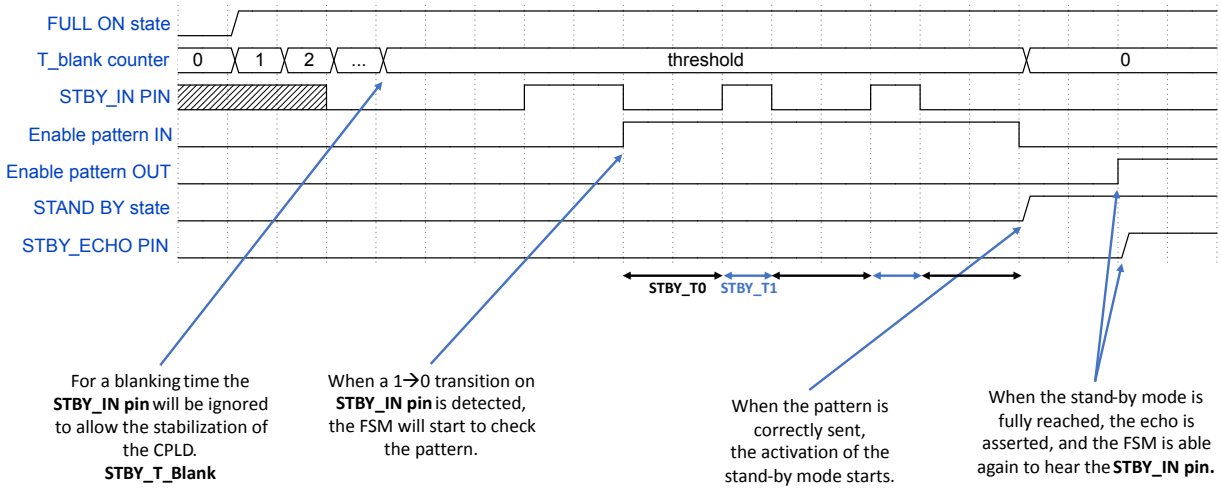
Table 22. Overcurrent and short to GND parameters in standby mode

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Note
OC_HV_th_stand-by	Overcurrent threshold (VSENSE-VOUT), VOUT > STG threshold	-	22.5	27.5	35	mV	SENSE, OUT
OC_HV_stand-by_flt	Overcurrent filter time	Guaranteed by scan	80	-	100	µs	-
OC_HV_fast_stand-by_th	Overcurrent threshold (VSENSE-VOUT), VOUT > STG threshold	-	40	50	60	mV	SENSE, OUT
OC_HV_fast_stand-by_flt	Overcurrent filter time	Guaranteed by scan and design	1	-	3	µs	-
STG_flt	Short to ground filter time	Guaranteed by scan and design	1	-	3	µs	-
CP_UV_flt	CP undervoltage filter time	Guaranteed by scan	0.9	-	1.2	ms	-

5.1.5 STAND-BY mode enter/exit

For the transition to standby mode, the generation of a specific pattern at the input of STBY_IN is required, according to the below description. T0 and T1 are related to Figure 13. The pattern is considered valid if the timing of T0 and T1 is inside the specified range. Out of range, the pattern detection is not guaranteed.

Figure 13. Standby pattern mechanism



After standby mode transition, the STBY_IN pin must be kept at 0 logic level. Bringing it high longer than STBY_Exit_flt, STPM801 can come back from standby to normal mode. Behavior is reported in Figure 14.

Figure 14. Standby exit sequence

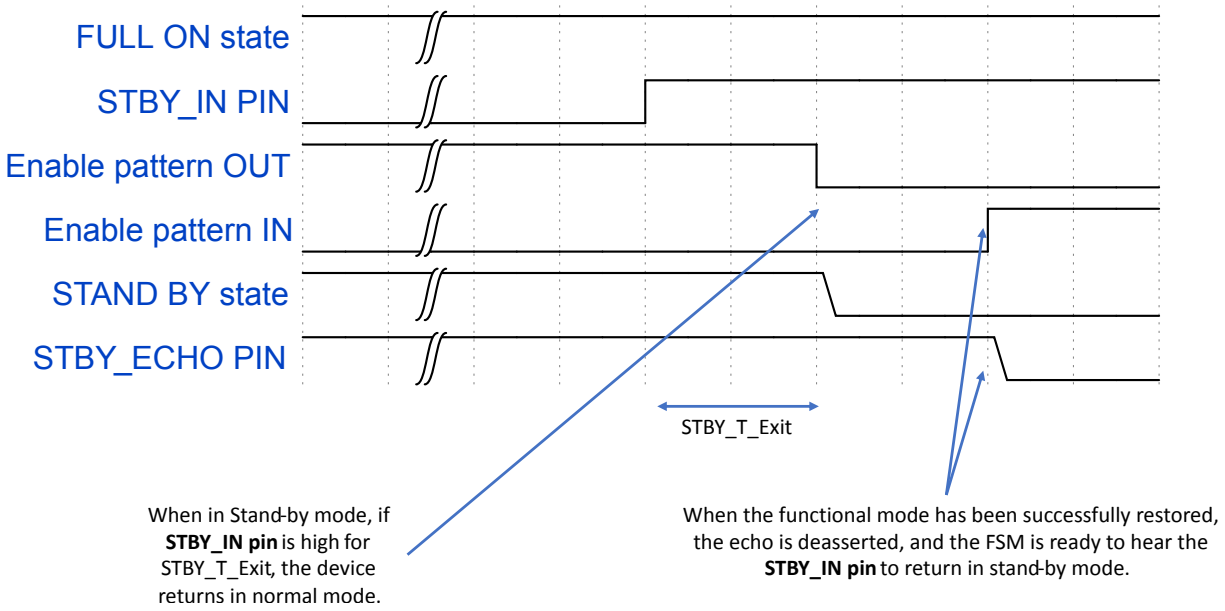


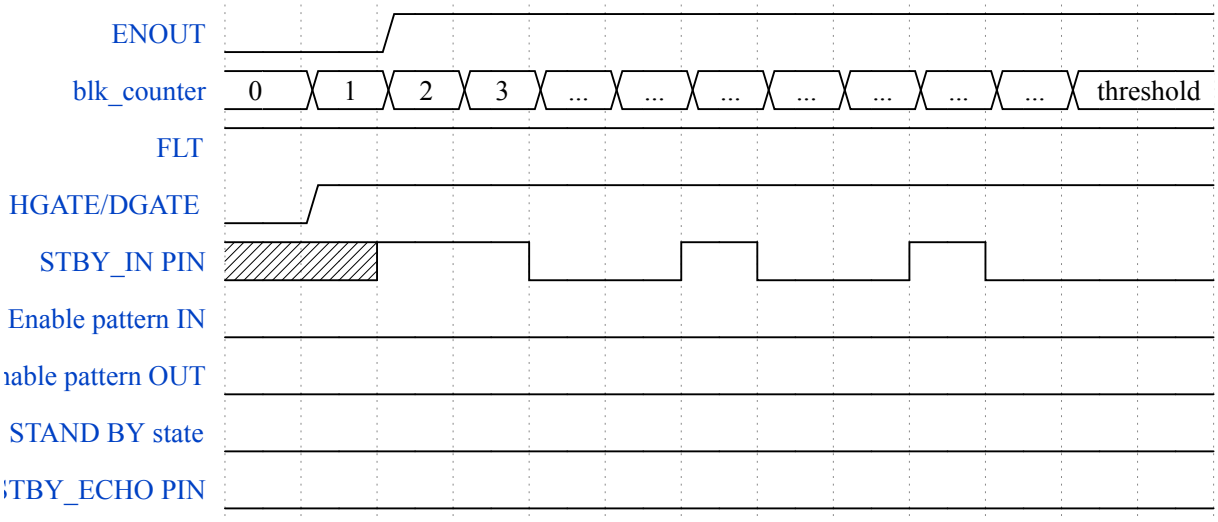
Table 23. **Standby pattern parameters**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
STAND-BY_T0min	Pattern minimum time logic level 0	Guaranteed by scan	160	-	-	µs
STAND-BY_T0max	Pattern maximum time logic level 0	Guaranteed by scan	-	-	240	µs
STAND-BY_T1min	Pattern minimum time logic level 1	Guaranteed by scan	80	-		µs
STAND-BY_T1max	Pattern maximum time logic level 1	Guaranteed by scan	-	-	120	µs
STAND-BY_T_Blank	Blanking time from Power up to consider the standby pattern	Guaranteed by scan	140	-	160	ms
STAND-BY_Exit_flt	Filter time on STAND-BY_IN pin to exit from standby mode	Guaranteed by scan	0.9	-	1.1	ms
STAND-BY_ECHO_LH	Time between validated stand-by_pattern_in and ECHO pin assertion	Guaranteed by scan	-	-	300	µs
STAND-BY_ECHO_HL	Time between validated stand-by_pattern_out and ECHO pin assertion	Guaranteed by scan	-	-	300	µs
STAND-BY_PIN _in_hl_th	High input voltage range	-	2	-	-	V
STBY_PIN _in_ll_th	Low input voltage range	-	-	-	0.8	V
STAND-BY_PIN _in_pu	Internal pull up current	Pin = 0 V	20	40	60	µA
STAND-BY_ECHO_LOW	Stand-By ECHO LOW Level	PullUP current 1 mA, used as OpenDrain	-	-	0.4	V
STAND-BY_ECHO_HIGH	Stand-By ECHO push pull signal HIGH	PullDOWN current 100 µA	2	-	-	V

5.1.6 STAND-BY exception

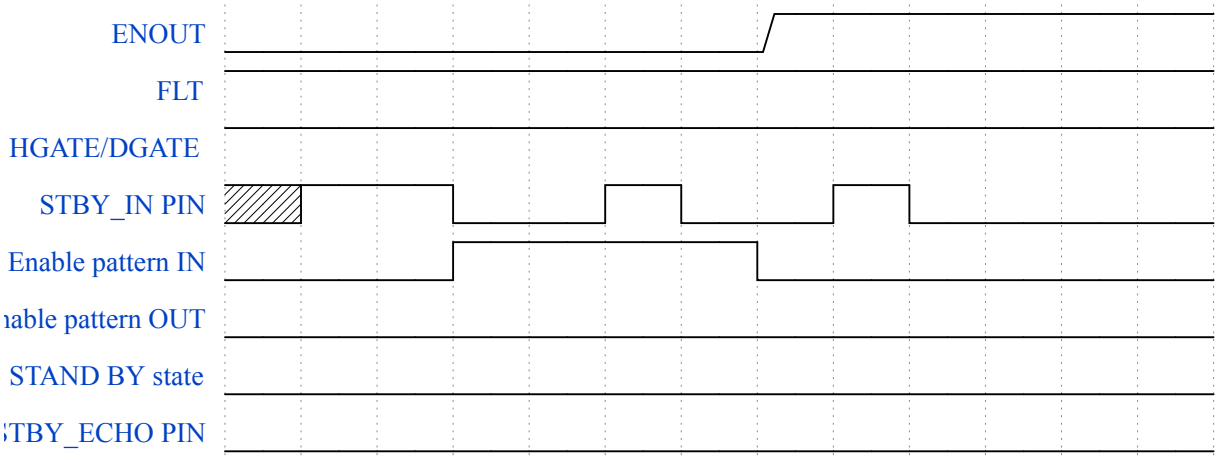
STPM801 can reject the standby enter request by pattern, according to the below pictures.

Figure 15. **Standby pattern during blanking time**



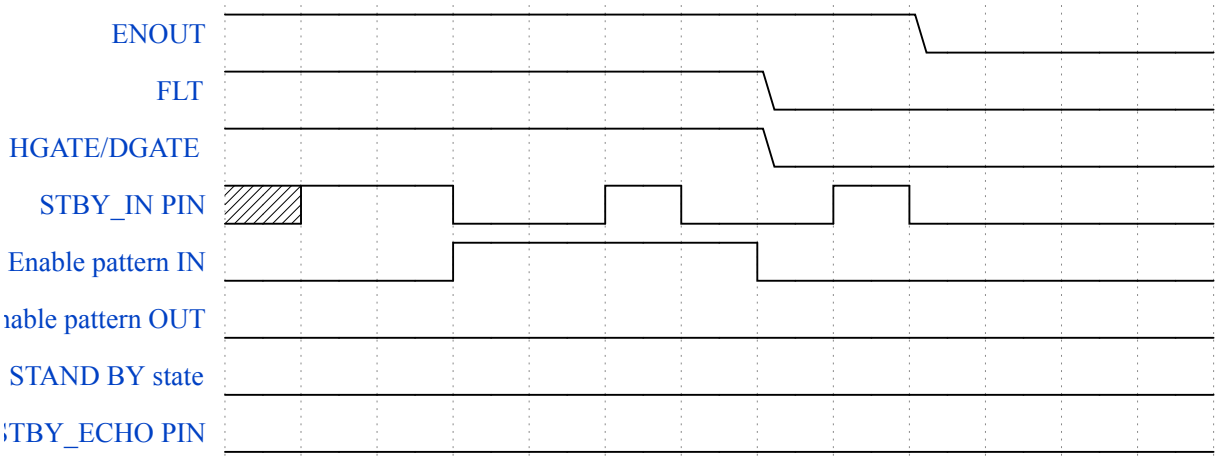
Note: If standby pattern is received before blanking time expiration it will be ignored.

Figure 16. **Standby pattern during ENOUT low state**



Note: If standby pattern is received before ENOUT high logic level assertion it will be ignored.

Figure 17. **Standby pattern during FLT assertion**



Note: If standby pattern is received during a FLT assertion it will be ignored.

6 Application and implementation

6.1 Applications information

In the Figure 18 the typical application schematic is shown. In the Table 24 the reference bill of material (BOM) is listed.

In the application note you can find a more detailed description about the choice criteria for external components and the application setup.

Figure 18. Typical application schematic

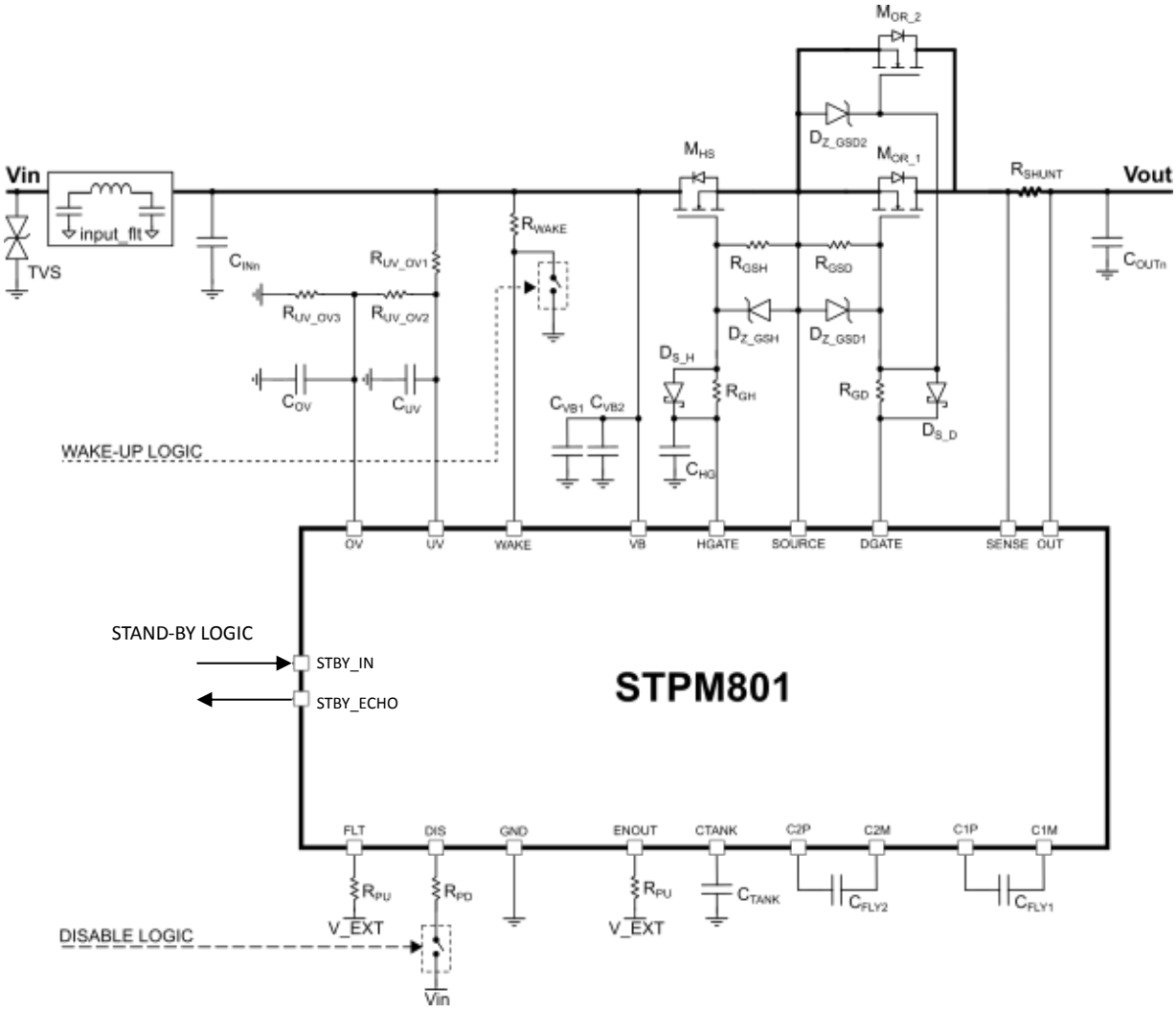


Table 24. Reference BOM

Name	Min	Typ	Max	Unit	Quantity	Minimum requirement	Note
C_{IN1}	-	10	-	nF	4	Ceramic, 20%, 100 V	-
C_{IN2}	-	4.7	-	µF	4	Ceramic, 10%, 100 V	-
C_{HG}	-	10	-	nF	1	Ceramic, 10%, 100 V	-
C_{OV}	-	1	-	nF	1	Ceramic, 10%, 50 V	To be placed close to OV pin
C_{UV}	-	1	-	nF	1	Ceramic, 10%, 50 V	To be placed close to UV pin
C_{FLYn}	-	100	-	nF	2	Ceramic, 10%, 25 V	n = 1, 2
C_{TANK}	-	220	-	nF	1	Ceramic, 10%, 50 V	-
C_{VB1}	-	4.7	-	µF	1	Ceramic, 10%, 50 V	To be placed close to VB pin
C_{VB2}	-	0.1	-	µF	1	Ceramic, 10%, 50 V	To be placed close to VB pin
C_{OUT1}	-	270	-	µF	4	Ceramic, 20%, 100 V	-
C_{OUT2}	-	4.7	-	µF	2	Ceramic, 10%, 100 V	-
C_{OUT3}	-	100	-	nF	2	Ceramic, 20%, 100 V	-
D_{Z_GSH} D_{Z_GSDn}	-	-	-	-	3	MM5Z12VT1G	n = 1, 2 12 V clamp
D_{S_H} D_{S_D}	-	-	-	-	2	SD0805S020S1R0	-
M_{HS}	-	-	-	-	1	STH315N10F7-6	100 V breakdown
M_{OR_n}	-	-	-	-	2	BUK9Y6R0-60E, 115	n = 1, 2 60 V breakdown
R_{SHUNT}	-	1	-	mΩ	1	0.1%, 2 W	-
R_{GSH}	-	1	-	MΩ	1	0.1%, 0.1 W	-
R_{GSD}	-	510	-	kΩ	1	1%, 0.1 W	-
R_{UV_OV1}	-	205	-	kΩ	1	1%, 0.1 W	For 12 V system
R_{UV_OV2}	-	56.2	-	kΩ	1	1%, 0.1 W	
R_{UV_OV3}	-	10	-	kΩ	1	1%, 0.1 W	
R_{UV_OV1}	-	392	-	kΩ	1	1%, 0.1 W	For 24 V system
R_{UV_OV2}	-	47	-	kΩ	1	1%, 0.1 W	
R_{UV_OV3}	-	10	-	kΩ	1	1%, 0.1 W	
R_{WAKE}	-	1	-	kΩ	1	1%, 0.1 W	-
R_{GH} R_{GD}	-	10	-	W	2	1%, 0.1 W	-
R_{PU}	-	4.7	-	kΩ	2	1%, 0.1 W	-
TVS	-	-	-	-	1	SM30T39CAY	For 12 V system
TVS	-	-	-	-	1	SM30T39CAY	For 24 V system
input_fit	-	-	-	-	-	-	Input LC filter (according to customer's needs)

6.1.1 MOSFET reference information

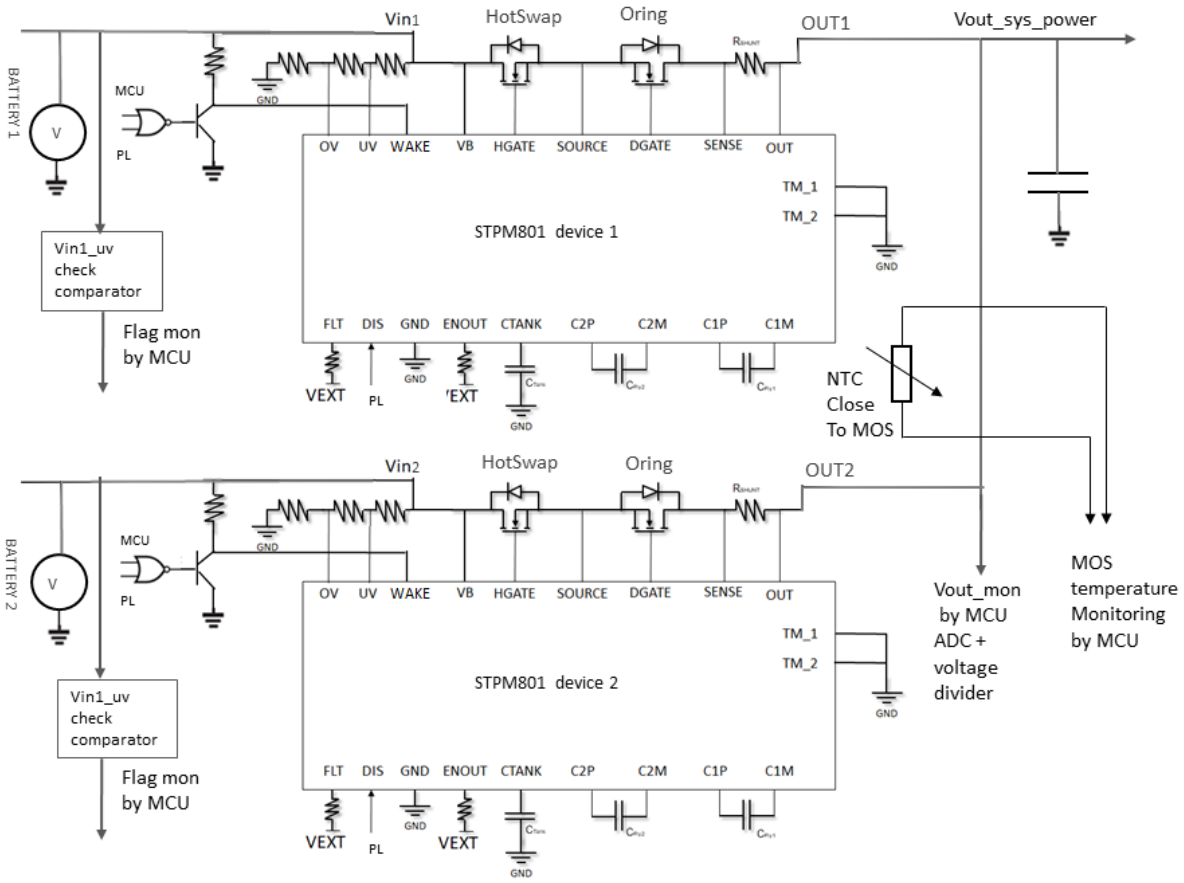
The external MOSFET realizing the hot swap and oring functions, must be properly chosen considering the application requirements, in terms of current and voltages, and all the STPM801 parameters related to HGATE and DGATE driving.

On the product application note more details about the choice of external FETs are described.

6.1.2 Dual line application scenario

Device can also be used in double line application, as shown in the Figure 19.

Figure 19. Double line application



The two-lines scheme is useful when a second battery supply line is recommended as auxiliary line in case the main battery is not available anymore (under voltage condition or any other malfunction).

In this way the voltage on the output line is the OR of the supply voltages of the two single lines. The higher voltage supply is transferred to the output line; on the other line a reverse condition is detected by STPM801, oring MOSFET is switched OFF, avoiding current back feeding from OUT to VB.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 VFQFN (5x5x0.9, 32+4L) package information

Figure 20. VFQFN (5x5x0.9, 32+4L) package outline

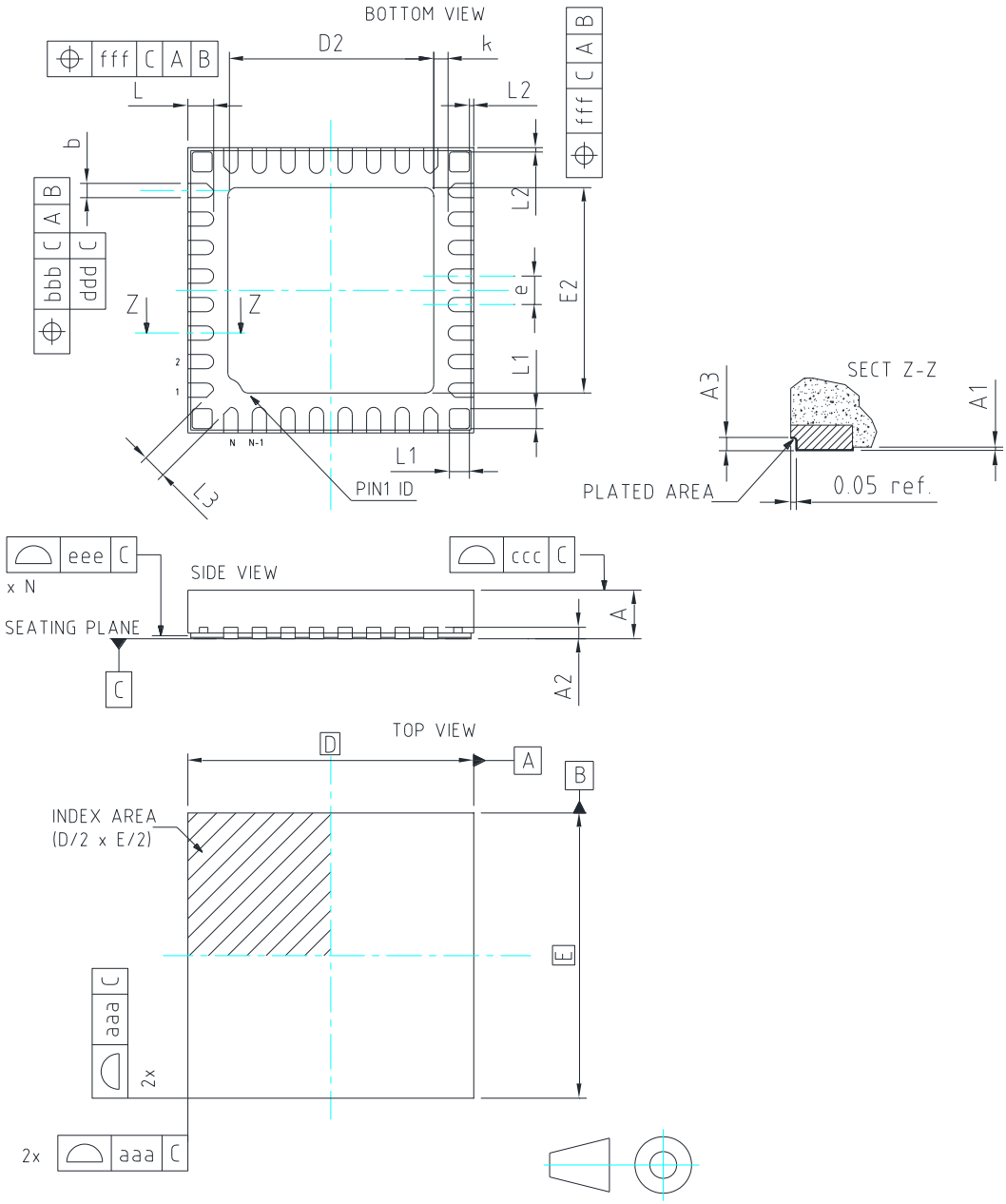


Table 25. VFQFN (5x5x0.9, 32+4L) package mechanical data

Symbol	Dimension in mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2		0.2 REF	
A3	0.10	-	-
b	0.20	0.25	0.30
D	-	5.00	-
e	-	0.5	-
E	-	5.00	-
L	0.35	0.45	0.55
L1	-	0.35	-
L2	-	0.075	-
L3	-	0.42	-
k	0.20	-	-
N		32+4	
Tolerance of form and position			
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	
Expose PAD variation			
D2	3.55	3.60	3.65
E2	3.55	3.60	3.65

Note: 4L additive corner pins are electrically floating but it is recommended to solder them towards GND in order to guarantee the mechanical integrity of the package.

Revision history

Table 26. **Document revision history**

Date	Version	Changes
23-May-2022	1	Initial release.
28-Nov-2022	2	Updated: • Section Features; • Section 5.1.1 STAND-BY mode feature description; • Table 3. Relative absolute maximum ratings; • Table 8. Power supply parameters; • Table 16. Oring pre-driver parameters; • Table 21. Hot swap driver in standby; • Table 23. Standby pattern parameters. Minor text changes in: • Section Description; • Section 4.1.1 VB power supply; • Section 4.1.10 DISABLE; • Section 4.2.1 Fault table; • Table 4. Maximum operating voltage; • Table 11. Over current and short to GND parameters. Removed watermark "Restricted".

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