ESD Protection Diode

Ultra−Low Capacitance Micro−Packaged Diodes for ESD Protection

ESD7410

The ESD7410 is designed to protect voltage sensitive components that require ultra−low capacitance from ESD and transient voltage events. It has industry leading capacitance linearity over voltage making it ideal for RF applications. This capacitance linearity combined with the extremely small package and low insertion loss makes this part well suited for use in antenna line applications for wireless handsets and terminals.

Features

- Ultra−Low Capacitance: < 1.0 pF Max
  - Industry Leading Capacitance Linearity Over Voltage
- Insertion Loss: 0.1 dB at 1 GHz; 0.3 dB at 3 GHz
- Low Leakage: < 1 μA
- IEC61000−4−2 (ESD): Level 4 ±30 kV Contact
- ISO 10605 (ESD) 330 pF/2 kΩ ±30 kV Contact
- SZESD7410MXWT5G − Wettable Flank Package for optimal Automated Optical Inspection (AOI)
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- RF Signal ESD Protection
- Active Antenna ESD Protection
- Near Field Communications

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

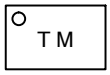
Rating	Symbol	Value	Unit
IEC 61000−4−2 Contact (Note 1) IEC 61000−4−2 Air ISO 10605 Contact (330 pF / 330 Ω) ISO 10605 Contact (330 pF / 2 kΩ) ISO 10605 Contact (150 pF / 2 kΩ)	ESD	±30 ±30 ±30 ±30 ±30	kV kV kV kV kV
Total Power Dissipation (Note 2) @ T_A = 25°C Thermal Resistance, Junction−to−Ambient	P_D $R_{\theta JA}$	300 400	mW °C/W
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Second Duration)	T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Non−repetitive current pulse at T_A = 25°C, per IEC61000−4−2 waveform.
2. Mounted with recommended minimum pad size, DC board FR−4

MARKING DIAGRAM

X2DFN2
CASE 714AB



T = Specific Device Code
M = Date Code

X2DFNW2
CASE 711BG

D = Specific Device Code
M = Date Code

ORDERING INFORMATION

Device	Package	Shipping†
ESD7410N2T5G	X2DFN2 (Pb−Free)	8000 / Tape & Reel
SZESD7410N2T5G	X2DFN2 (Pb−Free)	8000 / Tape & Reel
ESD7410MXWT5G	X2DFNW2 (Pb−Free)	8000 / Tape & Reel
SZESD7410MXWT5G	X2DFNW2 (Pb−Free)	8000 / Tape & Reel

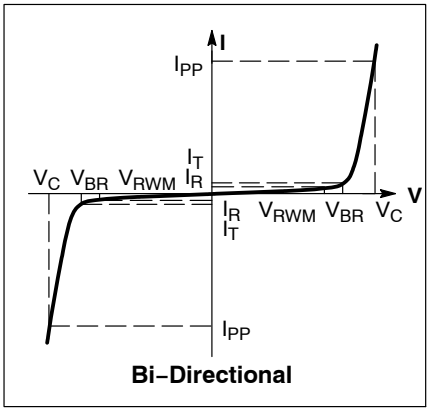
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



Bi−Directional

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}				9.5	V
Breakdown Voltage	V_{BR}	I_T = 1 mA (Note 3)	10			V
Reverse Leakage Current	I_R	V_{RWM} = 9.5 V			1.0	μA
Clamping Voltage	V_C	IEC 61000−4−2, ±8 kV Contact	See Figures 1 and 2			V
Clamping Voltage, TLP (Note 4)	V_C	I_{PP} = 8 A I_{PP} = 16 A I_{PP} = −8 A I_{PP} = −16 A		18 20 −18 −20		V
Reverse Peak Pulse Current	I_{PP}	IEC 61000−4−2 (8/20 μs)	5.0			A
Clamping Voltage (8/20 μs)	V_C	I_{PP} = 5.0 A		18.4	19.4	V
Dynamic Resistance	R_{DYN}	TLP Pulse		1.0		Ω
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz V_R = 0 V, f = 1 GHz		0.40 0.35	1.0 0.7	pF
Insertion Loss		f = 1 GHz f = 3 GHz		0.1 0.3		dB

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Breakdown voltage is tested from pin 1 to 2 and pin 2 to 1.
4. ANSI/ESD STM5.5.1 − Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.
   TLP conditions: Z_0 = 50 Ω, t_p = 100 ns, t_r = 4 ns, averaging window; t_1 = 30 ns to t_2 = 60 ns.

TYPICAL CHARACTERISTICS

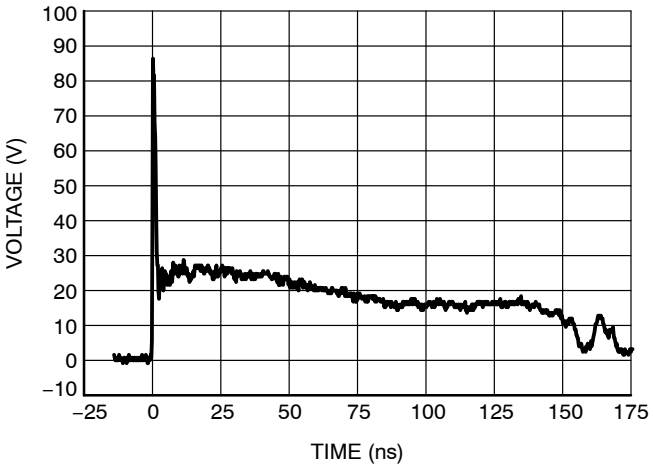


Figure 1. Typical IEC61000−4−2 +8 kV Contact ESD Clamping Voltage

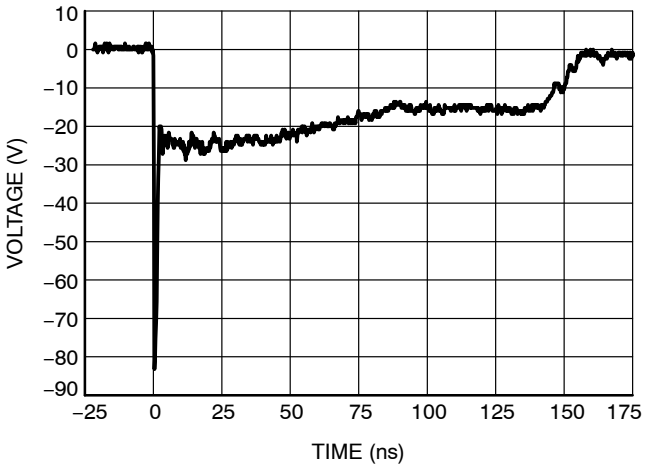


Figure 2. Typical IEC61000−4−2 −8 kV Contact ESD Clamping Voltage

TYPICAL CHARACTERISTICS

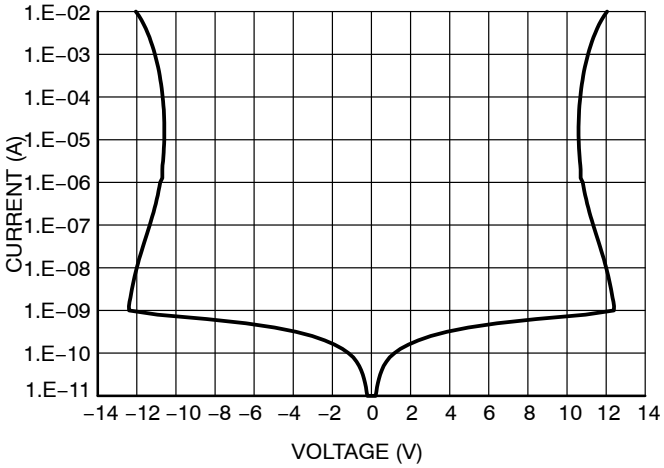


Figure 3. Typical IV Characteristics

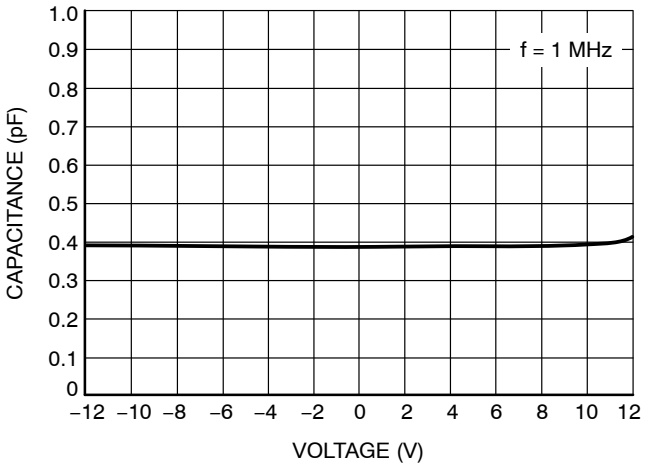


Figure 4. Typical CV Characteristics

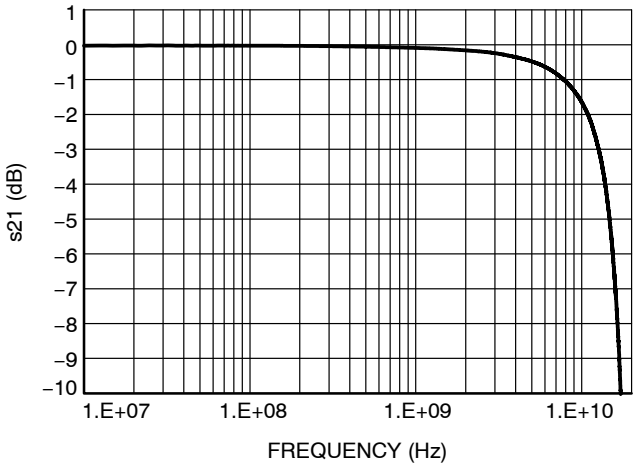


Figure 5. Typical Insertion Loss
ESD7410N2T5G

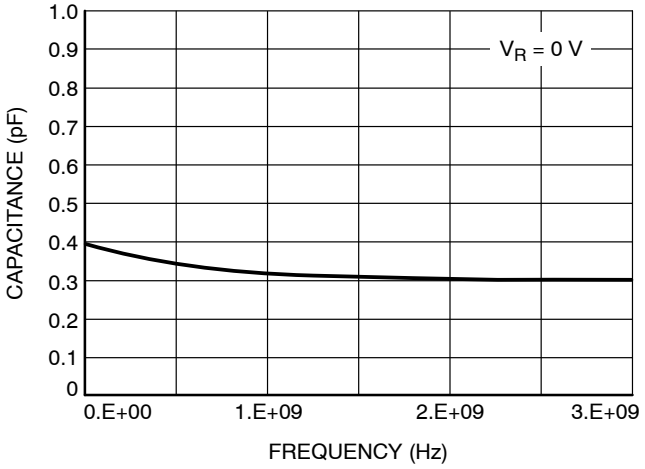


Figure 6. Typical Capacitance over Frequency
ESD7410N2T5G

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

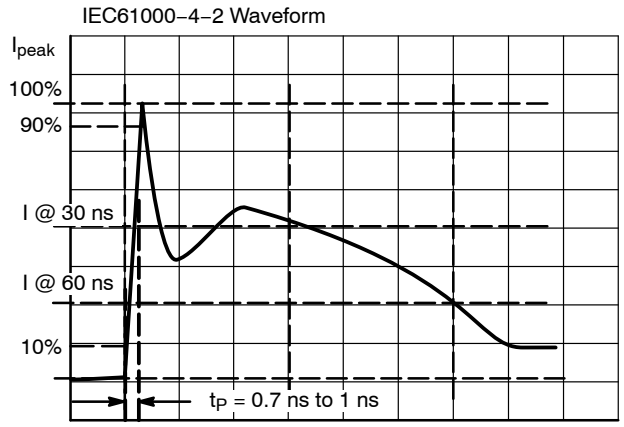


Figure 7. IEC61000−4−2 Spec

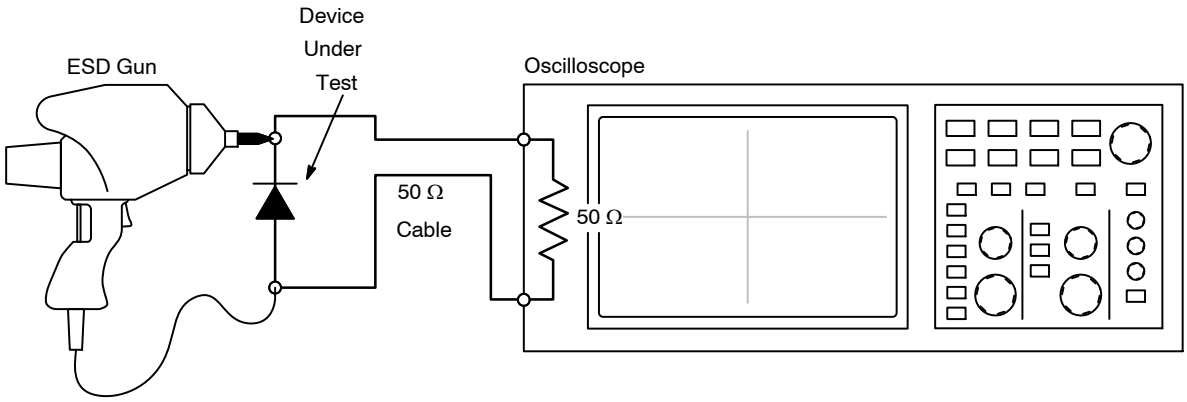


Figure 8. Diagram of ESD Clamping Voltage Test Setup

The following is taken from Application Note AND8308/D − Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

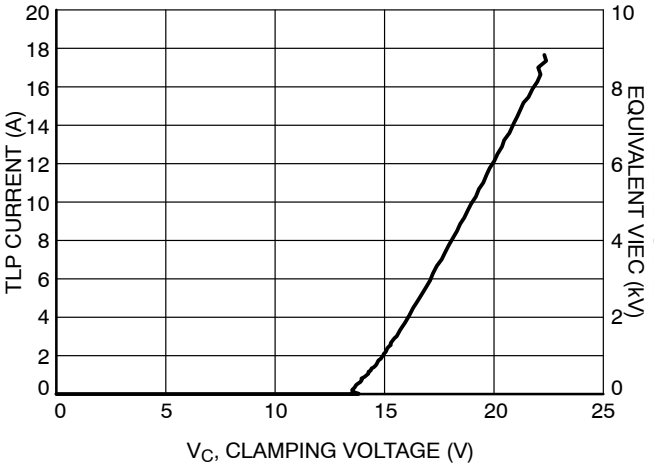


Figure 9. Positive TLP I−V Curve

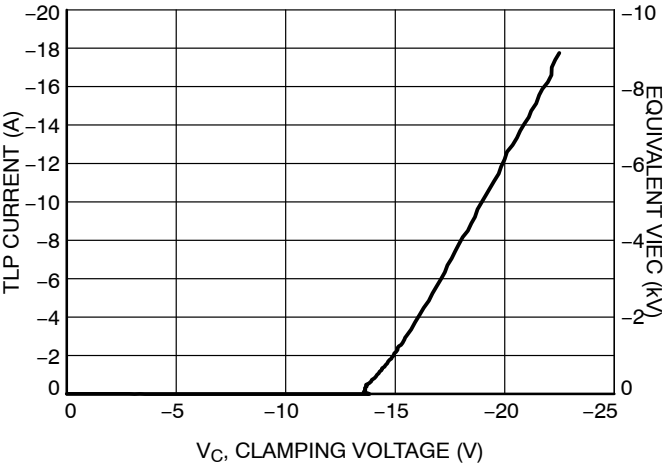


Figure 10. Negative TLP I−V Curve

NOTE: TLP parameter: Z_0 = 50 Ω, t_p = 100 ns, t_r = 300 ps, averaging window: t_1 = 30 ns to t_2 = 60 ns. V_{IEC} is the equivalent voltage stress level calculated at the secondary peak of the IEC 61000−4−2 waveform at t = 30 ns with 2 A/kV. See TLP description below for more information.

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I−V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 11. TLP I−V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 12 where an 8 kV IEC 61000−4−2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I−V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

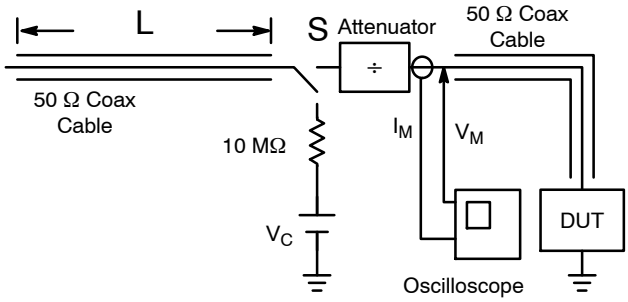


Figure 11. Simplified Schematic of a Typical TLP System

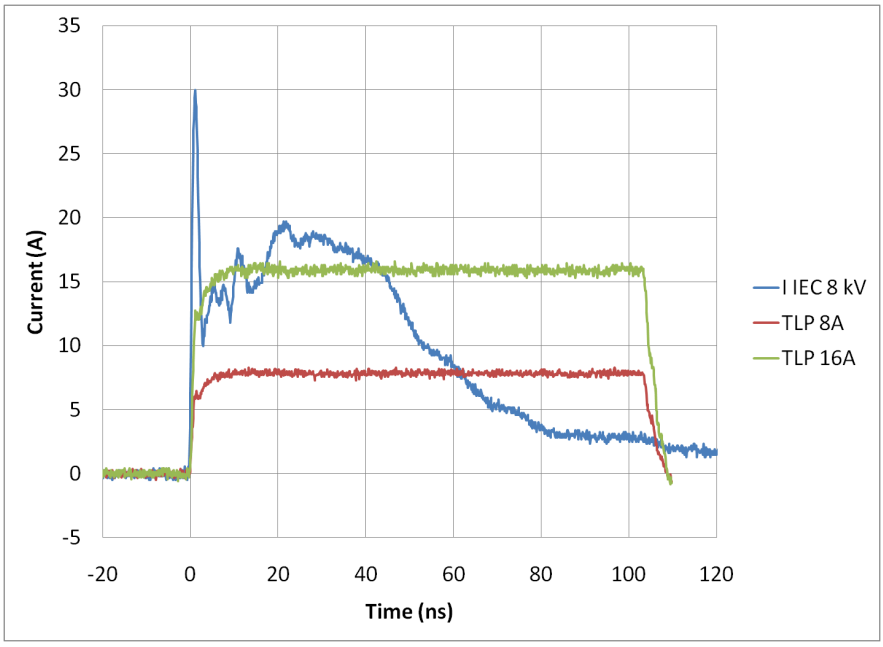


Figure 12. Comparison Between 8 kV IEC 61000−4−2 and 8 A and 16 A TLP Waveforms

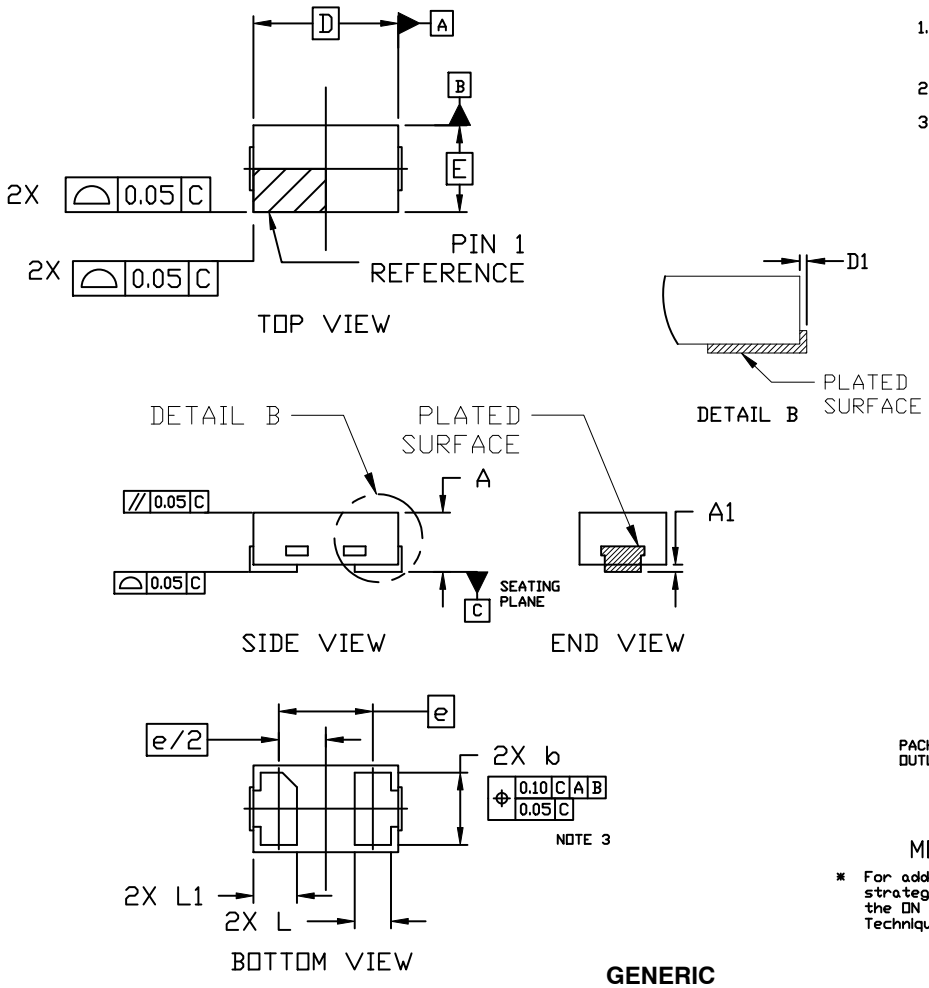
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

X2DFNW2 1.0x0.6, 0.65P
CASE 711BG
ISSUE C

SCALE 8:1

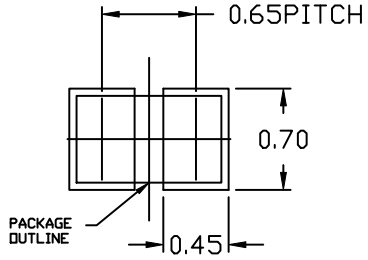
DATE 13 SEP 2019



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO THE PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 FROM THE TERMINAL TIP.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.34	0.37	0.40
A1	---	---	0.05
b	0.45	0.50	0.55
D	0.90	1.00	1.10
D1	---	---	0.05
E	0.50	0.60	0.70
e	0.65 BSC		
L	0.22 REF		
L1	0.24	0.285	0.34



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON15241G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**X2DFNW2 1.0X0.6, 0.65P**	**PAGE 1 OF 1**

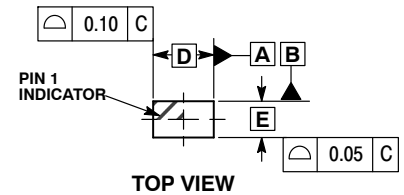
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

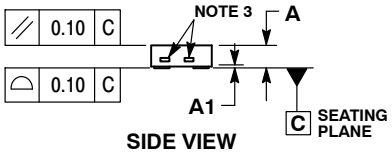
X2DFN2 1.0x0.6, 0.65P
CASE 714AB
ISSUE B

DATE 21 NOV 2017

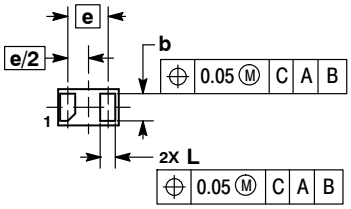
SCALE 8:1



TOP VIEW



SIDE VIEW

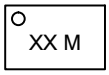


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. EXPOSED COPPER ALLOWED AS SHOWN.

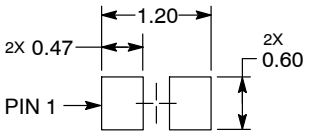
	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.34	0.37	0.40
A1	---	0.03	0.05
b	0.45	0.50	0.55
D	0.95	1.00	1.05
E	0.55	0.60	0.65
e	0.65 BSC		
L	0.20	0.25	0.30

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code

RECOMMENDED SOLDER FOOTPRINT*



DIMENSIONS: MILLIMETERS

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON98172F**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**X2DFN2 1.0X0.6, 0.65P**	**PAGE 1 OF 1**