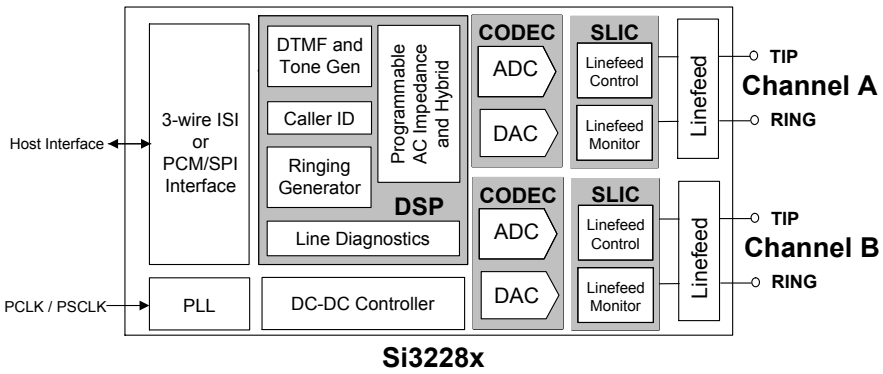
Si3228x: ProSLIC® Single-Chip Dual FXS Solution

The Si3228x Dual ProSLIC® devices, in a single package, implement two complete foreign exchange station (FXS) telephony interfaces. The Si3228x devices operate from a 3.3 V supply and have standard PCM/SPI or 3-wire ISI digital interfaces. A pair of built-in dc-dc converter controllers can be used to automatically generate the optimal battery voltage required for each line-state, optimizing efficiency and minimizing heat generation. The Si3228x devices are designed to operate with capacitive boost tracking battery supply for lower power, cost, and footprint vs. other tracking or shared battery supplies in the industry. Self-testing and metallic loop testing (MLT) is facilitated by the built-in DSP, monitor ADC, and test load. The devices are available with wideband audio for better than PSTN voice quality, DTMF detection, and Smart Ringing. Smart Ringing reduces the peak current with 2-channel ringing for lower-cost ac-dc adapters. The Si3228x devices are available in a 7 x 7 mm 48-pin QFN or 8 x 8 mm 56-pin QFN package.

Applications:

- VoIP gateways and routers
- xDSL IADs
- Optical Network Terminals/Units (ONT/U)
- Analog Terminal Adapters (ATA)
- Cable eMTA
- Wireless Fixed Terminals (WFT)
- Wireless Local Loop (WLL)
- WiMAX CPE
- Private Branch Exchange (PBX)
- VoIP MDU gateways



Functional Block Diagram

KEY FEATURES

- Two complete FXS channels in a single 7x7 or 8x8 mm package
- Performs all BORSCHT functions
- Ideal for short- or medium-loop applications
- Ultra-low power consumption
- Patented low-power ringing
- Patent-pending Smart Ringing
  - Reduces peak current with 2-channel ringing
- Adaptive ringing
- Simplified configuration and diagnostics
  - Supported by ProSLIC API
  - Audio diagnostics with loopback
  - Integrated test load
- Wideband voice support
- On-hook transmission
- Loop or ground start operation
- Smooth polarity reversal
- Programmable interrupts
- Software-programmable parameters:
  - Ringing frequency, amplitude, cadence, and waveshape
  - Two-wire ac impedance
  - Transhybrid balance
  - DC current loop feed (10–45 mA)
  - Loop closure and ring trip thresholds
  - Ground key detect threshold
- Flexible integrated tracking DC-DC controller supporting patent-pending low-cost capacitive boost configuration
- DTMF Generation
- DTMF Detection (Si32281/3/5/7)
- 3-wire Integrated Serial Interface (ISI) or PCM interface
- A-Law/μ-Law companding, linear PCM
- Pulse metering
- 3.3 V operation
- Pb-free/RoHS-compliant packaging

1. Ordering Guide

Table 1.1. Si3228x Ordering Guide

P/N[1]	Description	Package Type	Max V_{BAT}	Temperature
Si32280-A-FM	Wideband Dual FXS, ISI interface	QFN48[2]	–106 V	0 to 70 °C
Si32280-A-GM	Wideband Dual FXS, ISI interface	QFN48[2]	–106 V	–40 to 85 °C
Si32281-A-FM	Wideband Dual FXS, ISI interface, DTMF detection	QFN48[2]	–106 V	0 to 70 °C
Si32281-A-GM	Wideband Dual FXS, ISI interface, DTMF detection	QFN48[2]	–106 V	–40 to 85 °C
Si32282-A-FM	Wideband Dual FXS, PCM interface, daisy-chain mode	QFN56[2]	–106 V	0 to 70 °C
Si32282-A-GM	Wideband Dual FXS, PCM interface, daisy-chain mode	QFN56[2]	–106 V	–40 to 85 °C
Si32283-A-FM	Wideband Dual FXS, PCM interface, DTMF detection, daisy-chain mode	QFN56[2]	–106 V	0 to 70 °C
Si32283-A-GM	Wideband Dual FXS, PCM interface, DTMF detection, daisy-chain mode	QFN56[2]	–106 V	–40 to 85 °C
Si32284-A-FM	Wideband Dual FXS, ISI interface, Smart Ringing	QFN48[2]	–106 V	0 to 70 °C
Si32284-A-GM	Wideband Dual FXS, ISI interface, Smart Ringing	QFN48[2]	–106 V	–40 to 85 °C
Si32285-A-FM	Wideband Dual FXS, ISI interface, DTMF detection, Smart Ringing	QFN48[2]	–106 V	0 to 70 °C
Si32285-A-GM	Wideband Dual FXS, ISI interface, DTMF detection, Smart Ringing	QFN48[2]	–106 V	–40 to 85 °C
Si32286-A-FM	Wideband Dual FXS, PCM interface, daisy-chain mode, Smart Ringing	QFN56[2]	–106 V	0 to 70 °C
Si32286-A-GM	Wideband Dual FXS, PCM interface, daisy-chain mode, Smart Ringing	QFN56[2]	–106 V	–40 to 85 °C
Si32287-A-FM	Wideband Dual FXS, PCM interface, DTMF detection, daisy-chain mode, Smart Ringing	QFN56[2]	–106 V	0 to 70 °C

P/N[1]	Description	Package Type	Max V_{BAT}	Temperature
Si32287-A-GM	Wideband Dual FXS, PCM interface, DTMF detection, daisy-chain mode, Smart Ringing	QFN56[2]	–106 V	–40 to 85 °C
Si32280-A-ZM1	Wideband Dual FXS, ISI interface, customer-specific	QFN48[2]	–106 V	0 to 70 °C
Si32281-A-ZM1	Wideband Dual FXS, ISI interface, DTMF detection, customer-specific	QFN48[2]	–106 V	0 to 70 °C
Si32282-A-ZM1	Wideband Dual FXS, PCM interface, daisy-chain mode, customer-specific	QFN56[2]	–106 V	0 to 70 °C
Si32283-A-ZM1	Wideband Dual FXS, PCM interface, DTMF detection, daisy-chain mode, customer-specific	QFN56[2]	–106 V	0 to 70 °C
Si32284-A-ZM1	Wideband Dual FXS, ISI interface, Smart Ringing, customer-specific	QFN48[2]	–106 V	0 to 70 °C
Si32285-A-ZM1	Wideband Dual FXS, ISI interface, DTMF detection, Smart Ringing, customer-specific	QFN48[2]	–106 V	0 to 70 °C
Si32286-A-ZM1	Wideband Dual FXS, PCM interface, daisy-chain mode, Smart Ringing, customer-specific	QFN56[2]	–106 V	0 to 70 °C
Si32287-A-ZM1	Wideband Dual FXS, PCM interface, DTMF detection, daisy-chain mode, Smart Ringing, customer-specific	QFN56[2]	–106 V	0 to 70 °C
Si32280-A-ZM2	Wideband Dual FXS, ISI interface, customer-specific	QFN48[2]	–106 V	0 to 70 °C
Si32281-A-ZM2	Wideband Dual FXS, ISI interface, DTMF detection, customer-specific	QFN48[2]	–106 V	0 to 70 °C
Si32282-A-ZM2	Wideband Dual FXS, PCM interface, daisy-chain mode, customer-specific	QFN56[2]	–106 V	0 to 70 °C
Si32283-A-ZM2	Wideband Dual FXS, PCM interface, DTMF detection, daisy-chain mode, customer-specific	QFN56[2]	–106 V	0 to 70 °C
Si32284-A-ZM2	Wideband Dual FXS, ISI interface, Smart Ringing, customer-specific	QFN48[2]	–106 V	0 to 70 °C

P/N[1]	Description	Package Type	Max V_{BAT}	Temperature
Si32285-A-ZM2	Wideband Dual FXS, ISI interface, DTMF detection, Smart Ringing, customer-specific	QFN48[2]	–106 V	0 to 70 °C
Si32286-A-ZM2	Wideband Dual FXS, PCM interface, daisy-chain mode, Smart Ringing, customer-specific	QFN56[2]	–106 V	0 to 70 °C
Si32287-A-ZM2	Wideband Dual FXS, PCM interface, DTMF detection, daisy-chain mode, Smart Ringing, customer-specific	QFN56[2]	–106 V	0 to 70 °C

Note:
1. Adding the suffix "R" to the part number (e.g., Si32282-C-FMR) denotes tape and reel.
2. QFN - Quad-Flat No-leads

Table 1.2. Evaluation Kit Ordering Guide

Part Number	Description	V_{BAT} Max
Si32285ACB20SL0EVB	2 FXS evb with lowest-cost capacitive boost dc-dc converter for Si32280/1/4/5	–100 V
Si32287ACB20SL0EVB	2 FXS evb with lowest-cost capacitive boost dc-dc converter for Si32282/3/6/7	–100 V

1.1 Product Identification

The product identification number is a finished goods part number or is specified by a finished goods part number, such as a special customer part number.

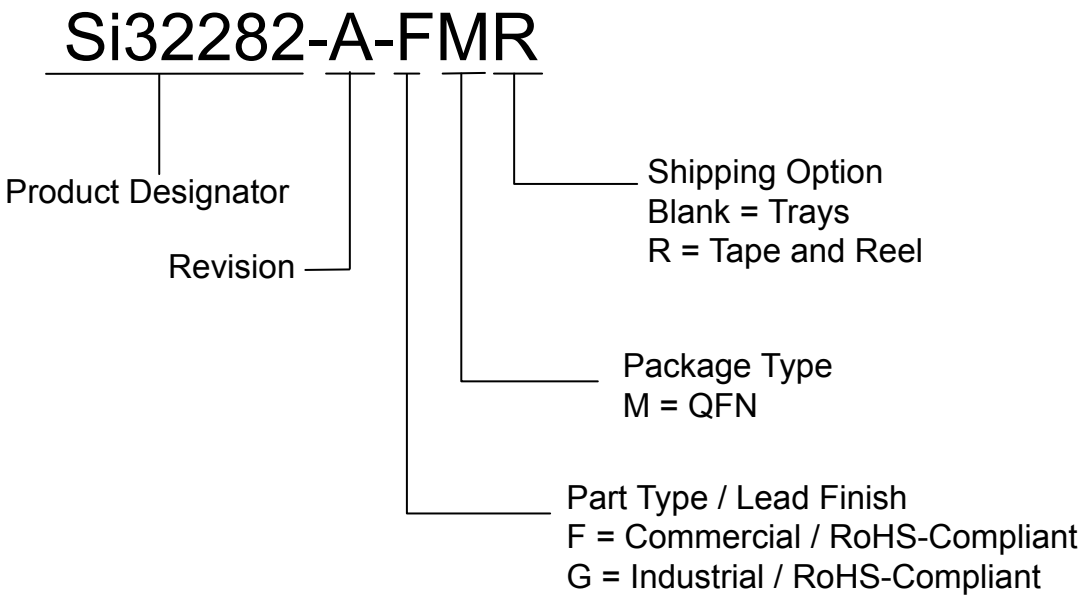


Figure 1.1. Example Product Identification Number

Table of Contents

2. Functional Description

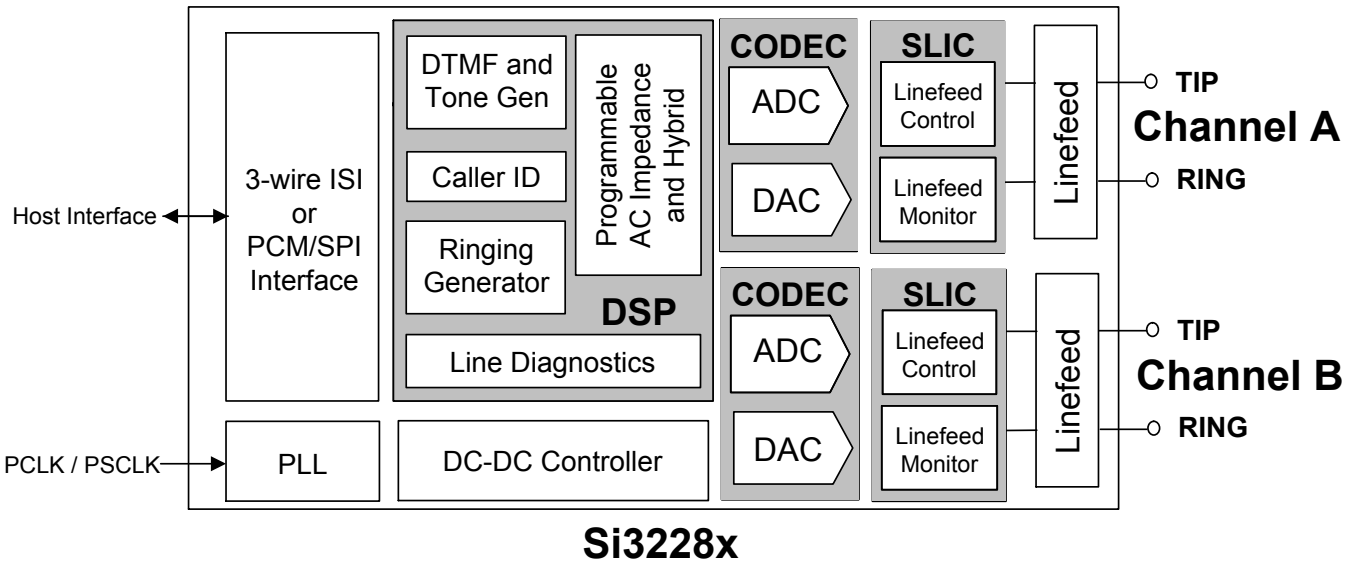


Figure 2.1. Functional Block Diagram

The Si3228x dual ProSLIC devices provide all SLIC, codec, DTMF detection, and signal generation functions needed for two complete analog telephone interfaces. They perform all battery, over-voltage, ringing, supervision, codec, hybrid, and test (BORSCHT) functions, and also support extensive metallic loop and self-test capabilities.

The Si3228x supports wideband audio (150Hz-6.8kHz) compliant with PKT-SP-HDV-104-120823, and is configurable to support the full ITU-T-G.722-201209 bandwidth (50Hz-7kHz). The wideband mode provides an expanded audio band with a 16 kHz sample rate for enhanced audio quality while the standard voice-band mode provides standard telephony audio bandwidth.

The Si3228x series supports either a standard PCM/SPI digital interface, or a 3-wire ISI digital interface.

The Si3228x devices incorporate two programmable dc-dc converter controllers that operate in battery tracking mode. The dc-dc converter controllers react to line conditions to provide the optimal battery voltage required for each line-state. Si3228x ICs support a Vbat voltage rating of –106V. The Si3228x devices are available with DTMF detection and Smart Ringing. Smart Ringing provides reduced peak current 2-channel ringing for lower-cost ac-dc adapters. See Section 1. Ordering Guide.

Programmable on-hook voltage, programmable offhook loop current, reverse polarity operation, loop or ground start operation, and on-hook transmission are supported. Loop current and voltage are continuously monitored by an integrated monitoring ADC. The Si3228x dual ProSLIC devices support ringing with or without a programmable dc offset, and can operate in low power ringing and adaptive ringing modes. The available offset, frequency, waveshape, and cadence options are designed to ring the widest variety of terminal devices and to reduce external controller requirements.

A complete audio transmit and receive path is integrated, including ac impedance and hybrid gain. These features are software-programmable, allowing a single hardware design to meet global requirements.

3. Electrical Specifications

Table 3.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min[1]	Typ	Max[1]	Unit
Ambient Temperature	T_A	F-grade	0	25	70	°C
		G-grade	–40	25	85	°C
Silicon Junction Temperature, High Voltage Die	T_{JHV}	Continuous	—	—	Internally Limited	°C
Silicon Junction Temperature, Low Voltage Die	T_{JLV}	Continuous	—	—	125	°C
Supply Voltages	V_{DDA}, V_{DDD}		3.13	3.3	3.47	V
Battery Voltage[2]	V_{BAT}		–106	—	–15	V

Note:

1. All minimum and maximum specifications apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.
2. Minimum and maximum battery voltage limits are dependent upon loop conditions and dc-dc converter configuration.

Table 3.2. Power Supply Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Currents: Reset	I_{DD}	V_T and V_R = Hi-Z , RSTB = 0	—	3.61	—	mA
	I_{VBAT}		—	0.00	—	mA
Supply Currents: High Impedance, Open	I_{DD}	V_T and V_R = Hi-Z	—	21.75	—	mA
	I_{VBAT}		—	0.6	—	mA
Supply Currents: Forward/Reverse, On-hook	I_{DD}	V_{TR} = –48 V, Automatic Power Save Mode Enabled	—	10.28	—	mA
	I_{VBAT}		—	0.4	—	mA
Supply Currents: Forward/Reverse, On-hook	I_{DD}	V_{TR} = -48 V, Automatic Power Save Mode Disabled	—	34.40	—	mA
	I_{VBAT}		—	2.2	—	mA
Supply Currents: Tip/Ring Open, On-hook	I_{DD}	V_T or V_R = –48 V	—	10.27	—	mA
	I_{VBAT}	V_R or V_T = Hi-Z, Automatic Power Save Mode Enabled	—	0.4	—	mA
Supply Currents: Tip/Ring Open, On-hook	I_{DD}	V_T or V_R = -48 V	—	33.60	—	mA
	I_{VBAT}	V_R or V_T = Hi-Z, Automatic Power Save Mode Disabled	—	1.5	—	mA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Currents: Forward/Reverse OHT, On-hook	I_{DD}	V_{TR} =48 V	—	51.22	—	mA
	I_{VBAT}		—	3	—	mA
Supply Currents: Forward/Reverse Active, Off-hook	I_{DD}	I_{LOOP} = 20 mA, R_{LOAD} = 200 Ω	—	51.71	—	mA
	I_{VBAT}		—	2.2 + I_{LOOP}	—	mA
Supply Currents: Ringing	I_{DD}	V_{TR} = 55 V_{RMS} + 0 V_{DC}, low power ringing, sinusoidal, f = 20 Hz R_{LOAD} = 5 REN = 1400 Ω	—	37.07	—	mA
	I_{VBAT}		—	33.32	—	mA

Note:
1. All specifications are for a single channel of Si3228x with a low-cost capacitive boost dc-dc converter at 25 °C. V_{DDA} = V_{DDD} = 3.3 V; V_{DC}= 12 V.
2. I_{DD} = I_{DDA} + I_{DDD}.

Table 3.3. AC Characteristics

Parameter	Test Condition	Min	Typ	Max	Unit
TX/RX Performance					
Overload Compression	2-Wire - PCM	See Figure 3.6 Overload Compression Performance on page 17.	—	—	—
Single Frequency Distortion (0 dBm0 input)	200 Hz to 3.4 kHz (u-law/A-law)	—	—	–40	dBm0
	200 Hz to 3.4 kHz (16-bit linear)	—	—	–63	dBm0
Signal-to-(Noise + Distortion) Ratio[1]	200 Hz to 3.4 kHz transmit or receive path Active off-hook, and OHT, any Z_T	See Figure 3.5 Transmit and Receive Path SNDR on page 17.	—	—	—
Audio Tone Generator Signal-to-Distortion Ratio[1]	0 dBm0, Active off-hook, and OHT, any Z_T	46	—	—	dB
Intermodulation Distortion		—	—	-41	dB
Gain Accuracy[1]	2-Wire to PCM or PCM to 2-Wire	—	—	—	—
	1014 Hz, any gain setting	—	—	—	—
		-0.2	—	0.2	dB
Attenuation Distortion vs. Freq.	0 dBm 0[5]	See Figure 3.7 Receive Path Frequency Response on page 18 and Figure 3.8 Transmit Path Frequency Response on page 18.			
Group Delay vs. Frequency		See Figure 3.9 Transmit Group Delay Distortion on page 19 and Figure 3.10 Receive Group Delay Distortion on page 19.			

Parameter	Test Condition	Min	Typ	Max	Unit
Gain Tracking[2]	1014 Hz sine wave, reference level -10 dBm Signal level:	—	—	—	—
	3 dB to –37 dB	—	—	0.25	dB
	–37 dB to -50 dB	—	—	0.5	dB
	–50 dB to -60 dB	—	—	1.0	dB
Round-Trip Group Delay	1014 Hz, Within same time-slot	—	450	500	µs
2-Wire Return Loss[3]	200 Hz to 3.4 kHz	26	30	—	dB
Transhybrid Balance[3]	300 Hz to 3.4 kHz	26	30	—	dB
Noise Performance					
Idle Channel Noise[4]	C-Message weighted	—	8	12	dBrnC
	Psophometric weighted	—	–82	-78	dBmP
PSRR from V_{DDD}, V_{DDA} @ 3.3 V	RX and TX, 200 Hz to 3.4 kHz	—	55	—	dB
Longitudinal Performance					
Longitudinal to Metallic/PCM Balance (forward or reverse)	200 Hz to 1 kHz	—	60	—	dB
	1 kHz to 3.4 kHz	—	58	—	dB
Longitudinal Impedance	200 Hz to 3.4 kHz at TIP or RING	—	50	—	Ω
Longitudinal Current Capability	Active off-hook 60 Hz Reg 73 = 0x0B	—	25	—	mA

Note:

1. Analog signal measured as V_{TIP} - V_{RING}. Assumes ideal line impedance matching.
2. The quantization errors inherent in the µ/A-law companding process can generate slightly worse gain tracking performance in the signal range of 3 to -37 dB for signal frequencies that are integer divisors of the 8 kHz PCM sampling rate.
3. V_{DDD}, V_{DDA} = 3.3 V, V_{BAT} = -52 V, no fuse resistors; R_L = 600 Ω, Z_S = 600 Ω synthesized using RS register coefficients.
4. The level of any unwanted tones within the bandwidth of 0 to 4 kHz does not exceed -55 dBm.
5. 0 dBm0 is equal to 0 dBm into 600 Ω.

Table 3.4. Linefeed Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Feed Current		Differential	—	—	45	mA
		Common Mode	—	—	30	mA
		Differential + Common Mode	—	—	45	mA
DC Loop Current Accuracy		I_{LIM} = 18 mA	—	—	10	%
DC Open Circuit Voltage Accuracy		Active Mode; V_{OC} = 48 V, $V_{TIP} – V_{RING}$	—	—	4	V
DC Differential Output Resistance	R_{DO}	$I_{LOOP} < I_{LIM}$	160	—	640	Ω
DC On-Hook Voltage Accuracy-Ground Start (TIP Open)	V_{OHTO}	$I_{RING} < I_{LIM}$; V_{RING} wrt ground, V_{RING} = -51 V	—	—	4	V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Output Resistance-Ground Start (TIP Open)	R_{ROTO}	$I_{RING}<I_{LIM}$; RING to ground	160	—	640	Ω
DC Output Resistance-Ground Start (TIP Open)	R_{TOTO}	TIP to ground	400	—	—	kΩ
Loop Closure Detect Threshold Accuracy		I_{THR} = 13 mA	—	—	10	%
Ground Key Detect Threshold Accuracy		I_{THR} = 13 mA	—	—	10	%
Ring Trip Threshold Accuracy		AC detection, V_{RING} = 70 Vpk, no offset, I_{TH} = 80 mA	—	—	4	mA
		DC detection, 20 V dc offset, I_{TH} = 13 mA	—	—	1	mA
		DC Detection, 48 V DC offset, R_{loop} = 1500 Ω	—	—	3	mA
Ringing Amplitude	$V_{RINGING}$	Open circuit, V_{BAT} = –106 V	–100	—	—	V_{PK}
Sinusoidal Ringing Total Harmonic Distortion	R_{THD}	50 V_{RMS}, 0 V_{OFFSET}, 0–5 REN	—	1	—	%
Ringing Frequency Accuracy		f = 16 Hz to 60 Hz	—	—	1	%
Ringing Cadence Accuracy		Accuracy of ON/OFF times	—	—	50	ms
Loop Voltage Sense Accuracy		V_{TIP} - V_{RING} = 48 V	—	2	4	%
Loop Current Sense Accuracy		I_{LOOP} = 18 mA	—	7	10	%
Power Alarm Threshold Accuracy		Power Threshold = 1.0 W V_{BAT} = –56 V, I_{VDD} = 40 mA, R_{LOAD} = 600 Ω	—	15	—	%

Table 3.5. Digital I/O Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}	SCLK, CSB, SPI_MOSI, PCLK, FSYNC, PCM_MOSI, RSTB	2.0	—	V_{DDD}	V
Low Level Input Voltage	V_{IL}	SCLK, CSB, SPI_MOSI, PCLK, FSYNC, PCM_MOSI, RSTB	0	—	0.8	V
High Level Output Voltage	V_{OH}	SPI_MISO, SPI_MOSI_THRU, PMC_MISO, INTB: I_O = –4 mA	V_{DDD} –0.6	—	—	V
Low Level Output Voltage	V_{OL}	SPI_MISO, SPI_MOSI_THRU, PMC_MISO, INTB: I_O = 4 mA	—	—	0.4	V
SPI_MOSI_THRU and RSTB Internal Pullup Current			33	42	80	µA
Input Leakage Current	I_L		—	—	10	µA

Table 3.6. Charge Pump Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage (DCDRVa/b, DCFFa/b)	VCP		2 x V_{DDD} – 1	—	2 x V_{DDD}	V
Output Current	ICP		—	—	3[1]	mA

Note:
1. Peak drive current capability is >60 mA.

Table 3.7. Switching Characteristics General Inputs

Parameter	Symbol	Min	Typ	Max	Unit
RSTB Pulse Width (PCM/SPI or ISI Interface)	t_{RST}	200	—	—	µs
RSTB High to First SPI Transfer Start (PCM/SPI Interface) or First Register/RAM Access (ISI Interface)	t_{RCS}	5	—	—	ms

Note:
1. All timing is referenced to the 50% level of the waveform. Input test levels are V_{IH} = V_{DD} - 0.4 V, V_{IL} = 0.4 V. Rise and Fall times are referenced to the 20% and 80% levels of the waveform.

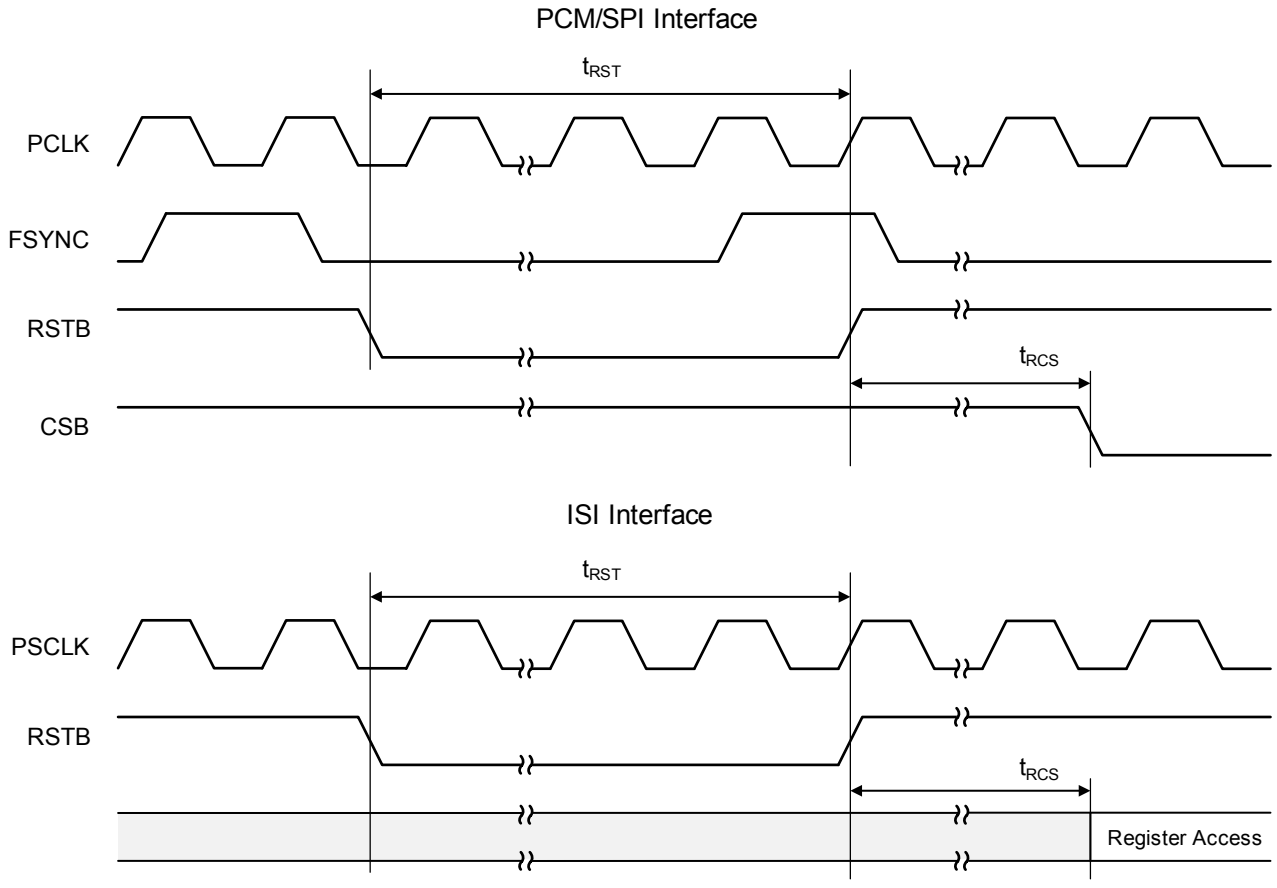


Figure 3.1. Reset Timing Diagram

Table 3.8. Switching Characteristics SPI

Parameter	Symbol	Min	Typ	Max	Unit
Cycle Time SCLK	t_c	83	—	—	ns
Rise Time, SCLK	t_r	—	—	25	ns
Fall Time, SCLK	t_f	—	—	25	ns
Delay Time, SCLK Fall to SPI_MISO Active	t_{d1}	—	—	20	ns
Delay Time, SCLK Fall to SPI_MISO Transition	t_{d2}	—	—	20	ns
Delay Time, CSB Rise to SPI_MISO Tristate	t_{d3}	—	—	20	ns
Setup Time, CSB to SCLK Fall	t_{su1}	25	—	—	ns
Hold Time, CSB to SCLK Rise	t_{h1}	20	—	—	ns
Setup Time, SPI_MOSI to SCLK Rise	t_{su2}	25	—	—	ns
Hold Time, SPI_MOSI to SCLK Rise	t_{h2}	20	—	—	ns
Delay Time between Chip Selects	t_{cs}	220	—	—	ns
SPI_MOSI to SPI_MOSI_THRU Propagation Delay	t_{d4}	—	4	10	ns

Note:

1. All timing is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_{DDD}$ -0.4 V, V_{IL} = 0.4 V.
2. Characteristics for outputs specified with CL = 20 pF.

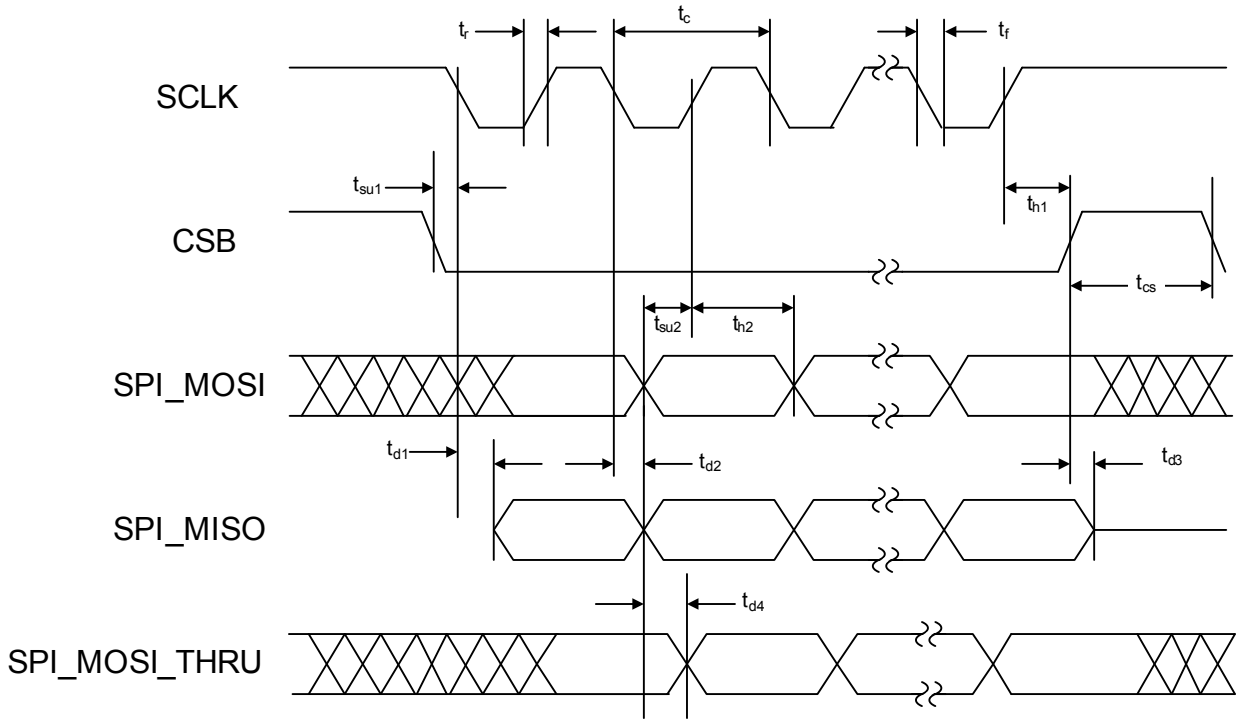


Figure 3.2. SPI Timing Diagram

Table 3.9. Switching Characteristics PCM Highway Interface

Parameter	Symbol	Min[2]	Typ[2]	Max[2]	Unit
PCLK Period	t_p	122	—	1953	ns
PCLK Jitter Tolerance	t_{jitter}	—	—	8	ns_{RMS}
Valid PCLK Inputs[3]		—	512	—	kHz
			768		kHz
			1.024		MHz
			1.536		MHz
			1.544		MHz
			2.048		MHz
			4.096		MHz
			8.192		MHz
FSYNC Period[4]	t_{fs}	—	125	—	µs
PCLK Duty Cycle Tolerance	t_{dty}	40	50	60	%
FSYNC Jitter Tolerance[5]	t_{jitter}	—	—	±120	ns
Rise Time, PCLK	t_r	—	—	25	ns
Fall Time, PCLK	t_f	—	—	25	ns
Delay Time, PCLK Rise to PCM_MISO Active	t_{d1}	—	—	20	ns
Delay Time, PCLK Rise to PCM_MISO Transition	t_{d2}	—	—	20	ns
Delay Time, PCLK Rise to PCM_MISO Tristate[6]	t_{d3}	—	—	20	ns
Setup Time, FSYNC to PCLK Fall	t_{su1}	25	—	—	ns
Hold Time, FSYNC to PCLK Fall	t_{h1}	20	—	—	ns
Setup Time, PCM_MOSI to PCLK Fall	t_{su2}	25	—	—	ns
Hold Time, PCM_MOSI to PCLK Fall	t_{h2}	20	—	—	ns
FSYNC Pulse Width	t_{wfs}	t_p	—	125 µs – t_p	µs

Note:

1. Characteristics for outputs specified with CL = 20 pF.
2. All timing is referenced to the 50% level of the waveform. Input test levels are $V_{IH} = V_{DDD} – 0.4$ V, $V_{IL} = 0.4$ V.
3. A constant PCLK and FSYNC are required.
4. FSYNC source is assumed to be 8 kHz under all operating conditions.
5. FSYNC Jitter Tolerance relative to PCLK.
6. Specification applies to PCLK fall to DTX tristate when that mode is selected.

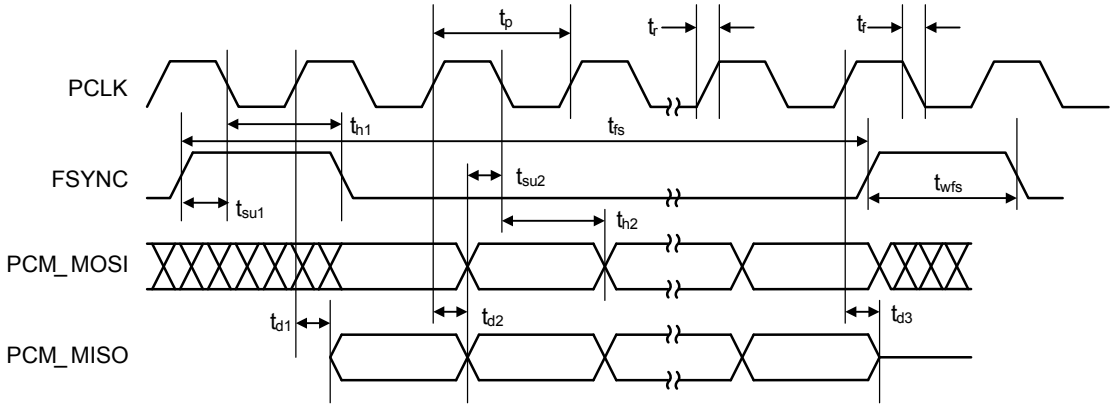


Figure 3.3. PCM Highway Interface Timing Diagram

Table 3.10. Switching Characteristics ISI

Parameter	Symbol	Min	Typ	Max	Unit
Setup Time, ISI_MOSI to PSCLK Fall	t_{su}	7.5	—	—	ns
Hold Time, ISI_MOSI to PSCLK Fall	t_h	5	—	—	ns
Delay Time, PSCLK Rise to ISI_MISO	t_d	—	—	16	ns
PSCLK Period	t_p	—	40.69	—	ns
PSCLK Duty Cycle		40	50	60	%

Note:
1. Timing should be guaranteed by ISI-enabled host SoC.

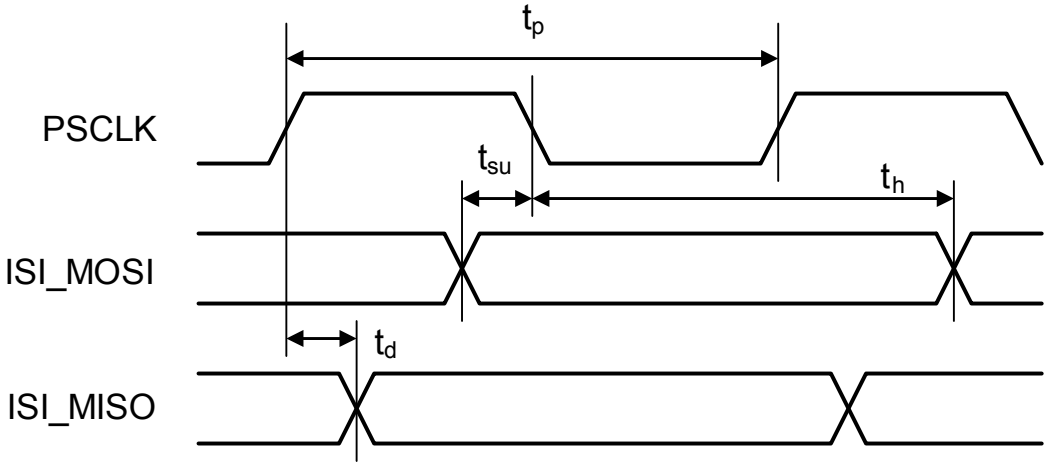


Figure 3.4. ISI Timing Diagram

Table 3.11. Thermal Conditions

Parameter	Symbol	Test Condition	Value	Unit
Storage Temperature Range	T_{STG}		-55 to 150	°C

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance, Typical [1] QFN-56	θ_{JA}		27.9	°C/W
	θ_{JB}		13.8	°C/W
	θ_{JC}		14.3	°C/W
Thermal Resistance, Typical[1] QFN-48	θ_{JA}		28.5	°C/W
	θ_{JB}		13.4	°C/W
	θ_{JC}		15.2	°C/W
Maximum Junction Temperature, (High Voltage Die)[3]	T_{JHV}	Continuous	145	°C
Maximum Junction Temperature (Low Voltage Die)[2]	T_{JLV}	Continuous	125	°C

Note:

1. The thermal resistance of an exposed pad package is assured when the recommended printed circuit board layout guidelines are followed correctly. The specified performance requires that the exposed pad be soldered to an exposed copper surface of at least equal size and that multiple vias are added to enable heat transfer between the top-side copper surface and a large internal/bottom copper plane. Thermal resistance values are based on JEDEC thermal test standard JESD1.
2. Operation of the Si3228x above 125 °C junction temperature may degrade device reliability.
3. Si3228x linefeed is equipped with on-chip thermal limiting circuitry that shuts down the circuit when the junction temperature exceeds the thermal shutdown threshold. The thermal shutdown threshold is normally set to 145 °C; when in the ringing state the thermal shutdown is set to 200 °C.

Table 3.12. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DDA}, V_{DDD}	–0.5 to 4.0	V
Digital Input Voltage	V_{IND}	–0.5 to 4.0	V
Battery Supply Voltage	V_{BAT}	+0.4 to –112	V
Tip or Ring Voltage	V_{TIP}, V_{RING}	V_{BAT}–0.4	V
TIP, RING Current	I_{TIP}, I_{RING}	±100	mA

Note:

1. Permanent device damage may occur or the reliability of the device may be affected if the device is operated at or above the absolute maximum ratings.

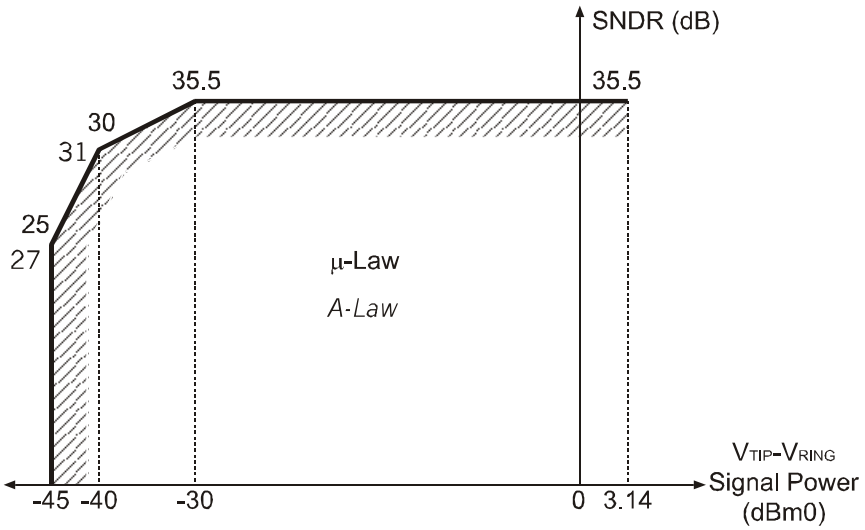


Figure 3.5. Transmit and Receive Path SNDR

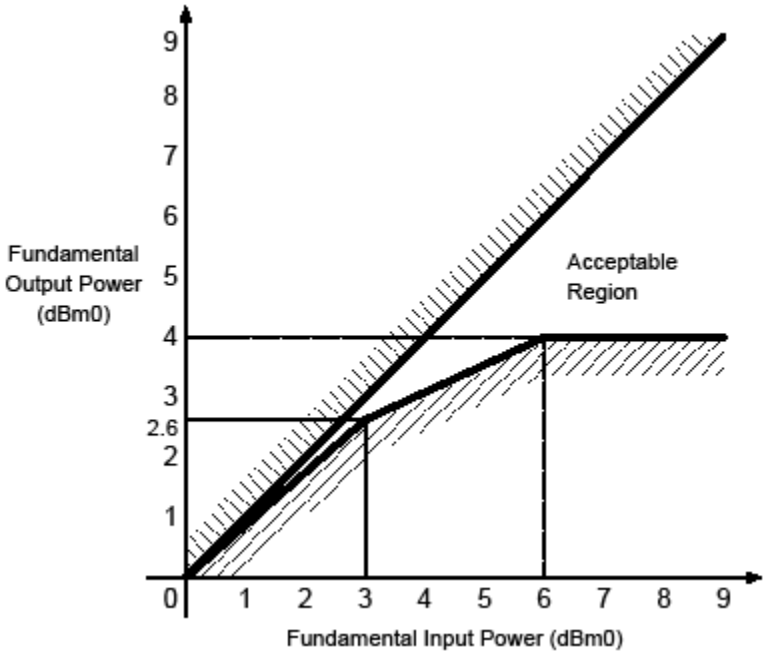


Figure 3.6. Overload Compression Performance

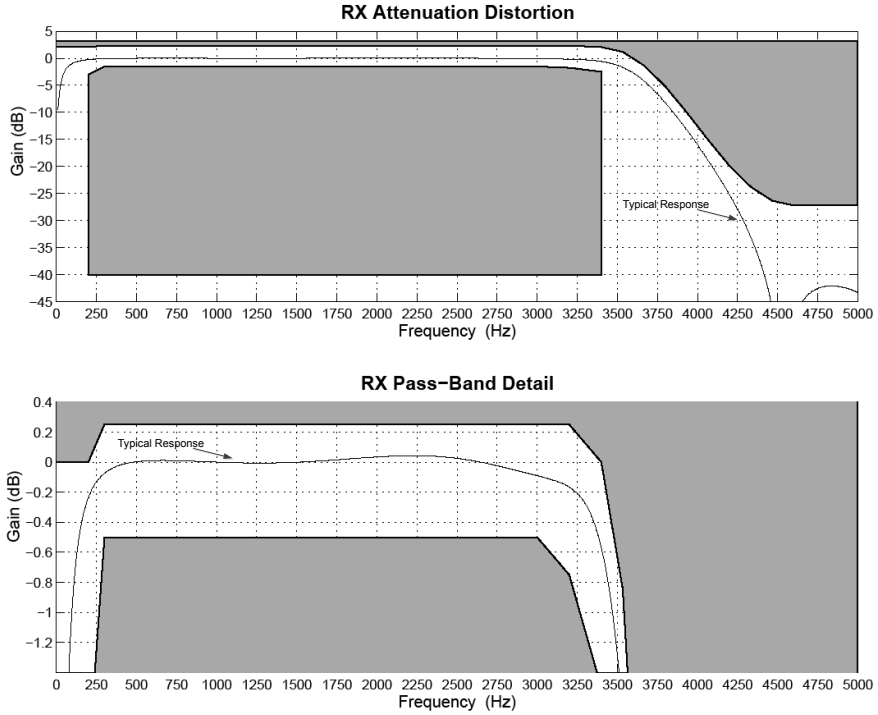


Figure 3.7. Receive Path Frequency Response

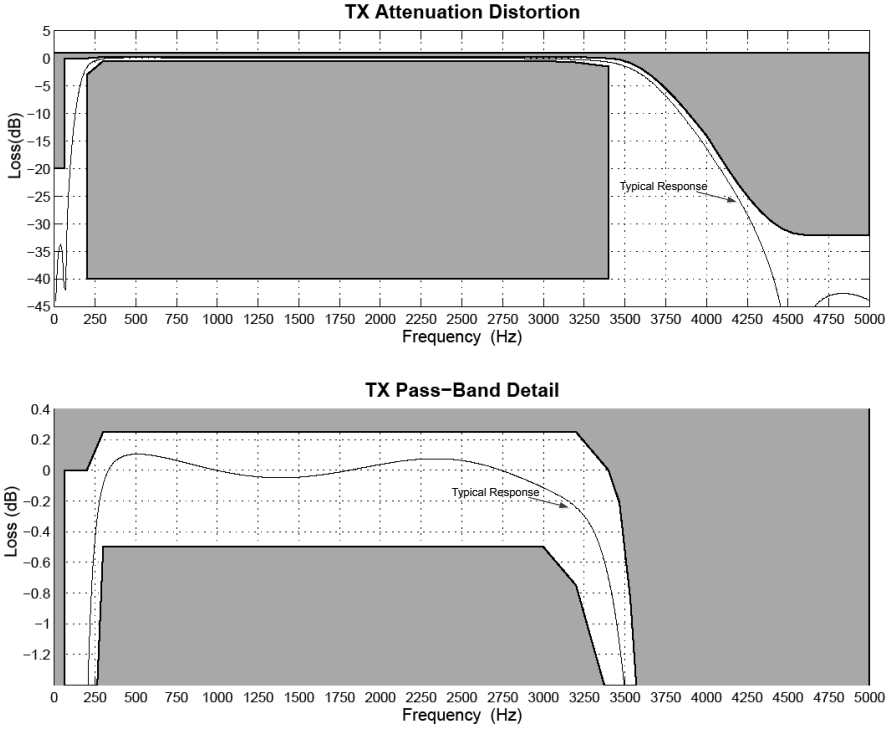


Figure 3.8. Transmit Path Frequency Response

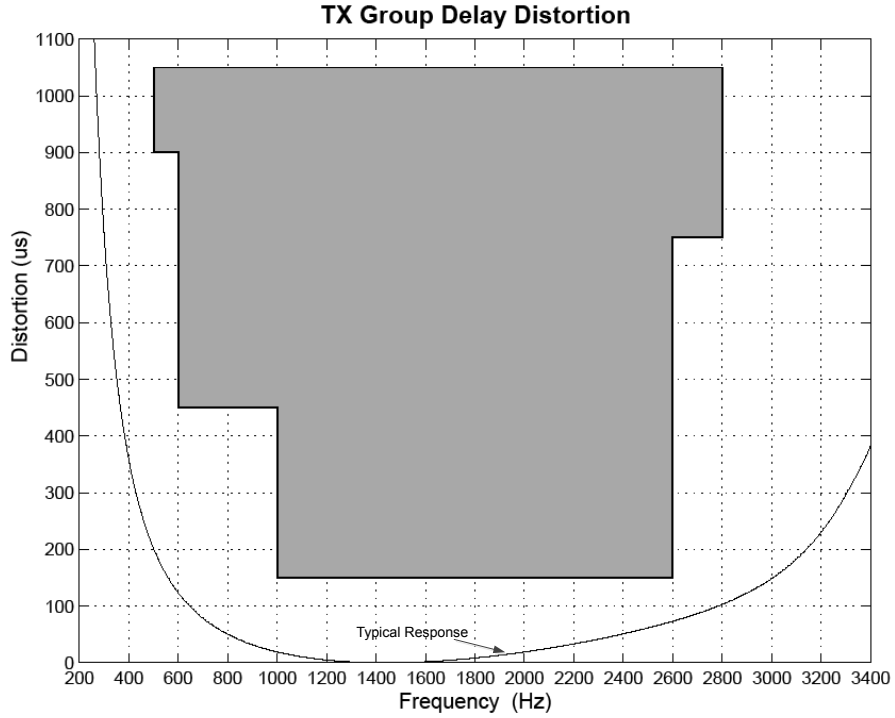


Figure 3.9. Transmit Group Delay Distortion

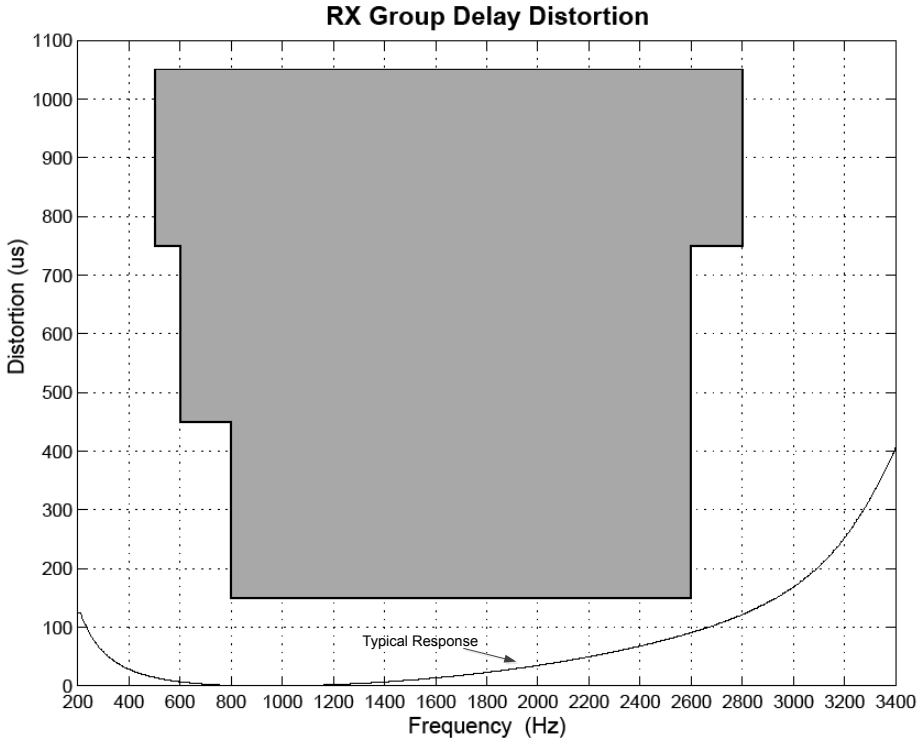


Figure 3.10. Receive Group Delay Distortion

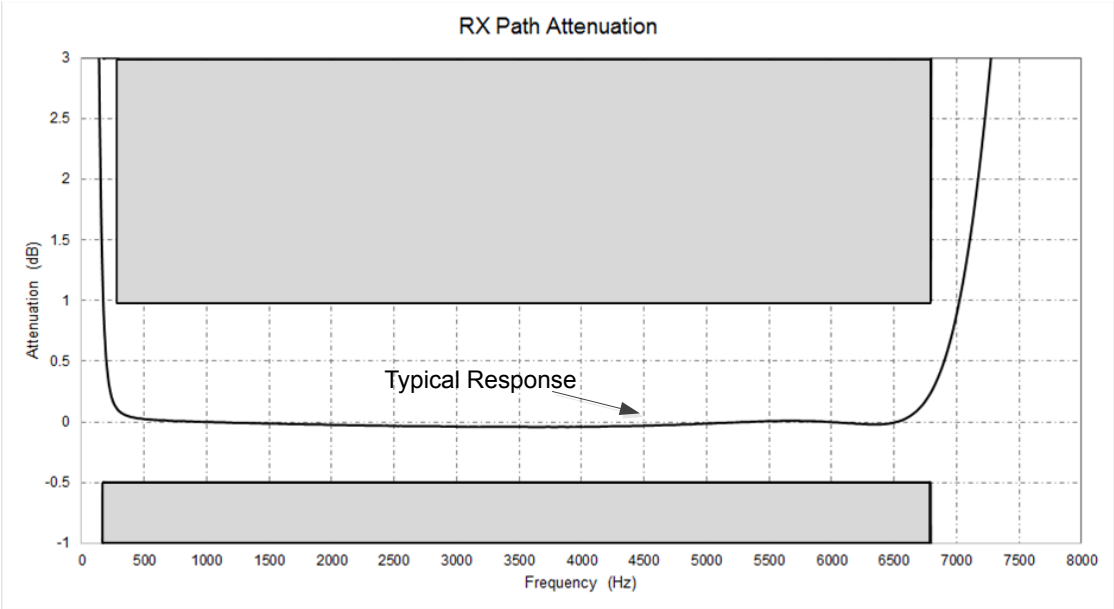


Figure 3.11. Wideband Audio RX Path

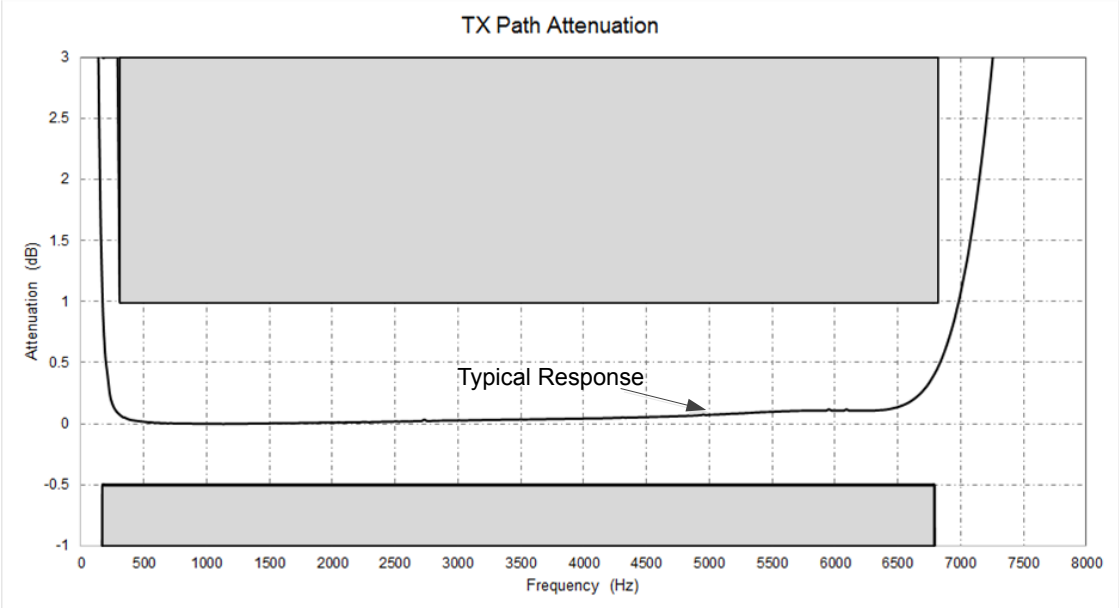


Figure 3.12. Wideband Audio TX Path

4. FXS Features

4.1 DC Feed Characteristics

ProSLIC internal linefeed circuitry provides completely programmable dc feed characteristics.

When in the active state, the ProSLIC operates in one of three dc linefeed operating regions: a constant-voltage region, a constant-current region, or a resistive region, as shown in the figure below. The constant-voltage region has a low resistance, typically 160 Ω. The constant-current region approximates infinite resistance.

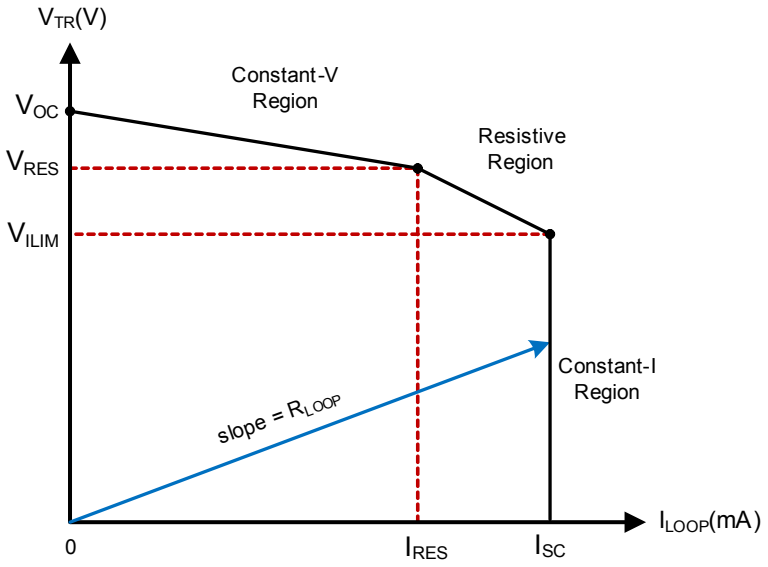


Figure 4.1. Dual ProSLIC DC Feed Characteristics

4.2 Linefeed Operating States

The linefeed interface includes nine different register-programmable operating states as listed in Table 4.1 Linefeed Operating States on page 22. The open state is the default condition in the absence of any preloaded register settings. The device may also automatically enter the open state in the event of a linefeed fault condition.

4.3 Line Voltage and Current Monitoring

The ProSLIC continuously monitors the TIP, RING, and battery voltages and currents via an on-chip Monitor ADC and stores the resulting values in individual RAM locations. Additionally, VTIP, VRING, loop current, and longitudinal current values are calculated based on the differential and common mode voltage measurements. The ADC updates all registers at a rate of 2 kHz or greater.

4.4 Power Monitoring and Power Fault Detection

The Si3228x line monitoring functions are used to continuously protect against excessive power conditions.

If the Si3228x detects an overpower condition, it automatically sets that line to the open state and generates a "power alarm" interrupt.

The interrupt can be masked, but masking the automatic transition to open is not recommended.

4.5 Thermal Overload

If the die temperature exceeds the maximum junction temperature threshold (TJmax) of 145 or 200 °C, depending on the operating state, the device has the ability to shut itself down to a low-power state without user intervention. A thermal alarm interrupt is generated to notify host that the device has been switched to open state.

Table 4.1. Linefeed Operating States

Linefeed State	Description
Open	Output is high-impedance, and audio is not transmitted. This is the default state after powerup or following a hardware reset. This state can also be used in the presence of line fault conditions and to generate open switch intervals (OSIs). This state is used in line diagnostics mode as a high impedance state during linefeed testing. A power fault condition may also force the device into the open state.
Forward Active Reverse Active	Linefeed circuitry is active, and audio is active when off hook. In Forward Active state, the TIP lead is more positive than the RING lead; in Reverse Active state, the RING lead is more positive than the TIP lead.
Forward OHT Reverse OHT	Provides data transmission during an on-hook loop condition (e.g., transmitting caller ID data between ringing bursts). Linefeed circuitry and audio are active. In Forward OHT state, the TIP lead is more positive than the RING lead; in Reverse OHT state, the RING lead is more positive than the TIP lead.
TIP Open	Provides an active linefeed on the RING lead and sets the TIP lead to high impedance (>400 kΩ) for ground start operation in forward polarity. Loop closure and ground key detect circuitry are active.
RING Open	Provides an active linefeed on the TIP lead and sets the RING lead to high impedance (>400 kΩ) for ground start operation in reverse polarity. Loop closure and ground key detect circuitry are active.
Ringing	Drives programmable ringing signal onto TIP and RING leads with or without dc offset.

4.6 Loop Closure Detection

The Si3228x provides a completely programmable loop closure detection mechanism. The loop closure detection scheme provides two thresholds to allow hysteresis, and also includes a programmable debounce filter to eliminate false detection. A loop closure detect status bit provides continuous status, and a maskable interrupt bit is also provided.

4.7 Ground Key Detection

The Si3228x provides a ground key detect mechanism using a programmable architecture similar to the loop closure scheme. The ground key detect scheme provides two thresholds to allow hysteresis and also includes a programmable debounce filter to eliminate false detection. A ground key detect status bit provides continuous status, and a maskable interrupt bit is also provided.

4.8 Ringing Generation

The Si3228x supports the patented Low-Power Ringing (LPR) method exclusively, which when used with a tracking battery scheme, maximizes the ringing power transferred to the load and reduces overall power consumption. The figure below illustrates the fundamental differences between LPR and the traditional balanced or unbalanced ringing. Ringing is fully programmable including frequency, amplitude, dc offset, wave shape, and crest factor. The Si3228x also supports automatic ring cadencing and ringtrip detection (ac and dc). Smart ringing is available on some versions of the Si3228x to reduce the cost of ac-dc power adapters. Smart ringing reduces the peak current required by ringing the two channels out-of-phase with each other.

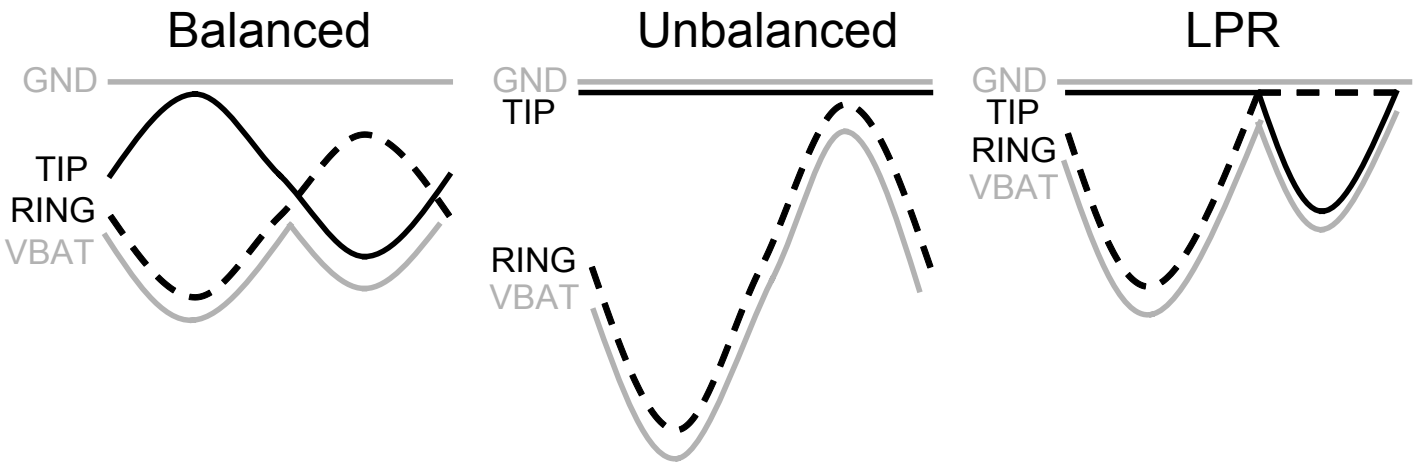


Figure 4.2. Low Power Ringing

4.9 Polarity Reversal

The Si3228x supports polarity reversal for message waiting and various other signaling modes. The ramp rate can be programmed for a smooth or abrupt transition to accommodate different application requirements.

4.10 Two-Wire Impedance Synthesis

The ac two-wire impedance synthesis is generated on-chip using a DSP-based scheme to optimally match the output impedance of the Si3228x to the reference impedance. Most real or complex two-wire impedances can be generated with appropriate register coefficients.

4.11 Transhybrid Balance Filter

The trans-hybrid balance function is implemented on-chip using a DSP-based scheme to effectively cancel the reflected receive path signal from the transmit path.

4.12 Tone Generators

The Si3228x includes two digital tone generators that allow a wide variety of single- or dual-tone frequency and amplitude combinations. Each tone generator has its own set of registers that hold the desired frequency, amplitude, and cadence to allow generation of DTMF and call progress tones for different requirements. The tones can be directed to either receive or transmit paths.

4.13 DTMF Detection (Si32281/3/5/7 Only)

The Dual ProSLIC performs DTMF detection.

4.14 Pulse Metering

The pulse metering system for the Si3228x is designed to inject a 12 or 16 kHz billing tone into the audio path with maximum amplitude of 1 VRMS at TIP and RING into a 200 Ω ac load impedance. The tone is generated in the DSP via a table lookup that guarantees spectral purity by not allowing drift. The tone will ramp up until it reaches a host-programmed threshold, at which point it will maintain that level until instructed to ramp down, thus creating a trapezoidal envelope.

The amplitude is controlled by an automatic gain control circuit (AGC). While the tone is ramping up, the AGC takes the feedback audio and applies it to a band pass filter, which is programmed for the 12 or 16 kHz frequency of interest. When the peak is detected, the ramp is stopped.

4.15 DC-DC Controller

The Si3228x integrates two dc-dc controllers that can be used to control external dc-dc converters to generate high voltage supplies to the SLIC channels.

The integrated line feeds are designed to work with a single tracking high voltage input, one for each channel.

The Vbat voltage for each channel is optimized to minimize power consumption by closely tracking the SLIC state, even tracking the ringing waveforms.

Both of the dc-dc controller outputs DCDRVa/b are driven by an internal charge pump which allows them to connect directly to the gate of the MOSFET switch of a dc-dc converter. This connection eliminates the need for external MOSFET pre-drive circuitry, even when VTH is greater than VDD. The Si3228x can use a capacitive boost tracking battery supply for lower power, cost, and footprint compared to other tracking or shared battery supplies in the industry. See Table 3.6 Charge Pump Characteristics on page 12.

4.16 Wideband Audio

The Si3228x supports wideband audio (150Hz—6.8 kHz) compliant with PKT-SP-HDV-104-120823, and is configurable to support the full ITU-T-G.722-201209 bandwidth (50Hz–7 kHz).

4.17 Test Facilities

The Si3228x supports a rich set of metallic loop tests to diagnose external faults, as well as a set of inward self-tests to support diagnostics of the Si3228x-based voice port. Implementation of metallic loop tests requires the ProSLIC™ MLT API, while the inward self-tests are included in the standard ProSLIC™ API.

Table 4.2. Supported Tests

Test	Description
Metallic Loop Tests	
Voltages	Measures ac and dc voltages from T-R, T-G, and R-G.
Receiver Off-hook	Discriminates between resistive fault and off-hook terminating device.
REN	Measures Ringer Equivalence Number (REN).
REN Capacitance	Measures T-R capacitance of on-hook load.
Capacitance	Measures 3-Terminal Capacitance.
Resistance	Measures resistance from T-R, T-G, or R-G.
Inward Self-Tests	
PCM Loopback	Configures Si3228x for 8- or 16-bit PCM loopback.
DC Feed	Verify dc Feed I/V and loop closure using integrated test load.
Ringing and Ringtrip	Verify ringing voltage (ac and dc). Optional ringtrip check to support system level signaling verification.
Battery	Verify VBAT.
Audio Gain	Measure gain of RX (host to line) and TX (line to host) paths without using an external load, test equipment, or requiring the host to provide audio samples.

In addition to these specific test suites, the user is free to use the general test facilities listed in the following table:

Table 4.3. General Test Facilities

Test	Description
Monitor ADC	Provides TIP/RING voltages (inside and outside overcurrent protection), TIP/RING currents and VBAT voltage.
Audio Diagnostic Filters	Three cascaded second-order Biquad filters with peak hold and averaging capabilities.
Loopback Modes	Digital and analog loopback modes to isolate portions of the audio path.
Tone Generators	The dual-tone generators may be used as general-purpose test signal generators.

5. System Interfaces

5.1 SPI Control Interface

The controller interface to the Si32282/3/6/7 is a 4-wire interface modeled after microcontroller and serial peripheral devices. The interface consists of a clock (SCLK), chip select (CSB), serial data input (SPI_MOSI), and serial data output (SPI_MISO). In addition, the ProSLIC devices feature a serial data through output (SPI_MOSI_THRU) to support operation of up to 16 channels using a single chip select line. The FXS port occupies one SPI channel. The device operates with both 8-bit and 16-bit SPI controllers.

5.2 PCM Interface and Companding

The Si32282/3/6/7 contains a flexible, programmable interface for the transmission and reception of digital PCM samples. PCM data transfer is controlled by the PCM clock (PCLK) and frame sync (FSYNC) inputs as well as the PCM Mode Select, PCM Transmit Start, and PCM Receive Start settings.

The interface can be configured to support from 8 to 128 8-bit time slots in each 125 µs frame, corresponding to a PCM clock (PCLK) frequency range of 512 kHz to 8.192 MHz. 1.544 MHz is also supported.

The Si3228x supports both µ-255 Law (µ-Law) and A-law companding formats in addition to 16-bit linear data mode with no companding.

5.3 Integrated Serial Interface

The Si32280/1/4/5 devices' integrated serial interface (ISI) is a three-wire proprietary interface which serializes SPI and PCM communications and interrupts, reducing the SoC interface from nine wires to three (PSCLK, ISI_MISO, ISI_MOSI). SPI communications and PCM data transfers are embedded in the serial data. The host side of the ISI is integrated onto selected SoCs from several vendors.

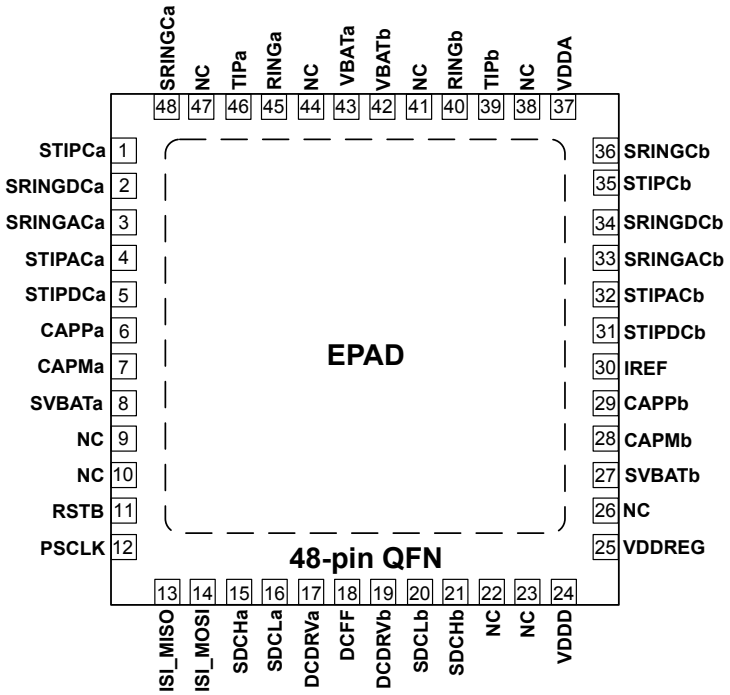
ISI is a point to point interface; therefore, it is not possible to daisy-chain more than one ISI ProSLIC device. Both µ-255 Law (µ-Law) and A-law companding formats are supported in addition to 16-bit linear data mode with no companding.

5.4 Input/Output Voltage

Si3228x devices have the ability to gluelessly interface directly to 3.3 V devices via the PCM, SPI, Interrupt and RESET pins (SCLK, CSB, SPI_MOSI, SPI_MISO, SPI_MOSI_THRU, PCLK, FSYNC, PCM_MISO, PCM_MOSI, INTB, RSTB).

6. Pin Descriptions

6.1 Si32280/1/4/5 7x7 mm Pinout



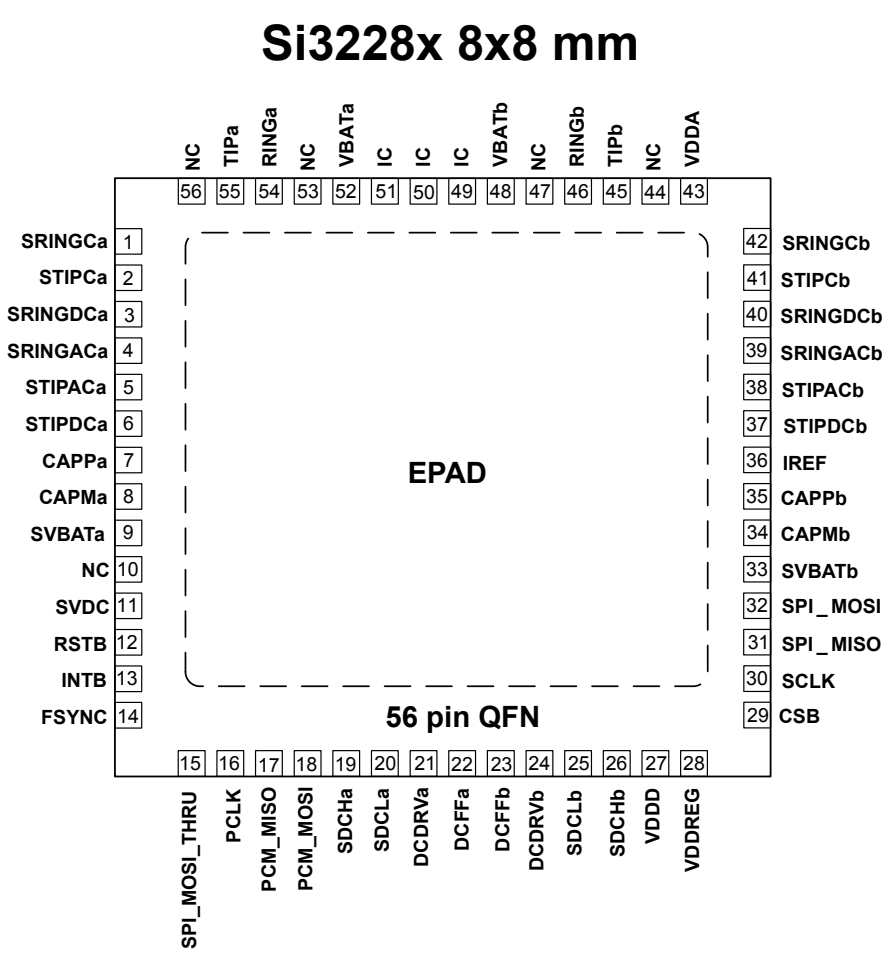
Pin #	Pin Name	Description
1	STIPCa	**TIP Coarse Sense Input—Channel A** TIP Channel A voltage sensing outside protection circuit.
2	SRINGDCa	**RING DC Sense—Channel A** Analog dc input used to sense voltage on Channel A RING lead.
3	SRINGACa	**RING AC Sense—Channel A** Analog ac input used to detect voltage on Channel A RING lead.
4	STIPACa	**TIP AC Sense—Channel A** Analog ac input used to detect voltage on Channel A TIP lead.
5	STIPDCa	**TIP DC Sense—Channel A** Analog dc input used to sense voltage on Channel A TIP lead.
6	CAPPa	**SLIC Stabilization Capacitor—Channel A** Capacitor used in dc feed low-pass filter on channel A.
7	CAPMa	**SLIC Stabilization Capacitor—Channel A** Capacitor used in dc feed low-pass filter on channel A.

Pin #	Pin Name	Description
8	SVBATa	**VBAT Sense—Channel A** Input used to sense voltage on Channel A dc-dc converter output voltage lead.
9	NC	**No Connect** This pin should be left unconnected.
10	NC	**No Connect** This pin should be left unconnected.
11	RSTB	**Reset Input** Active low input. Hardware reset used to place all control registers in the default state.
12	PSCLK	**ISI Bus Clock Input** Clock input for ISI bus timing.
13	ISI_MISO	**ISI Data Output** ISI Master Input, Slave Output. Output data to ISI bus.
14	ISI_MOSI	**ISI Data Input** ISI Master Output, Slave Input. Input data from ISI bus.
15	SDCHa	**DC Monitor—Channel A** DC-DC converter monitor input used to sense switch current in the Channel A converter.
16	SDCLa	**DC Monitor—Channel A** DC-DC converter monitor input used to sense switch current in the Channel A converter.
17	DCDRVa	**DC Drive—Channel A** DC-DC converter control signal output which drives external transistor on Channel A.
18	DCFF	**DC-DC Charge Pump Output**
19	DCDRVb	**DC Drive—Channel B** DC-DC converter control signal output which drives external transistor on Channel B.
20	SDCLb	**DC Monitor—Channel B** DC-DC converter monitor input used to sense switch current in the Channel B converter.
21	SDCHb	**DC Monitor—Channel B** DC-DC converter monitor input used to sense switch current in the Channel B converter.
22	NC	**No Connect** This pin should be left unconnected.
23	NC	**No Connect** This pin should be left unconnected.

Pin #	Pin Name	Description
24	VDDD	**IC Voltage Supply** 3.3 V digital supply for internal circuitry.
25	VDDREG	**Regulated Core Power Supply**
26	NC	**No Connect** This pin should be left unconnected.
27	SVBATb	**VBAT Sense—Channel B** Input used to sense voltage on Channel A dc-dc converter output voltage lead.
28	CAPMb	**SLIC Stabilization Capacitor—Channel B** Capacitor used in dc feed low-pass filter on channel B.
29	CAPPb	**SLIC Stabilization Capacitor—Channel B** Capacitor used in dc feed low-pass filter on channel B.
30	IREF	**Current Reference Input** Connects to an external resistor used to provide a high accuracy reference current.
31	STIPDCb	**TIP DC Sense—Channel B** Analog dc input used to sense voltage on Channel B TIP lead.
32	STIPACb	**TIP AC Sense—Channel B** Analog ac input used to detect voltage on Channel B TIP lead.
33	SRINGACb	**RING AC Sense—Channel B** Analog ac input used to detect voltage on Channel B RING lead.
34	SRINGDCb	**RING DC Sense—Channel B** Analog dc input used to sense voltage on Channel B RING lead.
35	STIPCb	**TIP Coarse Sense Input—Channel B** TIP Channel B voltage sensing outside protection circuit.
36	SRINGCb	**RING Coarse Sense Input—Channel B** RING Channel B voltage sensing outside protection circuit.
37	VDDA	**Analog Supply Voltage** Analog 3.3 V power supply for internal analog circuitry.
38	NC	**No Connect** This pin should be left unconnected.
39	TIPb	**TIP Terminal—Channel B** Connect to the Channel B TIP lead of the subscriber loop.
40	RINGb	**RING Terminal—Channel B** Connect to the Channel B RING lead of the subscriber loop.

Pin #	Pin Name	Description
41	NC	**No Connect** This pin should be left unconnected.
42	VBATb	**Battery Voltage Supply—Channel B** Connect to Channel B battery supply from dc-dc converter.
43	VBATa	**Battery Voltage Supply—Channel A** Connect to Channel A battery supply from dc-dc converter.
44	NC	**No Connect** This pin should be left unconnected.
45	RINGa	**Ring Terminal—Channel A** Connect to the Channel A RING lead of the subscriber loop.
46	TIPa	**Tip Terminal—Channel A** Connect to the Channel A TIP lead of the subscriber loop.
47	NC	**No Connect** This pin should be left unconnected.
48	SRINGCa	**RING Coarse Sense Input—Channel A** RING Channel A voltage sensing outside protection circuit.

6.2 Si32282/3/6/7 8x8 mm Pinout



Pin #	Pin Name	Description
1	SRINGCa	**RING Coarse Sense Input—Channel A** RING Channel A voltage sensing outside protection circuit.
2	STIPCa	**TIP Coarse Sense Input—Channel A** TIP Channel A voltage sensing outside protection circuit.
3	SRINGDCa	**RING DC Sense—Channel A** Analog dc input used to sense voltage on channel A RING lead.
4	SRINGACa	**RING AC Sense—Channel A** Analog ac input used to detect voltage on channel A RING lead.
5	STIPACa	**TIP AC Sense—Channel A** Analog ac input used to detect voltage on Channel A TIP lead.
6	STIPDCa	**TIP DC Sense—Channel A** Analog dc input used to sense voltage on channel A TIP lead.
7	CAPPa	**SLIC Stabilization Capacitor—Channel A** Capacitor used in dc feed low-pass filter on channel A.

Pin #	Pin Name	Description
8	CAPMa	**SLIC Stabilization Capacitor—Channel A** Capacitor used in dc feed low-pass filter on channel A.
9	SVBATa	**VBAT Sense—Channel A** Input used to sense voltage on Channel A dc-dc converter output voltage lead.
10	NC	**No Connect** This pin must be left unconnected.
11	SVDC	**DC-DC Input Voltage Sensor** Senses VDC input to dc-dc converters.
12	RSTB	**Reset Input** Active low input. Hardware reset used to place all control registers in the default state.
13	INTB	**Interrupt Output** Maskable interrupt output. Open drain output for wire-Ored operation.
14	FSYNC	**Frame Sync Clock Input** 8 kHz frame synchronization signal for the PCM bus. May be short or long pulse format.
15	SPI_MOSI_THRU	**SPI_MOSI Pass-Through** Cascaded SPI_MOSI signal for daisy-chain mode.
16	PCLK	**PCM Clock Input** Clock input for PCM bus timing.
17	PCM_MISO	**PCM Data Output** PCM Master Input, Slave Output. Output data to PCM bus.
18	PCM_MOSI	**PCM Data Input** PCM Master Output, Slave Input. Input data from PCM bus.
19	SDCHa	**DC Monitor—Channel A** DC-DC converter monitor input used to sense switch current in the Channel A converter.
20	SDCLa	**DC Monitor—Channel A** DC-DC converter monitor input used to sense switch current in the Channel A converter.
21	DCDRVa	**DC Drive—Channel A** DC-DC converter control signal output which drives external transistor on Channel A.
22	DCFFa	**DC-DC Charge Pump Output—Channel A**
23	DCFFb	**DC-DC Charge Pump Output—Channel B**
24	DCDRVb	**DC Drive—Channel B** DC-DC converter control signal output which drives external transistor on Channel B.

Pin #	Pin Name	Description
25	SDCLb	**DC Monitor—Channel B** DC-DC converter monitor input used to sense switch current in the Channel B converter.
26	SDCHb	**DC Monitor—Channel B** DC-DC converter monitor input used to sense switch current in the Channel B converter.
27	VDDD	**IC Voltage Supply** 3.3 V digital power supply for internal circuitry.
28	VDDREG	**Regulated Core Power Supply**
29	CSB	**Chip Select Input** Active low. When inactive, SCLK and SPI_MOSI are ignored and SPI_MISO is high impedance. When active, the serial port is operational.
30	SCLK	**Serial Port Bit Clock Input** Serial port clock input. Controls the serial data on SPI_MISO and latches the data on SPI_MOSI.
31	SPI_MISO	**Serial Port Data Output** SPI Master Input, Slave Output. Output control data to Serial Peripheral Interface bus.
32	SPI_MOSI	**Serial Port Data Input** SPI Master Output, Slave Input. Input control data from Serial Peripheral Interface bus.
33	SVBATb	**VBAT Sense—Channel B** Input used to sense voltage on channel A dc-dc converter output voltage lead.
34	CAPMb	**SLIC Stabilization Capacitor—Channel B** Capacitor used in dc feed low-pass filter on channel B.
35	CAPPb	**SLIC Stabilization Capacitor—Channel B** Capacitor used in dc feed low-pass filter on channel B.
36	IREF	**Current Reference Input** Connects to an external resistor used to provide a high accuracy reference current.
37	STIPDCb	**TIP DC Sense—Channel B** Analog dc input used to sense voltage on Channel B TIP lead.
38	STIPACb	**TIP AC Sense—Channel B** Analog ac input used to detect voltage on Channel B TIP lead.
39	SRINGACb	**RING AC Sense—Channel B** Analog ac input used to detect voltage on Channel B RING lead.

Pin #	Pin Name	Description
40	SRINGDCb	**RING DC Sense—Channel B** Analog dc input used to sense voltage on Channel B RING lead.
41	STIPCb	**TIP Coarse Sense Input—Channel B** TIP channel B voltage sensing outside protection circuit.
42	SRINGCb	**RING Coarse Sense Input—Channel B** RING channel B voltage sensing outside protection circuit.
43	VDDA	**Analog Supply Voltage** Analog 3.3 V power supply for internal analog circuitry.
44	NC	**No Connect** This pin must be left unconnected.
45	TIPb	**TIP Terminal—Channel B** Connect to the Channel B TIP lead of the subscriber loop.
46	RINGb	**RING Terminal—Channel B** Connect to the Channel B RING lead of the subscriber loop.
47	NC	**No Connect** This pin should be left unconnected.
48	VBATb	**Battery Voltage Supply—Channel B** Connect to Channel B battery supply from dc-dc converter.
49	IC	**Internal Connect** This pin must be left unconnected.
50	IC	**Internal Connect** This pin must be left unconnected.
51	IC	**Internal Connect** This pin must be left unconnected.
52	VBATa	**Battery Voltage Supply—Channel A** Connect to Channel A battery supply from dc-dc converter.
53	NC	**No Connect** This pin must be left unconnected.
54	RINGa	**RING Terminal—Channel A** Connect to the Channel A RING lead of the subscriber loop.
55	TIPa	**TIP Terminal—Channel A** Connect to the Channel A TIP lead of the subscriber loop.
56	NC	**No Connect** This pin must be left unconnected.

7. Packaging

7.1 Package Outline: 48-Pin QFN

The figure below illustrates the package details for the 48-pin QFN package. The table lists the values for the dimensions shown in the illustration.

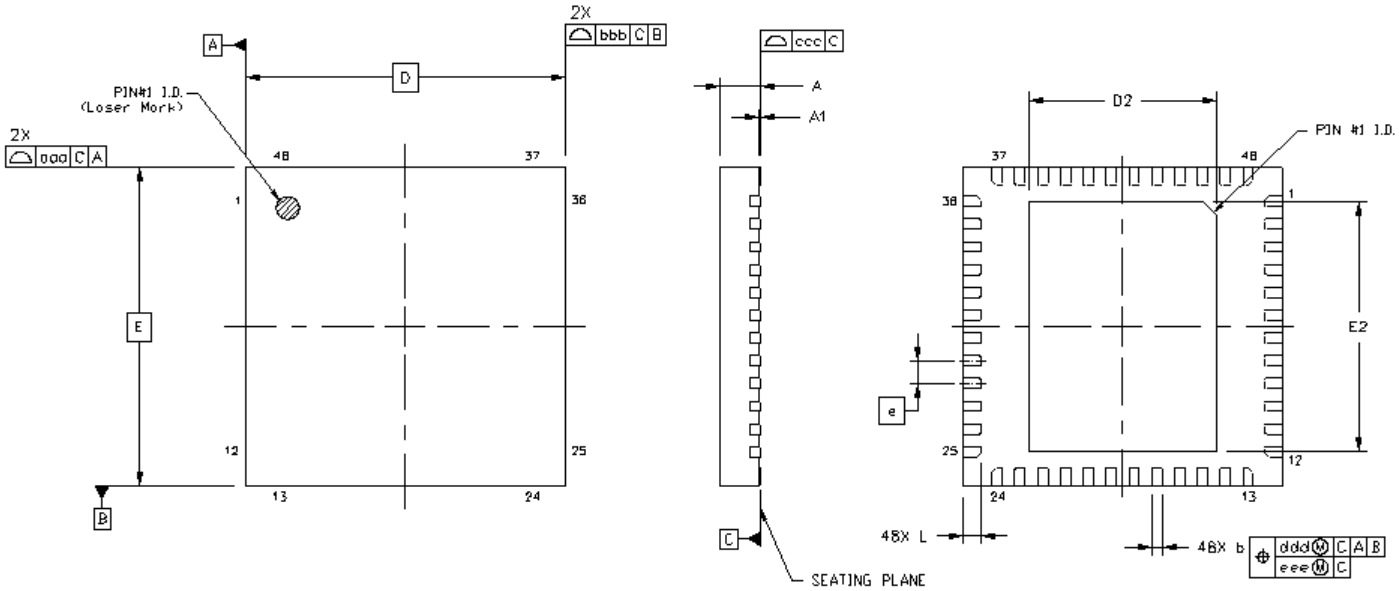


Figure 7.1. 48-Pin QFN Package

Table 7.1. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		7.00 BSC	
D2	4.00	4.10	4.20
e		0.50 BSC	
E		7.00 BSC	
E2	5.40	5.50	5.60
L	0.30	0.40	0.50
aaa	—	—	0.15
bbb	—	—	0.15
ccc	—	—	0.08
ddd	—	—	0.10

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020D specification for Small Body Components.

7.2 Package Outline: 56-Pin QFN

The figure below illustrates the package details for the 56-pin QFN package. The table lists the values for the dimensions shown in the illustration.

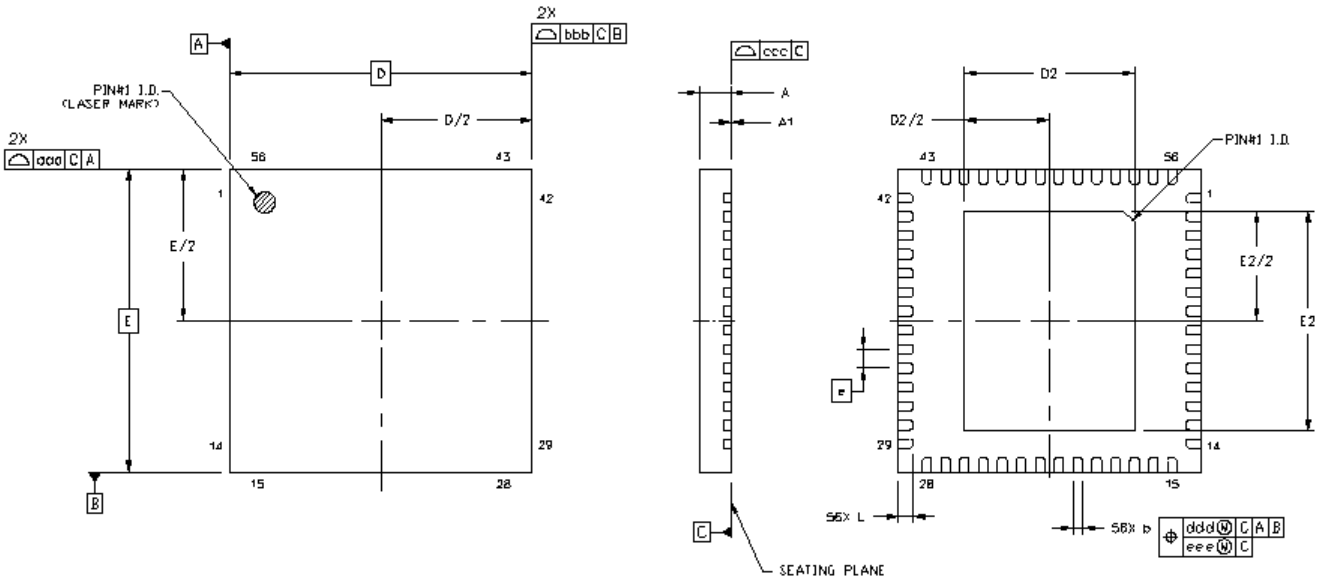


Figure 7.2. 56-Pin QFN Package

Table 7.2. Package Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		8.00 BSC	
D2	4.40	4.50	4.60
e		0.50 BSC	
E		8.00 BSC	
E2	5.70	5.80	5.90
L	0.30	0.40	0.50
aaa	—	—	0.15
bbb	—	—	0.15
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.05

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.3 Land Pattern: 48-Pin QFN

The figure below shows the recommended land pattern details for the 48-pin QFN package. The table lists the values for the dimensions shown in the illustration.

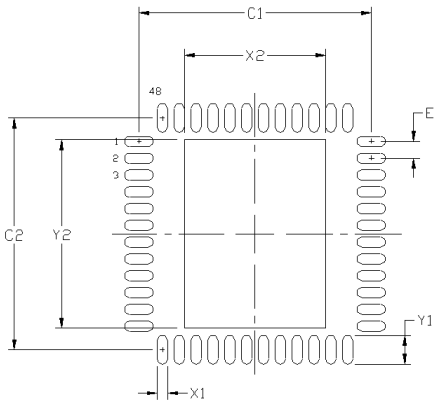


Figure 7.3. 48-Pin QFN Land Pattern

Table 7.3. PCB Land Pattern

Dimension	mm
C1	6.90
C2	6.90
E	0.50
X1	0.30
Y1	0.85
X2	4.20
Y2	5.60

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
8. A 4x3 array of 1.10 mm square openings on 1.40 mm pitch should be used for the center ground pad to achieve a target solder coverage of ~50%.
9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for small body components.
11. A minimum of eight thermal vias are required in each center pad.
12. The recommended via diameter is 0.20–0.30 mm (8-12 mils).
13. Thermal vias placed in the center pads must have a minimum spacing of 1.0 mm from the edge of the via to the closest pin pad metal (≥1.0 mm).
14. Vias placed within the center pad areas must be either filled or tented on the top side of the board to prevent solder thieving from under the device.

7.4 Land Pattern: 56-Pin QFN

The figure below shows the recommended land pattern details for the 56-pin QFN package. The table lists the values for the dimensions shown in the illustration.

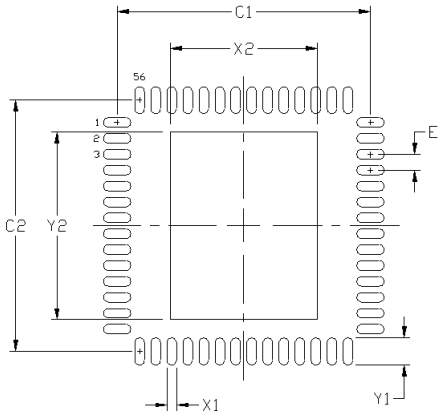


Figure 7.4. 56-Pin QFN Land Pattern

Table 7.4. PCB Land Pattern

Dimension	mm
C1	7.90
C2	7.90
E	0.50
X1	0.30
Y1	0.85
X2	4.60
Y2	5.90

Note:

1. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 4x3 array of 1.05 mm square openings on 1.5 mm pitch should be used for the center ground pad to achieve a target solder coverage of ~50%.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for small body components.
10. High-Tg PCB materials (Tg 170C) are recommended for Pb-free reflow profiles, per standard industry practice.
11. A minimum of eight thermal vias are required in each center pad.
12. The recommended via diameter is 0.20-0.30 mm (8-12 mils).
13. Thermal vias placed in the center pad must have a minimum spacing of 1.0 mm from the edge of the via to the closest pin pad metal (≥1.0 mm).
14. Vias placed within the center pad areas must be either filled or tented on the top side of the board to prevent solder thieving from under the device.

7.5 Top Marking: 48-Pin QFN

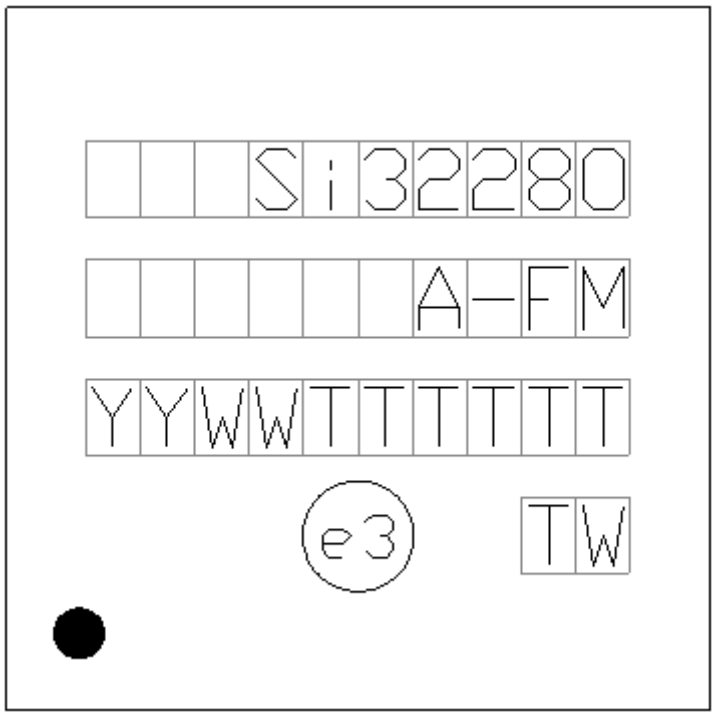


Figure 7.5. Top Marking

Table 7.5. Top Marking Explanation

Line 1 Marking:	Device Root Part Number	e.g., Si32280
Line 2 Marking:	Device Part Number Suffix	Revision, temperature rating, and package type
Line 3 Marking:	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the assembly release.
	TTTTTT=Manufacturing Code	Manufacturing code to track lot information.
Line 4 Marking:	Circle = 0.5 mm Diameter Lower Left-Justified	Pin 1 Identifier
	Circle = 1.3 mm Diameter Center-Justified	"e3" Pb-Free Symbol
	Country of Origin ISO Code Abbreviation	e.g., TW

7.6 Top Marking: 56-Pin QFN

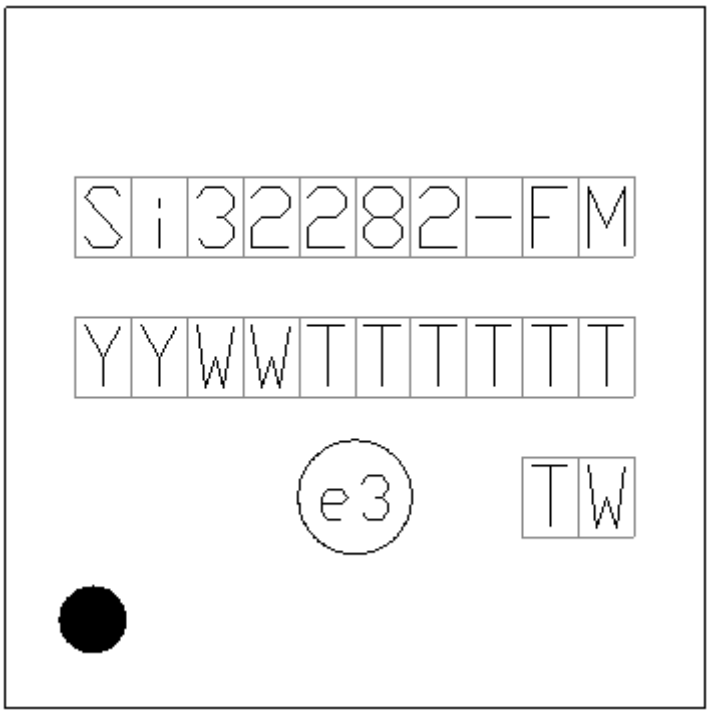


Figure 7.6. Top Marking

Table 7.6. Top Marking Explanation

Line 1 Marking:	Device Part Number	e.g., Si32282. Root part number, temperature rating, and package type.
Line 2 Marking:	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the assembly release.
	TTTTTT = Manufacturing Code	Manufacturing code to track lot information.
Line 3 Marking:	Circle = 1.3 mm Diameter Center-Justified	"e3" Pb-Free Symbol
	Country of Origin ISO Code Abbreviation	e.g., TW
Line 4 Marking:	Circle = 0.5 mm Diameter Lower Left-Justified	Pin 1 Identifier

8. Document Change List

Revision 0.1 to Revision 0.2

- Updated power supply characteristics.
- Updated timing diagrams.
- Updated pin references and descriptions.
- Added package outline information.
- Added PCB land pattern information.
- Added top mark information.

Revision 0.2 to Revision 0.3

- Updated pinout.
- Updated Vbat max to –106 V.
- Updated EVB and orderable part numbers.
- Added Smart Ringing functional description.

Revision 0.3 to Revision 0.4

- Replaced selectable PCM/ISI interface with dedicated PCM only interface using 8 x 8 mm QFN56.
- Added ISI only interface using 7 x 7 mm QFN48

Revision 0.4 to Revision 0.5

- Updated single frequency distortion spec.

Revision 0.5 to Revision 1.0

- Corrected DCCFa to DCFFa typo on 8x8 mm pinout.
- Corrected 8x8 mm description for pin numbers 41 and 42.
- Added orderable part numbers for Si3228x-A-ZMx.
- Updated Table 3.2 Power Supply Characteristics on page 8.
- Numerous clarifications.