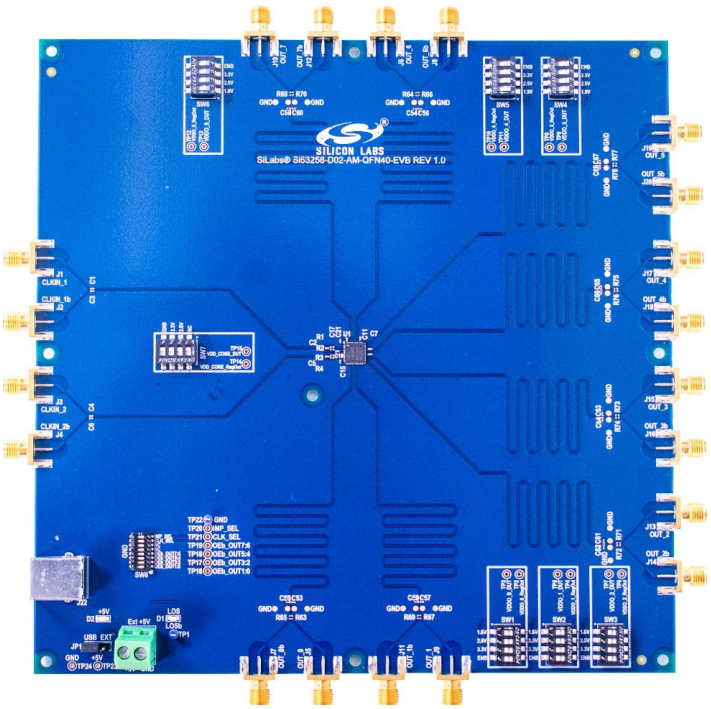
UG400: Si53258-EVB User's Guide (Using Si53258-D02-AM-QFN40-EVB)

The Si53258-EVB is used for evaluating the two input, eight output Si53258A-D02AM Automotive grade PCIe Reference Clock Buffer. The Si53258A-D02AM device selects one of two differential input clocks to buffer 8 copies of a 100 MHz HCSL format output clock compliant to PCIe Gen 1/2/3/4/5 common clock and separate reference clock specifications.



EVB FEATURES

- Powered from either USB port or external +5V power supply.
- Two differential input clocks to select from for buffering.
- Eight buffered HCSL format differential output clocks.
- Programmable device core VDD supply for operation at 3.3 V, 2.5 V, or 1.8 V.
- Programmable VDDO (output driver) supplies allow each of the clock output banks to have its own power supply voltage selectable from 3.3 V, 2.5 V, or 1.8 V.
- SMA connectors for all output clocks.
- Internal output termination switch selectable for 100 Ω or 85 Ω operation.
- Output enable (OE) control switch per output.
- All output trace lengths matched to 10 inches.
- Loss of Signal (LOS) indication LED.

Table of Contents

1. Functional Block Diagram

Below is a functional block diagram of the Si53258-EVB PCIe Buffer Evaluation Board. The +5V required by the EVB can come from a powered USB connection (only +5V is required) or from an external +5V power supply.

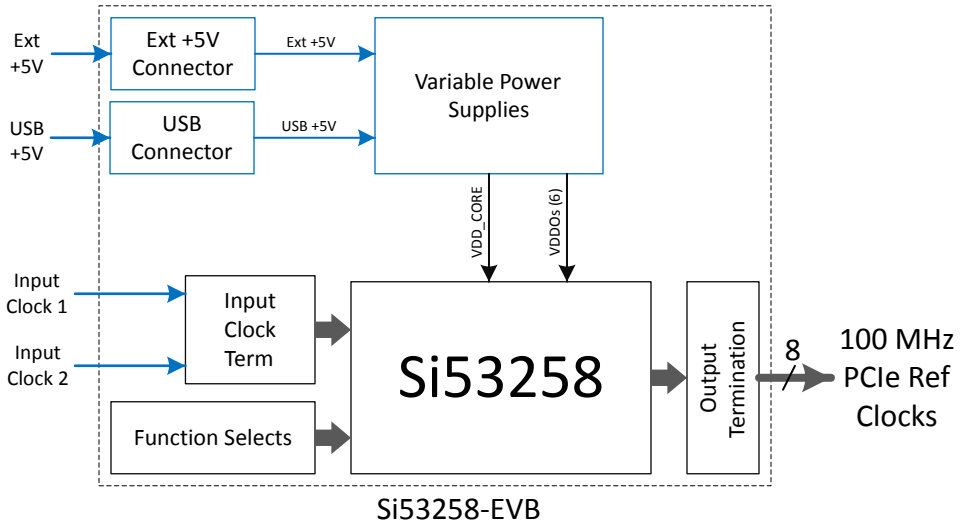


Figure 1.1. Si53258-EVB Functional Block Diagram

2. Si53258-EVB Operation

2.1 EVB Configuration: Switches & Jumpers

Power Supplies:

DIP switches SW1 – SW7 control the on-board power supplies. The table below is a guide to show how to select output voltages for each supply and the EVB default settings. Jumper JP1 selects the source of the +5V used by all the power supply regulators. JP1 jumper pin 1 to 2 selects USB as power source (default) and pin 2 to 3 selects external +5V source via J21 terminal block (refer to schematic).

Switch Position:		1	2	3	4	
DIP Switch #	Control Function	1.8V*	2.5V*	3.3V*	Enable	EVB Default
SW1	VDDO0	0	1	1	0	Enabled, +1.8V
SW2	VDDO1	0	1	1	0	Enabled, +1.8V
SW3	VDDO2	0	1	1	0	Enabled, +1.8V
SW4	VDDO3	0	1	1	0	Enabled, +1.8V
SW5	VDDO4	0	1	1	0	Enabled, +1.8V
SW6	VDDO5	0	1	1	0	Enabled, +1.8V
SW7	VDD_CORE	NC	1	1	0	Enabled, +1.8V

Note:
- 0 = Switch Position Closed (On)
- 1 = Switch Position Open (Off)

***Caution:** Only 1 voltage select switch position can be 0 (On) at a time. Do not set more than 1 position to On and only change switches with power OFF.

Output Enables, Input Clock Select, Impedance Select:

DIP switch SW8 is used to control the clock output enables, input clock selection, and output impedance control. There are 4 output enables (OE), one per output clock pair as shown. The input clock select control is 0 to select Input Clock 1, and 1 to select Input Clock 2. The output impedance select is 0 for 100 Ω and 1 for 85 Ω. The EVB default setting all outputs enabled, Clock 1 selected, and 85 Ω.

Switch Position:		1	2	3	4	5	6	7	8	
DIP Switch #	Control Function	OEb_ OUT1:0	OEb_ OUT3:2	OEb_ OUT5:4	OEb_ OUT7:6	NC	NC	CLK_ SEL	IMP_ SEL	EVB Default
SW8	Output Enables	0	0	0	0	–	–	–	–	All Enabled
	Clock Select	–	–	–	–	–	–	0	–	Input Clock 1
	Impedance	–	–	–	–	–	–	–	1	85 Ω

Note:
- 0 = Switch Position Closed (On)
- 1 = Switch Position Open (Off)

Location of DIP Switches:

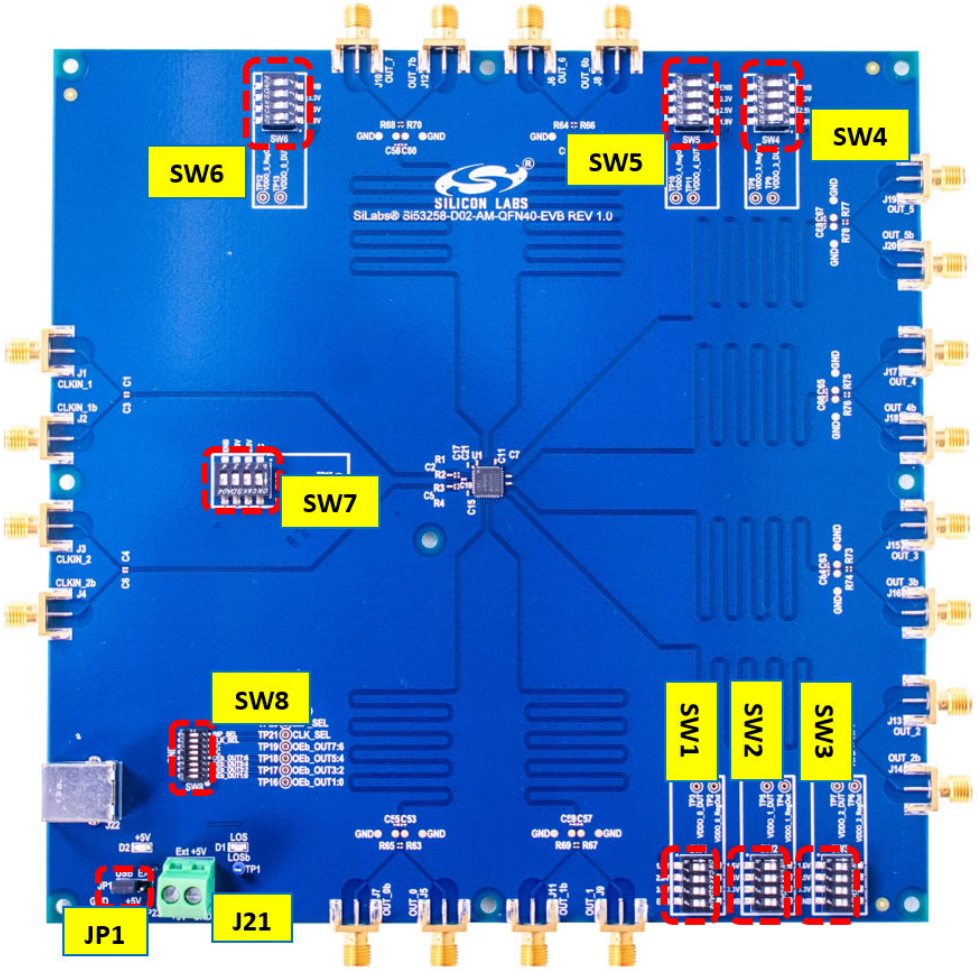


Figure 2.1. DIP Switches Location

3. LEDs

The Si53258-EVB has 2 LEDs defined below.

D2: **Blue LED** indicating +5V presence.

D3: **Red LED** indicating Loss of Signal (LOS). When lit, this LED indicates selected input clock is not present.

4. Output Clocks

The Si53258-EVB supports all 8 differential pair output clocks, each terminated as shown in the figure below. The EVB has locations to install 2 pf parallel termination capacitors if desired, which are tagged with “NI” in schematic to indicate they are not installed by default. The outputs are otherwise direct DC coupled to the SMA connectors. Convenient connection pads are also provided for measuring the output with a differential probe, in which case removal of the 0 Ω resistors to isolate the SMA “stub” from the transmission line is suggested.

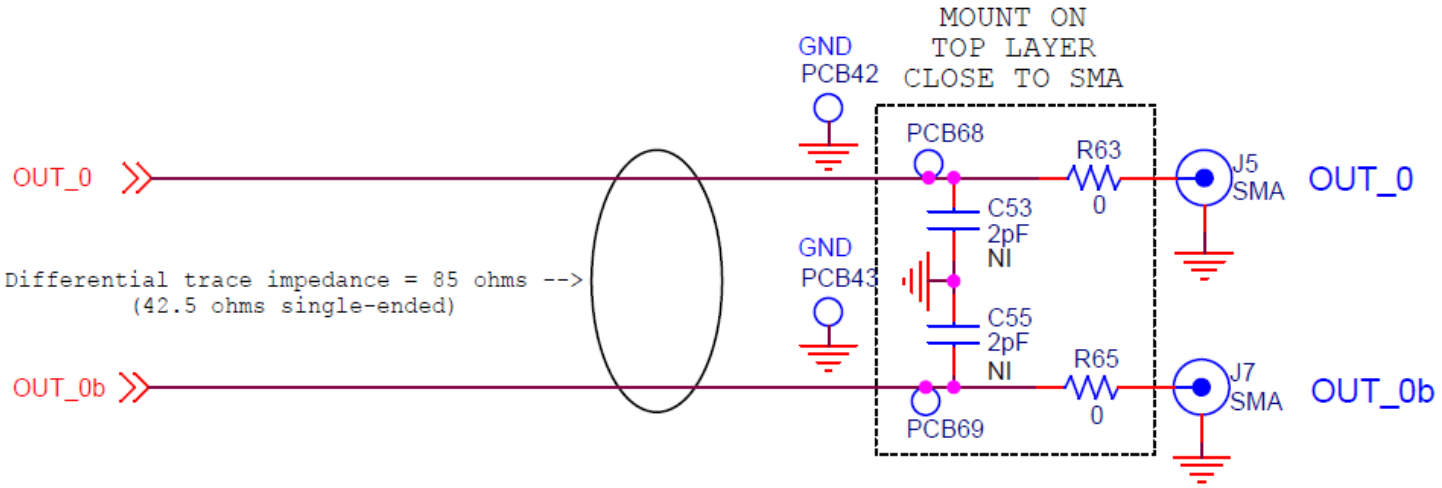


Figure 4.1. Si53258-EVB Output Clock Differential Pair Termination Circuit

5. Input Clocks

The Si53258-EVB supports 2 input clocks (selectable) with input termination as shown below. Each input pair is AC coupled through a 0.1uF capacitor with on-board 50 Ω AC termination from each leg to GND.

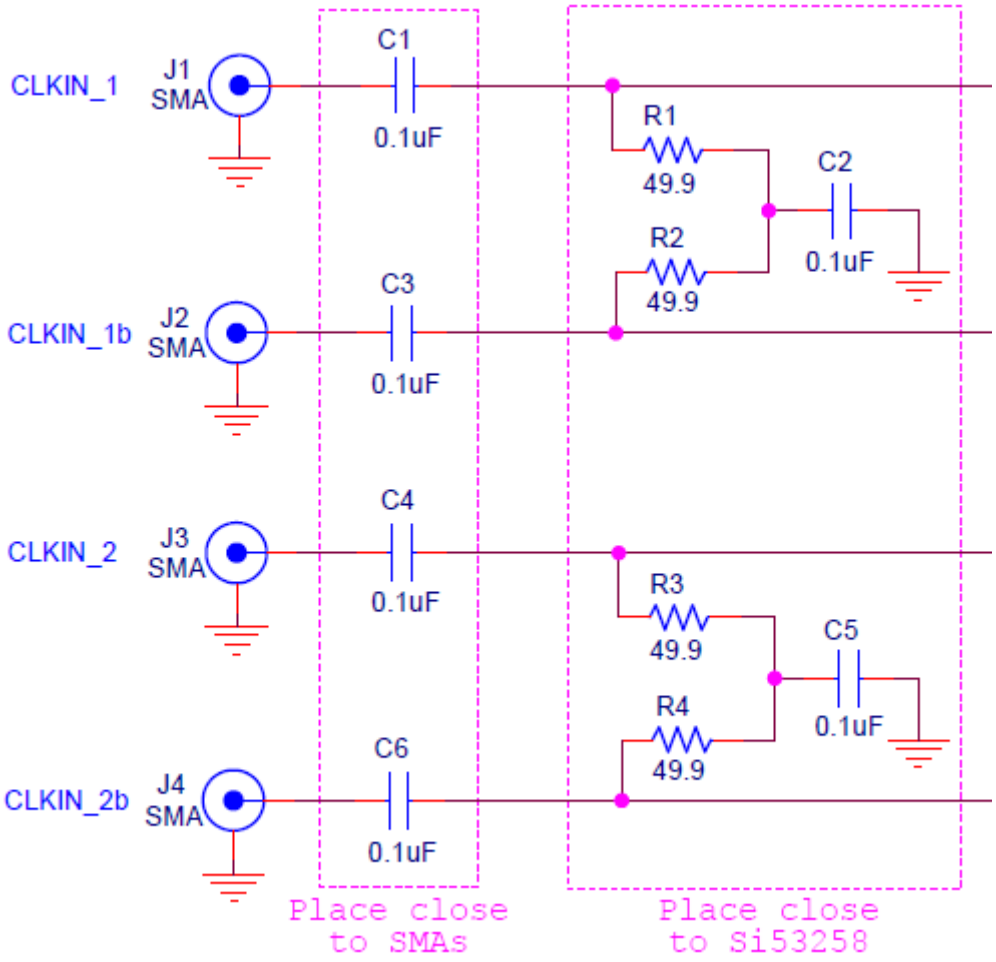
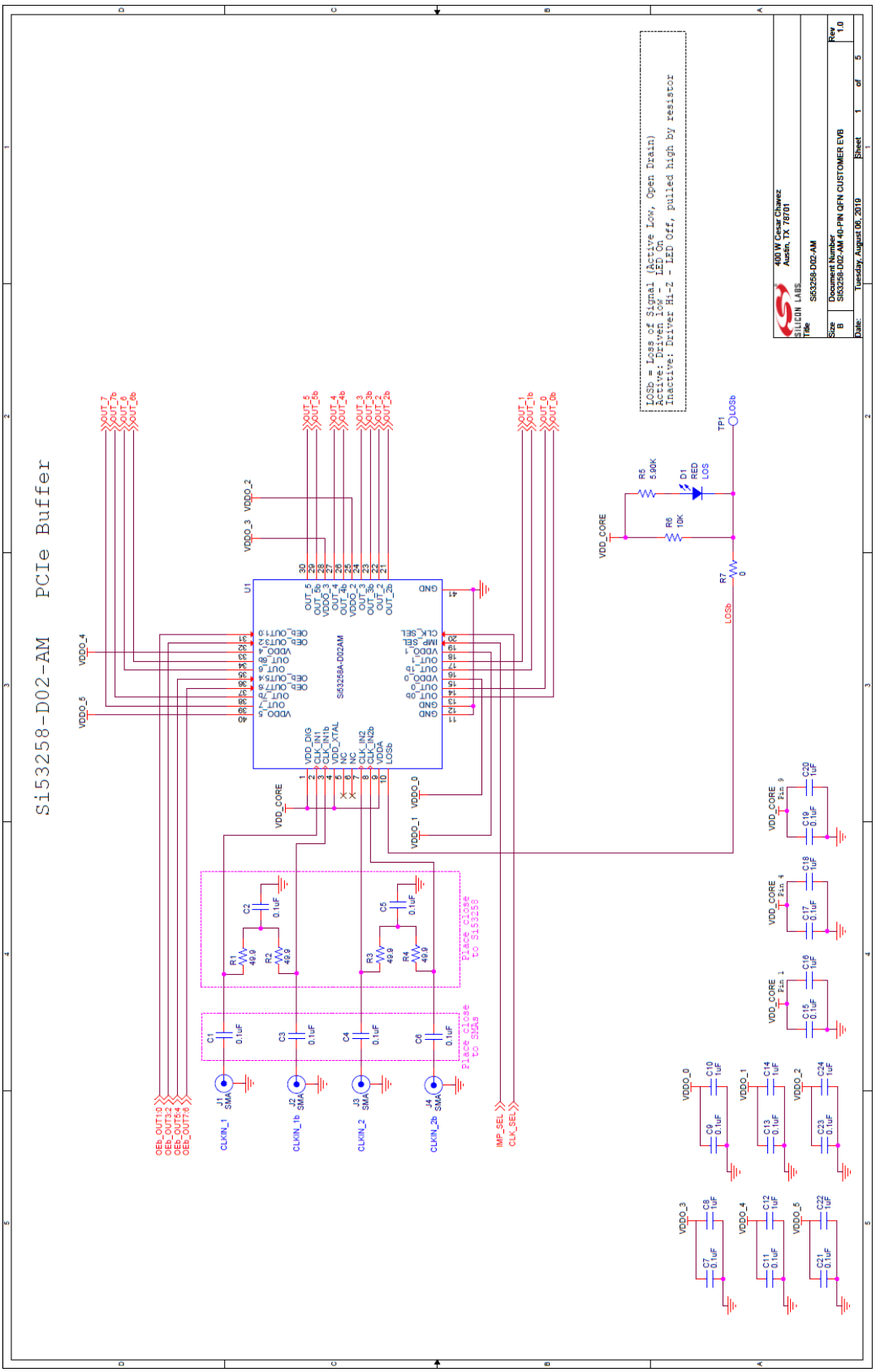
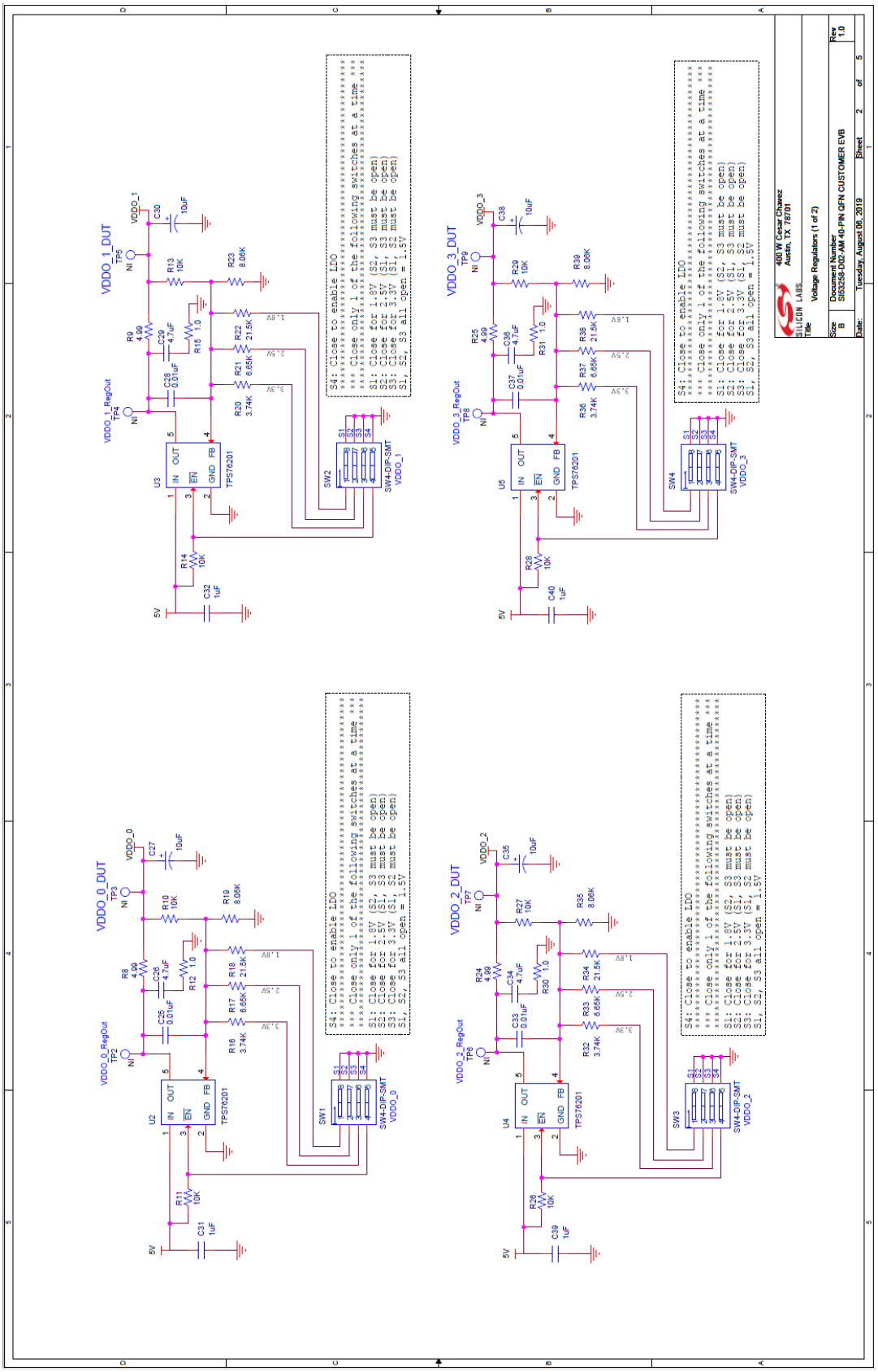


Figure 5.1. Si53258-EVB Input Clock Differential Pair Termination Circuit

6. Si53258-EVB Rev 1.0 Schematics




VDDO_1_DUT
VDDO_3_DUT
VDDO_0_DUT
VDDO_2_DUT
TPS76201
SW4-DIP-SMT
S4: Close to enable LDO
*** Close only 1 of the following switches at a time ***
S1: Close for 1.8V (S2, S3 must be open)
S2: Close for 2.5V (S1, S3 must be open)
S3: Close for 3.3V (S1, S2 must be open)
S1, S2, S3 all open = 1.5V
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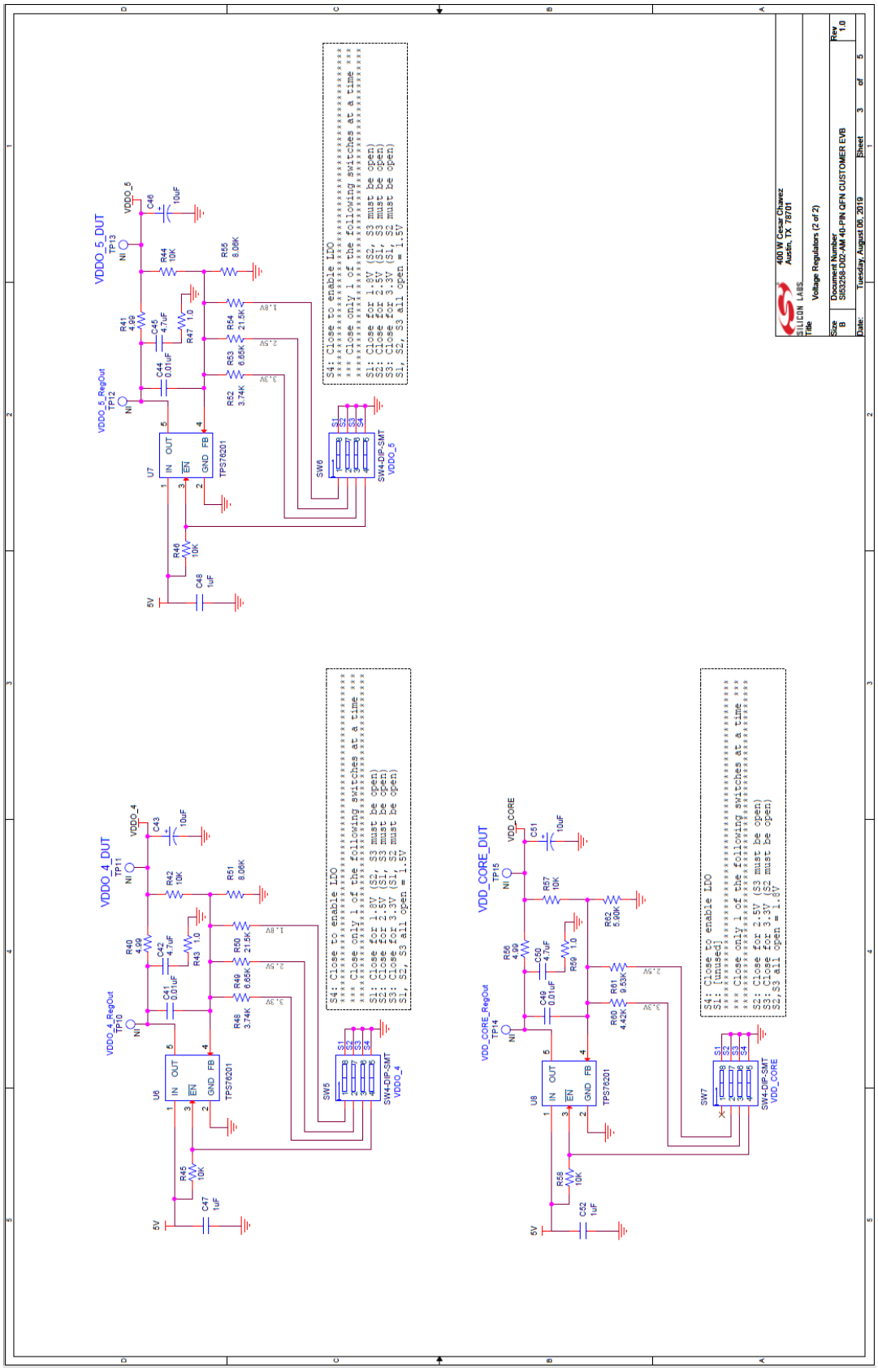
Voltage Regulators (1 of 2)
Document Number
SI53258-D02-AM 40-PIN QFN CUSTOMER EVB
Rev 1.0
Tuesday, August 06, 2019
Sheet 2 of 5


VDDO_5_DUT
VDDO_4_DUT
VDD_CORE_DUT
TPS76201
SW4-DIP-SMT
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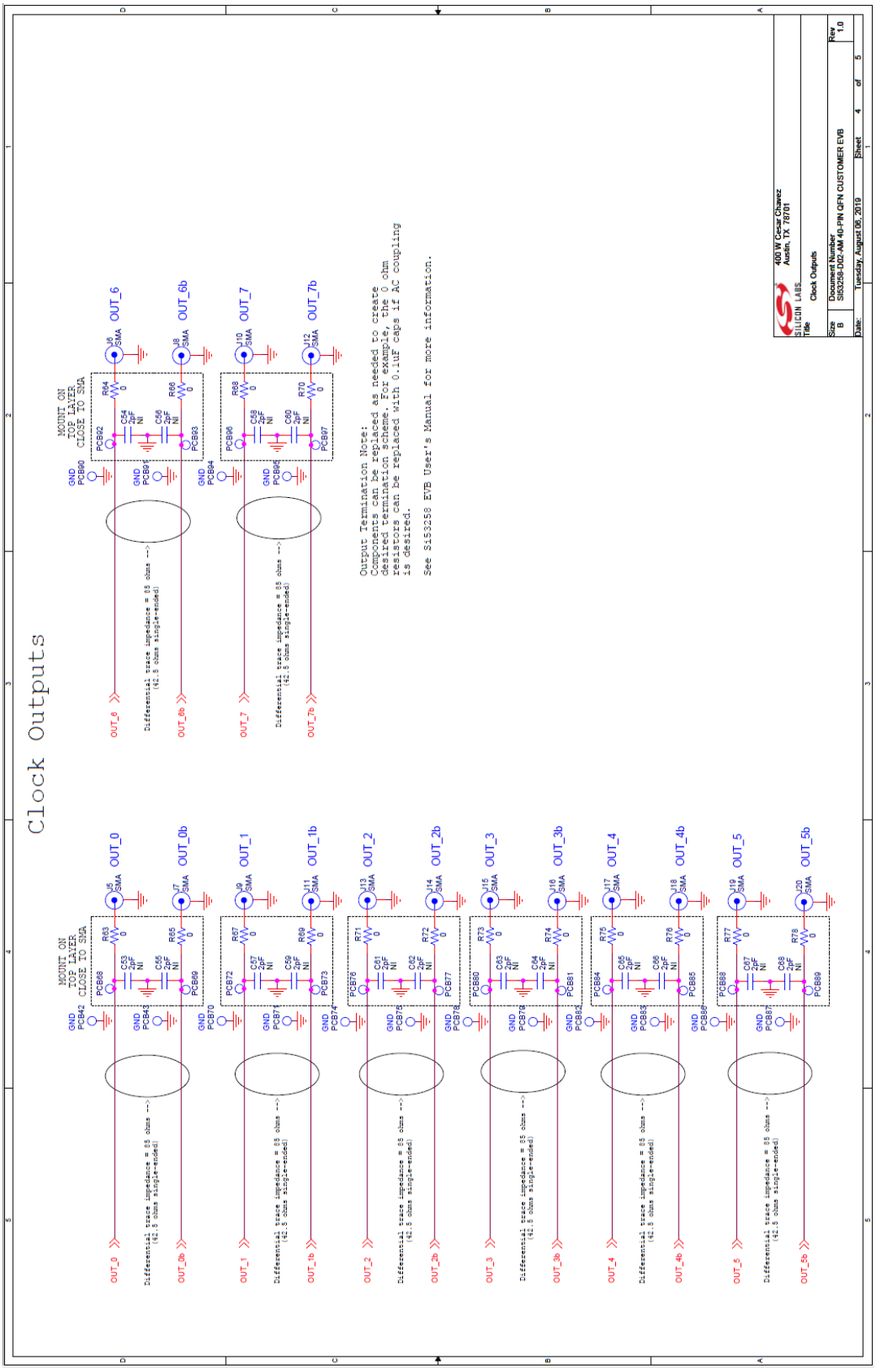
Voltage Regulators (2 of 2)
Si53258-D02-AM 40-PIN QFN CUSTOMER EVB
Tuesday, August 06, 2019


Clock Outputs
Output Termination Note:
Components can be replaced as needed to create
desired termination scheme. For example, the 0 ohm
resistors can be replaced with 0.1uF caps if AC coupling
is desired.
See Si53258 EVB User's Manual for more information.
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Clock Outputs
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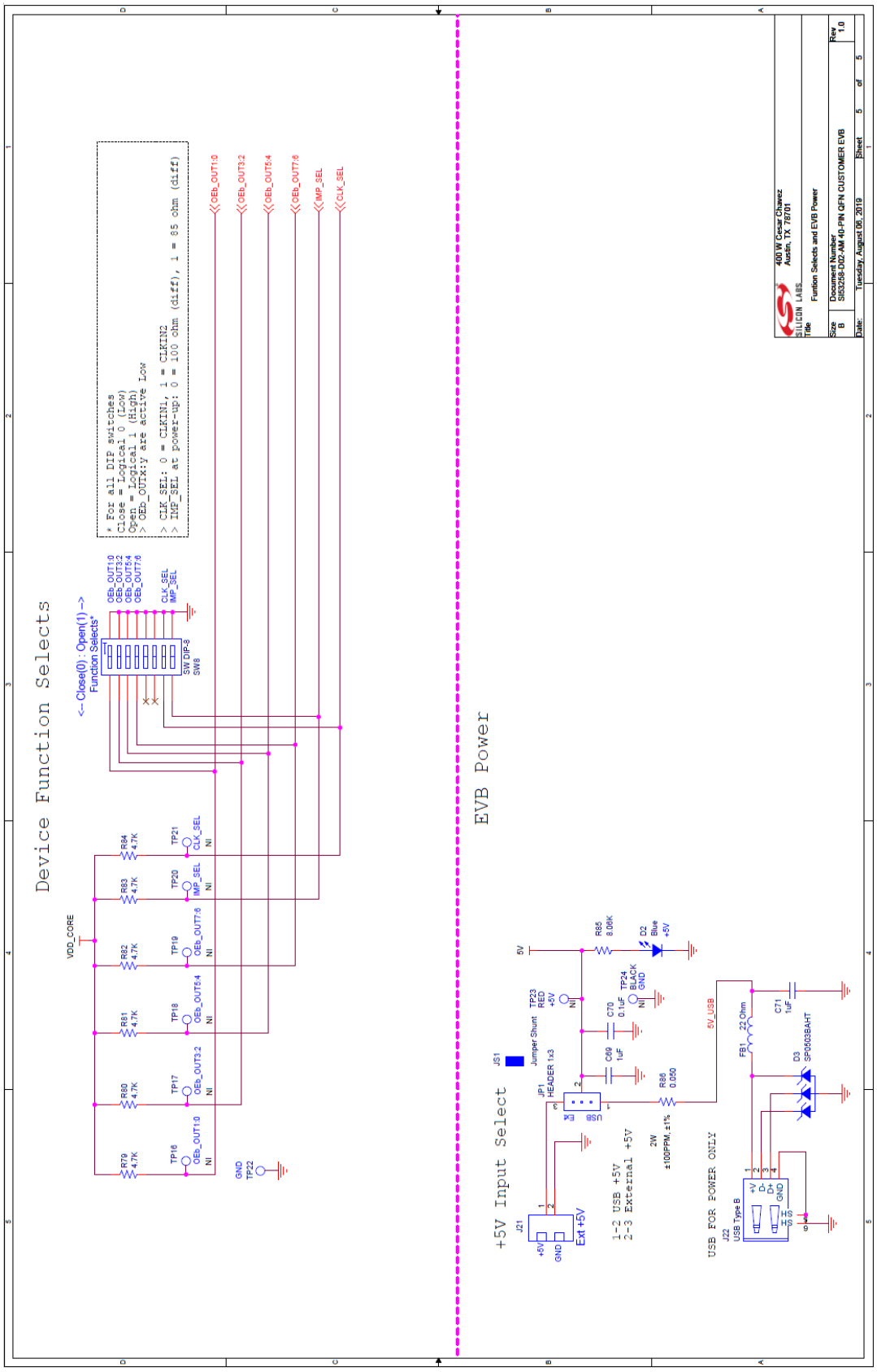
Device Function Selects
EVB Power
+5V Input Select
* For all DIP switches
Close = Logical 0 (Low)
Open = Logical 1 (High)
> OEb_OUTx:y are active Low
> CLK_SEL: 0 = CLKIN1, 1 = CLKIN2
> IMP_SEL at power-up: 0 = 100 ohm (diff), 1 = 85 ohm (diff)
<-- Close(0) : Open(1) -->
Function Selects
SW DIP-8
SW8
OEb_OUT1:0
OEb_OUT3:2
OEb_OUT5:4
OEb_OUT7:6
IMP_SEL
CLK_SEL
VDD_CORE
GND
5V
5V_USB
USB FOR POWER ONLY
1-2 USB +5V
2-3 External +5V
Ext +5V
USB Type B
Jumper Shunt
HEADER 1x3
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Funtion Selects and EVB Power
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