Si5381/82 Rev E Data Sheet

Multi-DSPLL Wireless Jitter Attenuator / Clock Multiplier with Ultra-Low Noise

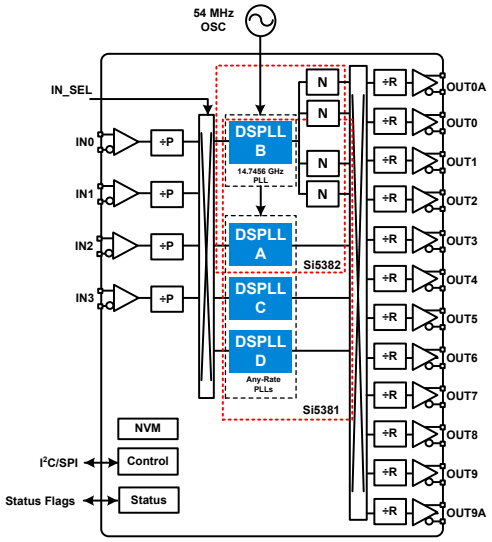
The Si5381/82 is an ultra high performance wireless jitter attenuator with multiple DSPLLs, optimized for wireless BBU (Baseband Unit) and DU (Distribution Unit) applications. The industry's first multi-PLL wireless jitter attenuator device is capable of replacing multiple discrete, high performance, VCXO-based jitter attenuators with a fully integrated single chip solution. The featured multi-PLL architecture supports timing paths for Ethernet and CPRI (Common Public Radio Interface) clock cleaning , and generates any low-jitter, general-purpose clocks. The fixed frequency oscillator provides frequency stability for free-run and holdover modes. This all-digital solution provides superior performance that is highly immune to external board disturbances such as power supply noise.

Applications:

- Wireless Infrastructure
  - eCPRI RRH (Remote Radio Head)
  - BBU (Baseband Unit)
  - DU (Distribution Unit)
- Test and Measurement

KEY FEATURES

- Supports simultaneous Ethernet, CPRI and general-purpose clocking in a single device
- Input frequency range:
  - Differential: 8 kHz - 750 MHz
  - LVCMOS: 8 kHz to 250 MHz
- Output frequency range:
  - CPRI: up to 2.94912 GHz
  - Other differential: up to 735 MHz
  - LVCMOS: up to 250 MHz
- Ultra-low RMS jitter:
  - 72 fs typ (12 kHz–20 MHz)
- Phase noise of 122.88MHz carrier frequency:
  - -118 dBc/Hz @ 100Hz offset
- ITU-T G.8262 compliant



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1. Features List

The Si5381/82 features are listed below:

- ITU-T G.8262 compliant
- Digital frequency synthesis eliminates external VCXO and analog loop filter components
  - DSPLL_B supports high-frequency, CPRI clocking. Remaining DSPLLs support Ethernet and general-purposing clocking
- Input frequency range:
  - Differential: 8 kHz to 750 MHz
  - LVCMOS: 8 kHz to 250 MHz
- Output frequency range:
  - CPRI: up to 2.94912 GHz with JESD204B support (DSPLL_B)
  - Other differential: up to 735 MHz (DSPLL_A/C/D)
  - LVCMOS: up to 250 MHz
- Ultra-low RMS jitter (12kHz - 20MHz):
  - 72 fs typ at 122.88 MHz (DSPLL_B)
  - 88 fs typ at 156.25 MHz (DSPLL_A/C/D)
  - 79 fs typ at 322.265625 MHz (DSPLL_A/C/D)
- Typical phase noise of 122.88 MHz carrier frequency (DSPLL_B):
  - -118 dBc/Hz @ 100 Hz offset
  - -133 dBc/Hz @ 1 kHz offset
  - -142 dBc/Hz @ 10 kHz offset
  - -149 dBc/Hz @ 100 kHz offset
  - -154 dBc/Hz @ 1 MHz offset
- Highly configurable outputs compatible with LVDS, LVPECL, LVCMOS, CML, and HCSL. CML outputs can be programmed to have 100-1600 mVpp single-ended swing.
- Status monitoring (LOS, OOF, LOL)
- Pin controlled input switching
- Optional zero delay mode
- Hitless input clock switching: automatic or manual
- Automatic free-run and holdover modes
- Fastlock feature
- Core voltage:
  - VDD: 1.8 V ±5%
  - VDDA: 3.3 V ±5%
- Independent output clock supply pins: 3.3 V, 2.5 V, or 1.8 V
- Output-output skew: 75 ps max
- Serial interface: I2C or SPI
- In-circuit programmable with non-volatile OTP memory
- ClockBuilder ProTM software simplifies device configuration
- Temperature range: –40 to +85 °C
- Pb-free, RoHS-6 compliant

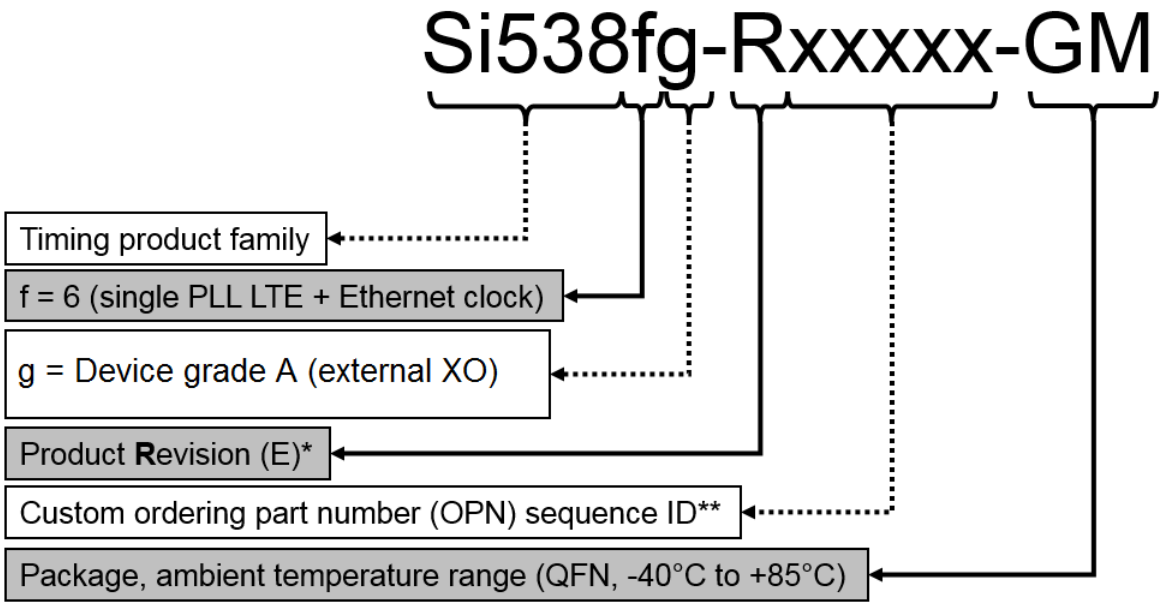
2. Ordering Guide

Table 2.1. Ordering Guide

Ordering Part Number	Reference	# DSPLL	Number of Clock Inputs/ Outputs	Maximum Output Frequency		Package	RoHS-6, Pb-Free	Temperature Range
				CPRI Clocks	Other Clocks			
Si5381A-E-GM	XO	4	4 / 12	2.94912 GHz	735 MHz	64-Lead 9x9 mm QFN	Yes	–40 to +85 °C
Si5382A-E-GM	XO	2	4 / 12	2.94912 GHz	735 MHz			
Si5381A-E-EVB	Evaluation Board							
Si5382A-E-EVB	Evaluation Board							

Note:

1. Add an “R” at the end of the device to denote tape and reel options.
2. Custom, factory pre-programmed devices are available. Ordering part numbers are assigned by ClockBuilder Pro. Part number format is: Si5381E-Exxxxx-GM, where “xxxxx” is a unique numerical sequence representing the pre-programmed configuration.



*See Ordering Guide table for current product revision.
** (Optional) 5 digits; assigned by ClockBuilder Pro for Custom, factory-preprogrammed OPN devices only;
(The “xxxxx” field is not included for “Base” OPNs).

Figure 2.1. Ordering Part Number Fields

3. Functional Description

The Si5381/82 integrates four/two any-frequency DSPLLs in a monolithic IC for applications that require a combination of CPRI, Ethernet, and general-purpose clocking. Any clock input can be routed to any DSPLL. The output of any DSPLL can be routed to any of the device clock outputs. Based on 4th generation DSPLL technology, the Si5381/82 provides a clock-tree-on-a-chip solution for applications that need a mix of different clock frequencies. DSPLL B acts as the high-frequency DSPLL, typically used for CPRI clocks while DSPLLs A/C/D act as Ethernet and general purpose DSPLLs.

As shown in the figure below, the DSPLL_B of Si5381/82 is locked to it's reference input. The output is then supplied to DSPLLs A/C/D. The benefit is a more efficient and cost effective, lower-jitter yet frequency flexible clock-tree in a chip architecture. However, it should be noted that large transients or loss of lock on DSPLL_B could have some minor impact on DSPLLs A/C/D.

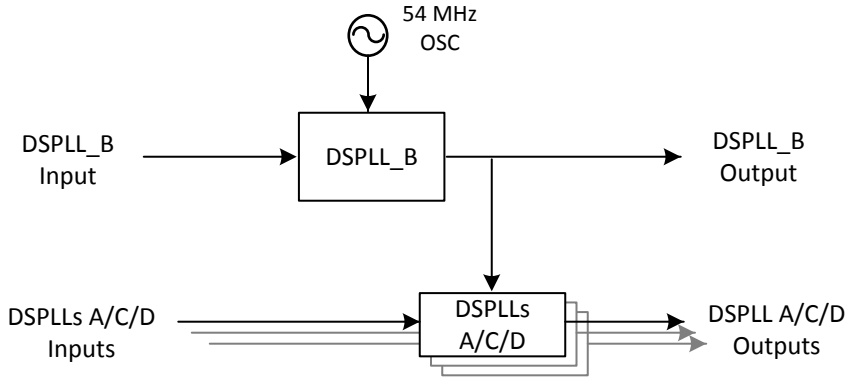


Figure 3.1. High-frequency DSPLL

3.1 Frequency Configuration

The frequency configuration for each of the DSPLLs is programmable through the serial interface and can also be stored in non-volatile memory. DSPLL_B is optimized for CPRI frequency, but can generate any other frequency as well. For DSPLL_A/C/D, fractional frequency multiplication (Mn/Md) allows each of the DSPLLs to lock to any input frequency and generate virtually any output frequency. However, DSPLL_A,C,D are not recommended to generate CPRI clocks as the performance is not as good as when using DSPLL_B. All divider values for a specific frequency plan are easily determined using the ClockBuilder Pro utility. The Si5382 supports one Ethernet or general-purpose DSPLL (DSPLL_A).

3.1.1 Si5381/82 CPRI Frequency Configuration

The combination of flexible integer dividers and a high frequency VCO allows the device to generate multiple output clock frequencies for applications that require ultra-low phase noise and spurious performance. The table below shows a list of possible output frequencies for wireless applications. Note that these CPRI frequencies may be generated with an Ethernet input clock to DSPLL_B. These frequencies are distributed to the output dividers using a configurable crosspoint mux. The R dividers allow further division for up to 10 unique integer-ratio related frequencies on the Si5381/82. The ClockBuilder Pro software utility provides a simple means of automatically calculating the optimum divider values (P, M, N and R) for the frequencies listed in the table below.

Table 3.1. Example of Possible Wireless Clock Frequencies

Device Clock Frequencies Fout (MHz)
15.36
19.20
30.72
38.40
61.44
76.80
122.88
153.60

Device Clock Frequencies Fout (MHz)
184.32
245.76
307.20
368.64
491.52
614.40
737.28
983.04
1228.80
1474.56
2949.12

3.1.2 Si5381/82 Configuration for Wireless Clock Generation

The Si5381/82 can be used as a high performance, fully integrated wireless jitter cleaner while eliminating the need for discrete VCXO and loop filter components. The Si5381/82 supports JESD204B subclass 0 and subclass 1 clocking by providing both device clocks (DCLK) and system reference clocks (SYSREF). The clock outputs can be independently configured as device clocks or SYSREF clocks to drive JESD204B converters, FPGAs, or other logic devices. An example frequency configuration is shown in the figure below. In this case, N and R dividers determine both device and sysref frequencies. The SYSREF clock is always periodic and can be controlled (on/off) without glitches by enabling or disabling its output through register writes.

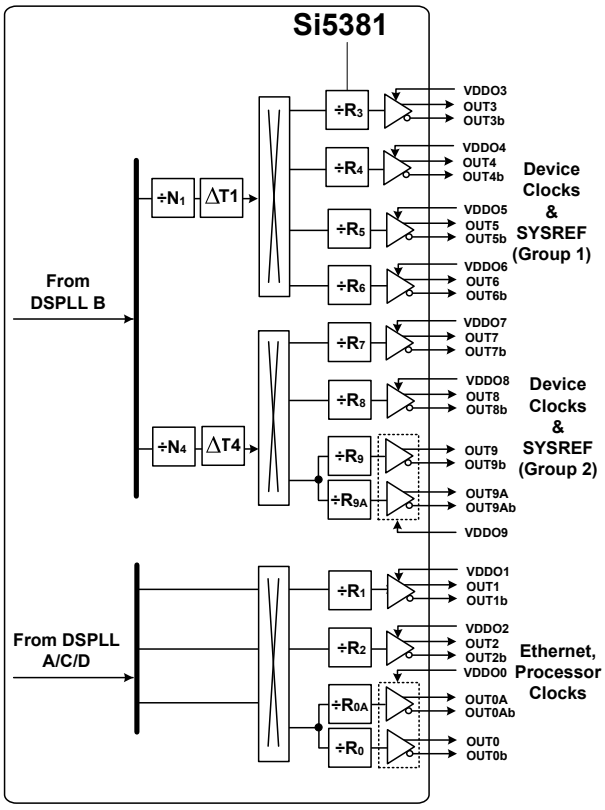


Figure 3.2. Example Divider Configuration for Generating JESD204B Subclass 1 Clocks

3.2 DSPLL Loop Bandwidth

The DSPLL loop bandwidth determines the amount of input clock jitter attenuation. Register configurable DSPLL loop bandwidth settings in the range of 20 Hz to 4 kHz are available for DSPLLB and in the range of 1 Hz to 4 kHz for DSPLLA/C/D. Since the loop bandwidth is controlled digitally, the DSPLL will always remain stable with less than 0.1 dB of peaking regardless of the loop bandwidth selection.

3.3 Fastlock Feature

Selecting a low DSPLL loop bandwidth (e.g., 1 Hz) will generally lengthen the lock acquisition time. The fastlock feature allows setting a temporary Fastlock Loop Bandwidth that is used during the lock acquisition process. Higher fastlock loop bandwidth settings will enable the DSPLLs to lock faster. Fastlock Loop Bandwidth settings of in the range of 100 Hz to 4 kHz are available for selection. The DSPLL will revert to its normal loop bandwidth once lock acquisition has completed.

3.4 Modes of Operation

Once initialization is complete the DSPLL operates in one of five modes: Free-run Mode, VCO Freeze Mode, Lock Acquisition Mode, Locked Mode, or Holdover Mode. A state diagram showing the modes of operation is shown in Figure 3.3 Modes of Operation on page 8. The following sections describe each of these modes in greater detail.

3.4.1 Initialization and Reset

Once power is applied, the device begins an initialization period where it downloads default register values and configuration data from NVM and performs other initialization tasks. Communicating with the device through the serial interface is possible once this initialization period is complete. No clocks are generated until the initialization is complete. There are two types of resets available. A hard reset is functionally similar to a device power-up. All registers are restored to the values stored in NVM, and all circuits including the serial interface is restored to their initial state. A hard reset is initiated using the RSTb pin or by asserting the hard reset register bit. A soft reset bypasses the NVM download. It is simply used to initiate register configuration changes.

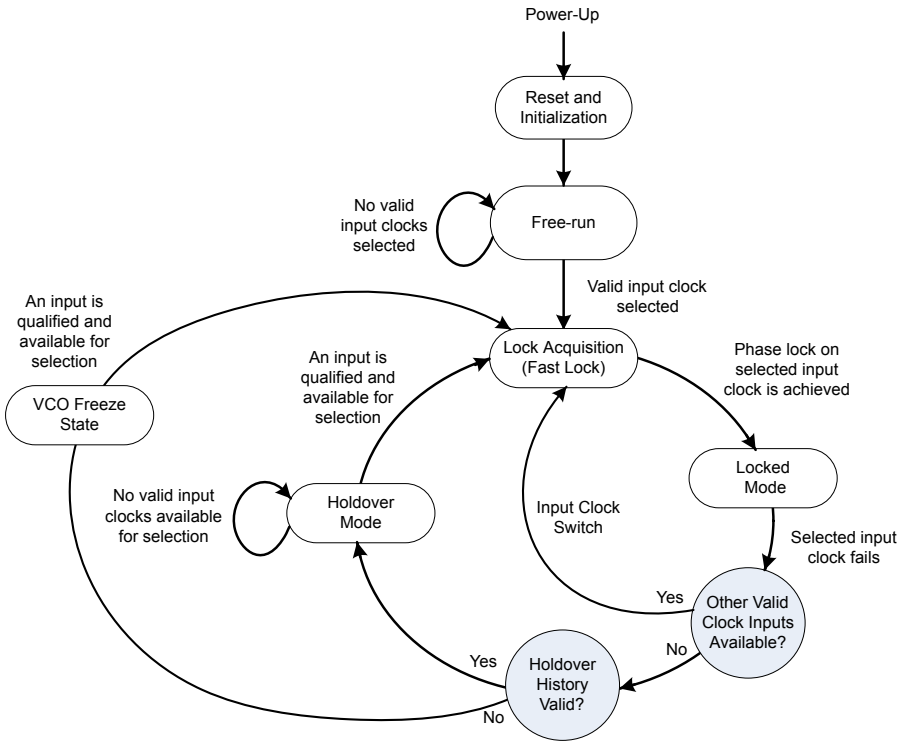


Figure 3.3. Modes of Operation

3.4.2 Freerun Mode

The DSPLL will automatically enter freerun mode once power is applied to the device and initialization is complete. The frequency accuracy of the generated output clocks in freerun mode is entirely dependent on the frequency accuracy of the reference clock on the XA/XB pins. For example, if the oscillator stability is ±50 ppm, then all the output clocks will be generated at their configured frequency with ±50 ppm stability in freerun mode. Any drift of the oscillator frequency is tracked at the output clock frequencies. Free run mode is maintained as long as no input clocks are valid.

3.4.3 Lock Acquisition Mode

The device monitors all inputs for a valid clock. If at least one valid clock is available for synchronization, the DSPLL automatically starts the lock acquisition process. If the fast lock feature is enabled, the DSPLL acquires lock using the Fastlock Loop Bandwidth setting and then transition to the DSPLL Loop Bandwidth setting when lock acquisition is complete. During lock acquisition, the output generates a clock that follows the VCO frequency change as it pulls in to the input clock frequency.

3.4.4 Locked Mode

Once locked, the DSPLL generates output clocks that are both frequency and phase locked to their selected input clocks. At this point, any oscillator frequency drift does not affect the output frequency. A loss of lock pin (LOL) and status bit indicate when lock is achieved. See 3.7.4 LOL Detection for more details on the operation of the loss-of-lock circuit.

3.4.5 Holdover Mode

If holdover history is valid, the DSPLL automatically enters holdover mode when the selected input clock becomes invalid and no other valid input clocks are available for selection. The DSPLL uses an averaged input clock frequency as its final holdover frequency to minimize the disturbance of the output clock phase and frequency when an input clock suddenly fails. The holdover circuit for the DSPLL stores up to 120 seconds of historical frequency data while locked to a valid clock input. The final averaged holdover frequency value is calculated from a programmable window within the stored historical frequency data. Both the window size and the delay are programmable as shown in the figure below. The window size determines the amount of holdover frequency averaging. The delay value allows ignoring frequency data that may be corrupt just before the input clock failure.

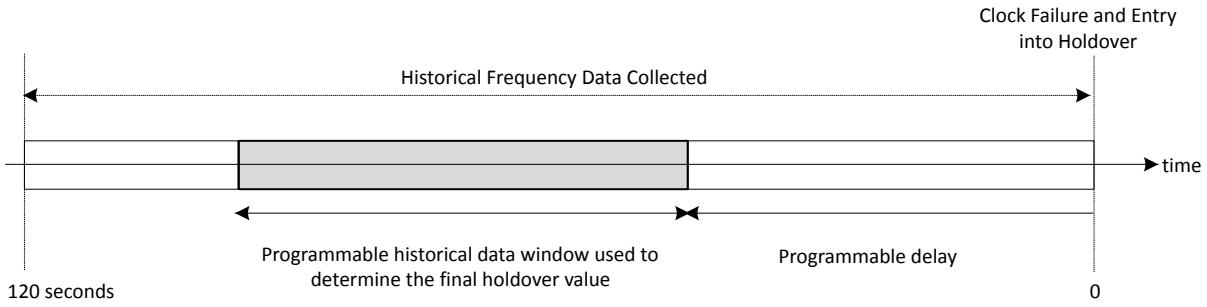


Figure 3.4. Programmable Holdover Window

When entering holdover, the DSPLL pulls its output clock frequency to the calculated averaged holdover frequency. While in holdover, the output frequency drift is entirely dependent on the external reference clock connected to the XA/XB pins. If the clock input becomes valid, the DSPLL automatically exits the holdover mode and re-acquires lock to the new input clock. This process involves pulling the output clock frequency to achieve frequency and phase lock with the input clock. This pull-in process is glitchless and its rate is controlled by the DSPLL or the Fastlock bandwidth.

The DSPLL output frequency when exiting holdover can be ramped (recommended). Just before the exit is initiated, the difference between the current holdover frequency and the new desired frequency is measured. Using the calculated difference and a user-selectable ramp rate, the output is linearly ramped to the new frequency. The ramp rate can be 0.2 ppm/s, 40,000 ppm/s, or any of about 40 values in between. The DSPLL loop BW does not limit or affect ramp rate selections (and vice versa). CBPro defaults to ramped exit from holdover. The same ramp rate settings are used for both exit from holdover and ramped input switching. For more information on ramped input switching, see 3.6.4 Ramped Input Switching.

Note: If ramped holdover exit is not selected, the holdover exit is governed either by (1) the DSPLL loop BW or (2) a user-selectable holdover exit BW.

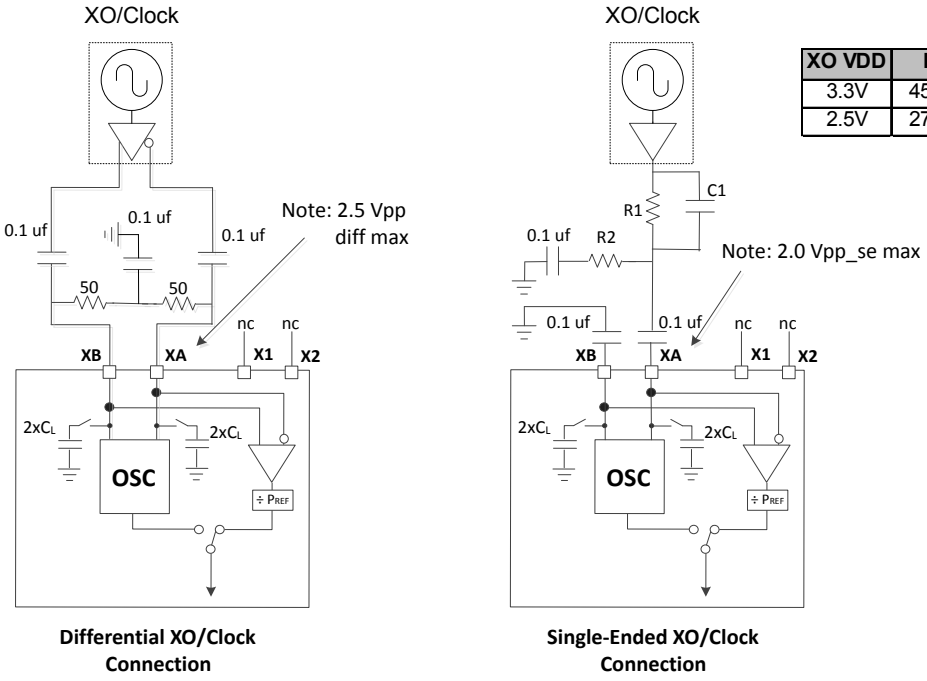
3.4.6 VCO Freeze Mode

If there are no valid clock inputs available for selection and the holdover history is not valid, the DSPLL automatically enters VCO Freeze mode. The DSPLL uses the last measured input frequency to set the output frequencies in VCO Freeze mode. If a valid input clock appears, the DSPLL automatically exits VCO Freeze mode and reacquires a lock to the new input clock.

3.5 External Reference (XA/XB)

An external crystal oscillator (XO) is required to set the reference for the Si5381/82. Only a 54 MHz XO is used as the reference to the wireless jitter attenuator. For the jitter and phase noise performance that is specified in this data sheet, only the recommended 54 MHz XO's specified for the Si5380/81/82/86 can be used in the Si534x/8x Jitter Attenuators Recommended Crystal, TCXO and OCXOs Reference Manual.

Place the XO as close to the XaXb pins as possible. See figure below for guidelines on how to connect the XO to the XaXb input. C1 increases the slew rate to the Xa input, which is needed to get the jitter and phase noise performance that is specifed in this data sheet.



XO VDD	R1	R2	C1	Appro. Vpp @ XA Input
3.3V	453 Ω	549 Ω	12 pf	1.8V
2.5V	274 Ω	732 Ω	30 pf	1.8V

Figure 3.5. XA/XB Input

3.6 Inputs (IN0, IN1, IN2, IN3)

There are four inputs that can be used to synchronize any of the DSPLLs. The inputs accept both differential and single-ended clocks. A crosspoint between the inputs and the DSPLLs allows any of the inputs to connect to any of the DSPLLs as shown in the figure below. See the Si5381/82 Rev E Family Reference Manual for details of input configuration and termination.

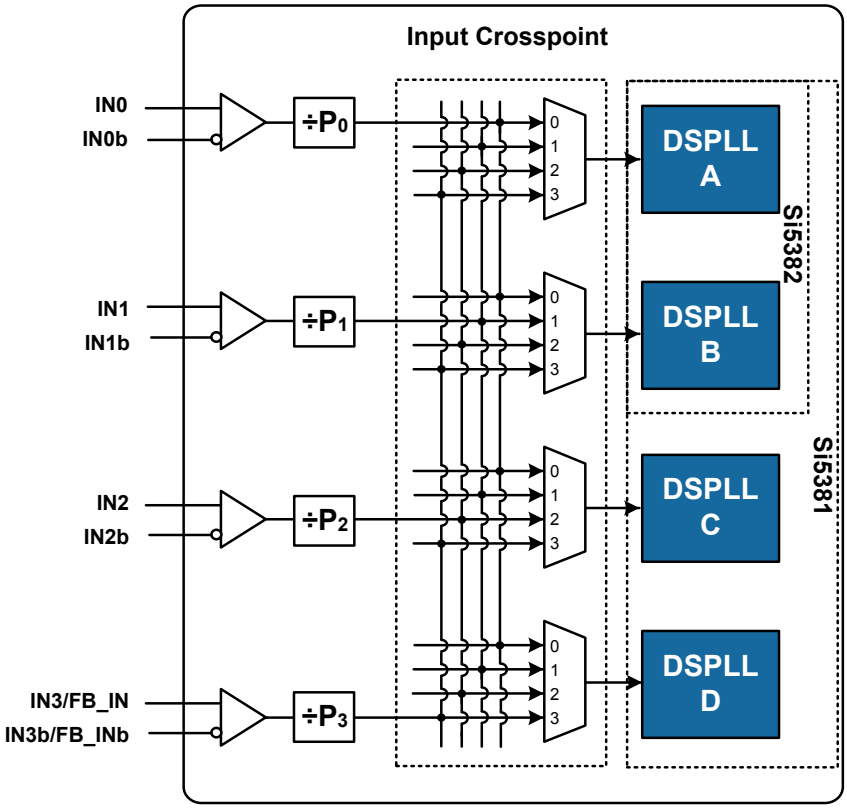


Figure 3.6. DSPLL Input Selection Crosspoint

3.6.1 Manual Input Switching (IN0, IN1, IN2, IN3)

Input clock selection can be made manually using the IN_SEL[1:0] pins or through a register. A register bit determines input selection as pin selectable or register selectable. The IN_SEL pins are selected by default. If there is no clock signal on the selected input, the device automatically enters free-run or holdover mode. When the zero delay mode is enabled, IN3 becomes the feedback input (FB_IN) and is not available for selection as a clock input.

Table 3.2. Manual Input Selection Using IN_SEL[1:0] Pins

IN_SEL[1:0]		Selected Input	
		Zero Delay Mode Disabled	Zero Delay Mode Enabled
0	0	IN0	IN0
0	1	IN1	IN1
1	0	IN2	IN2
1	1	IN3	Reserved

3.6.2 Automatic Input Selection (IN0, IN1, IN2, IN3)

An automatic input selection state machine is available in addition to the manual switching option. In automatic mode, the selection criteria is based on input clock qualification, input priority, and the revertive option. Only input clocks that are valid can be selected by the automatic clock selection state machine. If there are no valid input clocks available the DSPLL will enter the holdover mode. With revertive switching enabled, the highest priority input with a valid input clock is always selected. If an input with a higher priority becomes valid then an automatic switchover to that input is initiated. With non-revertive switching, the active input always remains selected while it is valid. If it becomes invalid an automatic switchover to a valid input with the highest priority is initiated.

3.6.3 Hitless Input Switching

Hitless switching is a feature that prevents a phase offset from propagating to the output when switching between two clock inputs that have a fixed phase relationship. A hitless switch can only occur when the two input frequencies are frequency locked meaning that they have to be exactly at the same frequency, or at a fractional frequency relationship to each other. When hitless switching is enabled, the DSPLL simply absorbs the phase difference between the two input clocks during a input switch. When disabled, the phase difference between the two inputs is propagated to the output at a rate determined by the DSPLL Loop Bandwidth. The hitless switching feature supports clock frequencies down to the minimum input frequency of 7.68 MHz.

3.6.4 Ramped Input Switching

When switching between two plesiochronous input clocks (i.e., the frequencies are "almost the same" but not quite), ramped input switching should be enabled to ensure a smooth transition between the two inputs. Ramped input switching avoids frequency transients and overshoot when switching between frequencies and so is the default switching mode in CBPro. The feature should be turned off when switching between input clocks that are always frequency locked (i.e., are always the same exact frequency). The same ramp rate settings are used for both holdover exit and clock switching. For more information on ramped exit from holdover see 3.4.5 Holdover Mode.

3.6.5 Glitchless Input Switching

The DSPLL has the ability of switching between two input clock frequencies that are up to 40 ppm apart. The DSPLL will pull-in to the new frequency using the DSPLL Loop Bandwidth or using the Fastlock Loop Bandwidth if enabled. The loss of lock (LOL) indicator will assert while the DSPLL is pulling-in to the new clock frequency. There will be no abrupt phase change at the output during the transition.

3.7 Fault Monitoring

All four input clocks (IN0, IN1, IN2, IN3/FB_IN) are monitored for loss of signal (LOS) and out-of-frequency (OOF) as shown in the figure below. The reference at the XA/XB pins is also monitored for LOS since it provides a critical reference clock for the DSPLLs. There is also a Loss Of Lock (LOL) indicator which is asserted when the DSPLL loses synchronization.

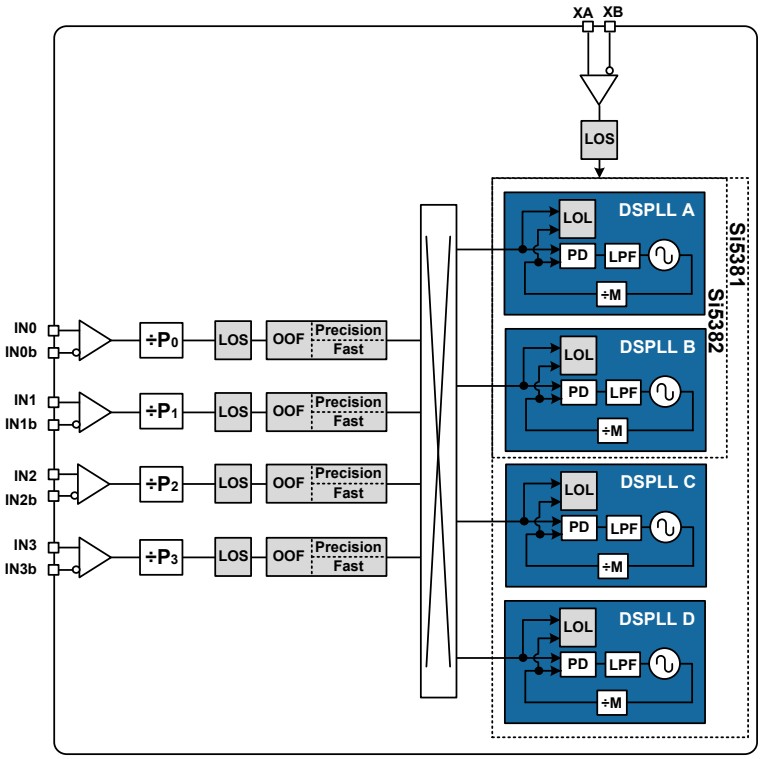


Figure 3.7. Si5381/82 Fault Monitors

3.7.1 Input LOS Detection

The loss of signal monitor measures the period of each input clock cycle to detect phase irregularities or missing clock edges. Each of the input LOS circuits has its own programmable sensitivity which allows ignoring missing edges or intermittent errors. Loss of signal sensitivity is configurable using the ClockBuilder Pro utility.

The LOS status for each of the monitors is accessible by reading a status register. The live LOS register always displays the current LOS state and a sticky register always stays asserted until cleared. An option to disable any of the LOS monitors is also available.

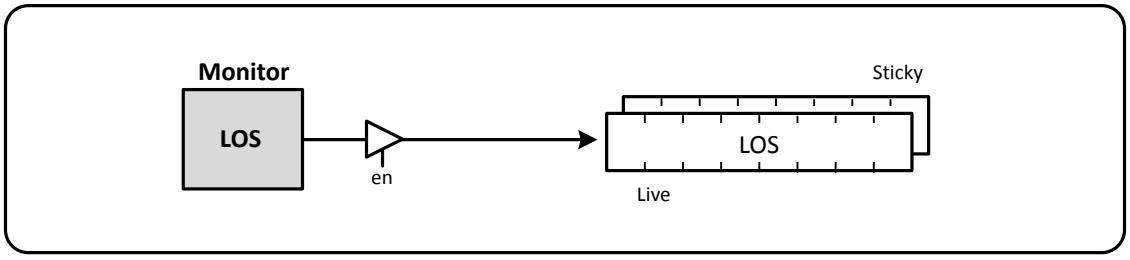


Figure 3.8. LOS Status Indicators

3.7.2 Reference Clock LOS Detection

A LOS monitor is available to ensure that the external reference oscillator is valid. By default the output clocks are disabled when XAXB_LOS is detected. This feature can be disabled such that the device will continue to produce output clocks when XAXB_LOS is detected.

3.7.3 OOF Detection

Each input clock is monitored for frequency accuracy with respect to a OOF reference which it considers as its “0_ppm” reference. This OOF reference can be selected as either:

- The XA/XB reference
- Any input clock (IN0, IN1, IN2, IN3)

The final OOF status is determined by the combination of both a precise OOF monitor and a fast OOF monitor as shown in the figure below. An option to disable either monitor is also available. The live OOF register always displays the current OOF state, and its sticky register bit stays asserted until cleared.

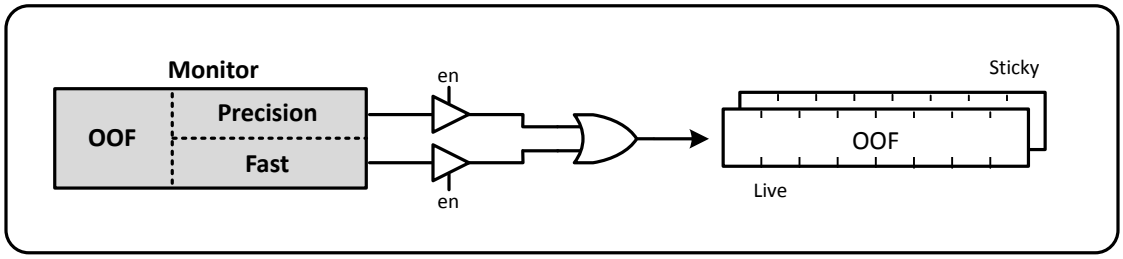


Figure 3.9. OOF Status Indicator

3.7.3.1 Precision OOF Monitor

The precision OOF monitor circuit measures the frequency of all input clocks to within ±1 ppm accuracy with respect to the selected OOF frequency reference. A valid input clock frequency is one that remains within the OOF frequency range which is register configurable up to 511 ppm in steps of 1/16 ppm. If the Xa input is chosen as the OOF reference frequency, then the minimum OOF assert threshold should be 60 ppm because the XO at the Xa input has a worst case tolerance of ±50 ppm. A configurable amount of hysteresis is also available to prevent the OOF status from toggling at the failure boundary. An example is shown in the figure below. In this case, the OOF monitor is configured with a valid frequency range of ±6 ppm and with 2 ppm of hysteresis. An option to use one of the input pins (IN0–IN3) as the 0 ppm OOF reference instead of the external XO reference is available. This option is register configurable.

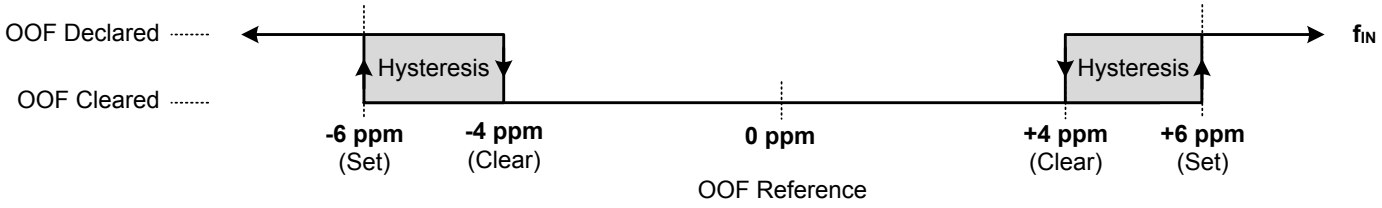


Figure 3.10. Example of Precise OOF Monitor Assertion and Deassertion Triggers

3.7.3.2 Fast OOF Monitor

Because the precision OOF monitor needs to provide 1/16 ppm of frequency measurement accuracy, it must measure the monitored input clock frequencies over a relatively long period of time. This may be too slow to detect an input clock that is quickly ramping in frequency. An additional level of OOF monitoring called the Fast OOF monitor runs in parallel with the precision OOF monitors to quickly detect a ramping input frequency. The Fast OOF monitor asserts OOF on an input clock when its input frequency is in error by ±1000 to ±16,000 ppm. This threshold can be configured by CBPro.

3.7.4 LOL Detection

The Loss Of Lock (LOL) monitor asserts a LOL register bit when the DSPLL has lost synchronization with its selected input clock.

There is also a dedicated loss of lock pin that reflects the loss of lock condition. The LOL monitor functions by measuring the frequency difference between the input and feedback clocks at the phase detector. There are two LOL frequency monitors, one that sets the LOL indicator (LOL Set) and another that clears the indicator (LOL Clear). An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely lock to the input clock. The timer is also useful to prevent the LOL indicator from toggling or chattering as the DSPLL completes lock acquisition. A block diagram of the LOL monitor is shown in the figure below. The live LOL register always displays the current LOL state and a sticky register always stays asserted until cleared. The LOL pin reflects the current state of the LOL monitor.

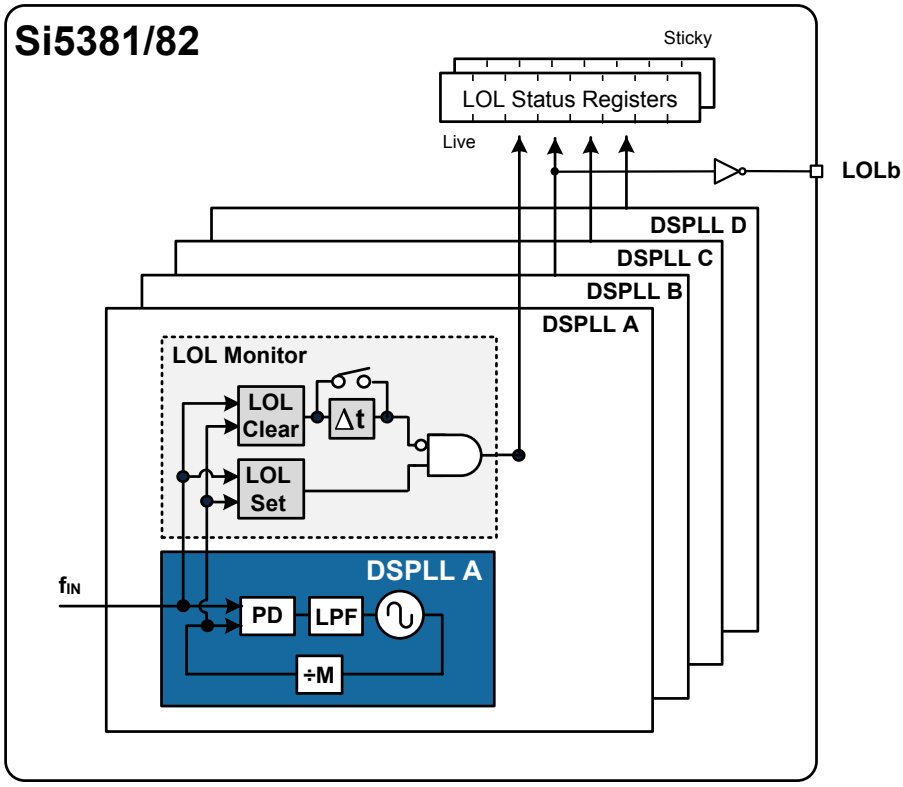


Figure 3.11. LOL Status Indicators

Each of the LOL frequency monitors has an adjustable sensitivity which is register configurable from 0.1 ppm to 10,000 ppm. Having two separate frequency monitors allows for hysteresis to help prevent chattering of LOL status.

An example configuration where LOCK is indicated when there is less than 0.1 ppm frequency difference at the inputs of the phase detector and LOL is indicated when there's more than 1 ppm frequency difference is shown in the following figure.

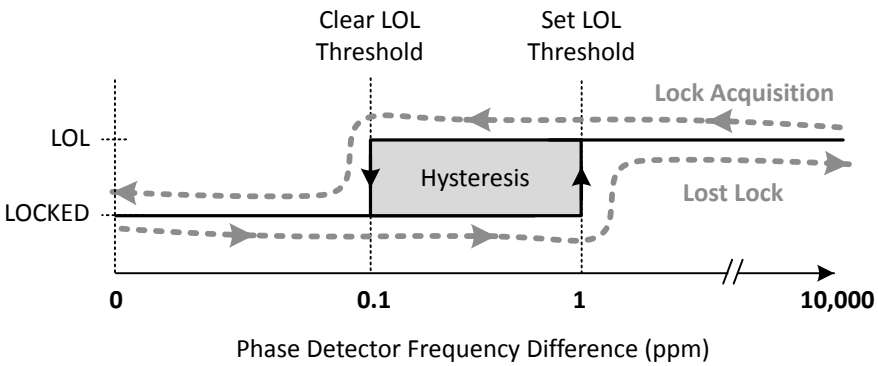


Figure 3.12. LOL Set and Clear Thresholds

Note: In this document, the terms, LVDS and LVPECL, refer to driver formats that are compatible with these signaling standards.

An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely lock to the input clock. The timer is also useful to prevent the LOL indicator from toggling or chattering as the DSPLL completes lock acquisition. The configurable delay value depends on frequency configuration and loop bandwidth of the DSPLL and is automatically calculated using the ClockBuilder Pro utility.

3.7.5 Interrupt Pin (INTRb)

An interrupt pin (INTRb) indicates a change in state with any of the status indicators for any of the DSPLLs. All status indicators are maskable to prevent assertion of the interrupt pin. The state of the INTRb pin is reset by clearing the sticky status registers.

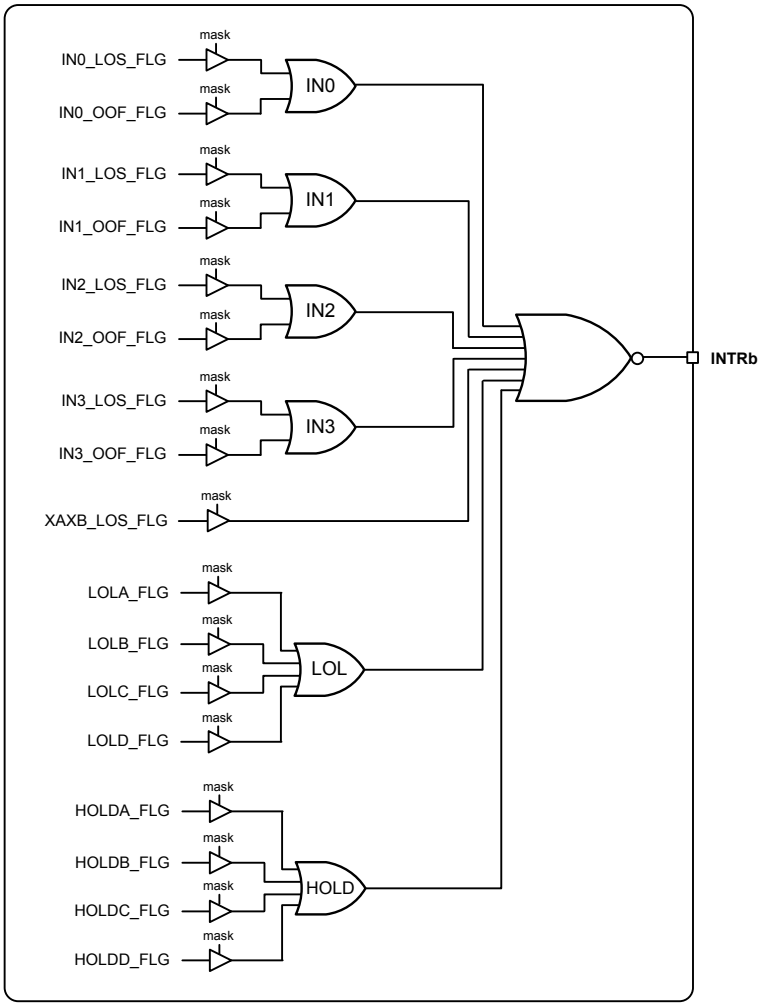


Figure 3.13. Interrupt Triggers and Masks

3.8 Outputs

The Si5381/82 supports up to twelve differential output drivers. Each driver has a configurable voltage swing and common mode voltage covering a wide variety of differential signal formats. In addition to supporting differential signals, any of the outputs can be configured as single-ended LVCMOS (3.3 V, 2.5 V, or 1.8 V) providing up to 24 single-ended outputs, or any combination of differential and single-ended outputs.

3.8.1 Output Crosspoint

A crosspoint allows any of the output drivers to connect with any of the MultiSynths as shown in the figure below. The crosspoint configuration is programmable and can be stored in NVM so that the desired output configuration is ready at power up.

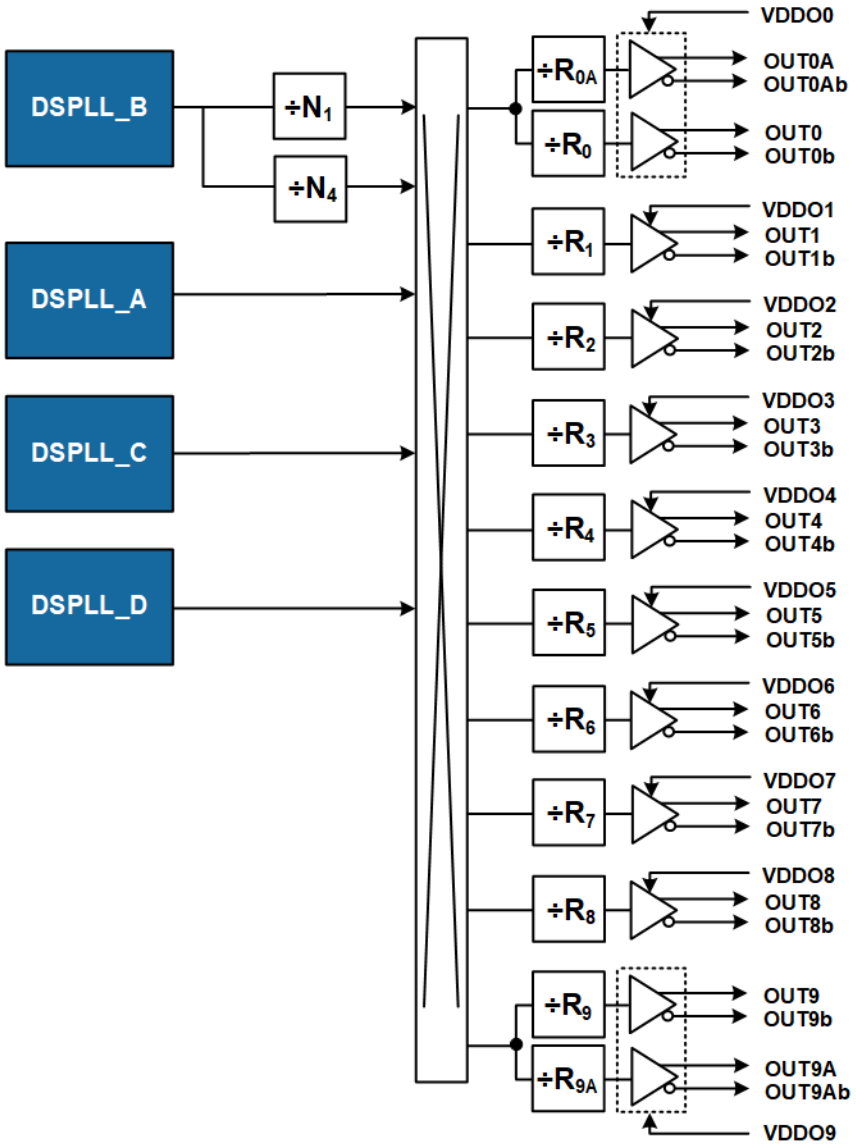


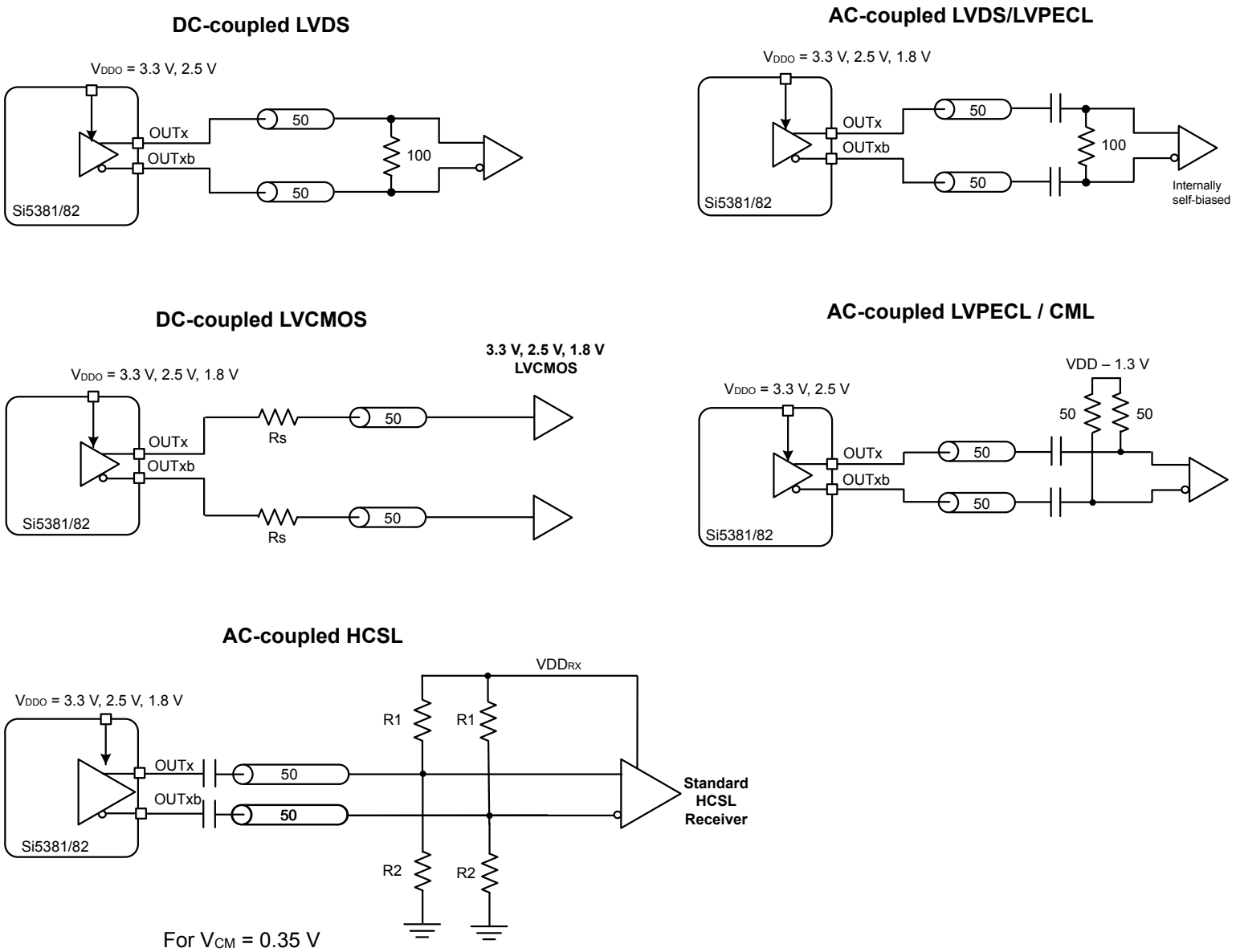
Figure 3.14. MultiSynth to Output Driver Crosspoint

3.8.2 Output Signal Format

The differential output swing and common mode voltage are both fully programmable covering a wide variety of signal formats including LVDS and LVPECL. In addition to supporting differential signals, any of the outputs can be configured as LVCMOS (3.3 V, 2.5 V, or 1.8 V) drivers providing up to 24 single-ended outputs, or any combination of differential and single-ended outputs.

3.8.3 Output Terminations

The output drivers support both ac-coupled and dc-coupled terminations as shown in the following figure.



For V_{CM} = 0.35 V

VDDRX	R1	R2
3.3 V	442 Ω	56.2 Ω
2.5 V	332 Ω	59 Ω
1.8 V	243 Ω	63.4 Ω

Figure 3.15. Supported Output Terminations

3.8.4 Programmable Common Mode Voltage For Differential Outputs

The differential outputs can be configured for DC or AC coupled LVDS or AC coupled LVPECL/CML. See the Reference Manual for programming the outputs to variable amplitudes when AC coupled.

3.8.5 LVCMOS Output Impedance and Drive Strength Selection

Each LVCMOS driver has a configurable output impedance to accommodate different trace impedances and drive strengths. A source termination resistor is recommended to help match the selected output impedance to the trace impedance. There are three programmable output impedance selections for each VDDO options as shown in the table below.

Table 3.3. LVCMOS Output Impedance and Drive Strength Selections

VDDO	OUTx_CMOS_DRV	Source Impedance (Zs)	Drive Strength (Iol/Ioh)
3.3 V	0x01	38 Ω	10 mA
	0x02	30 Ω	12 mA
	0x03*	22 Ω	17 mA
2.5 V	0x01	43 Ω	6 mA
	0x02	35 Ω	8 mA
	0x03*	24 Ω	11 mA
1.8 V	0x03*	31 Ω	5 mA
Note: Use of the lowest impedance setting is recommended for all supply voltages for best edge rates.			

3.8.6 LVCMOS Output Signal Swing

The signal swing (V_{OL}/V_{OH}) of the LVCMOS output drivers is set by the voltage on the VDDO pins. Each output driver has its own VDDO pin allowing a unique output voltage swing for each of the LVCMOS drivers.

3.8.7 LVCMOS Output Polarity

When a driver is configured as an LVCMOS output, it generates a clock signal on both pins (OUTx and OUTxb). By default, the clock on the OUTx pin is generated with the same polarity (in phase) as the clock on the OUTxb pin. The polarity of these clocks is configurable, enabling complementary clock generation and/or inverted polarity with respect to other output drivers.

3.8.8 Output Enable/Disable

The OEb pin provides a convenient method of disabling or enabling all of the output drivers at the same time. When the OEb pin is held high all outputs will be disabled. When held low, the outputs will all be enabled. Outputs in the enabled state can still be individually disabled through register control.

3.8.9 Output Disable During LOL

By default, a DSPLL that is out of lock will generate either free-running clocks or generate clocks in holdover mode. There is an option to disable the outputs when a DSPLL is LOL. This option can be useful to force a downstream PLL into holdover.

3.8.10 Output Disable During Reference LOS

The external XA/XB reference provides a critical function for the operation of the DSPLLs. In the event of the XO failure, the device will assert an XAXB_LOS alarm. By default, all outputs will be disabled during assertion of the XAXB_LOS alarm. There is an option to leave the outputs enabled during an XAXB_LOS alarm, but the frequency accuracy and stability is indeterminate during this fault condition.

3.8.11 Output Driver State When Disabled

The disabled state of an output driver is configurable as disable low or disable high.

3.8.12 Synchronous Output Disable Feature

The output drivers provide a selectable synchronous disable feature. Output drivers with this feature turned on will wait until a clock period has completed before the driver is disabled. This prevents unwanted runt pulses from occurring when disabling an output. When this feature is turned off, the output clock will disable immediately without waiting for the period to complete.

3.8.13 Static Output Skew Control

For DSPLLB, only the static phase adjust will allow a programmable phase offset between outputs on different N dividers. The resolution of the static phase adjustment is 68 ps with up to +/- 1 ms of total range. This feature is intended for use in JESD204B subclass 1 applications to adjust the phase of SYSREF signals with respect to DCLK. See the family Reference Manual and Application Note AN1165: Configuring Si538x Devices for JESD204B/C Wireless Applications for more details.

3.8.14 Dynamic Output Skew Control

For DSPLLB only the dynamic phase adjust will allow the device to dynamically and glitchlessly change the outputs phase using register writes while the device remains locked. The resolution of the dynamic phase adjustment is 68 ps step size with up to +/- 1 ms of total range. See the family Reference Manual for more details.

3.8.15 Zero Delay Mode

A zero delay mode is available for applications that require fixed and consistent minimum delay between the selected input and outputs. The zero delay mode is configured for DSPLL_B only by opening the internal feedback loop through software configuration and closing the loop externally as shown in the figure below.

This helps to cancel out the internal delay introduced by the dividers, the crosspoint, the input, and the output drivers. Any one of the outputs can be fed back to the FB_IN pins, although using the output driver that achieves the shortest trace length will help to minimize the input-to-output delay. Note that the nominal input-to-output delay is the trace delay from OUTx to FB_IN. The OUT9A and FB_IN pins are recommended for the external feedback connection. The FB_IN input pins must be terminated and ac-coupled when zero delay mode is used. A differential external feedback path connection is necessary for best performance. Note that the hitless switching feature is not available when zero delay mode is enabled.

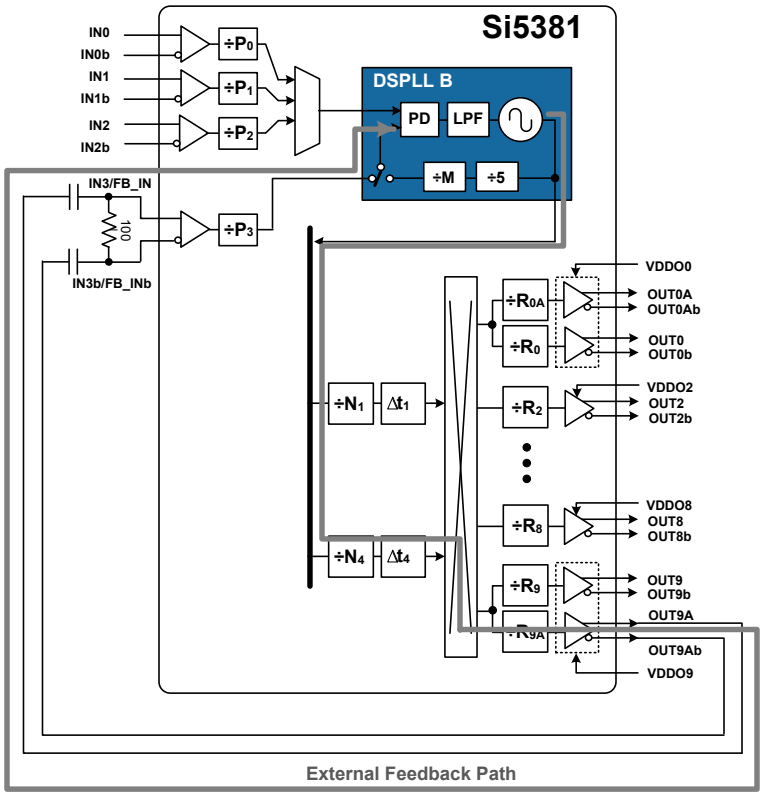


Figure 3.16. Si5381 Zero Delay Mode Setup

3.8.16 Output Divider (R) Synchronization

All the output R dividers are reset to a known state during the power-up initialization period. This ensures consistent and repeatable phase alignment across all output drivers. Resetting the device using the RSTb pin or asserting the hard reset bit will have the same result.

3.9 Power Management

Unused inputs and output drivers can be powered down when unused. Consult the Reference Manual and ClockBuilder Pro configuration utility for details.

3.10 In-Circuit Programming

The Si5381/82 is fully configurable using the serial interface (I^2C or SPI). At power-up the device downloads its default register values from internal non-volatile memory (NVM). Application specific default configurations can be written into NVM allowing the device to generate specific clock frequencies at power-up. Writing default values to NVM is in-circuit programmable with normal operating power supply voltages applied to its V_{DD} and V_{DDA} pins. The NVM is two time writable. Once a new configuration has been written to NVM, the old configuration is no longer accessible. Refer to the Reference Manual for a detailed procedure for writing registers to NVM.

3.11 Serial Interface

Configuration and operation of the Si5381/82 is controlled by reading and writing registers using the I^2C or SPI interface. The I2C_SEL pin selects I^2C or SPI operation. Communication with both 3.3 V and 1.8 V host is supported. The SPI mode operates in either 4-wire or 3-wire. The SCLK in SPI mode does not need to be present when CSb is high. See the timing diagram for SPI. See the Reference Manual for details.

3.12 Custom Factory Preprogrammed Parts

For applications where a serial interface is not available for programming the device, custom pre-programmed parts can be ordered with a specific configuration written into NVM. A factory preprogrammed part will generate clocks at power-up. Custom, factory-preprogrammed devices are available. The ClockBuilder Pro custom part number wizard can be used to quickly and easily generate a custom part number for your configuration.

In less than three minutes, you will be able to generate a custom part number with a detailed data sheet addendum matching your design's configuration. Once you receive the confirmation email with the data sheet addendum, simply place an order with your local Skyworks sales representative. Samples of your preprogrammed device will typically ship in about two weeks.

3.13 Enabling Features and/or Configuration Settings Unavailable in ClockBuilder Pro for Factory Preprogrammed Devices

As with essentially all modern software utilities, ClockBuilder Pro is continually being updated and enhanced. By registering at www.skyworksinc.com, you will be notified about changes and their impact. This update process will ultimately enable ClockBuilder Pro users to access all features and register setting values documented in this data sheet and the Reference Manual.

However, if you must enable or access a feature or register setting value so that the device starts up with this feature or a register setting, but the feature or register setting is not yet available in CBPro, you must contact a Skyworks applications engineer for assistance. After careful review of your project file and requirements, the Skyworks applications engineer will email back your CBPro project file with your specific features and register settings enabled. "Override" settings to match your request(s) will be listed in your design report file.

Once you receive the updated design file, simply open it in CBPro. The device will begin operation after startup with the values in the NVM file. The flowchart for this process is shown in the following figure.

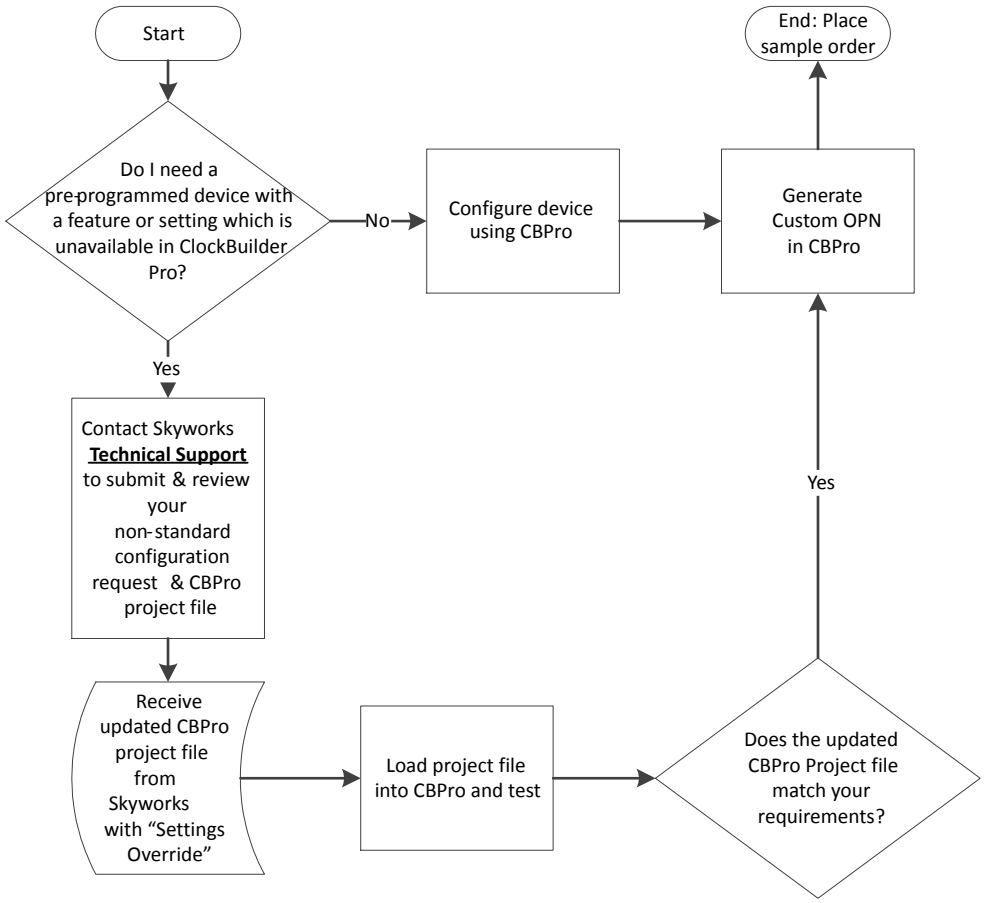


Figure 3.17. Process for Requesting Non-Standard CBPro Features

Note: Contact Skyworks Technical Support at https://www.skyworksinc.com/support-ia.

4. Register Map

The register map is divided into multiple pages where each page has 256 addressable registers. Page 0 contains frequently accessible registers, such as alarm status, resets, device identification, etc. Other pages contain registers that need less frequent access such as frequency configuration, and general device settings. A high level map of the registers is shown in “6.2. High-Level Register Map” . Refer to the Reference Manual for a complete list of register descriptions and settings. Skyworks strongly recommends using ClockBuilder Pro to create and manage register settings.

4.1 Addressing Scheme

The device registers are accessible using a 16-bit address that consists of an 8-bit page address plus an 8-bit register address. By default, the page address is set to 0x00. Changing to another page is accomplished by writing to the "Set Page Address" byte located at address 0x01 of each page.

4.2 High-Level Register Map

Table 4.1. High-Level Register Map

16-Bit Address		Content
8-bit Page Address	8-bit Register Address Range	
00	00	Revision IDs
	01	Set Page Address
	02–0A	Device IDs
	0B–15	Alarm Status
	17–1B	INTR Masks
	1C	Reset controls
	1D	FINC, FDEC Control Bits
	2B	SPI (3-Wire vs 4-Wire)
	2C–E1	Alarm Configuration
	E2–E4	NVM Controls
	FE	Device Ready Status
01	01	Set Page Address
	08–3A	Output Driver Controls
	41–42	Output Driver Disable Masks
	FE	Device Ready Status
02	01	Set Page Address
	02–05	Reference Clock Frequency Adjust
	08–2F	Input Divider (P) Settings
	30	Input Divider (P) Update Bits
	47–6A	Output Divider (R) Settings
	6B–72	User Scratch Pad Memory
	FE	Device Ready Status

16-Bit Address		Content
8-bit Page Address	8-bit Register Address Range	
03	01	Set Page Address
	02–37	MultiSynth Divider (N0–N4) Settings
	0C	MultiSynth Divider (N0) Update Bit
	17	MultiSynth Divider (N1) Update Bit
	22	MultiSynth Divider (N2) Update Bit
	2D	MultiSynth Divider (N3) Update Bit
	38	MultiSynth Divider (N4) Update Bit
	39–58	FINC/FDEC Settings N0–N4
	59–62	Output Delay (Δt) Settings
	FE	Device Ready Status
04	87	Zero Delay Mode Set Up
05	0E–14	Fast Lock Loop Bandwidth
	15–1F	Feedback Divider (M) Settings
	2A	Input Select Control
	2B	Fast Lock Control
	2C–35	Holdover Settings
	36	Input Clock Switching Mode Select
	38–39	Input Priority Settings
	3F	Holdover History Valid Data
06–08	00–FF	Reserved
09	01	Set Page Address
	1C	Zero Delay Mode Settings
	43	Control I/O Voltage Select
	49	Input Settings
10–FF	00–FF	Reserved

5. Electrical Specifications

Table 5.1. Recommended Operating Conditions

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C)					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
Ambient Temperature	T_A	–40	25	85	°C
Maximum Junction Temperature	TJ_{MAX}	—	—	125	°C
Core Supply Voltage	V_{DD}	1.71	1.80	1.89	V
	V_{DDA}	3.14	3.30	3.47	V
Output Driver Supply Voltage	V_{DDO}	3.14	3.30	3.47	V
		2.38	2.50	2.62	V
		1.71	1.80	1.89	V

Note:

1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.

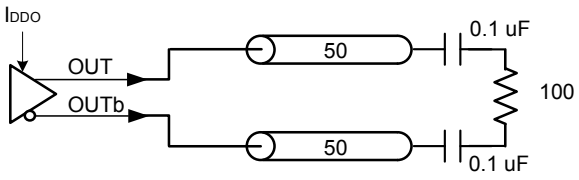
Table 5.2. DC Characteristics

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)						
Parameter	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
Core Supply Current[1, 2]	I_{DD}	Si5381	—	300	460	mA
	I_{DDA}		—	130	140	mA
	I_{DD}	Si5382	—	200	365	mA
	I_{DDA}		—	125	135	mA
Output Buffer Supply Current	I_{DDO}	LVPECL Output[3] @ 156.25 MHz	—	22	26	mA
		LVDS Output[3] @ 156.25 MHz	—	15	18	mA
		3.3 V LVCMOS[4] Output @ 156.25 MHz	—	22	30	mA
		2.5 V LVCMOS[4] Output @ 156.25 MHz	—	18	23	mA
		1.8 V LVCMOS[4] Output @ 156.25 MHz	—	12	16	mA
Total Power Dissipation[1, 5]	P_d	Si5381	—	1350	—	mW
		Si5382	—	1200	—	mW

Note:

1. Si5381/82 test configuration: 8 clock outputs enabled (2 x 983.04 MHz, 2 x 491.52 MHz, 1 x 245.76 MHz, 3 x 122.88 MHz; 2.5 LVDS). Excludes power in termination resistors.
2. VDDO0 supplies power to both OUT0 and OUT0A buffers. Similarly, VDDO9 supplies power to both OUT9 and OUT9A buffers.
3. Differential outputs terminated into an AC coupled 100 Ω load.
4. LVCMOS outputs measured into a 5-inch 50 Ω PCB trace with 5 pF load. The LVCMOS outputs were set to OUTx_CMOS_DRV = 3, which is the strongest driver setting. See the LVCMOS Output Test Configuration.
5. Detailed power consumption for any configuration can be estimated using ClockBuilder Pro when an evaluation board (EVB) is not available. All EVBs support detailed current measurements for any configuration.

Differential Output Test Configuration



LVCMOS Output Test Configuration

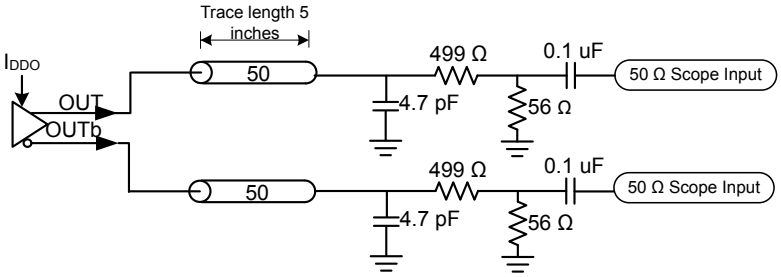


Table 5.3. Input Clock Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C)						
Parameter	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
Standard Differential or Single-Ended/LVCMOS — AC-coupled (IN0, IN1, IN2, IN3)						
Input Frequency Range	f_{IN_DIFF}	Differential (DSPLL B)	7.68	—	750	MHz
	f_{IN_SE}	Single-ended/ LVCMOS (DSPLL B)	7.68	—	250	
	f_{IN_DIFF}	Differential (DSPLL A/C/D)	0.008	—	750	
	f_{IN_SE}	Single-ended/ LVCMOS (DSPLL A/C/D)	0.008	—	250	
Input Voltage Amplitude	V_{IN_DIFF}	f_{IN_DIFF} < 250 MHz	100	—	1800	mVpp_se
		250 MHz < f_{IN_DIFF}< 750 MHz	225	—	1800	mVpp_se
Single-Ended Input Amplitude	V_{IN_SE}	f_{IN_SE}< 250 MHz	100	—	3600	mVpp_se
Slew Rate[1, 2]	SR		400	—	—	V/µs
Duty Cycle	DC		40	—	60	%
Capacitance	C_{IN}		—	2.4	—	pF
Input Resistance Differential	R_{in_DIFF}		—	16	—	kΩ
Input Resistance Single-Ended	Ri_{in_SE}		—	8	—	kΩ
LVCMOS / Pulsed CMOS DC-Coupled Input Buffer (IN0, IN1, IN2, IN3/FB_IN)[3]						

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C)						
Parameter	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
Input Frequency	f_{IN_CMOS}	Standard CMOS & Non-standard CMOS	0.008	—	250	MHz
		Pulsed CMOS	0.008	—	1	MHz
Input Voltage	V_{IL}	Standard CMOS	—	—	0.5	V
		Non-standard CMOS & Pulsed CMOS	—	—	0.4	V
	V_{IH}	Standard CMOS	1.3	—	—	V
		Non-standard CMOS & Pulsed CMOS	0.8	—	—	V
Slew Rate[1, 2]	SR		400	—	—	V/µs
Duty Cycle	DC	Standard CMOS & Non-standard CMOS	40	—	60	%
		Pulsed CMOS	5		95	
Minimum Pulse Width	PW	Standard CMOS & Non-standard CMOS (250 MHz @ 40% Duty Cycle)	1.6	—	—	ns
		Pulsed CMOS (1 MHz @ 5% Duty Cycle)	50	—	—	
Input Resistance	R_{IN}		—	8	—	kΩ
XO (applied to XA/XB)[4]						
Frequency	f_{IN_REF}		—	54	—	MHz
Total Frequency Tolerance[5]	f_{RANGE}		-50	—	+50	ppm
Input Voltage Amplitude	V_{IN_SE}	Single-ended Input	365	—	2000	mVpp_se
	V_{IN_DIFF}	Differential Input	365	—	2500	mVpp_diff
Slew Rate[1, 2]	SR	Single-ended Input	1500	—	—	V/µs
	SR_{IN_DIFF}	Differential Input	400	—	—	V/µs
Input Duty Cycle	DC		40	—	60	%
Activity Dip[6]					2	ppm/C

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C)						
Parameter	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**

Note:

1. Imposed for phase noise performance.
2. Rise and fall times can be estimated using the following simplified equation: tr/tf80-20 = ((0.8 - 0.2) * VIN_Vpp_se) / SR.
3. Pulsed CMOS mode is intended primarily for single-ended LVCMOS input clocks <1 MHz, which must be dc-coupled, having a duty cycle significantly less than 50%. A typical application example is a low frequency video frame sync pulse. See the Si5381/82 Reference Manual for details. Otherwise, for standard LVCMOS input clocks, use the “AC-coupled Singled-Ended” mode as shown in .
4. Refer to the Si534x/8x Jitter Attenuators Recommended Crystal, TCXO and OCXOs Reference Manual for recommended 54 MHz XOs.
5. Includes aging and temperature impacts from -40C to 85C.
6. Activity dip is also called frequency perturbation.

Table 5.4. Serial and Control Input Pin Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDS} = 3.3 V ±5%, 1.8 V ±5%, T_A = –40 to 85 °C)						
Parameter	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
Serial and Control Input Pins (IN_SEL[1:0], RSTb, OEb, PDNb, A1/SDO, SCLK, A0/CSb, SDA/SDIO)						
Input Voltage Thresholds	V_{IL}		—	—	0.3 x V_{DDIO}[1]	V
	V_{IH}		0.7 x V_{DDIO}[1]	—	—	V
Input Capacitance	C_{IN}		—	2	—	pF
Input Resistance	I_L		—	20	—	kΩ
Minimum Pulse Width	PW	RSTb, PDNb	100	—	—	ns

Note:

1. V_{DDIO} is determined by the IO_VDD_SEL bit. It is selectable as V_{DDA} or V_{DD}. See the Si5381/82 Reference Manual for more details on the register settings.

Table 5.5. Differential Clock Output Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)						
Parameter	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
Output Frequency DSPLL B[5]	f_{OUT}	N >= 10, R >= 2	0.0001	—	737.28	MHz
		N = 9, R = 2	—	819.2	—	MHz
		N = 8, R = 2	—	921.6	—	MHz
		N = 7, R = 2	—	14745.6/14	—	MHz
		N = 6, R = 2	—	1228.8	—	MHz
		N = 5, R = 2	—	1474.56	—	MHz
		N = 9, R = 1	—	1638.4	—	MHz
		N = 8, R = 1	—	1843.2	—	MHz
		N = 7, R = 1	—	2106.53	—	MHz
		N = 6, R = 1	—	2457.6	—	MHz
		N = 5, R = 1	—	2949.12	—	MHz
Output Frequency DSPLL A/C/D	f_{OUT}	N >= 10	0.0001	—	735	MHz
Duty Cycle	DC	fOUT < 400 MHz	48	—	52	%
		400 MHz < f_{OUT} < 737.28 MHz	45	—	55	%
		737.28 MHz < f_{OUT} < 1474.56 MHz	40	—	60	%
		f > 1474.56 MHz	25	—	75	%
Output-Output Skew[6]	T_{SK}	Differential outputs from DSPLLB that use the same integer N divider value	—	0	75	ps
		For outputs from DSPLLb but using different integer N dividers.[5]	-150	0	150	ps
Output Dynamic/Static Delay Adjustment	T_{delay_step}	Output on DSPLL B	—	68	—	ps
	T_{delay_range}	Outputs on DSPLL B	—	±1	—	ms
OUT-OUTb Skew	T_{SK_OUT}	Measured from the positive to negative output pins	—	0	50	ps

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)							
Parameter	**Symbol**	**Test Condition**		**Min**	**Typ**	**Max**	**Unit**
Output Voltage Amplitude[1, 2]	V_{OUT}	V_{DDO} = 3.3 V, 2.5 V, or 1.8 V	LVDS	350	450	530	mVpp_se
		V_{DDO} = 3.3 V, 2.5 V	LVPECL	610	780	950	
		High Speed Differential (f_{OUT} > 1474.56 MHz		400	750 @ 1700 MHz 700 @ 2000 MHz 650 @ 2500 MHz 550 @ 2900 MHz	1050	
Common Mode Voltage [1,2]	VCM	V_{DDO} = 3.3 V	LVDS	1.10	1.2	1.3	V
			LVPECL	1.90	2.0	2.1	
		V_{DDO} = 2.5 V	LVPECL, LVDS	1.1	1.2	1.3	
		V_{DDO} = 1.8 V	sub-LVDS	0.8	0.9	1.00	
Rise and Fall Times (20% to 80%)	t_R/t_F	LVPECL and LVDS Outputs		—	170	240	ps
Differential Output Impedance[2]	Z_O	LVPECL and LVDS Outputs		—	100	—	Ω
Power Supply Noise Rejection[3]	PSRR	10 kHz sinusoidal noise		—	–93	—	dBc
		100 kHz sinusoidal noise		—	–93	—	
		500 kHz sinusoidal noise		—	–84	—	
		1 MHz sinusoidal noise		—	–79	—	
Output-output Crosstalk[4]	XTALK	Differential		—	–75	—	dB

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)						
Parameter	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**

Note:

1. Output amplitude and common mode voltage are programmable through register settings and can be stored in NVM. Each output driver can be programmed independently. The LVDS maximum is 100 mV (or 80 mV) higher than the TIA/EIA-644 maximum. Refer to the Si5381/82 Reference Manual for recommended output settings.
2. Not all combinations of voltage amplitude and common mode voltages settings are possible.
3. Measured for 156.25 MHz carrier frequency. Sinewave noise added to VDDO (1.8 V = 50 mVpp, 2.5 V/3.3 V = 100 mVpp) and noise spur amplitude measured.
4. Measured across two adjacent outputs, both in LVDS mode, with the victim running at 122.88 MHz and the aggressor at 156.25 MHz. Refer to application note, "AN862: Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems", guidance on crosstalk minimization. Note that all active outputs must be terminated when measuring crosstalk.
5. VDDO = 2.5 V or 3.3 V required for fOUT > 1474.56 MHz
6. For any R divider settings that differ by a power of 2.

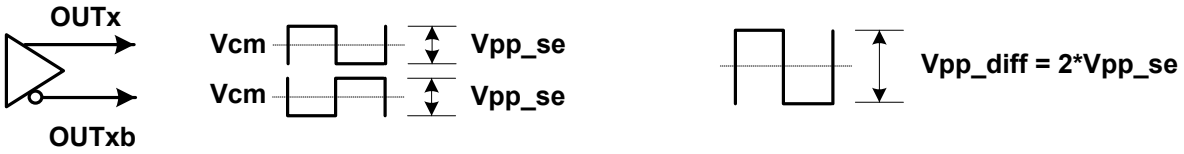


Table 5.6. LVCMOS Clock Output Specifications

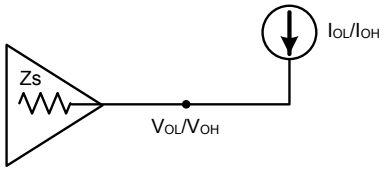
(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)							
Parameter	**Symbol**	**Test Condition**		**Min**	**Typ**	**Max**	**Unit**
Output Frequency	f_{OUT}			0.0001	—	250	MHz
Duty Cycle	DC	fOUT <100 MHz		48	—	52	%
		100 MHz < fOUT < 250 MHz		44	—	56	
Output Voltage High[1, 2]	V_{OH}	VDDO = 3.3 V					
		OUTx_CMOS_DRV=1	IOH = –10 mA	VDDO x 0.75	—	—	V
		OUTx_CMOS_DRV=2	IOH = –12 mA		—	—	
		OUTx_CMOS_DRV=3	IOH = –17 mA		—	—	
		VDDO = 2.5 V					
		OUTx_CMOS_DRV=1	IOH = –6 mA	VDDO x 0.75	—	—	V
		OUTx_CMOS_DRV=2	IOH = –8 mA		—	—	
		OUTx_CMOS_DRV=3	IOH = –11 mA		—	—	
		VDDO = 1.8 V					
		OUTx_CMOS_DRV=2	IOH = –4 mA	VDDO x 0.75	—	—	V
		OUTx_CMOS_DRV=3	IOH = –5 mA		—	—	

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDO} = 1.8 V ±5%, 2.5 V ±5%, or 3.3 V ±5%, T_A = –40 to 85 °C)							
Parameter	**Symbol**	**Test Condition**		**Min**	**Typ**	**Max**	**Unit**
Output Voltage Low[1, 2]	V_{OL}	VDDO = 3.3 V					
		OUTx_CMOS_DRV=1	IOL = 10 mA	—	—	VDDO x 0.15	V
		OUTx_CMOS_DRV=2	IOL = 12 mA	—	—		
		OUTx_CMOS_DRV=3	IOL = 17 mA	—	—		
		VDDO = 2.5 V					
		OUTx_CMOS_DRV=1	IOL = 6 mA	—	—	VDDO x 0.15	V
		OUTx_CMOS_DRV=2	IOL = 8 mA	—	—		
		OUTx_CMOS_DRV=3	IOL = 11 mA	—	—		
		VDDO = 1.8 V					
		OUTx_CMOS_DRV=2	IOL = 4 mA	—	—	VDDO x 0.15	V
		OUTx_CMOS_DRV=3	IOL = 5 mA	—	—		
LVCMOS Rise and Fall Times[3] (20% to 80%)	tr/tf	VDDO = 3.3 V		—	400	600	ps
		VDDO = 2.5 V		—	450	600	ps
		VDDO = 1.8 V		—	550	750	ps

Note:

1. Driver strength is a register programmable setting and stored in NVM. Options are OUTx_CMOS_DRV = 1, 2, 3. Refer to the Si5381/82 Reference Manual for more details on register settings.
2. IOL/IOH is measured at VOL/VOH as shown in the dc test configuration.
3. Using the AC Output Test Configuration below. The LVCMOS outputs were set to OUTx_CMOS_DRV = 3.

DC Test Configuration



AC Output Test Configuration

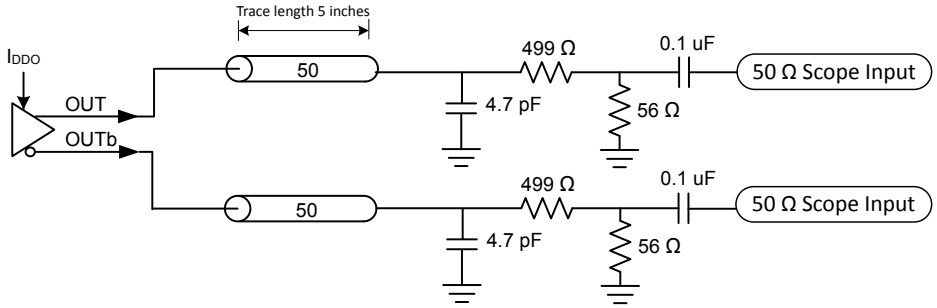


Table 5.7. Output Serial and Status Pin Specifications

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDS} = 3.3 V ±5%, 1.8 V ±5%, T_A = –40 to 85 °C)						
Parameter	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
Serial and Status Output Pins (INTRb, LOLb, SDA/SDIO[2], A1/SDO)						
Output Voltage	V_{OH}	IOH = –2 mA	V_{DDIO}[1] x 0.75	—	—	V
	V_{OL}	IOL = 2 mA	—	—	V_{DDIO}1 x 0.15	V

(V_{DD} = 1.8 V ±5%, V_{DDA} = 3.3 V ±5%, V_{DDS} = 3.3 V ±5%, 1.8 V ±5%, T_A = –40 to 85 °C)						
Parameter	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**

Note:

1. V_{DDIO} is determined by the IO_VDD_SEL bit. It is selectable as VDDA or VDD. Users normally select this option in the ClockBuilder Pro GUI. Alternatively, refer to the Si5381/82 Reference Manual for more details on register settings.
2. The V_{OH} specification does not apply to the open-drain SDA/SDIO output when the serial interface is in I2C mode or is unused with I2C_SEL pulled high internally. V_{OL} remains valid in all cases.

Table 5.8. Performance Characteristics

(V_{DD} = 1.8 V ±5%, or 3.3 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C)						
Parameter	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
PLL Loop Bandwidth	f_{BW}	DSPLL B	20	—	4000	Hz
Programming Range	$f_{BW\ DSPLLA,C,D}$	DSPLL A,C,D	1	—	4000	Hz
Initial Start-Up Time	t_{START}	Time from power-up or de-assertion of PDNb to when the device generates free-running clocks	—	370	625	ms
PLL Lock Time	t_{ACQ}	Fastlock enabled, fIN = 19.44 MHz[1]	—	280	300	ms
POR to Serial Interface Ready[2]	t_{RDY}		—	15	—	ms
Hard Reset to Serial Interface Ready	t_{RDYhr}	DSPLL B in ZDM	—	—	800	ms
Input-to-Output Delay Variation	$t_{IODELAY}$	Different parts and outputs	—	—	1.2	ns
Jitter Peaking	J_{PK}	25 MHz input, 25 MHz output, loop bandwidth of 4 Hz	—	—	0.1	dB
Jitter Tolerance	J_{TOL}	Compliant with G.8262 Options 1 and 2 for 1G, 10G, or 25G Synchronous Ethernet Jitter Modulation Frequency = 10 Hz	—	3180	—	UI pk-pk
Maximum Phase Transient During a Hitless Switch	t_{SWITCH}	Single manual or automatic switch between two 7.68 MHz inputs, DSPLL BW = 400 Hz - DSPLL A/B/C/D	—	—	0.3	ns
		Single manual or automatic switch between two 8 kHz inputs, DSPLL BW = 40 Hz - DSPLL A/C/D inputs only	—	—	0.8	ns
Pull-in Range	ω_P		-20	—	20	ppm
RMS Jitter Generation[3]	J_{GEN}	12 kHz to 20 MHz	—	72	—	fs RMS

(V_{DD} = 1.8 V ±5%, or 3.3 V ±5%, V_{DDA} = 3.3 V ±5%, T_A = –40 to 85 °C)						
Parameter	**Symbol**	**Test Condition**	**Min**	**Typ**	**Max**	**Unit**
Phase Noise Performance[3] (122.88 MHz Carrier Frequency)	PN	100 Hz	—	-118	—	dBc/Hz
		1 kHz	—	-133	—	dBc/Hz
		10 kHz	—	-142	—	dBc/Hz
		100 kHz	—	-149	—	dBc/Hz
		1 MHz	—	-154	—	dBc/Hz
		10 MHz	—	-163	—	dBc/Hz
Spur Performance (122.88 MHz Carrier Frequency)	SPUR	From 1 MHz to 20 MHz offset on a 122.88 MHz output from PLLB	—	-96	—	dBc

Note:

1. Lock Time can vary significantly depending on several parameters, such as bandwidths, LOL thresholds, etc. For this case, lock time was measured with nominal and fastlock bandwidths, both set to 100 Hz, LOL set/clear thresholds of 3/0.3 ppm respectively, using IN0 as clock reference by removing the reference and enabling it again, then measuring the delta time between the first rising edge of the clock reference and the LOL indicator de-assertion.
2. Measured as time from valid VDD/VDDA rails (90% of their value) to when the serial interface is ready to respond to commands.
3. Jitter generation test conditions: F_{in}= 156.25 MHz, F_{out} = 122.88 MHz, DSPLL LBW = 40 Hz. Jitter integrated from 12 kHz to 20 MHz offset. Does not include jitter from PLL input reference.

Table 5.9. I2C Timing Specifications (SCL,SDA)

Parameter	**Symbol**	**Test Condition**	**Min**	**Max**	**Min**	**Max**	**Unit**
			Standard Mode 100 kbps		**Fast Mode 400 kbps**		
SCL Clock Frequency	f_{SCL}		—	100	—	400	kHz
SMBus Timeout	—	When Timeout is Enabled	25	35	25	35	ms
Hold Time (Repeated) START Condition	$t_{HD:STA}$		4.0	—	0.6	—	µs
Low Period of the SCL Clock	t_{LOW}		4.7	—	1.3	—	µs
HIGH Period of the SCL Clock	t_{HIGH}		4.0	—	0.6	—	µs
Set-up Time for a Repeated START Condition	$t_{SU:STA}$		4.7	—	0.6	—	µs
Data Hold Time	$t_{HD:DAT}$		100	—	100	—	ns
Data Set-up Time	$t_{SU:DAT}$		250	—	100	—	ns
Rise Time of Both SDA and SCL Signals	t_r		—	1000	20	300	ns
Fall Time of Both SDA and SCL Signals	t_f		—	300	—	300	ns
Set-up Time for STOP Condition	$t_{SU:STO}$		4.0	—	0.6	—	µs

Parameter	Symbol	Test Condition	Min	Max	Min	Max	Unit
Bus Free Time between a STOP and START Condition	t_{BUF}		4.7	—	1.3	—	µs
Data Valid Time	$t_{VD:DAT}$		—	3.45	—	0.9	µs
Data Valid Acknowledge Time	$t_{VD:ACK}$		—	3.45	—	0.9	µs

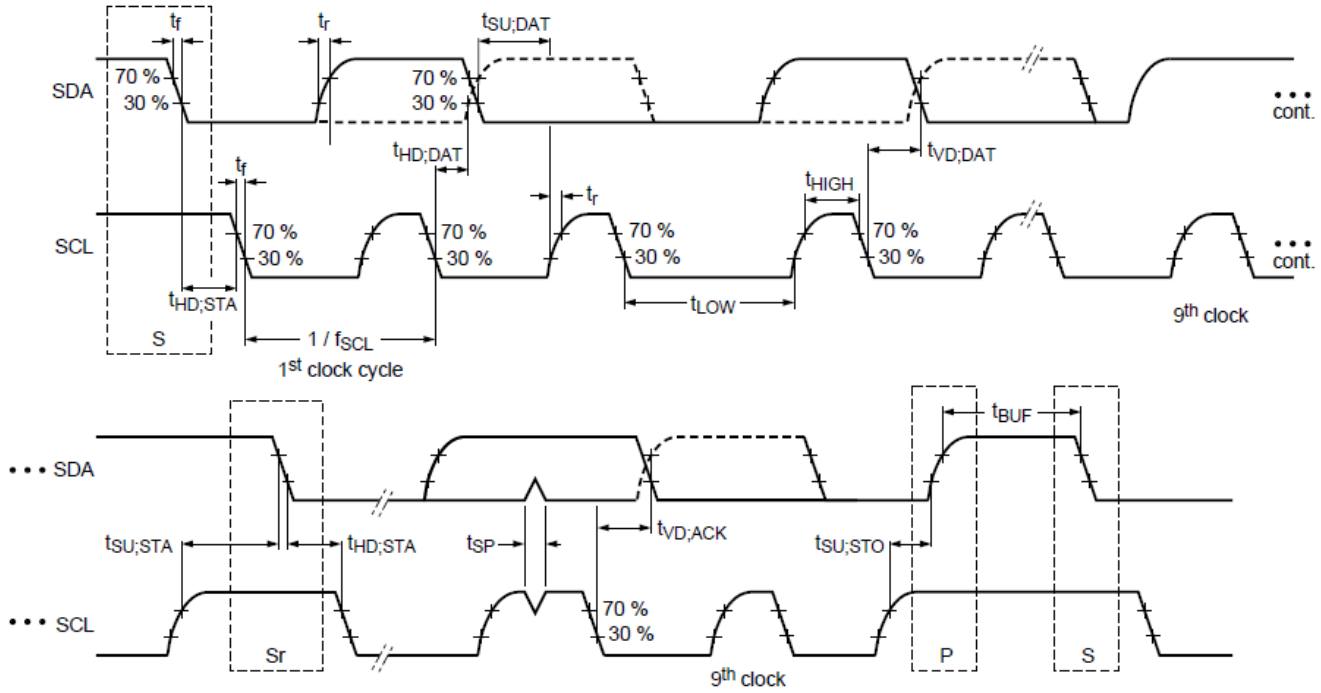


Figure 5.1. I²C Serial Port Timing Standard and Fast Modes

Table 5.10. SPI Timing Specifications (4-Wire)

Parameter	Symbol	Min	Typ	Max	Unit
SCLK Frequency	f_{SPI}	—	—	20	MHz
SCLK Duty Cycle	T_{DC}	40	—	60	%
SCLK Period	T_C	50	—	—	ns
Delay Time, SCLK Fall to SDO Active	T_{D1}	—	—	18	ns
Delay Time, SCLK Fall to SDO	T_{D2}	—	—	15	ns
Delay Time, CSb Rise to SDO Tri-State	T_{D3}	—	—	15	ns
Setup Time, CSb to SCLK	T_{SU1}	5	—	—	ns
Hold Time, SCLK Fall to CSb	T_{H1}	5	—	—	ns
Setup Time, SDI to SCLK Rise	T_{SU2}	5	—	—	ns
Hold Time, SDI to SCLK Rise	T_{H2}	5	—	—	ns

Parameter	Symbol	Min	Typ	Max	Unit
Delay Time Between Chip Selects (CSb)	T_{CS}	95	—	—	ns

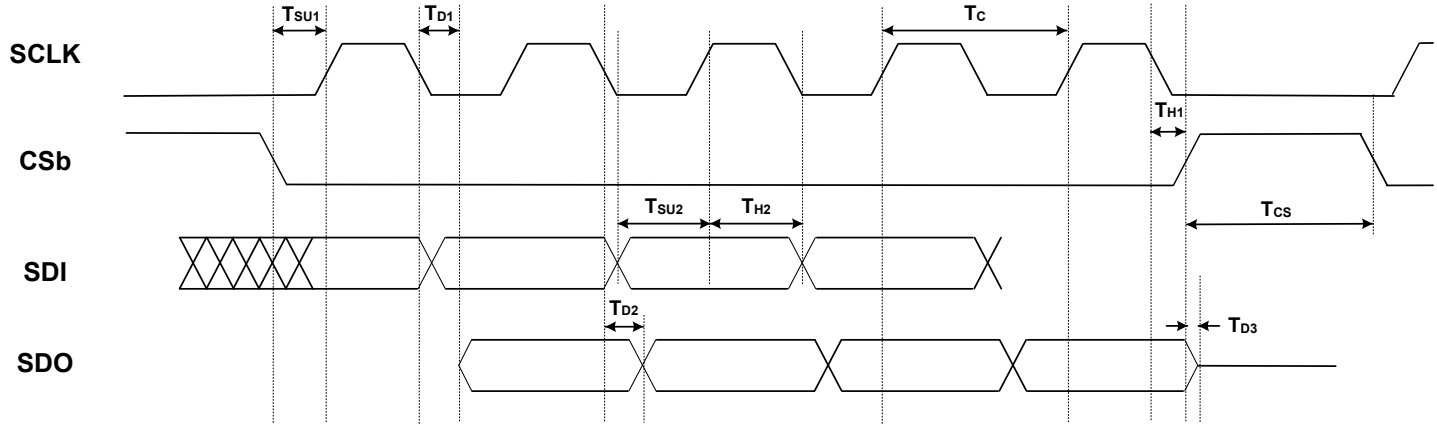


Figure 5.2. 4-Wire SPI Serial Interface Timing

Table 5.11. SPI Timing Specifications (3-Wire)

Parameter	Symbol	Min	Typ	Max	Unit
SCLK Frequency	f_{SPI}	—	—	20	MHz
SCLK Duty Cycle	T_{DC}	40	—	60	%
SCLK Period	T_C	50	—	—	ns
Delay Time, SCLK Fall to SDIO Turn-on	T_{D1}	—	—	20	ns
Delay Time, SCLK Fall to SDIO Next-bit	T_{D2}	—	—	15	ns
Delay Time, CSb Rise to SDIO Tri-State	T_{D3}	—	—	15	ns
Setup Time, CSb to SCLK	T_{SU1}	5	—	—	ns
Hold Time, SCLK Fall to CSb	T_{H1}	5	—	—	ns
Setup Time, SDI to SCLK Rise	T_{SU2}	5	—	—	ns
Hold Time, SDI to SCLK Rise	T_{H2}	5	—	—	ns
Delay Time Between Chip Selects (CSb)	T_{CS}	95	—	—	ns

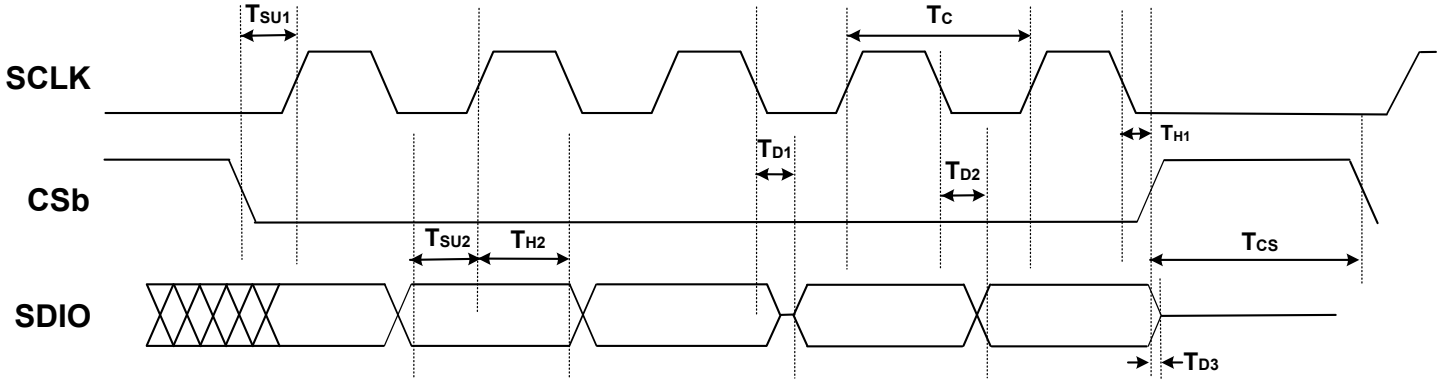


Figure 5.3. 3-Wire SPI Serial Interface Timing

Table 5.12. Thermal Characteristics (QFN-64)

Parameter	Symbol	Test Condition1	Value	Unit
Thermal Resistance Junction to Ambient	Θ_{JA}	Still Air	22	°C/W
		Air Flow 1 m/s	19.4	
		Air Flow 2 m/s	18.3	
Thermal Resistance Junction to Case	Θ_{JC}		9.5	
Thermal Resistance Junction to Board	Θ_{JB}		9.4	
	Ψ_{JB}		9.3	
Thermal Resistance Junction to Top Center	Ψ_{JT}		0.2	

Note:
1. Based on PCB Dimension: 3” x 4.5”, PCB Thickness: 1.6 mm, PCB Land/Via under GNP pad: 36, Number of Cu Layers: 4

Table 5.13. Absolute Maximum[1, Electrical Specifications, 2]

Parameter	Symbol	Test Condition	Value	Unit
DC Supply Voltage	VDD		–0.5 to 3.8	V
	VDDA		–0.5 to 3.8	V
	VDDO		–0.5 to 3.8	V
Input Voltage Range	VI1	IN0 – IN3	–1.0 to 3.8	V
	VI2	IN_SEL[1:0], RSTb, PDNb, OEb, I2C_SEL, SYNC SDA/SDIO, A1/SDO, SCLK, A0/CSb	–0.5 to 3.8	V
	VI3	XA/XB	–0.5 to 2.7	V
Latch-up Tolerance	LU		JESD78 Compliant	
ESD Tolerance	HBM	100 pF, 1.5 kΩ	2.0	kV
Junction Temperature	T_{JCT}		–55 to 125	°C
Storage Temperature Range	T_{STG}		–55 to +150	°C
Soldering Temperature (Pb-free profile)[2]	T_{PEAK}		260	°C
Soldering Temperature Time at TPEAK(Pb-free profile)[3]	T_P		20–40	sec

Parameter	Symbol	Test Condition	Value	Unit

Note:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. For detailed MSL and packaging information, go to https://www.skyworksinc.com/quality.
3. The device is compliant with JEDEC J-STD-020.

6. Typical Application Schematic

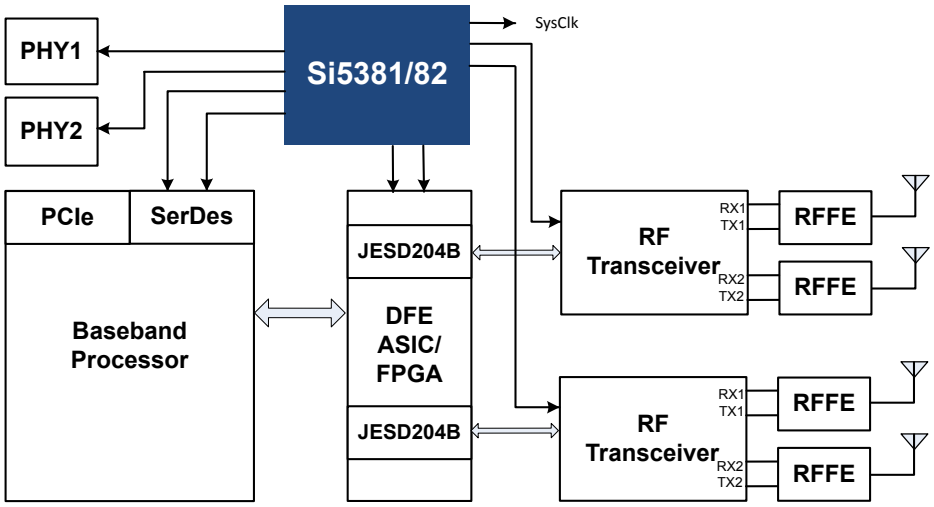


Figure 6.1. Application Block Diagram of µBTS

7. Detailed Block Diagrams

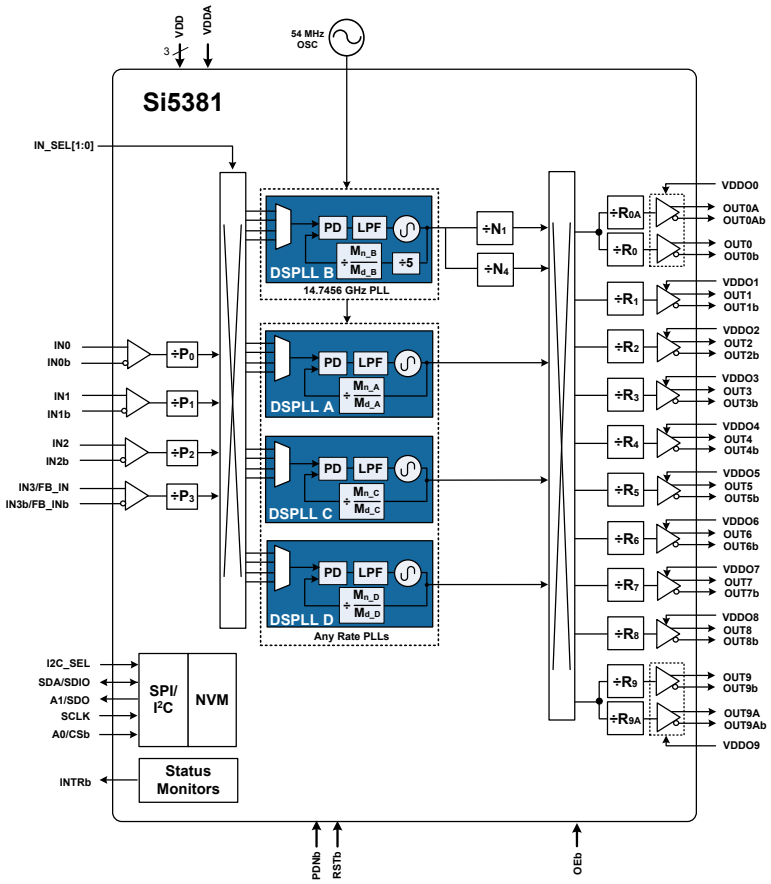


Figure 7.1. Si5381 Block Diagram

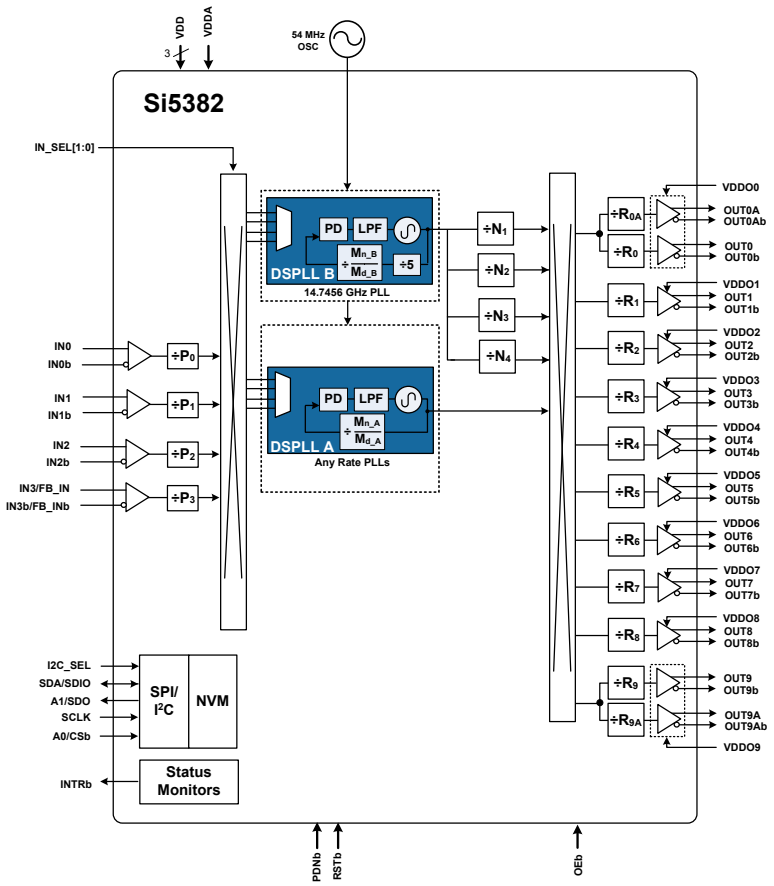


Figure 7.2. Si5382 Block Diagram

8. Typical Operating Characteristics

The phase noise plots below were taken under the following conditions: V_{DD} = 1.8 V; V_{DDA} = 3.3 V; V_{DDS} = 3.3 V, 1.8 V; OLBW = 40Hz; T_a = 25 °C.

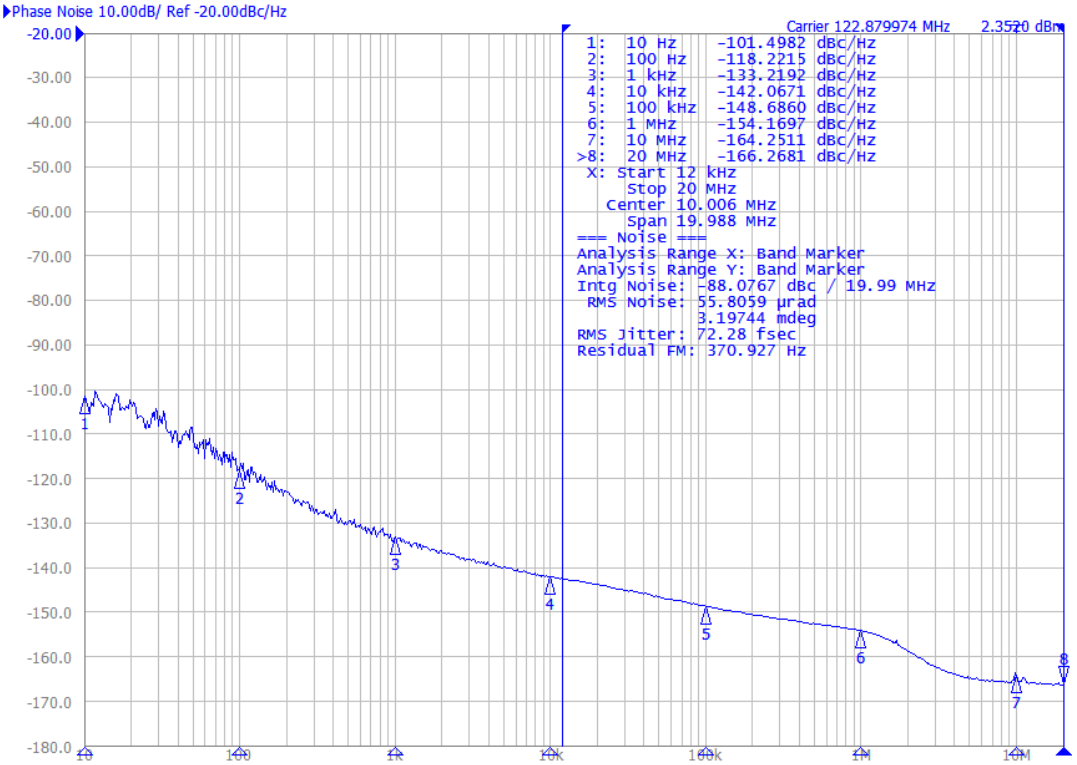


Figure 8.1. f_{IN} = 156.25 MHz, f_{OUT} = 122.88 MHz

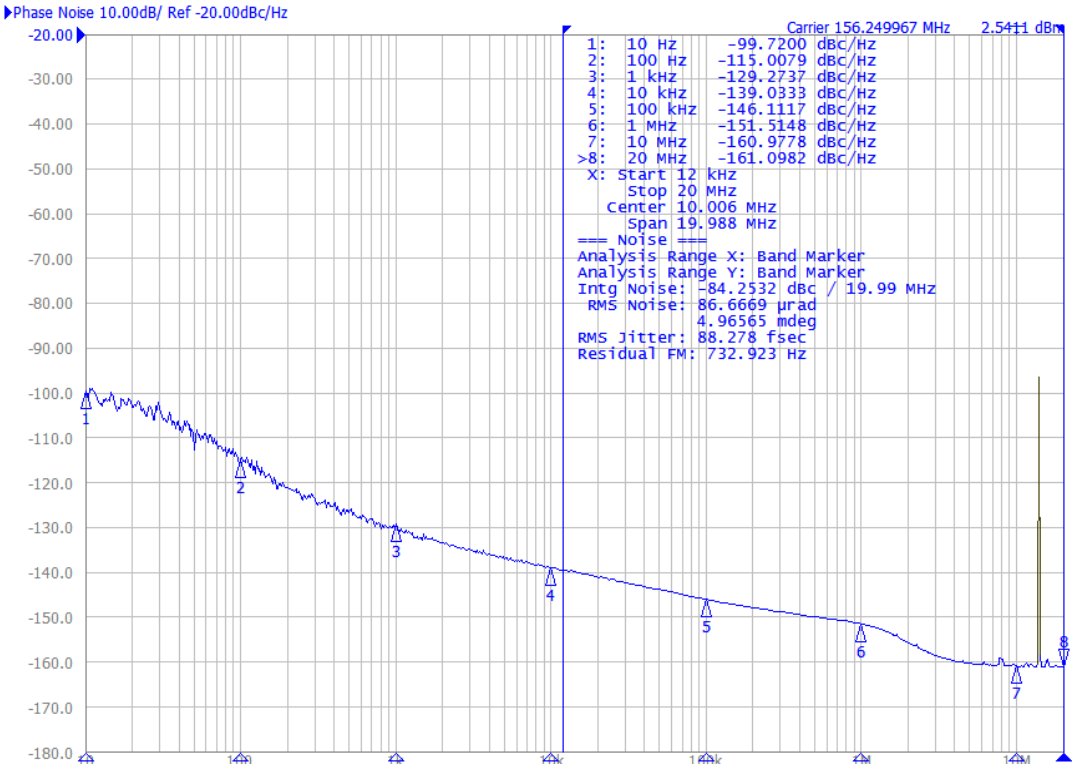


Figure 8.2. f_{IN} = 156.25 MHz, f_{OUT} = 156.25 MHz

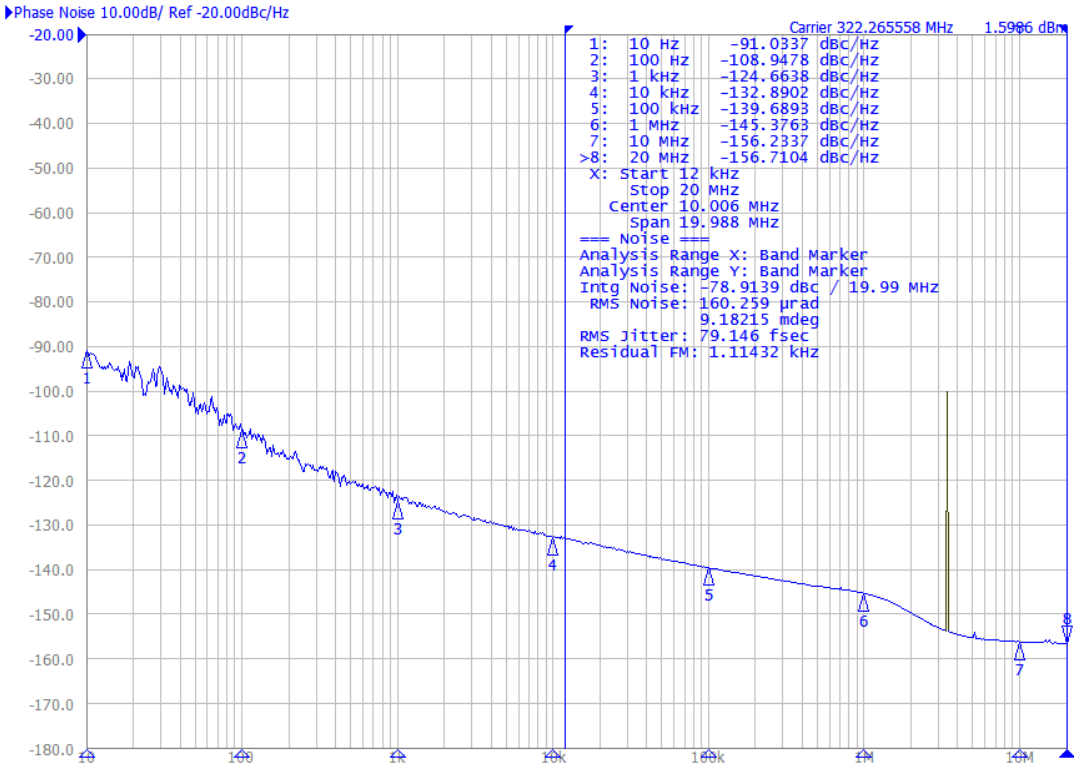


Figure 8.3. f_{IN} = 322.265625 MHz, f_{OUT} = 322.265625 MHz

9. Pin Descriptions

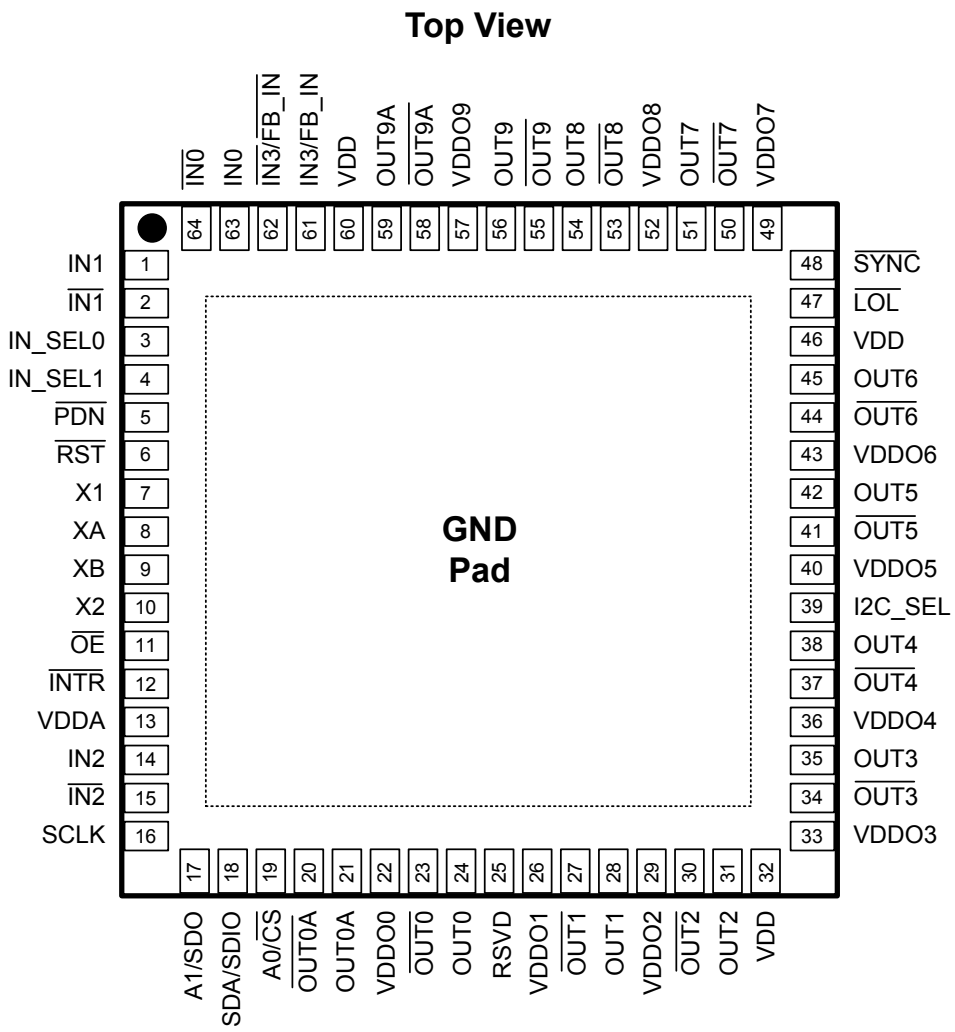


Table 9.1. Si5381/82 Pin Descriptions

Pin Name	Pin Number	Pin Type[1]	Function
Inputs			
IN0	63	I	Clock Inputs. These pins accept an input clock for synchronizing the device. They support both differential and single-ended clock signals. Refer to section 3.6 Inputs (IN0, IN1, IN2, IN3) for input termination options. These pins are high-impedance and must be terminated externally, when being used. The negative side of the differential input must be ac-grounded when accepting a single-ended clock. Unused inputs may be left unconnected.
IN0b	64	I	
IN1	1	I	
IN1b	2	I	
IN2	14	I	
IN2b	15	I	
IN3/FB_IN	61	I	Clock Input 3/External Feedback Input. By default, these pins are used as the 4th clock input (IN3/IN3). They can also be used as the external feedback input (FB_IN/FB_IN) for the optional zero delay mode. See section 3.6.1 Manual Input Switching (IN0, IN1, IN2, IN3) for details on the optional zero delay mode.
IN3/FB_INb	62	I	
Outputs			

Pin Name	Pin Number	Pin Type[1]	Function
OUT0A	21	O	Output Clocks. These output clocks support a programmable signal swing and common mode voltage. Desired output signal format is configurable using register control. Termination recommendations are provided in section 3.8.3 Output Terminations and section . Unused outputs should be left unconnected.
OUT0Ab	20	O	
OUT0	24	O	
OUT0b	23	O	
OUT1	28	O	
OUT1b	27	O	
OUT2	31	O	
OUT2b	30	O	
OUT3	35	O	
OUT3b	34	O	
OUT4	38	O	
OUT4b	37	O	
OUT5	42	O	
OUT5b	41	O	
OUT6	45	O	
OUT6b	44	O	
OUT7	51	O	
OUT7b	50	O	
OUT8	54	O	
OUT8b	53	O	
OUT9	56	O	
OUT9b	55	O	
OUT9A	59	O	
OUT9Ab	58	O	
Serial Interface			
I2C_SEL	39	I	**I2C Select.** This pin selects the serial interface mode as I**2C (I2C_SEL = 1) or SPI (I2C_SEL = 0). This pin is internally pulled high.**
SDA/SDIO	18	I/O	**Serial Data Interface.** This is the bidirectional data pin (SDA) for the I**2C mode, the bidirectional data pin (SDIO) in the 3-wire SPI mode, or the input data pin (SDI) in 4-wire SPI mode. When in I2C mode, this pin must be pulled-up using an external resistor of at least 1 k**W**. No pull-up resistor is needed when in SPI mode. This pin is 3.3 V tolerant.**

Pin Name	Pin Number	Pin Type[1]	Function
A1/SDO	17	I/O	**Address Select 1/Serial Data Output.** In I**2C mode this pin functions as the A1 address input pin. In 4-wire SPI mode, this is the serial data output (SDO) pin. This pin is 3.3 V tolerant.**
SCLK	16	I	**Serial Clock Input.** This pin functions as the serial clock input for both I**2C and SPI modes. When in I2C mode, this pin must be pulled-up using an external resistor of at least 1 kΩ. No pull-up resistor is needed when in SPI mode. This pin is 3.3 V tolerant.**
A0/CSb	19	I	Address Select 0/Chip Select. This pin functions as the hardware controlled address A0 in I2C mode. In SPI mode, this pin functions as the chip select input (active low). This pin is internally pulled-up. This pin is 3.3 V tolerant.
Control/Status			
INTRb	12	O	**Interrupt**[2]. This pin is asserted low when a change in device status has occurred. It should be left unconnected when not in use.
PDNb	5	I	**Power Down**[2]. The device enters into a low power mode when this pin is pulled low. This pin is internally pulled-up. This pin is 3.3 V tolerant. It can be left unconnected when not in use.
RSTb	6	I	**Device Reset.**[2] Active low input that performs power-on reset (POR) of the device. Resets all internal logic to a known state and forces the device registers to their default values. Clock outputs are disabled during reset. This pin is internally pulled-up. This pin is 3.3 V tolerant.
OEb	11	I	**Output Enable**[2]. This pin disables all outputs when held high. This pin is internally pulled low and can be left unconnected when not in use. This pin is 3.3 V tolerant.

Pin Name	Pin Number	Pin Type[1]	Function
LOLb	47	O	**Loss Of Lock**[2]. This output pin indicates when the DSPLL is locked (high) or out-of-lock (low). It can be left unconnected when not in use.
SYNC	48	I	**Output Clock Synchronization**[2]. An active low signal on this pin resets the output dividers for the purpose of re-aligning the output clocks. This pin is internally pulled-up and can be left unconnected when not in use.
IN_SEL0	3	I	**Input Reference Select**[2]. The IN_SEL[1:0] pins are used in manual pin controlled mode to select the active clock input as shown in Table 3.2 Manual Input Selection Using IN_SEL[1:0] Pins on page 11
IN_SEL1	4	I	
XA	8	I	Oscillator input. Single-ended input must be connected to the XA pin, with the XB pin appropriately terminated.
XB	9	I	
RSVD	7	NC	**Reserved.** Leave disconnected.
	10	NC	
	25	NC	
Power			
VDD	32	P	Core Supply Voltage. The device operates from a 1.8 V supply. A 1 uF bypass capacitor should be placed very close to each pin.
VDD	46	P	
VDD	60	P	
VDDA	13	P	Core Supply Voltage 3.3 V. This core supply pin requires a 3.3 V power source. A 1 uF bypass capacitor should be placed very close to this pin.

Pin Name	Pin Number	Pin Type[1]	Function
VDDO0	22	P	Output Clock Supply Voltage. Supply voltage (3.3 V, 2.5 V, 1.8 V) for OUTn, OUTn outputs. Note that VDDO0 supplies power to OUT0 and OUT0A; VDDO9 supplies power to OUT9 and OUT9A. Leave VDDO pins of unused output drivers unconnected. An alternative option is to connect the VDDO pin to a power supply and disable the output driver to minimize current consumption.
VDDO1	26	P	
VDDO2	29	P	
VDDO3	33	P	
VDDO4	36	P	
VDDO5	40	P	
VDDO6	43	P	
VDDO7	49	P	
VDDO8	52	P	
VDDO9	57	P	
GND PAD		P	Ground Pad. This pad provides connection to ground and must be connected for proper operation.

Note:

1. I = Input, O = Output, P = Power
2. The IO_VDD_SEL control bit (0x0943 bit 0) selects 3.3 V or 1.8 V operation.

10. Package Outlines

10.1 Si5381/82 9x9 mm 64-QFN Package Diagram

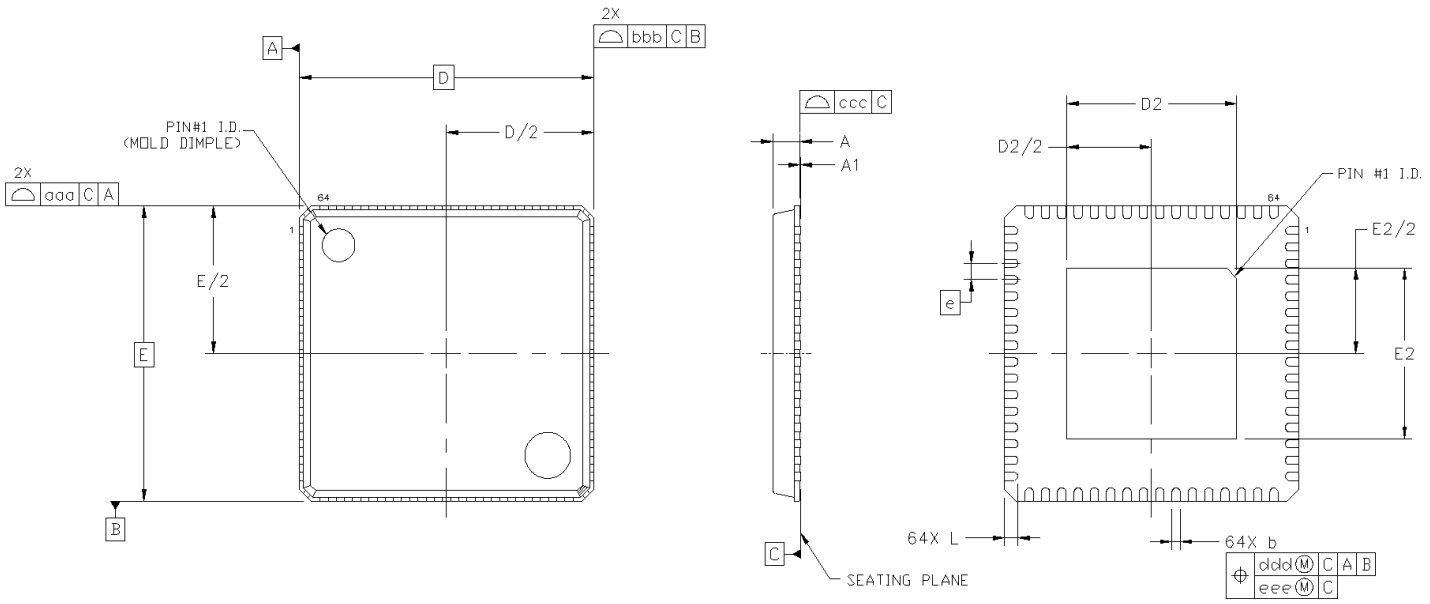


Figure 10.1. Si5381/82 9x9 mm 64-QFN Package Diagram

Table 10.1. Package Diagram Dimensions

Dimension	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		9.00 BSC	
D2	5.10	5.20	5.30
e		0.50 BSC	
E		9.00 BSC	
E2	5.10	5.20	5.30
L	0.30	0.40	0.50
aaa	—	—	0.15
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

11. PCB Land Pattern

The following figure illustrates the PCB land pattern details for the devices. The table lists the values for the dimensions shown in the illustration.

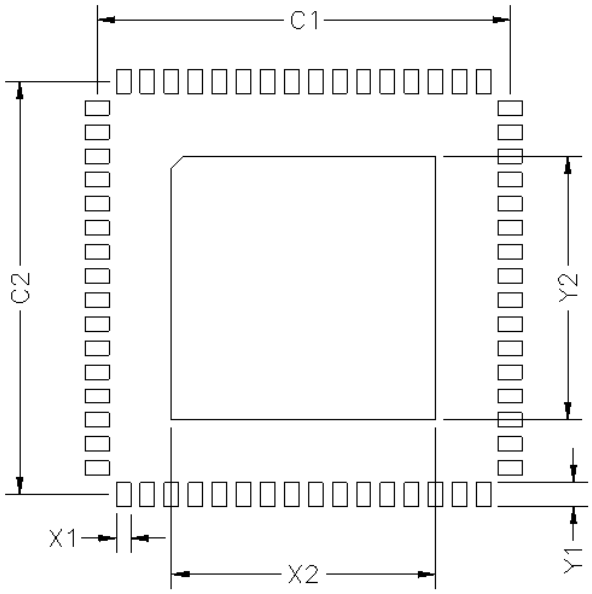


Figure 11.1. PCB Land Pattern

Table 11.1. PCB Land Pattern Dimensions

Dimension	Si5381/82 (Max)
C1	8.6
C2	8.6
E	0.50
X1	0.30
Y1	0.50
X2	5.5
Y2	5.5

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition is calculated based on a fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electropolished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. A 2x2 array of 0.65mm square openings on a 0.90mm pitch should be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

12. Top Marking

Figure 12.1. Si5381/82 Top Marking

Table 12.1. Top Marking Explanation

Line	Characters	Description
1	Si538fg-	Base part number and Device Grade for Any-frequency, Any-output, Jitter Cleaning Clock: f = 1, Quad DSPLL Clock f = 2, Dual DSPLL Clock g = A (External XO)
2	Rxxxxx-GM	R = Product revision. (Refer to 2. Ordering Guide for latest revision). xxxxx = Customer specific NVM sequence number. Optional NVM code assigned for custom, factory pre-programmed devices. Characters are not included for standard, factory default configured devices. See 2. Ordering Guide for more information. -GM = Package (QFN) and temperature range (–40 to +85 °C)
3	YYWWTTTTTT	YYWW = Characters correspond to the year (YY) and work week (WW) of package assembly. TTTTTT = Manufacturing trace code.
4	Circle w/ 1.6 mm (64-QFN) diameter	Pin 1 indicator; left-justified
	e4 TW	Pb-free symbol; Center-Justified TW = Taiwan; Country of Origin (ISO Abbreviation)

13. Device Errata

See https://www.skyworksinc.com/en/Products/Timing to access the device errata document.

14. Document Change List

14.1 Revision 1.0

February, 2020

- Updated Section 3. Functional Description.
- Updated Figure 3.2 Figure 3.2. Example Divider Configuration for Generating JESD204B Subclass 1 Clocks on page 7.
- Updated Section 3.6. Inputs.
- Updated Section 3.7.3. OOF Detection.
- Modified various tables on Section 5. Electrical Specifications.
- Modified various diagrams on Section 7. Detailed Block Diagrams.
- Updated Section 9. Pin Descriptions.

14.2 Revision 0.96

April, 2019

- Tightened Output-Out Skew (different MultiSynths) specifications.
- Added Input-Output Delay Variation specifications.

14.3 Revision 0.95

September, 2018

- Reorganized and rewritten to address updates that are focused on the ultra-high performance wireless jitter attenuator feature for optimized wireless BBU (Baseband Unit) and DU (Distribution Unit) applications.

14.4 Revision 0.9

September, 2017

- Initial release.