DATA SHEET

Si830x Smart Switch Data Sheet

Description

The Si830x provides four high-side or low-side switches with low R_{ON}. These switches are ideal for driving resistive and inductive loads like solenoids, relays, and lamps commonly found in industrial control systems like Programmable Logic Controllers (PLC). They are easily interfaced directly to an MCU, or controlled through a digital isolator or optocoupler-based isolation barrier.

The logic interface supports low-power 2.5 V to 5 V MCUs and is powered by the switch's high-voltage field power supply. The field power supply supports a wide supply range, from 9 V to 32 V, making it ideal for industrial voltage levels. The switches are capable of providing 0.7 A under any valid load condition. An innovative multi-voltage clamp efficiently handles an unlimited amount of demagnetization energy (EAS). Each switch offers complete fault protection. A unique power estimation based overcurrent protection keeps the device cool and operational, even during a short circuit event. Additionally, the device power supplies are monitored, and the switches are safely constrained or shutdown on faults.

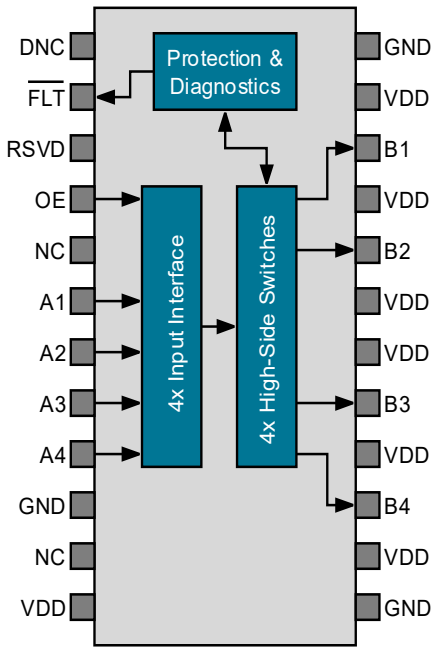
Three diagnostics are reported through an active-low, open-drain fault indicator pin ($\overline{FLT}$). It can be connected to an LED for instant user feedback, connected to an MCU for advanced software control, or tied together with additional fault pins from other devices to simplify user feedback or reduce board layout complexity.

Applications

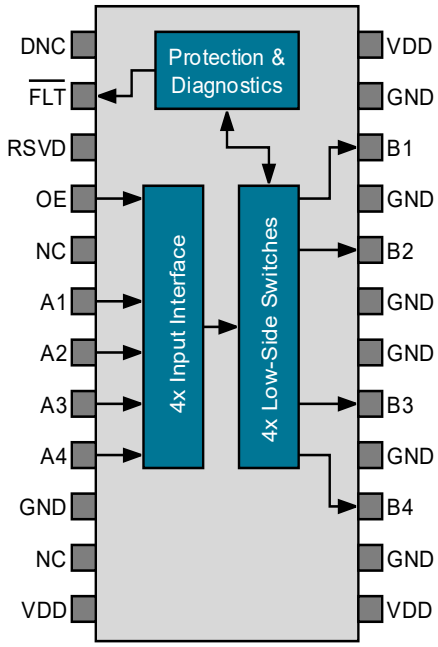
- Programmable logic controllers
- Industrial data acquisition
- Motion controllers
- Smart solid-state relays

Key Features

- High-side or low-side switch
- Switch Supply: 9 V–32 V
- Fast (10 µs) update rate
- High continuous current (700 mA) and low R_{ON} (150 mΩ)
  - Unique multi-voltage output clamp
  - Unlimited demagnetization (E_{AS})
- Efficient and fast turn-OFF
- Current-limited overload protection
- Over temperature protection
- Undervoltage protection
- Three different diagnostics
  - Overvoltage
  - Over temperature
  - Overcurrent
- Dedicated fault indicator
- Dedicated output enable input
- Designed to IEC 61131-2
- Compact TSSOP-24 package
- 3.5 kV ESD Protection
- –40 to 125 °C operating temperature



Si83004BF-IT



Si83014BF-IT

1. Ordering Guide

Table 1. Si830x Ordering Guide

Ordering Part Number[1,2]	Output Driver Type[3]	Input Interface	Output Channels	Continuous Output Current	Inrush Current Mode
Si83004BF-IT	Sourcing	Parallel	4	700 mA	No
Si83014BF-IT	Sinking	Parallel	4	700 mA	No

1. "Si" and "SI" are used interchangeably.
2. An "R" at the end of the Ordering Part Number indicates the tape and reel option.
3. Output switch can source current in a high-side, open-source configuration or sink current in a low-side, open-drain configuration.

2. System Overview

A single channel of the Si830x Smart Switch is analogous to a relay driver with protection against common fault mechanisms. The Si830x can be paired with a multi-channel digital isolator like the six-channel Si8661x from the Skyworks Si86xx digital isolator family, or an array of optocouplers. The combination of smart switch and isolator creates a complete, galvanically isolated output channel solution. Alternatively, the Si834x Isolated Smart Switch can be used for a fully integrated solution.

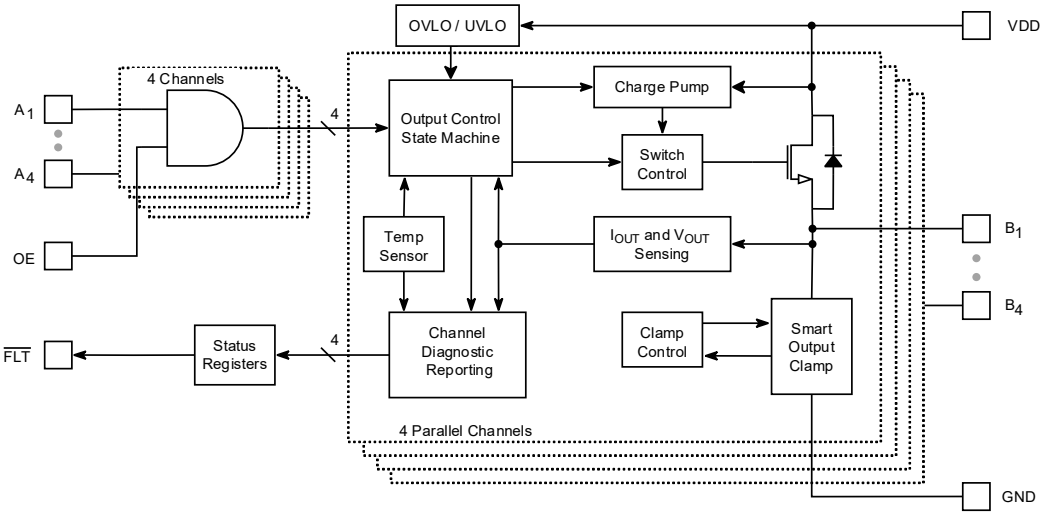


Figure 1. Parallel/SPI Sourcing Device System Diagram

The fundamental channel structure described above is augmented using a number of innovative technologies. The output switch is a low ON-State Resistance (R_{ON}) device capable of driving inductive and resistive loads at continuous currents of 700 mA. It includes precise voltage, current, and temperature sensors that continuously monitor the switch and load conditions, protecting the device by reducing driver performance or forcing a controlled shutdown when necessary.

The logic interface to the switch operates from the high-voltage field power supply (VDD), but remains compatible with TTL logic levels (see “5. Electrical Specifications” on page 28 for details on exact logic levels and maximum voltage rating.) This simplifies power supply design while maintaining the flexibility to control the smart switch with low-voltage devices like digital isolators, optocouplers, and MCUs where a low-voltage supply may or may not be required.

The switch uses a sophisticated multi-voltage output clamp, called a “smart output clamp”, that both protects the switch from harmful inductive kickback voltage (or back EMF) and offers fast demagnetization of inductors to reduce contact arcing and increase switching speed.

Four identical channels are packaged together into an Si830x device, each with its own set of sensors. Switches are controlled independently and gated by an asynchronous output-enable (OE) function to ensure safe operation only when the system is ready. Three different diagnostics are reported on an active-low, open-drain indicator pin ($\overline{FLT}$) designed to drive an LED or be read by the controller. See “3.5. Diagnostics” on page 19 for more information on the available diagnostic reports exposed on this pin.

3. Device Operation

This section describes the capabilities of the Si830x Isolated Smart Switch devices and how they should be used to achieve different goals within a design. Refer to "1. Ordering Guide" on page 3 and "4.1. Recommended Application Circuits" on page 22 for information on specific devices and how they are designed into different applications.

3.1. Truth Table

Table 2 describes the logical behavior of the Si830x Smart Switch devices. Use this table to determine the state of a specific channel's outputs on an Si830x device based on the device's current state and inputs. The state of other device channels also impacts some channel output states. When applicable, this is described in the table's footnotes.

Table 2. Si830xxxF Truth Table

Mode	Inputs[1]		State[2]		Outputs	
	An	OE	VDD[3]	Fault[4]	$\overline{FLT}$[5]	Bn[6]
Fault	X	X	NP	D	U	OFF
	X	X	P	D	ON	OFF[7]
Normal	L	X	P	ND	OFF	OFF
	X	L	P	ND	OFF	OFF
	H	H	P	ND	OFF	ON

1. "X" is any logic value, "H" is a logic high (true) value, and "L" is a logic low (false) value. Logic pins should always be connected to either logic high or low. Logic values listed in this table are assumed to transition at the same time as the device state.
2. "NP" is the "not powered" state; "P" is the "powered" state; "ND" is the "not detected" state, and "D" is the detected state.
3. "Not powered" (NP) state is defined as VDD < VDD_{UV}. "Powered" (P) state is defined as VDD > VDD_{UV}. See Table 7, "Power Supply Characteristics," on page 28 for details.
4. The VDD "not powered" (NP) state forces a Fault "detected" (D) state. One or more fault conditions will result in a "detected" (D) state. The fault state automatically changes to "not detected" (ND) when all fault conditions are removed. Fault conditions are defined in "3.4. Switch Protection" on page 9.
5. "Undetermined" (U) can be any value within the absolute maximum rating of the output. The output is both active-low and open-drain. See "4.1. Recommended Application Circuits" on page 22 for more information. The output is not synchronous with the detection of a fault state. See "3.2. Switch Timing Behavior" on page 6 for details. Not all fault conditions will generate a diagnostic report indicated by the FLT output. See "3.5. Diagnostics" on page 19 for details on what fault conditions generate a diagnostic report.
6. The electrical characteristics for ON and OFF vary based on device selection, switch protection conditions, and switch supply conditions. See "3.3. Switch Types" on page 8 and "3.4. Switch Protection" on page 9 for more information.
7. If an Over Temperature Constraint fault is detected while the output is ON, the output will not immediately shut-down. If an Over Temperature Constraint fault is detected while the output is OFF, the output will be prevented from turning ON. If an Overvoltage Constraint fault is detected, the output will operate normally, but demagnetization performance will be constrained. See "3.4. Switch Protection" on page 9 for more information.

In Table 2, all inputs, outputs, and states apply to the entire device, except for An and Bn, which apply to a specific channel n. The Fault state is "detected" (D) if any fault conditions are detected on any channel, and is "not detected" (ND) only when all fault conditions are removed from all channels. See "3.4. Switch Protection" on page 9 for details on what fault conditions can be detected by the smart switch. Some fault conditions when detected will result in a diagnostic report. The FLT output indicates when diagnostic reports are present. It is a logical OR of all diagnostic reports present for all channels within the device. See "3.5. Diagnostics" on page 19 for more details on the diagnostic reports that will cause the FLT output to turn on.

3.2. Switch Timing Behavior

The time required for the Si830x output switch to change states depends on the state of the power supply, the state of the inputs, or any detected fault conditions. In the first figure below, the analog power supply voltage (VDD) is plotted against the digital input and output state of the device, with relevant device timings listed. The same regulated power supply is used for VDD and for the device which produces the control signals An/OE. It is important to note that the analog behavior of the Si830x device changes based on the switch type selected. See "3.3. Switch Types" on page 8 for details.

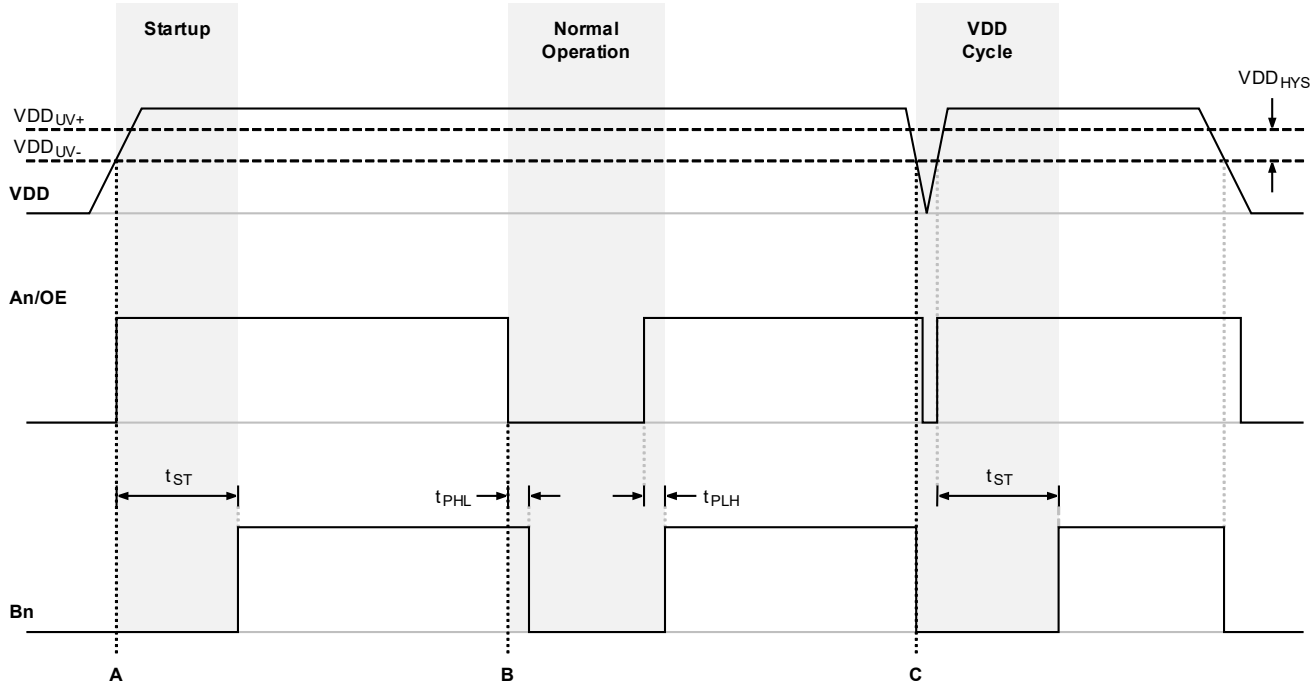


Figure 2. Switch Timing Behavior

At Marker A in the Switch Timing Behavior figure above, the power supply voltage (VDD) begins transitioning from unpowered to powered by crossing the falling undervoltage lockout threshold (VDD_{UV-}). At this point, the device begins to start up, and startup conditions must be met before the output state tracks the input: the Device Startup Time (t_{ST}) must elapse, and VDD must exceed the rising undervoltage lockout threshold (VDD_{UV+}). Note that the analog timing behavior from device input to device output is depicted in Figure 14, "Turn ON and Turn OFF Timing," on page 29.

At Marker B, the input control signal is turned off. After the Turn OFF Propagation Delay (t_{PHL}) elapses, the output will turn off. When the input is turned back on, an additional Turn ON Propagation Delay (t_{PHL}) must elapse before the output returns to the ON state.

At Marker C, VDD is turned completely off to begin a power cycle. When VDD drops below VDD_{UV-}, the output immediately turns off. The device must then meet the startup conditions before the output state tracks the input again.

In Figure 3 below, two unique fault conditions that generate diagnostic reports are plotted against the $\overline{FLT}$ output. The $\overline{FLT}$ output indicates if there are any fault reports in the device. The smart switch can detect and protect itself from a range of unique fault conditions, but only some fault conditions will generate a diagnostic report. See "3.4. Switch Protection" on page 9 and "3.5. Diagnostics" on page 19 for details on fault conditions, such as over-current and over-temperature, which also generate diagnostic reports.

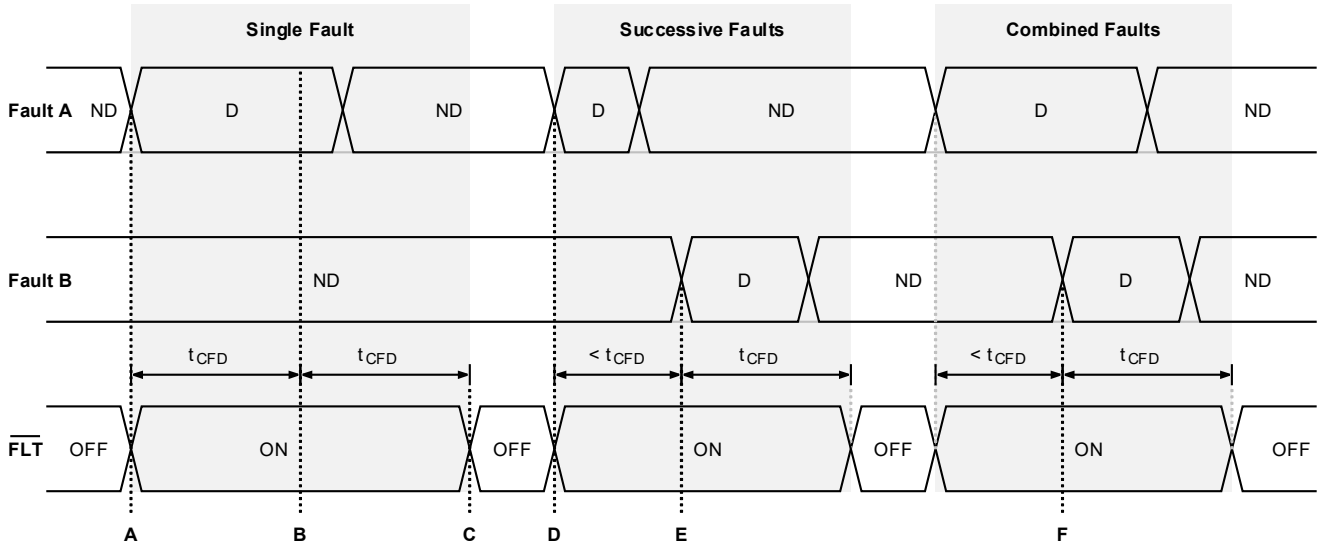


Figure 3. Switch Fault Behavior

At Marker A, a fault condition that generates a diagnostic report is detected (Fault A). The $\overline{FLT}$ output is immediately turned on and will remain on for the duration of the Clear Fault Delay (t_{CFD}). At Marker B, after t_{CFD} has expired, the fault condition is still detected and thus $\overline{FLT}$ remains on for another duration of t_{CFD}. The $\overline{FLT}$ output will only turn off after t_{CFD} has expired and no fault condition that generates a diagnostic report is detected, as depicted at Marker C. Otherwise, this cycle will repeat indefinitely as long as the fault condition remains detected.

At Marker D, the same fault condition (Fault A) is detected again and the $\overline{FLT}$ output is turned on. However, before t_{CFD} has expired, a different fault condition that generates a diagnostic report (Fault B) occurs. This new fault condition resets the t_{CFD} timer and the $\overline{FLT}$ output remains on, as depicted at Marker E.

It is important to note that any new fault condition that generates a diagnostic report will reset the t_{CFD} timer, even if other fault conditions remain present, as depicted at Marker F. This ensures that any diagnostic report is indicated on the $\overline{FLT}$ output for at least one duration of t_{CFD}, and may be indicated for multiples of t_{CFD} depending on the duration of the fault conditions that generate diagnostic reports within the device.

3.3. Switch Types

The Si830x Smart Switch is available in two switch configurations to meet a broad range of application requirements.

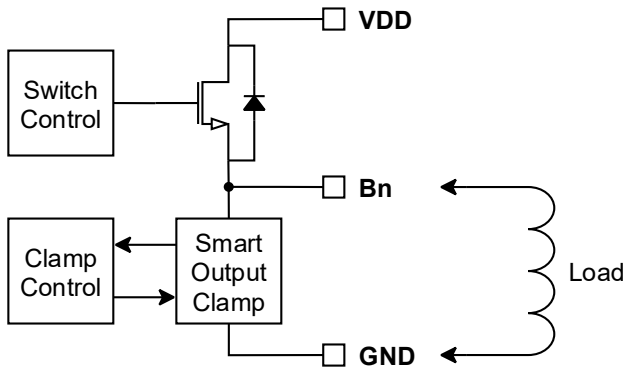


Figure 4. Sourcing Device

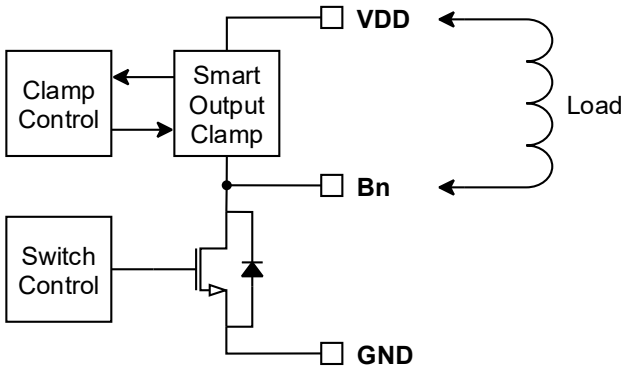


Figure 5. Sinking Device

As shown in the figures above, the sourcing configuration operates as an open-source output for high-side switching. Its analog behavior is to connect Bn to VDD when the switch is turned ON. The sinking configuration uses an open-drain output for low-side switching. Its analog behavior is to connect Bn to GND when the switch is turned ON. Both the sourcing and sinking output configurations are designed to be IEC61131-2 compliant. Each switch can source or sink 700 mA of continuous current.

To reliably achieve continuous currents of 700 mA, follow the circuit design and layout recommendations in this document. See “4.1. Recommended Application Circuits” on page 22 and “4.2. Layout Considerations” on page 24 for details on designing for high continuous current devices.

All switches include a smart output clamp to quickly and safely demagnetize inductive loads, as well as advanced overcurrent protection and over temperature protection. When the switch is OFF, the output can be considered high impedance (Hi-Z). However, the demagnetization clamp will engage in the OFF state if the voltage on the output pin exceeds the Demagnetization Clamp High Voltage (V_{CLMPH}) specification which will cause the clamp to conduct. The body diode of the switch will also conduct in the OFF state if the voltage on the output pin exceeds the supply voltage (VDD) on a sourcing device or the ground reference (GND) on a sinking device by more than a diode forward voltage drop (V_F.) See Figure 21 and Figure 22 on page 33 for details on the output behavior when the switch is OFF.

3.4. Switch Protection

The Si830x Smart Switch contains sophisticated protection technology. It is designed to operate for decades driving a broad range of loads. It can seamlessly recover from faults ranging from a simple power supply overvoltage, to a dead short on a driven output channel. The following sections detail individual methods of protection, and how they behave in common scenarios

3.4.1. Demagnetization Energy Protection

The Si830x Smart Switch includes a high efficiency, multi-voltage “smart” output clamp used to protect the switch from harsh demagnetization voltage, commonly referred to as back EMF, flyback voltage, inductive voltage “kick-back”, or a “voltage kick.” The smart clamp is actively controlled based on the current through the switch, the switch supply voltage, and the switch temperature. By dynamically adjusting the clamp voltage based on device and load conditions, the Si830x balances safety with performance. It limits device power dissipation to safe levels while still delivering fast turn-off performance that ensures fast relay switching as well as reduces arcing and arc welding failures in relays.

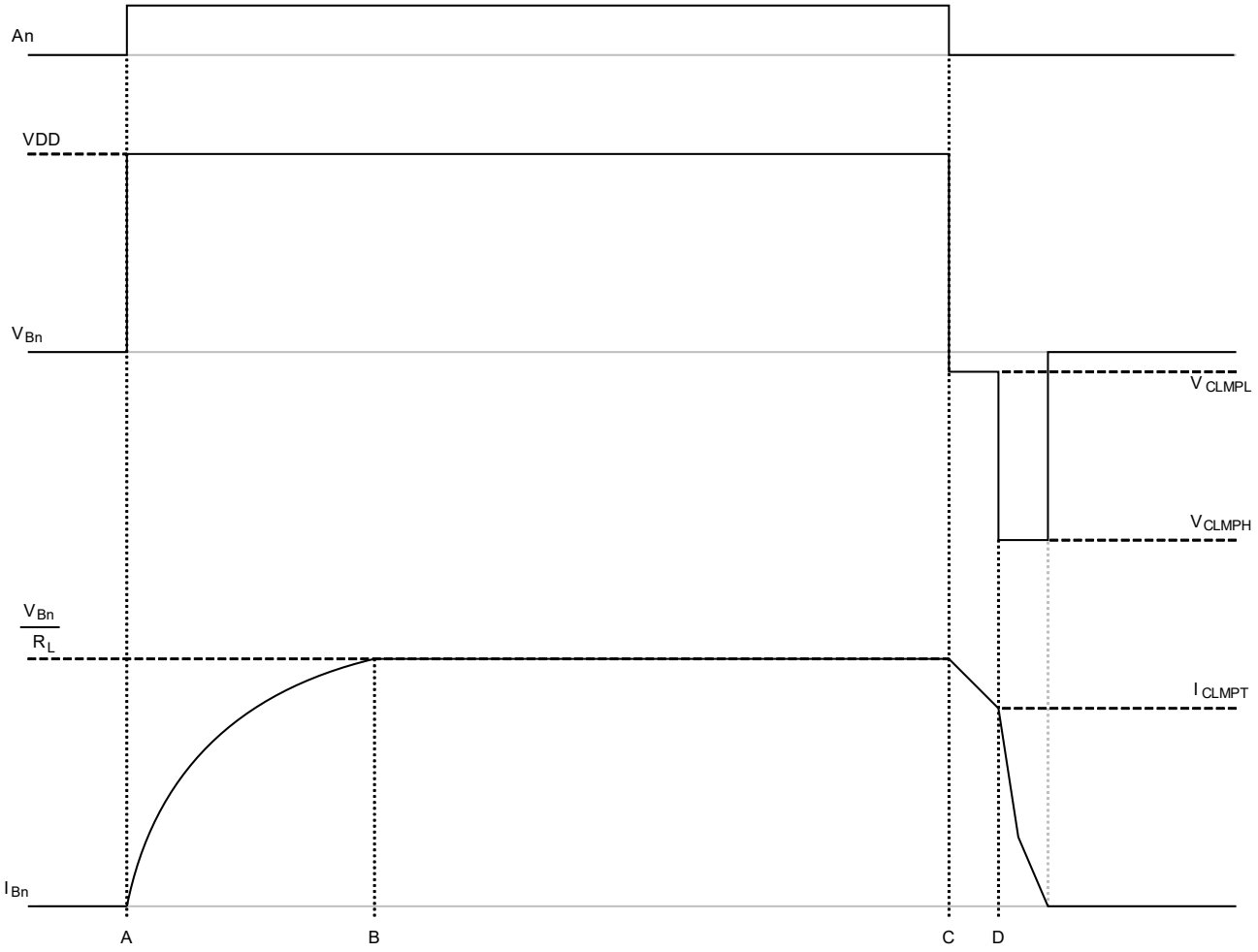


Figure 6. Demagnetization Protection Behavior

The figure above illustrates the behavior of a high-side (sourcing) Si830x switch when driving a relay at the switch's typical ON State Load Current ($I_{O(ON)}$) and under normal operating conditions. It plots the digital input to the switch (An) as well as the output voltage (V_{Bn}) and output current (I_{Bn}) from the switch. It assumes a simplified model for the relay coil of a simple inductor (L) in series with a resistor (R_L). All plots are for a specific channel, with n specifying the channel number.

In order to understand the switches demagnetization protection, it is important to remember the equation for voltage and current through an inductor.

$$\frac{dI_L(t)}{dt} = \frac{1}{L}V_L(t)$$

Equation 1.

Where:
I_L is the current through the inductor (I.)
L is the inductance (H.)
V_L is the voltage across the inductor (V.)

At Marker A, the channel is turned on and begins to energize the load inductance.

At Marker B, the load inductance is fully energized.

At Marker C, the switch is turned off while driving a fully charged coil. The coil inductance resists a change in current by generating a very large negative voltage at the switch output (Bn) and across the smart output clamp. Initially, the clamp voltage is constrained to the Demagnetization Clamp Low Voltage (V_{CLMPL}) because the current through the smart clamp exceeds the Demagnetization Clamp Current Threshold (I_{CLMPT}). Despite the large load current, the power dissipation in the channel is low because the clamp voltage is low.

At Marker D, the current through the clamp falls below I_{CLMPT} and the clamp voltage is changed to Demagnetization Clamp High Voltage (V_{CLMPH}). The higher clamp voltage increases the rate of demagnetization in the inductor. The increased power dissipation during this phase of protection will cause a small temperature rise in the channel, but with inductor current sufficiently constrained below I_{CLMPT}, this rise is easily tolerated by other channels in the Si830x device.

This two-step approach to turning off an inductor gives the Si830x the ability to demagnetize an unlimited amount of energy from a single turn-off pulse, on a single channel ($E_{AS(1CH)}$). See Table 12, "Absolute Maximum Ratings," on page 31 for maximum energy dissipation under other conditions.

3.4.2. Overcurrent Protection

The Si830x Smart Switch includes short circuit-proof over current protection with automated restart. The Si830x rapidly samples current through the switch, disabling the output while an overcurrent condition remains present. This contrasts with other switches that depend on an increased switch resistance and thermal protection alone to limit the current through the switch. The novel approach used by the Si830x drastically reduces the power dissipation through the switch during an over-current condition, eliminating the need for thermal independence of separate channels, increasing the lifespan of the switch, simplifying the thermal requirements and power supply design of the end-system, and still ensuring safe operation of the switch even with a dead short present for an indefinite amount of time.

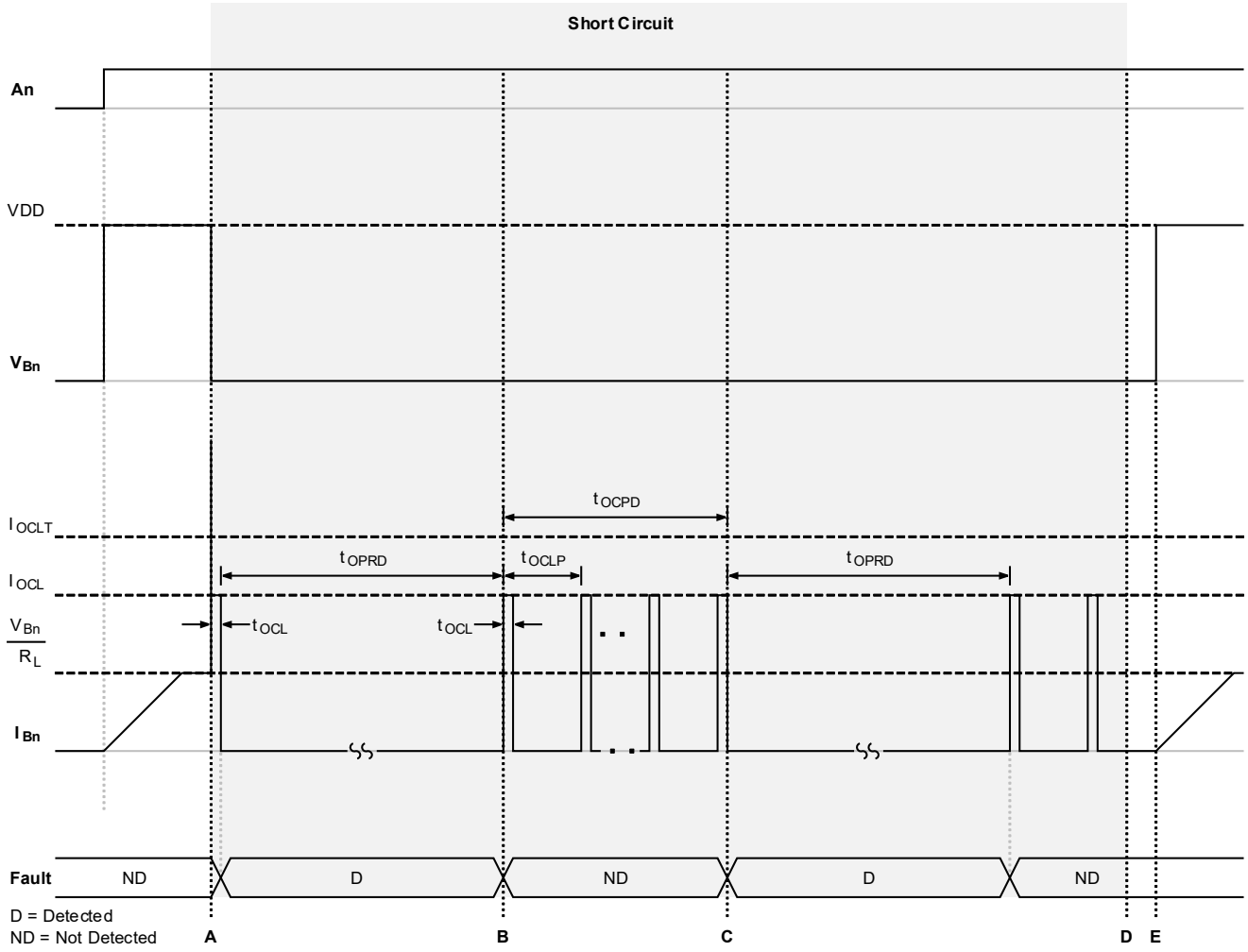


Figure 7. Over-Current Shutdown Behavior

The figure above illustrates the behavior of a high-side (sourcing) Si830x switch when driving an inductor at the switches' typical ON State Load Current ($I_{O(ON)}$). Initially, normal operating conditions exist, but a short circuit occurs at Marker A. Note that Marker B depicts the Si830x switches' behavior when it is turned on in a short circuit state. The figure plots the digital input to the switch (An) as well as the output voltage (V_{Bn}) and output current (I_{Bn}) from the switch where *n* is a specific channel number. It also illustrates the Fault state of the device under the assumption that no fault conditions are present other than an Overcurrent Shutdown event. See "3.1. Truth Table" on page 5 for details on the device state. See Figure 2, "Switch Timing Behavior," on page 6 for a description of how the Fault state impacts the behavior of the $\overline{FLT}$ output.

Initially, the switch channel is turned on and the load inductor is fully charged. The current must exceed the Output Current Limit Threshold (I_{OCLT}) for the switch to detect an overcurrent condition and engage its overcurrent protection. At Marker A, a dead short (roughly 0 Ω resistance) is placed on the output to the switch channel which causes an immediate voltage drop and current rise well above I_{OCLT}. The Si830x device then engages its overcurrent protection and limits the current to the Output Current Limit (I_{OCL}) by altering the resistance of the switch. If the overcurrent condition is not removed within the Output Current Limit Pulse time (t_{OCL}), the output is immediately shut down and a Fault is detected (D). The channel will remain shut down for the duration of the Overcurrent Protection Retry Delay (t_{OPRD}).

After the Overcurrent Protection Retry Delay has expired at Marker B, the Fault state is cleared (ND) if no other faults are present, and the channel is turned on again. On startup, the resistance of the switch will once again be adjusted to limit the current to I_{OCL} for no longer than t_{OCL}, at which point the channel will shut down again to protect itself from high power dissipation. The switch will attempt to turn on again in the same way, multiple times, at a retry period equal to Output Current Limit Period (t_{OCLP}), and for up to the Overcurrent Protection Duration (t_{OCPD}). If the overcurrent condition is no longer detected at any time during an Over Current Limit Pulse (t_{OCL}), the switch resistance is immediately reduced to normal ON-State Output Resistance (R_{ON}). If a short circuit or other overcurrent condition is not resolved after t_{OCPD}, as depicted at Marker C, the output is once again shut down for t_{OPRD} and a Fault state is detected. This cycle will repeat indefinitely as long as the overcurrent condition remains detected.

At Marker D, the dead short is removed. The channel remains shut down until t_{OPRD} expires and no changes in the overcurrent condition are detected or reported. At Marker E, on the next retry attempt, the channel is turned on and resumes normal operation.

3.4.3. Over-Temperature Protection

The Si830x Smart Switch includes independent over temperature protection for each channel. It has two levels of protection that balance device safety with switch performance. The Si830x will continue to operate safely with reduced performance when individual channels are over temperature. Channels will only be shut down when all channels are detected to be over temperature.

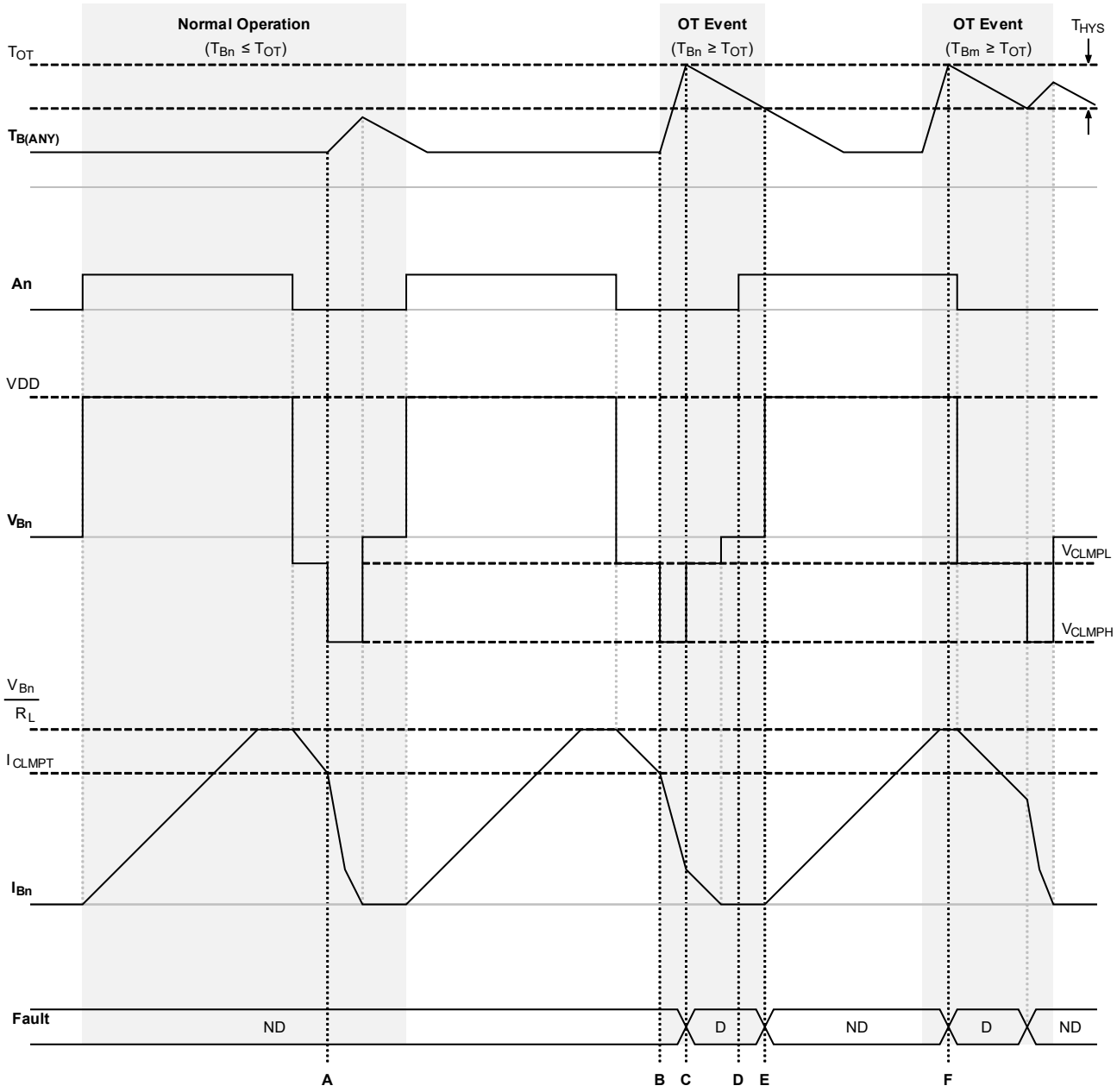


Figure 8. Over-Temperature Constraint Behavior

The figure above illustrates the behavior of a high-side (sourcing) Si830x switch when driving a coil at the switch's typical ON State Load Current ($I_{O(ON)}$), but then experiencing two different over temperature events (OT Event). The "Normal Operation" section is a simplification of Figure 6, "Demagnetization Protection Behavior," on page 9 and is included for reference. The figure plots the digital input to the switch (An), the temperature of any output channel ($T_{B(ANY)}$), as well as the output voltage (V_{Bn}) and output current (I_{Bn}) from the switch where *n* is a specific channel number. It also illustrates the Fault state of the device under the assumption that no faults are present other than the Over Temperature Constraint event. See "3.1. Truth Table" on page 5 for details on the device state. See Figure 2, "Switch Timing Behavior," on page 6 for a description of how the Fault state impacts the behavior of the FLT output.

Under normal conditions where the ambient temperature is limited to the Derated Ambient (T_{AD}, calculated in "4.3. Power Dissipation Considerations" on page 25), the most likely cause of over temperature is demagnetizing a large inductor (E_{AS}). This typically happens when the smart clamp is set to the Demagnetization Clamp High Voltage (V_{CLMPH}) and power dissipation is at its peak. This temperature rise is illustrated in the figure above at Marker A for an E_{AS}, which falls below the maximum specification of the device. See Table 12, "Absolute Maximum Ratings," on page 31 for more details on the absolute maximum specifications.

Marker B illustrates the switch behavior when the dissipated E_{AS} is too large for the current ambient temperature. When the Si830x smart clamp transitions to V_{CLMPH}, the switch temperature rises quickly until it reaches the Over Temperature Threshold (T_{OT}) at Marker C. At this point, the smart clamp for each Si830x channel is constrained to the Demagnetization Clamp Low Voltage (V_{CLMPL}), and a Fault state is detected. This protects the device by reducing power dissipation and forcing all inductors attached to the Si830x to demagnetize more slowly.

While the Si830x is over temperature on any channel, all channels are prevented from turning on in order to further reduce power dissipation and recover quickly, as illustrated at Marker D. Note that a channel experiencing an Overcurrent Shutdown will also have it's retry attempts suppressed during its Overcurrent Protection Duration (t_{OCPD}) period. Once the temperature of the channel falls below the Over Temperature Hysteresis (T_{HYS}) level as illustrated by Marker E, the Fault state is cleared if no other diagnostic reports are present, and all channels resume normal operation.

It is important to note that an over temperature condition on any channel will cause all channels to be constrained in the manner described above, such as preventing a channel from turning on. This is illustrated at Marker F where a different channel *m* (not illustrated) exceeds T_{OT}, forcing the illustrated channel (*n*) to remain at V_{CLMPL} and constraining its demagnetization performance.

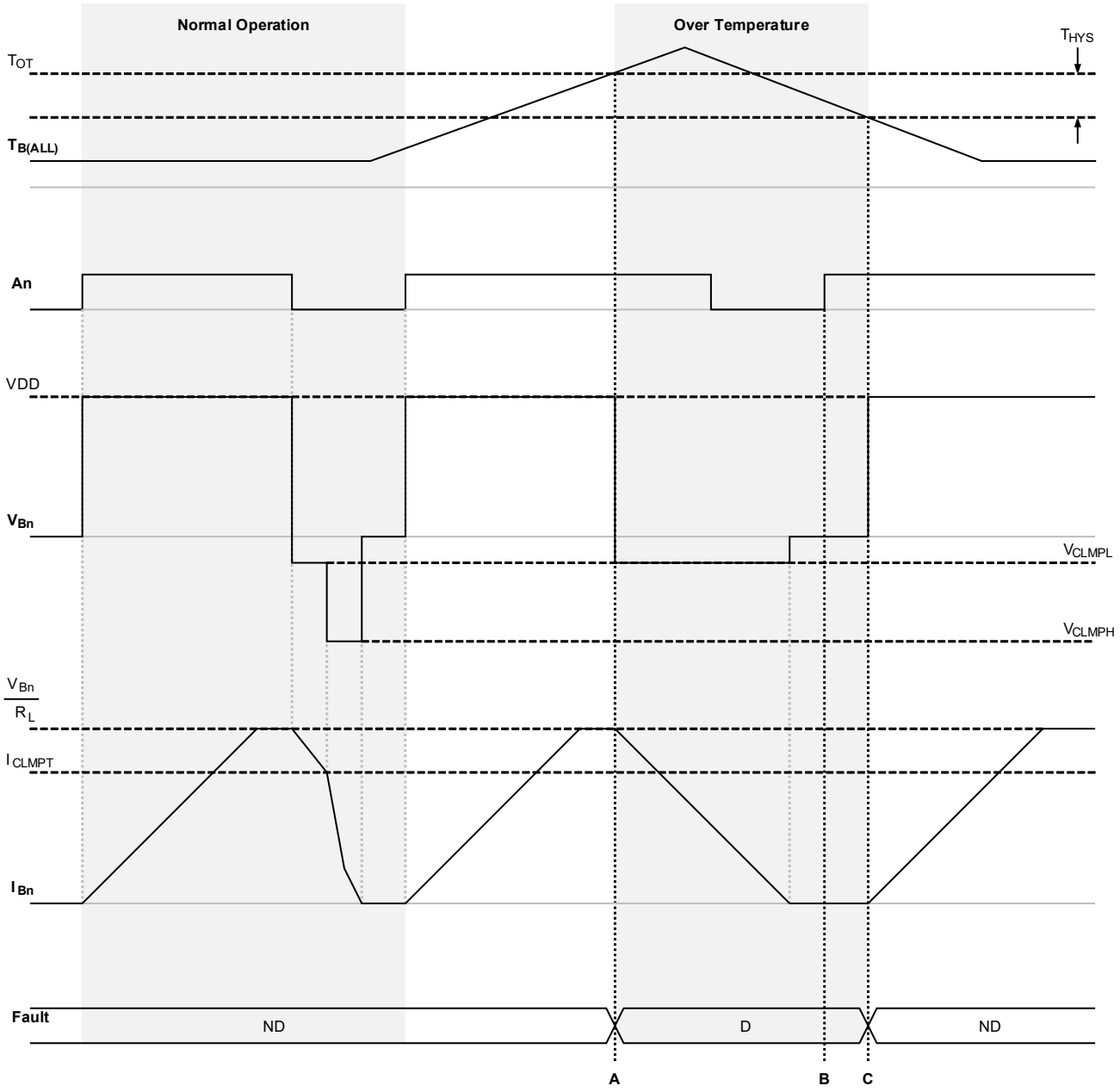


Figure 9. Over-Temperature Shutdown Behavior

If ambient temperature is not limited to T_{AD}, or if E_{AS} is much larger than the specified maximum, it is possible that the temperature of all channels ($T_{B(ALL)}$) will exceed T_{OT} as illustrated at Marker A in the figure above. In this event, all channels are immediately shut down, and a Fault state is detected. If a channel is driving an inductor, the smart clamp will be constrained to V_{CLMPL} and demagnetization time will be increased to help reduce power dissipation. All channels will be prevented from turning on (Marker B) until the temperature of all channels falls below T_{HYS} as depicted at Marker C. The Fault state will then be cleared if no other diagnostic reports are present, and all channels will resume normal operation.

3.4.4. Power Supply Protection

The Si830x Smart Switch monitors the power supply, protecting the device and load when the power supply is out of specification. Like the over temperature protection, the Si830x balances performance with safety by constraining switch performance under some power supply conditions and safely shutting down under others.

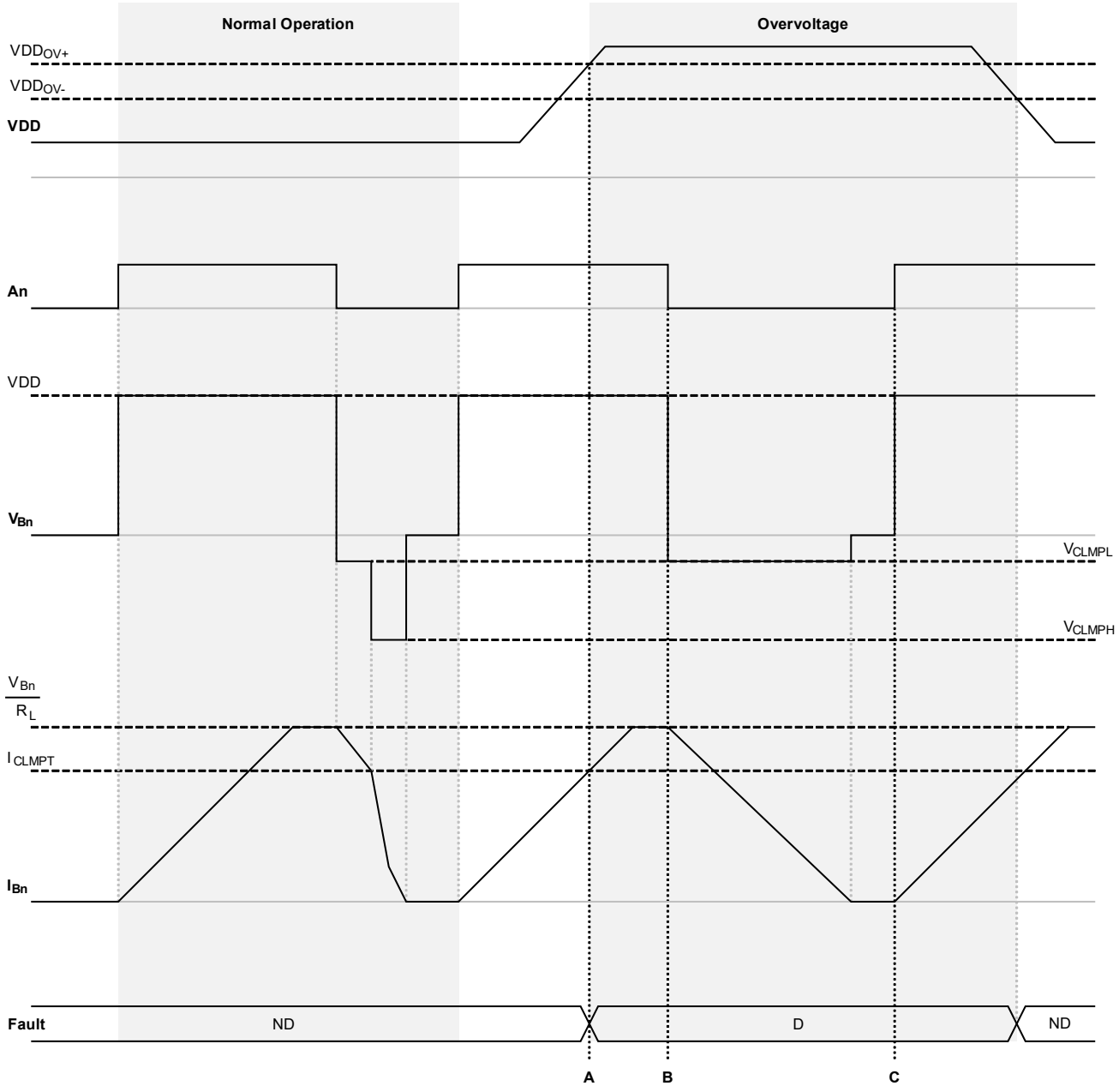


Figure 10. VDD Overvoltage Constraint Behavior

Figure 10 illustrates the behavior of a high-side (sourcing) Si830x switch when driving a coil at the switches' typical ON State Load Current ($I_{O(ON)}$) but then experiencing an overvoltage condition on the switch power supply (VDD). The "Normal Operation" section is a simplification of the Demagnetization Protection Behavior figure and is included for reference. The figure plots the digital input to the switch (An), the VDD supply voltage (VDD), as well as the output voltage (V_{Bn}) and output current (I_{Bn}) from the switch where *n* is a specific channel number. It also illustrates the Fault state of the device when no other fault conditions are present, other than an Overvoltage Constraint event. See the Truth Tables for details on the device state. See the Switch Timing Behavior for a description of how the Fault state impacts the behavior of the $\overline{FLT}$ output.

At Marker A, VDD exceeds the VDD Overvoltage Threshold (VDD_{OV+}). In order to reduce power dissipation to a safe level, the smart clamp for each channel is constrained to Demagnetization Clamp Low Voltage (V_{CLMPL}), and a Fault state is detected. While the smart clamp for each channel is limited to V_{CLMPL}, demagnetization performance is constrained and all inductive loads turn off more slowly as illustrated at Marker B. Unlike an Over Temperature Constraint, the output channels are not prevented from turning on (Marker C). Once VDD falls below VDD_{OV-} the smart clamp returns to "Normal Operation" and the Fault state is cleared if no other diagnostic reports are present.

It is important to note that overvoltage is not prevented from damaging the device if VDD remains above VDD_{OV+} or exceeds the absolute maximum specification. It only protects the device from higher power dissipation when demagnetizing an inductive load at higher voltages and generates a diagnostic report on the $\overline{FLT}$ output. If VDD exceeds the VDD ESD Clamp Threshold (VDD_{CLMP}), the VDD ESD clamp will engage, damaging the device.

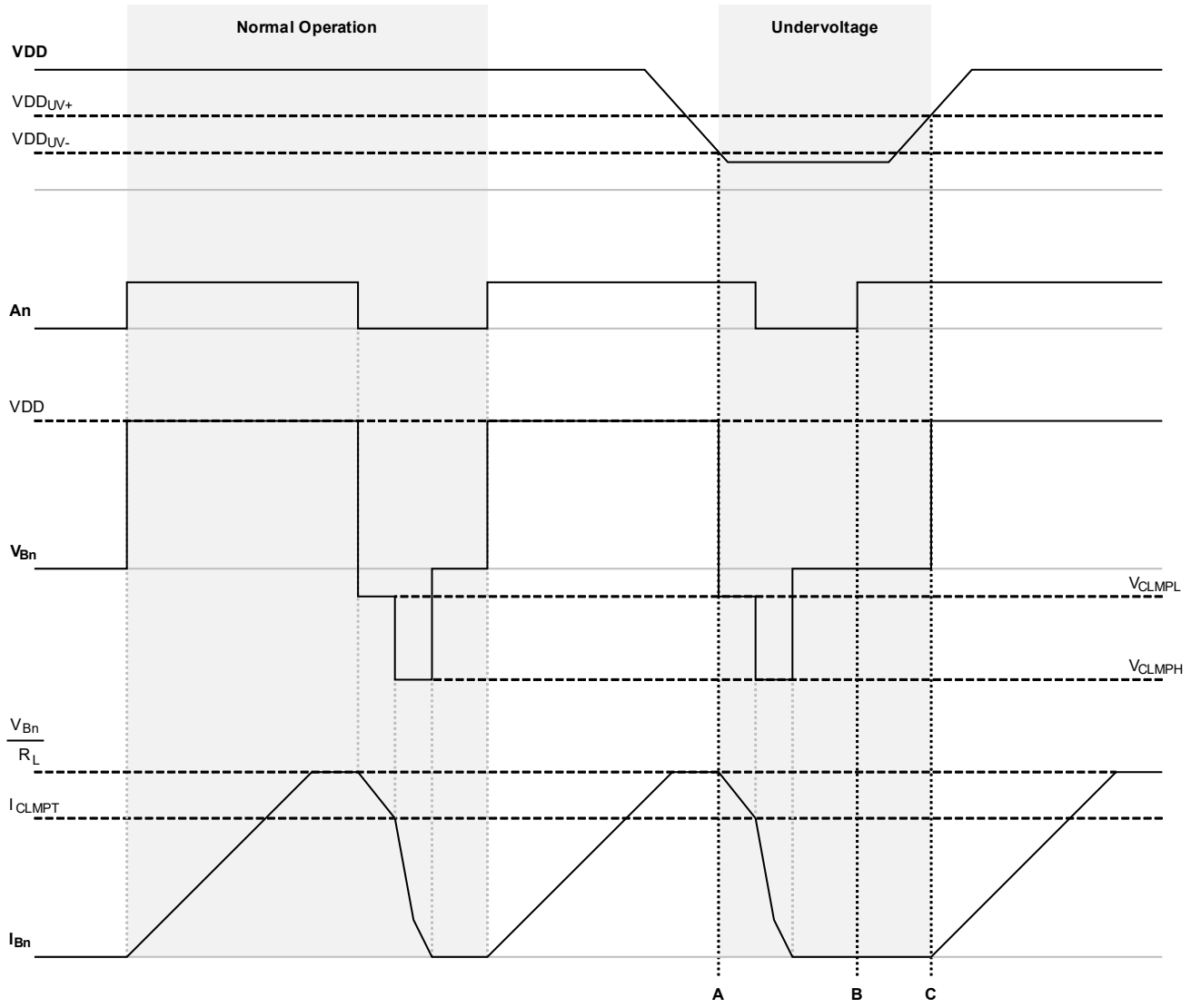


Figure 11. VDD Undervoltage Shutdown Behavior

The switch is protected against a VDD undervoltage condition in a very similar manner to VDD overvoltage conditions, as illustrated by the figure above. At marker A, VDD falls below the VDD Undervoltage Threshold (VDD_{UV-}). All channels are immediately shut down. Note that the smart clamp behavior during shutdown differs from normal operation, but should continue to protect the switch. While VDD is undervoltage, all channels are prevented from turning on (marker B). Only after VDD rises above VDD Undervoltage Threshold (VDD_{UV+}) again will all channels be allowed to return to normal operation as illustrated at Marker C.

It is important to note that VDD must remain powered to offer undervoltage protection in the manner described above. If VDD is undervoltage (below $UVLO_{UV-}$), the smart clamp voltage is not well-defined. Also, while VDD is undervoltage, the $\overline{FLT}$ output may be turned on. However, as VDD continues to approach 0 V, the $\overline{FLT}$ output will reach an undetermined state and cannot be relied upon to accurately reflect an undervoltge diagnostic report. Finally, when power is restored to VDD, the device must wait for the Device Startup Time (t_{ST}) to pass before normal operation will resume. See “3.2. Switch Timing Behavior” on page 6 for details.

3.5. Diagnostics

The Si830x Smart Switch communicates diagnostic information to the host controller including the condition of the load, power supply, and built-in protection. Three diagnostic reports are indicated on an active-low, open-drain $\overline{FLT}$ indicator output.

Table 3. Diagnostics Overview

Diagnostic[1]	Severity	Description
Overcurrent	Shutdown	At least one channel is overloaded. Affected outputs are immediately turned off.
Over Temperature	Constraint	At least one channel is too hot. Inductors limited to V_{CLMPL} and demagnetize slowly. Once off, an output will not turn back on.
	Shutdown	All channels are too hot. All outputs are immediately turned off. Inductors limited to V_{CLMPL} and demagnetize slowly.
VDD Overvoltage	Constraint	VDD is over VDD_{OV}. Inductors limited to V_{CLMPL} and demagnetize slowly.

1. Diagnostics are reported on the $\overline{FLT}$ output for at least one period of Clear Fault Delay (t_{CFD}). See "3.2. Switch Timing Behavior" on page 6 and "3.4. Switch Protection" on page 9 for details.

The $\overline{FLT}$ indicator output can drive an LED to provide end-user feedback, it can be combined with a pull-up resistor and read by the controller, or multiple indicator pins can be combined to simplify diagnostic reporting across multiple devices. All fault reports present within the device are combined using a logical OR to control the indicator pin such that any fault on any channel will turn on the output, and the output will only turn off when all fault conditions are cleared.

A diagnostic report is cleared from the Si830x device once the condition that caused the report is removed from the device. Additionally, a diagnostic report will be indicated for at least one Clear Fault Delay (t_{CFD}) period before being cleared. See "3.4. Switch Protection" on page 9 for details on the fault conditions that cause diagnostic reports, and see "3.2. Switch Timing Behavior" on page 6 for details on how these reports are indicated using the $\overline{FLT}$ indicator output.

It is important to note that the operation of an output channel is not affected by the presence of a diagnostic report. Switch protection operates independently from switch diagnostics. For example, it is possible for a diagnostic report to persist after the condition that caused the report is removed. Once the condition that caused the report is removed, the channel will resume normal operation regardless of the diagnostic report state.

3.5.1. Overcurrent Diagnostics

The Si830x Smart Switch indicates an overcurrent diagnostic report from any channel on the $\overline{FLT}$ output. The $\overline{FLT}$ output will remain on until all overcurrent diagnostic reports are cleared from the device.

Table 4. Over-Current Diagnostics

Diagnostic	An[1]	Output Current	$\overline{FLT}$[2]	Output Behavior[3]	
				Switch	Clamp
Current OK	L	—	—	Normal	Normal
	H	IBn < I_{OCLT}	—	Normal	Normal
Overcurrent Shutdown	H	IBn > I_{OCLT}	ON	Turns OFF	Normal

1. "X" is any logic value, "H" is a logic high (true) value, and "L" is a logic low (false) value. Logic pins should always be connected to either logic high or low.
2. The $\overline{FLT}$ output is both active-low and open-drain. "–" denotes that this diagnostic does not turn on the output, but other diagnostics might. If the $\overline{FLT}$ output is in the ON state and no other diagnostic reports are present, it will stay ON for at least one multiple of Clear Fault Delay (t_{CFD}). See "3.2. Switch Timing Behavior" on page 6 for details.
3. Behavior assumes only the defined diagnostic condition is present. Exceptions to normal behavior due to a fault are defined here; see "3.4. Switch Protection" on page 9 more information.

The table above describes the overcurrent diagnostic report when it is reported and provides a brief overview of how the output behavior changes with the report. An Overcurrent Shutdown can only be reported when the channel input is high (true).

3.5.2. Over-Temperature Diagnostics

The Si830x Smart Switch reports two different over temperature conditions on the $\overline{FLT}$ indicator output. The switch output behavior is different depending on the condition, but the $\overline{FLT}$ indicator output remains the same.

Table 5. Over-Temperature Diagnostics

Diagnostic	Switch Temperature	Channels	$\overline{FLT}$[1]	Output Behavior[2]	
				Switch	Clamps
Temperature OK	$T_{Bn} < T_{OT}$	All Channels	—	Normal	Normal
Over Temperature Constraint	$T_{Bn} > T_{OT}$	Any Channels	ON	Stays OFF[3]	$V_{CLMP} = V_{CLMPL}$
Over Temperature Shutdown		All Channels	ON	Turns OFF[4]	$V_{CLMP} = V_{CLMPL}$

1. The $\overline{FLT}$ output is both active-low and open-drain. "–" denotes that this diagnostic does not turn on the output, but other diagnostics might. If the $\overline{FLT}$ output is in the ON state and no other diagnostic reports are present, it will stay ON for at least one multiple of Clear Fault Delay (t_{CFD}). See "3.2. Switch Timing Behavior" on page 6 for details.
2. Behavior assumes only the defined diagnostic condition is present. Exceptions to normal behavior due to a fault are defined here; see "3.4. Switch Protection" on page 9 more information. Clamp behavior applies to all smart output clamps, for all channels.
3. During Over Temperature Constraint, channels that are in the ON state will remain ON until turned off. Channels that are OFF or turned off during this period will remain OFF until the Over Temperature Constraint is removed.
4. During Over Temperature Shutdown, channels that are ON will be immediately turned off, and channels that are OFF will remain OFF until the Over Temperature Shutdown condition is removed.

The table above describes the over temperature diagnostic reports when they are reported and provides a brief overview of how the output behavior changes with each report.

3.5.3. Power Supply Diagnostics

The Si830x Smart Switch indicates an overvoltage diagnostic report on the $\overline{FLT}$ output when the power supply exceeds the recommended voltage range.

Table 6. Switch Power Supply Diagnostics

Diagnostic	Supply Voltage[1]	$\overline{FLT}$[2]	Output Behavior[3]	
			Switch	Clamps
VDD Voltage OK	$VDD_{UV} < VDD < VDD_{OV}$	—	Normal	Normal
VDD Overvoltage Constraint	$VDD > VDD_{OV}$	ON	Normal	$V_{CLMP} = V_{CLMPL}$

1. Supply voltage must remain within this voltage range long enough to be measured for a change to be reported. If supply voltage changes sufficiently quickly, the diagnostic state will remain unchanged.
2. The FLT output is both active-low and open-drain. "–" denotes that this diagnostic does not turn on the output, but other diagnostics might. If the $\overline{FLT}$ output is in the ON state and no other diagnostic reports are present, it will stay ON for at least one multiple of Clear Fault Delay (t_{CFD}). See "3.2. Switch Timing Behavior" on page 6 for details.
3. Behavior assumes only the defined diagnostic condition is present. Exceptions to normal behavior due to a fault are defined here; see "3.4. Switch Protection" on page 9 for more information. Clamp behavior applies to all smart output clamps, for all channels.

The table above describes the switch power supply diagnostic report when it is reported and provides a brief overview of how the output behavior changes with the report. It is important to note that when VDD is under VDD_{UV}, the switch offers undervoltage protection, but the $\overline{FLT}$ output is in an unknown state. A glitch may be observed on the $\overline{FLT}$ pin while in this undetermined state. See "3.4. Switch Protection" on page 9 for more details on undervoltage protection.

4. Application Information

The Si830x is designed to be both flexible and robust to meet a wide range of application requirements, safely survive unexpected loads, and rapidly recover normal operation if a fault occurs. To achieve these objectives, the Si830x must be designed with certain considerations in mind. Moreover, some features will only be available with additional circuit elements included in the design.

4.1. Recommended Application Circuits

The following examples illustrate typical circuit configurations using the Si830x Smart Switch.

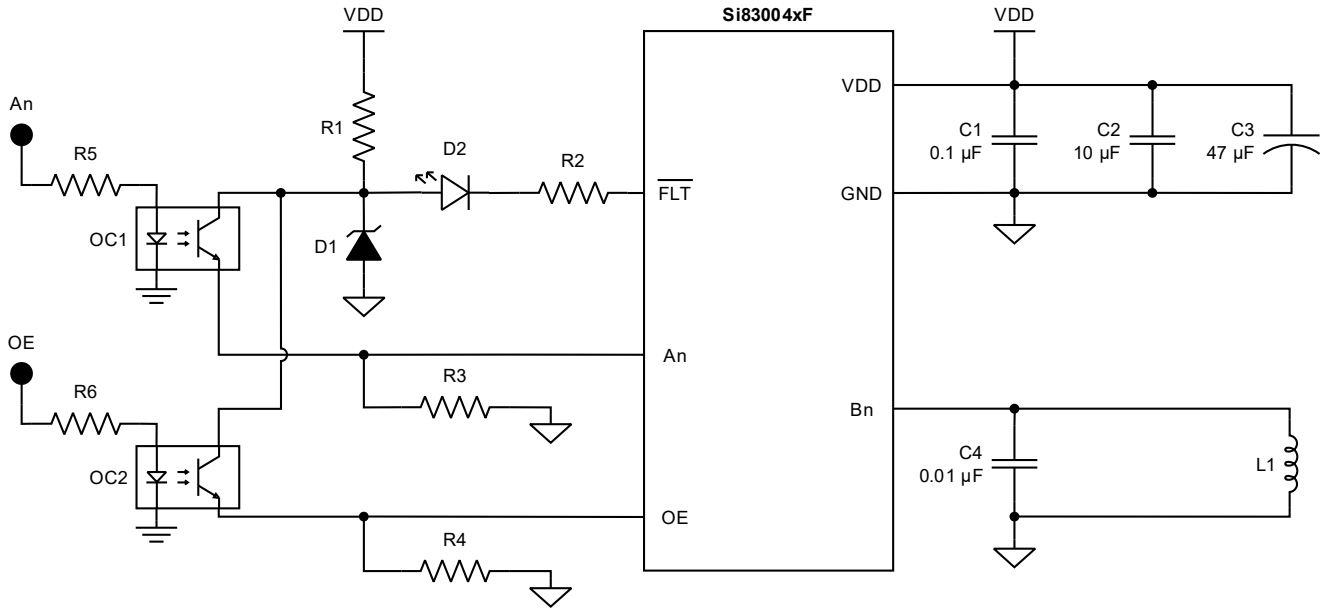


Figure 12. Recommended Si83004xF Application Circuit

In the figure above, the Si830x is isolated and controlled via a simple set of optocouplers (OC1 and OC2) and current-limiting resistors (R5 and R6). An output enable signal is also supplied through the isolation barrier for increased fault tolerance, safety, and state control. Pull-down resistors (R3 and R4) are added to ensure An and OE are reliably held low when the optocouplers are turned off. Indicator LED D2 is connected to the Si830x through a current-limiting resistor R2 for end-user diagnostic feedback. If an indicator is not desired, the FLT output can be passed through the isolation barrier by replacing D2 with the input of another optocoupler. Care must be taken not to exceed the absolute maximum ratings of the logic interface pins when interfacing with the device. See “5. Electrical Specifications” on page 28 for details. A Zener diode D1 and resistor R1 can serve this purpose by creating a simple low-voltage power supply from the high-voltage power supply (VDD). The bypass capacitors on the high-voltage power supply (C1, C2, and C3) should be placed as close to the chip as possible. Be sure to correctly size the decoupling capacitors based on the load and switching requirements. See “4.2. Layout Considerations” on page 24 for more information on sizing the decoupling capacitors. Due to the sophisticated built-in switch protection of the Si830x, connecting and switching channels in parallel to increase the continuous current capability is not supported.

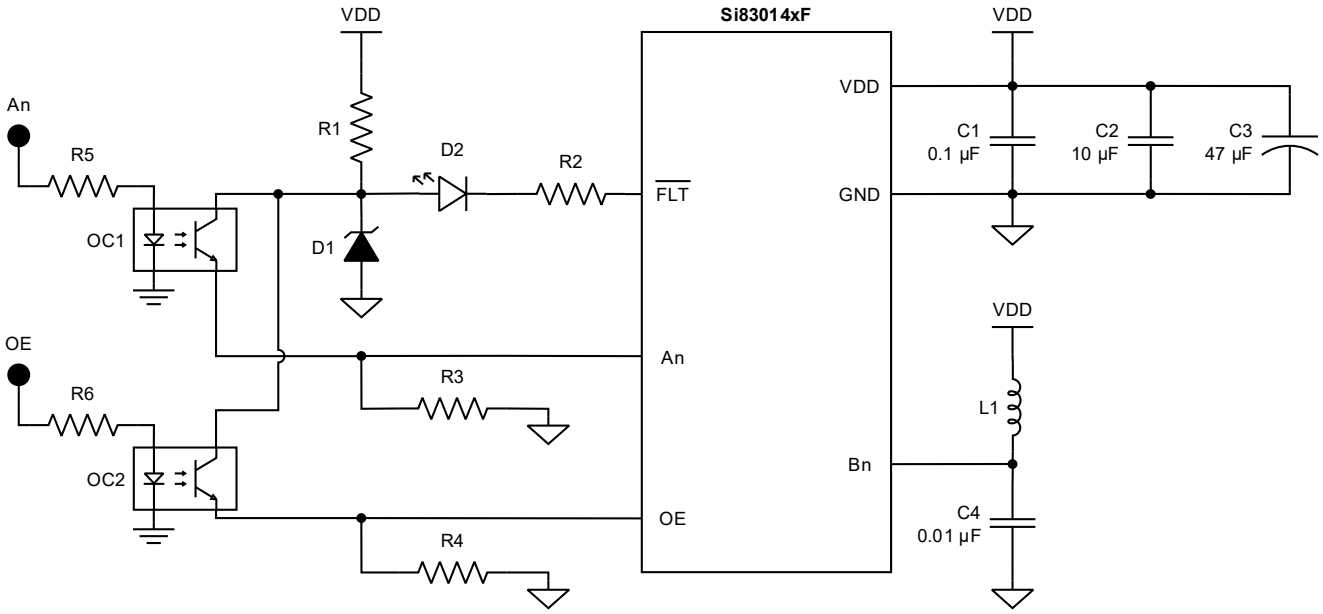


Figure 13. Recommended Si83014xF Application Circuit

In the figure above, a low-side (sinking) Si83014AF device is illustrated. It is identical to Figure 12 on page 22, with the exception of the circuit attached to the switch output Bn. Note that a high-side switch must source current into a load, such as the inductor L1 in Figure 12. A low-side switch must sink current from a load, such as the inductor, L1, in Figure 13.

Note that, under normal conditions, the Si830x Smart Switch requires no additional components to protect the switch output circuit such as fuses for short circuit protection or diodes for demagnetization voltage protection (back EMF or voltage kick-back). If the application must meet a surge specification, additional protection may be required. See AN1214: Advanced Device Protection for the Si834x Isolated Smart Switch for more details.

4.2. Layout Considerations

Several layout recommendations should be taken into consideration when designing for the Si830x Smart Switch device. These recommendations improve signal integrity, mitigate inrush current concerns, optimize heat dissipation, and improve the manufacturability of the end-system.

1. An entire PCB plane should be dedicated to the GND reference to improve signal integrity. If an entire PCB plane is not dedicated to the GND reference, be cautious of a signal's ground path when connected to the Si830x logic interface.
2. It is recommended to use a resistor on each logic interface pin to improve signal integrity and reduce EMI concerns, especially for long traces. They should be placed as close to the controller as possible. See “4.1. Recommended Application Circuits” on page 22 for details.
3. To improve heat dissipation, add an array of vias from the PCB pad connected to the ePAD and its ground plane, through the PCB connecting any inner ground plane layers, and exposed on the opposite side of the board. Use small-diameter vias, as large-diameter vias may reduce manufacturability.
4. Heat dissipation can further be improved by adding a pour on the top and bottom layers of the PCB to increase surface area associated with heat dissipation. The pour on the same side as the Si830x should ideally be an extension of the PCB pad connected to the ePAD to maximize thermal conductivity and heat dissipation. Additionally, an array of thermal relief vias extending across the surface area of the board connected between the top and bottom pours, as well as any internal ground planes. Use the same type of vias as prescribed for the ePAD pcb above.
5. Open board space around the Si830x device, on the side of the PCB opposite to the device, and around the thermal relief vias further improves heat dissipation.
6. Place a pair of bypass capacitors as close as possible to the VDD power supply pin. A 0.1 µF capacitor and a 10 µF or larger capacitor are recommended. It is important that the decoupling capacitors are selected such that the maximum VDD Slew Rate specification found in Table 12, “Absolute Maximum Ratings,” on page 31 is not exceeded.
7. Bulk bypass capacitance can be added to the existing bypass capacitors on the power supply. Size the bulk capacitor based upon end-system load requirements, suge requirements, and the specified maximum VDD slew rate.
8. Use 15 mil traces for the switch output pins in order to adequately handle the maximum continuous switch current, while minimizing the impact on surge and electrical fast transient (EFT) performance.
9. To reduce EMI concerns and channel crosstalk, minimize the length of the current return path for switch outputs. Be sure to consider the additional current return path through the bulk capacitor, especially when using a low-side (sinking) device.

4.3. Power Dissipation Considerations

When the Si830x device is operating within the recommended operating conditions, the only significant source of temperature rise is the demagnetization of inductive loads. The Si830x was designed to drive and demagnetize 1.15 H loads on all channels simultaneously without exceeding the thermal limitations of the device. If the user exceeds the temperature limitations of the device, it will reduce the demagnetization clamp voltage to VCLMPL for all channels, which will extend the turn-OFF time of all inductive loads, and all channels will be prevented from turning on again. This reduces power dissipation until the device temperature is reduced to acceptable levels. See "3.4.3. Over-Temperature Protection" on page 13 for details on this process.

Due to the innovative Over-Temperature Protection feature, the designer should only be concerned about the switch temperature at the beginning of the load switching cycle. The switch temperature must be maintained below the Over-Temperature Threshold. Therefore, the Derated Ambient temperature (T_{AD}) is dependent on device power dissipation and thermal impedance. The estimated device power dissipation is composed of quiescent power dissipation (P_Q) and power dissipation for each channel (P_{CH}) as shown in Equation 2 and supported by Equations 3 and 4.

$$T_{OT} - T_{HYS} - \theta_{JA}(P_Q + n_{CH} \times P_{CH}) > T_{AD}$$

Equation 2.

Where:
T_{OT} is the Over-Temperature Threshold (°C)
T_{HYS} is the Over-Temperature Hysteresis (°C)
$ø_{JA}$ is the Junction-to-Ambient thermal resistance (°C/W).
n_{CH} is the number of channels actively driving a load.

The logic interface contributes a negligible amount of power to the total device power dissipation. To simplify the estimate, it has been removed from both P_Q and P_{CH} in the equations below.

$$P_Q = IDD_Q \times VDD$$

Equation 3.

Where:
IDD_Q is the VDD Supply Quiescent Current (A).
VDD is the Supply Voltage (V).

For a conservative power dissipation estimate, the maximum quiescent current specification $IDD_{Q(MAX)}$ should be used in Equation 3.

The power dissipated by a single channel is estimated by Equation 4 and supported by Equations 5 through 8. It is comprised of the power dissipation when the channel is ON (P_{ON}), the power dissipated when the channel is turning on (P_{SW}), and the power dissipated when the channel is turning off and demagnetizing an inductor (P_{CLMP}).

$$P_{CH} = P_{ON} + P_{SW} + P_{CLMP}$$

Equation 4.

The estimated power dissipation when the channel is ON, given by Equation 5, is dependent on the current through the load, the switch's ON-State Resistance, and how long the load is driven.

$$P_{ON} = I_L^2 \times R_{ON} \times \frac{t_{ON}}{t_{SW}}$$

Equation 5.

Where:
I_L is the current through the load (A).
R_{ON} is the ON-State Output Resistance (Ω).
t_{ON} is the time during a single switching period that the channel is ON (s).
t_{SW} is the switching period of the channel (s).

For a conservative power dissipation estimate, the maximum current through the load and the maximum ON-State Output Resistance should be used in Equation 5.

The estimated power dissipation when the channel is turning on, given by Equation 6, is dependent on the switch supply voltage, the load capacitance, and the switching period.

$$P_{SW} = VDD^2 \times \frac{C_L}{2 \times t_{SW}}$$

Equation 6.

Where:
VDD is the Supply Voltage (V).
C_L is the load capacitance (C).
t_{SW} is the switching period of the channel (s).

Note that the load capacitance (C_L) should include any capacitance built into the circuit, such as the 10 nF capacitor recommended in “4.2. Layout Considerations” on page 24.

The estimated power dissipation when the channel is turning off and demagnetizing an inductor is dependent on the current through the load, the smart output clamp voltage, and the switching period. If the current through the load is greater than the Demagnetization Clamp Current Threshold ($I_L > I_{CLMPT}$), then use Equation 7 for the power dissipated by a single channel (P_{CH}).

$$P_{CLMP} = V_{CLMPL} \times \frac{I_L + I_{CLMPT}}{2} \times \frac{L(I_L - I_{CLMPT})}{\left(R_L \frac{I_L + I_{CLMPT}}{2} + V_{CLMPL}\right) T_{SW}} + V_{CLMPH} \times \frac{I_{CLMPT}}{2} \times \frac{I_{CLMPT} \times L}{\left(\frac{I_{CLMPT} \times R_L}{2} + V_{CLMPH}\right) T_{SW}}$$

Equation 7.

Where:
V_{CLMPL} is the Demagnetization Clamp Low Voltage (V).
V_{CLMPH} is the Demagnetization Clamp High Voltage (V).
I_L is the current through the load (A).
I_{CLMPT} is the Demagnetization Clamp Current Threshold (A).
L is the inductance of the load (H).
R_L is the resistance of the load (Ω).
T_{SW} is the switching period of the channel (s).

For a conservative power dissipation estimate, the maximum current through the load should be used in Equations 7 and 8. The time during a single switching period (T_{SW}) that the channel is OFF must be large enough to completely discharge the load inductance.

If the current through the load is less than the Demagnetization Clamp Current Threshold ($I_L < I_{CLMPT}$), use Equation 8 for the power dissipated by a single channel (P_{CH}).

$$P_{CLMP} = V_{CLMPH} \times \frac{I_L}{2} \times \frac{I_L \times L}{\left(\frac{I_L \times R_L}{2} + V_{CLMPH}\right) T_{SW}}$$

Equation 8.

Where:
V_{CLMPH} is the Demagnetization Clamp High Voltage (V).
I_L is the current through the load (A).
L is the inductance of the load (H).
R_L is the resistance of the load (Ω).
T_{SW} is the switching period of the channel (s).

5. Electrical Specifications

Table 7. Power Supply Characteristics

Operating range for the following specifications: VDD = 9 – 32 V; T_A = –40 to +125 °C; Typical specs: VDD = 24 V; T_A = 25 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Voltage	VDD		9.0	24	32	V
Undervoltage Threshold	VDD_{UV+}	VDD rising	8.2	8.6	9.0	V
	VDD_{UV-}	VDD falling	8.0	8.4	8.7	
Undervoltage Hysteresis	VDD_{UVHYS}		—	200	—	mV
ESD Clamp Threshold	VDD_{CLMP}	I_{CLMP} = 1 mA	—	48	—	V
Supply Quiescent Current	IDD_Q	All An = LOW	5.0	6.5	8.0	mA
Supply Active Current						
1 Channel Active	IDD_{CH}	Active Bn outputs toggling at 1 kHz (50% duty cycle), no load	—	7.0	—	mA
All Channels Active	IDD_{ALL}		5.0	7.0	9.0	
Device Startup Time[1]	t_{ST}		—	60	—	µs

1. Startup, power cycle, and shutdown timing are detailed in "3.2. Switch Timing Behavior" on page 6.

Table 8. Logic Interface Characteristics

Operating range for the following specifications: VDD = 9 – 32 V; T_A = –40 to +125 °C; Typical specs: VDD = 24 V; T_A = 25 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Low Level Input Voltage	V_{IL}	VDD = 24 V ± 10%	—	—	0.8	V
High Level Input Voltage	V_{IH}	VDD = 24 V ± 10%	2.0	—	—	V
Input Hysteresis	V_{HYS}		—	100	—	mV
Input Capacitance	C_I		—	2.0	—	pF
Input Leakage Current	$\lvert I_{LKG} \rvert$	V_{An} = 5.5 V, V_{OE} = 5.5 V	—	10	16	µA
Indicator Output Impedance [1]	Z_{OLED}	V_{OLED} = 0.5 V	—	66	—	Ω
Indicator Output Current[1]	I_{OLED}	V_{OLED} = 0.5 V	10	12	—	mA
Clear Fault Delay	t_{CFD}		—	1.0	—	s

1. Parameter applies to $\overline{FLT}$ indicator output pin. Indicator output uses an active-low, open-drain configuration where current is sinked into the pin. See "4.1. Recommended Application Circuits" on page 22 for more information.

Table 9. Load Driving Characteristics

Operating range for the following specifications: VDD = 9 – 32 V; T_A = –40 to +125 °C; Typical specs: VDD = 24 V; T_A = 25 °C; C_L = 10 nF; R_{LOAD} = 47 Ω

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Recommended High or Low Pulse Width	MPW	An or OE pins	10	—	—	µs
Turn ON Propagation Delay[1]						
Si8300x Sourcing Devices	t_{PLH}		0.5	2.4	3.4	µs
Si8301x Sinking Devices			0.5	2.4	3.4	
Turn OFF Propagation Delay[2]						
Si8300x Sourcing Devices	t_{PHL}		2.0	3.2	4.5	µs
Si8301x Sinking Devices			1.4	2.4	3.4	
Channel-Channel Skew[3]	t_{PSK}		—	—	300	ns
Si8300x Sourcing Output Rise Time[4]	t_R		0.5	2.0	3.0	µs
Si8301x Sinking Output Fall Time[5]	t_F		0.5	2.0	4.0	µs
Turn ON Voltage Slope						
Si8300x Sourcing Devices	dV/dt_{ON}		—	6.5	—	V/µs
Si8301x Sinking Devices			—	6.5	—	
Turn OFF Voltage Slope						
Si8300x Sourcing Devices	dV/dt_{OFF}		—	6.5	—	V/µs
Si8301x Sinking Devices			—	9.0	—	
OFF State Output Current	$\lvert I_{O(OFF)} \rvert$	$V_{O(OFF)}$ = 0 V to VDD	—	—	100	µA
ON State Load Current	$\lvert I_{O(ON)} \rvert$	Continuous operation	—	0.5	0.7	A
ON State Output Resistance	R_{ON}	$\lvert I_{O(ON)} \rvert$ = 0.5 A, VDD = 24 V	—	150	300	mΩ
Load Capacitance	C_L		0.01	—	10	µF
Demagnetization Current to Engage Clamp	$I_{CLMP(MIN)}$		1.0	—	—	mA

1. Turn ON propagation delay is measured from the time the input (An or OE) is 50% ON to the time the output (Bn) is 20% ON and rising. See Figure 14, "Turn ON and Turn OFF Timing," on page 29 for measurement details.
2. Turn OFF propagation delay is measured from the time the input (An or OE) is 50% ON to the time the output (Bn) is 80% ON and falling. See "Figure 14. Turn ON and Turn OFF Timing" for measurement details.
3. Channel-channel skew is the magnitude of the difference in turn ON or turn OFF propagation delay times measured between different channels operating at the same supply voltages, load, and ambient temperature.
4. Output rise time is measured from the time the output is 20% ON to the time the output is 80% ON. For sinking output devices (Si8301x), rise time is determined by load conditions. See "Figure 14. Turn ON and Turn OFF Timing" for measurement details.
5. Output fall time is measured from the time the output is 80% ON to the time the output is 20% ON. For sourcing output devices (Si8300x), fall time is determined by load conditions. See "Figure 14. Turn ON and Turn OFF Timing" for measurement details.

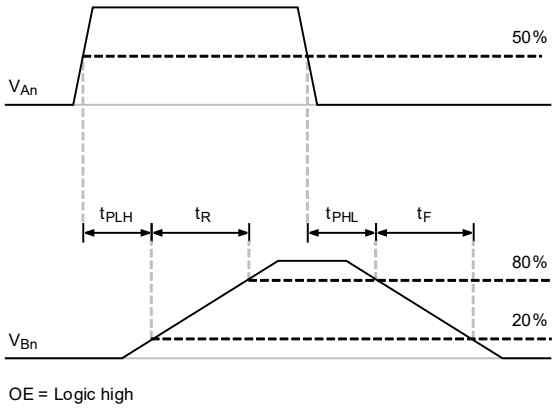


Figure 14. Turn ON and Turn OFF Timing

Table 10. Protection and Diagnostics

Operating range for the following specifications: VDD = 9 – 32 V; T_A = –40 to +125 °C; Typical specs: VDD = 24 V; T_A = 25 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Current Limit[1]	I_{OCL}		0.70	0.95	1.15	A
Output Current Limit Threshold [2]	I_{OCLT}		0.70	1.15	1.40	A
Output Current Limit Pulse[3]	t_{OCL}		—	155	—	µs
Output Current Limit Period[3]	t_{OCLP}[4]		—	0.86	—	ms
Overcurrent Protection Duration[3]	t_{OCPD}		—	6.0	—	ms
Overcurrent Protection Retry Delay	t_{OPRD}		—	518	—	ms
Demagnetization Clamp High Voltage[5]						
Si8300x Sourcing Devices	V_{CLMPH}	VDD = 24 V, I_O = 1 mA	—	-17.5	—	V
Si8301x Sinking Devices			—	VDD+17.5	—	
Demagnetization Clamp Low Voltage[5]						
Si8300x Sourcing Devices	V_{CLMPL}	VDD = 24 V, $I_O \geq I_{CLMPT}$	—	-2.5	—	V
Si8301x Sinking Devices			—	VDD+2.5	—	
Demagnetization Clamp Current Threshold[5]	I_{CLMPT}		0.34	0.40	0.46	A
VDD Overvoltage Threshold[6]	VDD_{OV+}	VDD rising	—	33.5	—	V
	VDD_{OV-}	VDD falling	—	33.0	—	
Over Temperature Threshold[7]	T_{OT}		159	167	175	°C
Over Temperature Hysteresis	T_{HYS}		—	33.0	—	°C

1. The current limit is applied when an output is first turned ON, and when overcurrent conditions are present on the output. It is applied in a pulsed fashion for t_{OCL} and repeats for t_{OCPD}. See “3.4. Switch Protection” on page 9 for details.
2. The current measured through the output must exceed this threshold in order to be detected as an overcurrent condition and for the Output Current Limit (I_{OCL}) to be enforced. See “3.4. Switch Protection” on page 9 for details.
3. Period may be reduced during operation if overcurrent conditions are removed. See “3.4. Switch Protection” on page 9 for details.
4. Peak output current is only available for a short time period t_{OPCL}, and only during a perceived overcurrent condition detected when the output is first turned ON or after the Overcurrent Protection Retry Delay. See “3.4. Switch Protection” on page 9 for details.
5. The demagnetization clamp voltage is V_{CLMPL} while the current through the output is equal to or above I_{CLMPT}. When the current through the output is below I_{CLMPT}, the demagnetization clamp voltage is V_{CLMPH}. Under certain fault conditions, this behavior is modified and performance is constrained. See “3.4. Switch Protection” on page 9 for details.
6. Inductive load demagnetization performance is constrained above this threshold. See “3.4. Switch Protection” on page 9 for details.
7. Any channel that exceeds the Over Temperature Threshold will have its demagnetization performance constrained. If all channels exceed the Over Temperature Threshold, all channels will be unconditionally shutdown. By default, this behavior will persist until the Over Temperature condition(s) are removed. See “3.4. Switch Protection” on page 9 for details.

Table 11. Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Max	Unit
Ambient Temperature [1]	T_A		-40	125	°C
eTSOP-24 Package Thermal Resistance					
Junction-to-Ambient	θ_{JA}	4-layer, 2s2p JEDEC test board	—	26	ºC/W
	θ_{JAE}	2-layer, Si830x-KIT evaluation board	—	25	ºC/W
Junction-to-Case (Exposed Pad)	θ_{JC}	4-layer, 2s2p JEDEC test board	—	2.2	ºC/W

1. The maximum ambient temperature is dependent on data frequency, output load conditions, fault conditions, number of operating channels, and supply voltages. See "4.3. Power Dissipation Considerations" on page 25

Table 12. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Max	Unit
VDD Supply Voltage	VDD	-0.3	40	V
VDD Slew Rate[2]	VDD_Δ	—	1	V/µs
Storage Temperature	T_{STG}	-65	+150	°C
Junction Temperature	T_J	—	+175	°C
Voltage on Any Logic Interface Pin with Respect to Ground	V_{IO-G}	-0.3	Min(VDD + 0.3, 5.5)	V
One Channel Single Pulse Turn OFF Energy Dissipation[3]	$E_{AS(1CH)}$	—	Unlimited	J
All Channels Simultaneously Driven Single Pulse Turn OFF Energy Dissipation[3]				
Si8300x Sourcing Devices	$E_{AS(ALL)}$	—	8	J
Si8301x Sinking Devices		—	2.5	J
Lead Solder Temperature (10 s)		—	260	°C
Human Body Model (JEDEC JS-001) ESD Rating	ESD_{HBM}	3.5	—	kV
Charged Device Model (JEDEC JS-002) ESD Rating	ESD_{CDM}	2	—	kV

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Absolute maximum slew rate only applies to supply voltage changes larger than 3 V.
3. Tested at T_A = 125 °C and maximum Load Current IO(ON) for the channel. See Table 9, "Load Driving Characteristics," on page 29 for details.

5.1. Typical Operating Characteristics

The typical performance characteristics depicted in the figures below are for information purposes only. Refer to the data tables in “5. Electrical Specifications” on page 28 for actual specification limits.

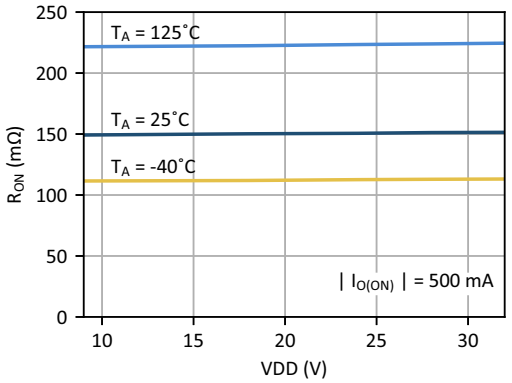


Figure 15. On Resistance vs. Supply Voltage

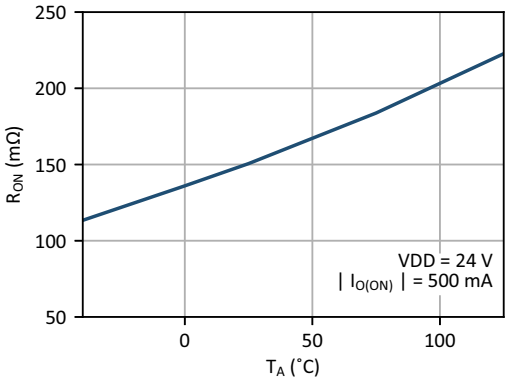


Figure 16. On Resistance vs. Ambient Temperature

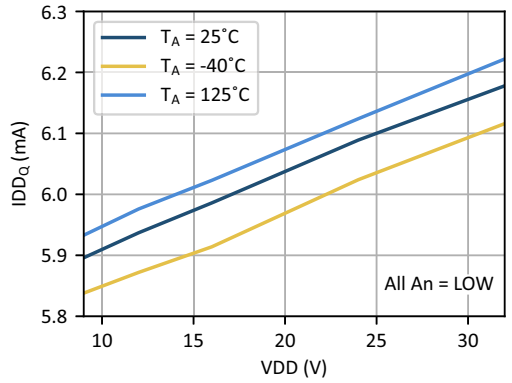


Figure 17. Supply Quiescent Current vs. Supply Voltage

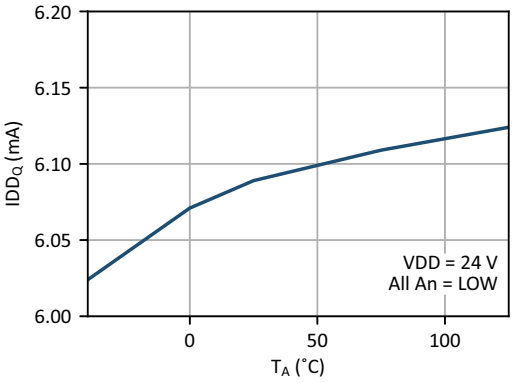


Figure 18. Supply Quiescent Current vs. Ambient Temperature

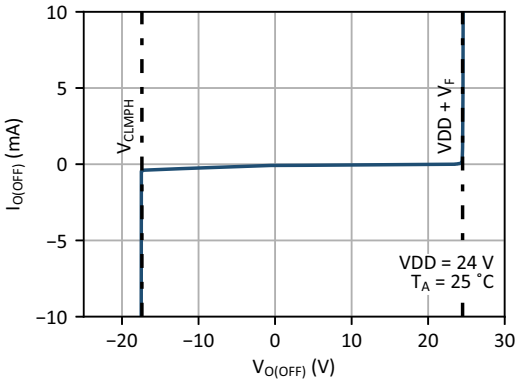


Figure 19. OFF State Output Current vs. Output Voltage for Sourcing Devices

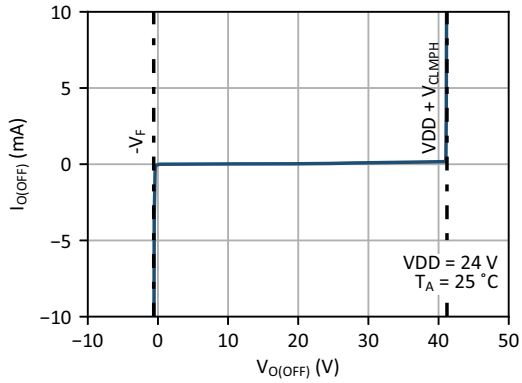


Figure 20. OFF State Output Current vs. Output Voltage for Sinking Devices

6. Pin and Package Descriptions

6.1. Device Pinouts

The Si830x consists of a single die in a package. There are two options available: one for sourcing current output and one for sinking current output. Each option is represented by a pin-out below. “1. Ordering Guide” on page 3 describes the part number and features for these products.

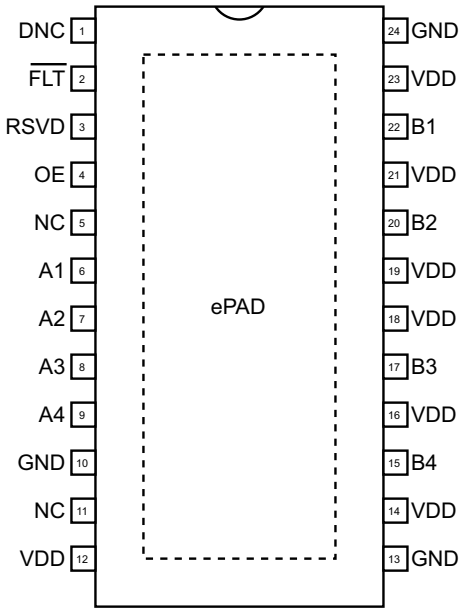


Figure 21. Si83004xF-IT Pinout

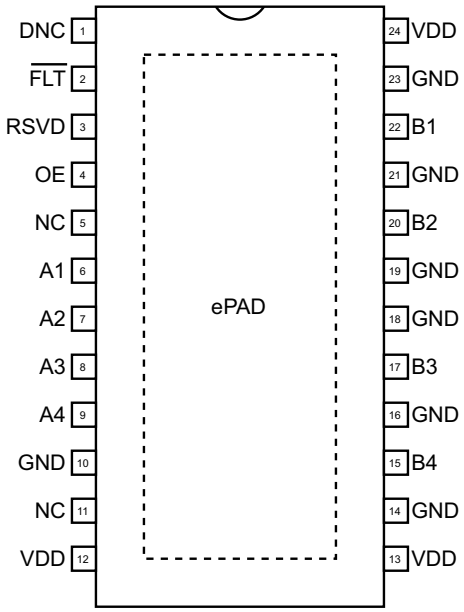


Figure 22. Si83014xF-IT Pinout

Table 13. Si830x Pin Descriptions

Pin Name	Type	Description
A1 – A4	Input	Input channels
B1 – B4	Sourcing/Sinking Output	Output channels
OE	Input	Output enable, active-high
$\overline{\text{FLT}}$	Open-drain Output	Active-low output that indicates any diagnostic reports currently present in the smart switch
GND	Ground	Switch ground. All GND pins must be used and tied together
VDD	Supply	Switch power supply. All VDD pins must be used and tied together
NC	Other	Not connected. Pin is not used and should be tied to GND
DNC	Other	Do not connect. Pin must be left floating
RSVD	Other	Reserved without specific function. Pin must be tied to GND
ePAD	Ground	Exposed thermal pad. Pad must be tied to GND

6.2. Package Drawing

The figure below illustrates the package details for the Si830x in a TSSOP-24 package. Table 14 lists the values for the dimensions shown in the illustration.

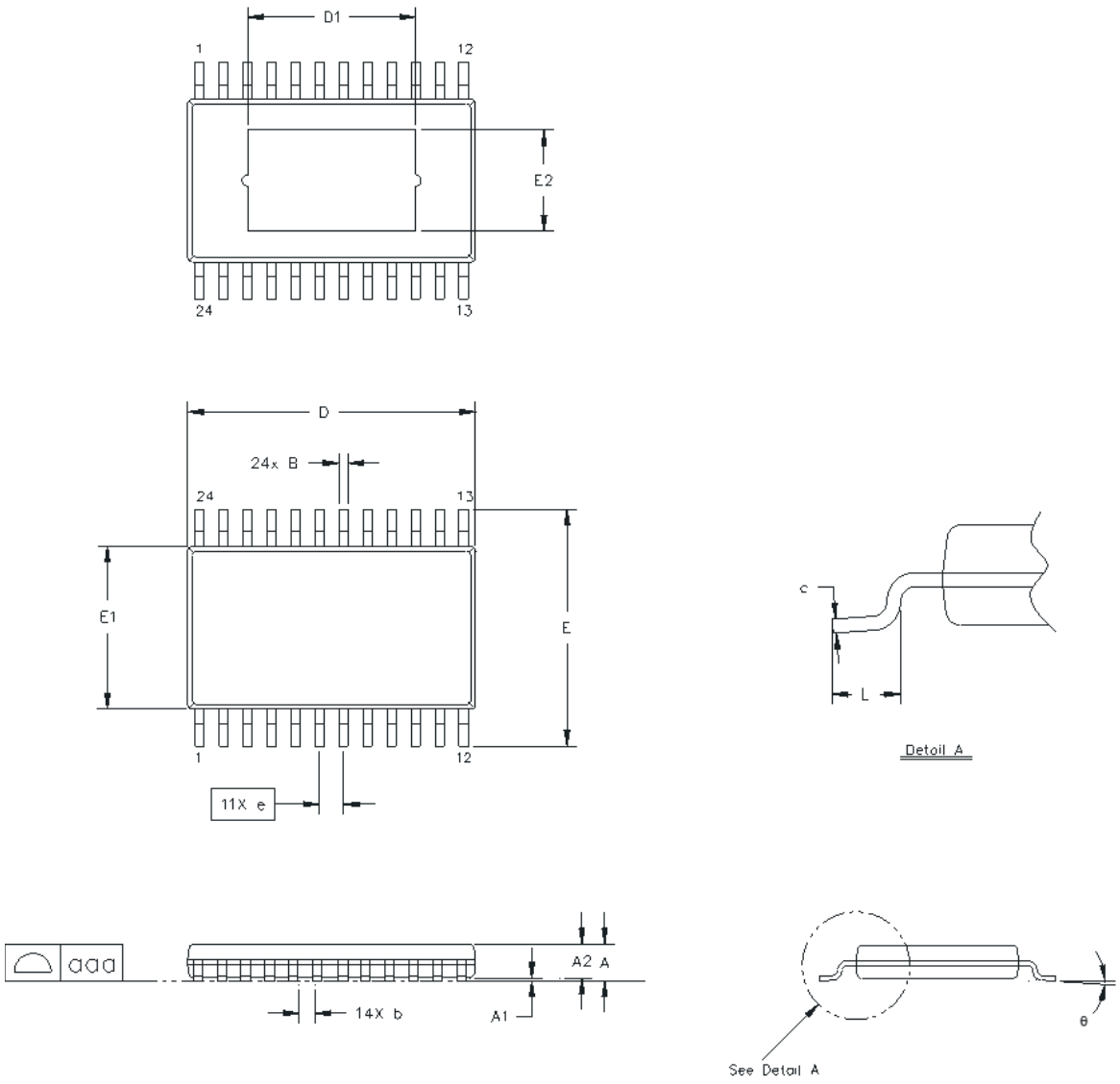


Table 14. 24-Pin TSSOP Package Diagram Dimensions[1,2,3]

Dimension	Min	Max
A		1.10
A2	0.85	0.95
B	0.19	0.30
C	0.09	0.20
D	7.70	7.90
D1	4.47	4.62
E	6.25	6.55
E1	4.30	4.50
E2	2.67	2.82
e	0.65 BSC	
L	0.46	0.76
Ø	0˚	8˚
aaa	0.10	

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1982.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020B specification for Small Body Components.

6.3. Land Pattern

The figure below illustrates the recommended land pattern details for the Si830x in a 24-pin TSSOP package. Table 15 lists the values for the dimensions shown in the illustration.

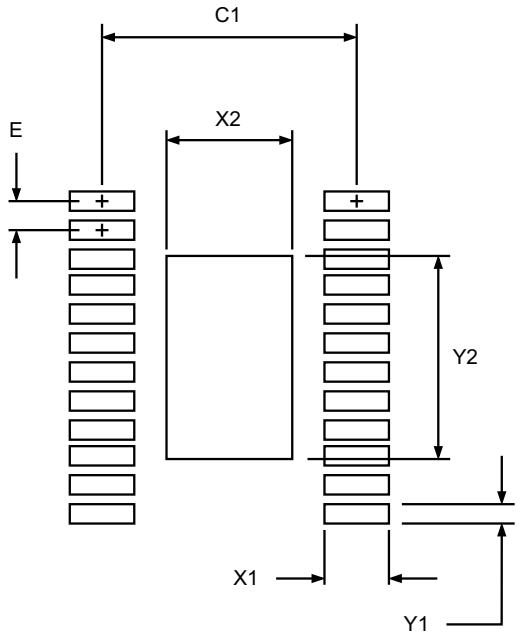


Table 15. PCB Land Pattern Dimensions[1,2,3,4,5,6,7,8,9,10]

Dimension	Feature	mm
C1	Pad Column Spacing	5.80
E	Pad Row Pitch	0.65
Y1	Pad Width	0.45
X1	Pad Length	1.45
Y2	ePAD Length	4.60
X2	ePAD Width	2.80

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.
5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
6. A stainless steel, laser-cut, and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
9. An array of square openings with approximately 50% coverage may be used for the center ground pad (ePAD).
10. A No-Clean, Type-3 solder paste is recommended.

The above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine-tune their SMT process as required for their application and tooling.

6.4. Top Marking

The figure below illustrates the top marking details for the Si830x in a 24-pin TSSOP package. Table 16 lists the values for the top marking shown in the illustration.

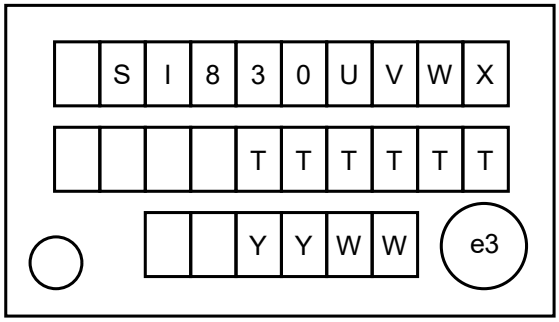


Table 16. 24-Pin TSSOP Top Marking Explanation

Line 1 Marking:	Base Part Number Ordering Options (See "1. Ordering Guide" on page 3 for more information)	Si830 = Smart Switch series U = Switch Type 0 = Sourcing output (high-side) 1 = Sinking output (low-side) V = Input & Output Configuration 4 = 4 channel output, parallel input only W = Switch Protection Configuration B = All protection methods enabled, default configuration X = Indicator Configuration F = FLT indicator
Line 2 Marking:	TTTTTT = Mfg Code	Manufacturing Traceability Code
Line 3 Marking:	YY = Year WW = Workweek	Assigned by the assembly house. Corresponds to the year and workweek of the mold date.

7. Revision History

Revision 206520A

March, 2023

- Initial release.