QorIQ Communications Platforms

T Series—QorIQ T1040/20 and T1042/22 communication processors

The QorIQ T1 family of communications processors combines up to four 64-bit cores, built on Power Architecture® technology, with high-performance Data Path Acceleration Architecture (DPAA) and network peripheral bus interfaces required for networking and telecommunications.

OVERVIEW

This scalable, pin-compatible family features the industry's first 64-bit embedded processor with an integrated Gigabit Ethernet switch, the T1040 (and dual-core T1020), which simplifies hardware design, reduces power and overall system cost.

TARGET MARKETS AND APPLICATIONS

The T1 family is ideally suited for use in mixed control and data plane applications such as fixed routers, switches, Internet access devices, firewall and other packet filtering applications, as well as general-purpose embedded computing. Its high level of integration offers significant performance benefits and greatly helps to simplify board design.

- **Enterprise equipment:** Fixed routers, Ethernet switches, UTM equipment
- **Service provider:** Edge routers, mobile backhaul
- **Aerospace, defense and government:** Ruggedized network appliances
- **Industrial computing:** Single board computers, factory automation, smart grid

e5500 CORE

The T1 family is based on the 64-bit e5500 Power Architecture core, which uses a seven-stage pipeline for low latency response to unpredictable code execution paths, boosting single-threaded performance.

e5500 Core Features

- Supports up to 1.5 GHz core frequencies
- Tightly coupled low latency cache hierarchy
- 32 KB I/D (L1), 256 KB L2 per core
- Up to 256 KB of shared platform cache (L3)
- 3.0 DMIPS/MHz per core
- Up to 64 GB of addressable memory space
- Hybrid 32-bit mode to support legacy software and seamless transition to 64-bit architecture

VIRTUALIZATION

The T1 family includes support for hardware-assisted virtualization. The e5500 core offers an extra core privilege level (hypervisor). Virtualization software for the T1 family includes kernel-based virtual machine (KVM), Linux® OS containers, NXP hypervisor and commercial virtualization software from Green Hills® Software and Enea®.

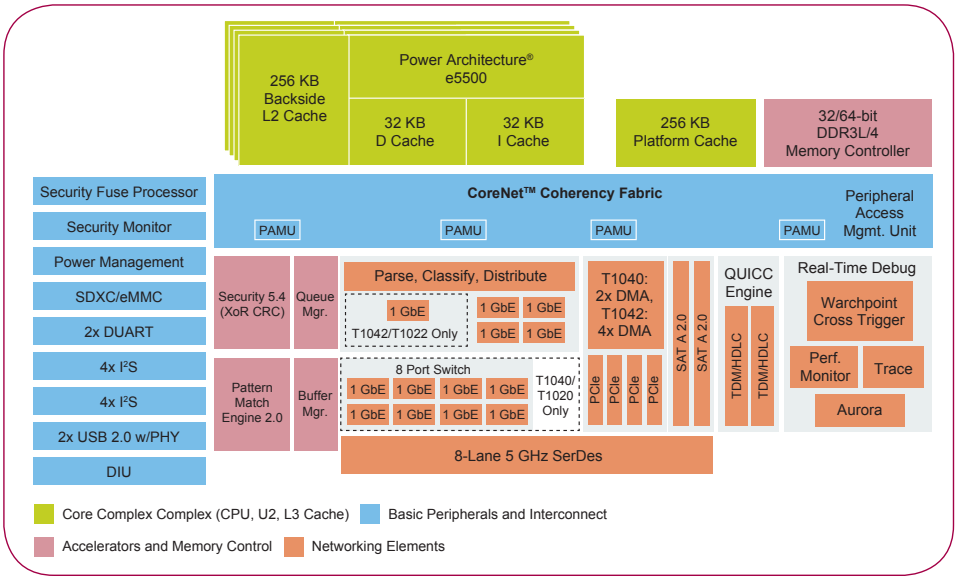
DATA PATH ACCELERATION ARCHITECTURE (DPAA)

The T1 family integrates the QorIQ DPAA, an innovative multicore infrastructure for scheduling work to cores (physical and virtual), hardware accelerators and network interfaces.

DPAA HARDWARE ACCELERATORS

Frame manager (FMAN)	13 Gb/s classify, parse and distribute
Buffer manager (BMAN)	64 buffer pools
Queue manager (QMAN)	Up to 2^{24} queues
Security (SEC)	5 Gb/s: 3DES, AES

QorIQ T1040 AND T1042 COMMUNICATIONS PROCESSORS



T1 FAMILY FEATURE LIST

Two or four e5500 single-threaded cores built on Power Architecture® technology	• Up to 1.5 GHz with 64-bit ISA support • Three levels of instructions: User, supervisor, hypervisor • Hybrid 32-bit mode to support legacy software and transition to a 64-bit architecture
CoreNet platform cache	• 256 KB shared platform cache
Hierarchical interconnect fabric	• CoreNet fabric supporting coherent and non-coherent transactions with prioritization and bandwidth allocation amongst CoreNet endpoints • QMAN fabric supporting packet-level queue management and quality of service
64-bit DDR3L/4 SDRAM memory controller with ECC support	• Up to 1600 MT/s
DPAA incorporating acceleration for the following functions	• Packet parsing, classification and distribution • Queue management for scheduling, packet sequencing and congestion management • Hardware buffer management for buffer allocation and de-allocation • Cryptography acceleration (SEC 5.x)
SerDes	• Eight lanes at up to 5 Gb/s • Supports SGMII, QSGMII, PCI Express® and SATA
Ethernet interfaces	• 8-port Gigabit Ethernet switch (available with T1040 and T1020 only) • Up to 5x 1 Gb/s Ethernet MACs
QUICC Engine module	• Support for legacy protocols TDM, HDLC, UART and ISDN
High-speed peripheral interfaces	• Four PCI Express 2.0 controllers
Additional peripheral interfaces	• Two serial ATA (SATA 2.0) controllers • Two High-Speed USB 2.0 controllers with integrated PHYs • Enhanced secure digital host controller (SD/MMC/eMMC) • Enhanced serial peripheral interface • Two I²C controllers • Four UARTS • Integrated flash controller supporting NAND and NOR flash memory
DMA	• Dual four channel
Support for hardware virtualization and partitioning enforcement	• Extra privileged level for hypervisor support
QorIQ trust architecture	• Secure boot, secure debug, tamper detection, volatile key storage