

Applications

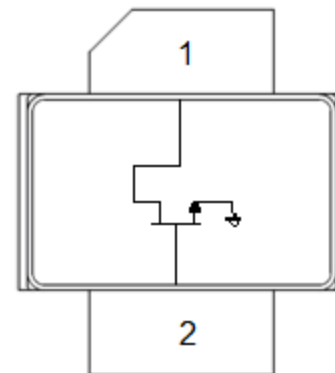
- Military radar
- Civilian radar
- Professional and military radio communications
- Test instrumentation
- Wideband or narrowband amplifiers
- Jammers



Product Features

- Frequency: DC to 3.5 GHz
- Output Power (P_{3dB}): 120 W Peak (24 Watts Avg.) at 3.3 GHz
- Linear Gain: >15 dB at 3.3 GHz
- Operating Voltage: 36 V
- Low thermal resistance package

Functional Block Diagram



General Description

The TriQuint T1G4012036-FS is a 120 W Peak (24 W Avg.) (P_{3dB}) discrete GaN on SiC HEMT which operates from DC to 3.5 GHz. The device is constructed with TriQuint's proven TQGaN25HV process, which features advanced field plate techniques to optimize power and efficiency at high drain bias operating conditions. This optimization can potentially lower system costs in terms of fewer amplifier line-ups and lower thermal management costs.

Lead-free and ROHS compliant

Evaluation boards are available upon request.

Pin Configuration

Pin No.	Label
1	V_D / RF OUT
2	V_G / RF IN
Flange	Source

Ordering Information

Part	ECCN	Description
T1G4012036-FS	EAR99	Packaged part Flangeless
T1G4012036-FS-EVB1	EAR99	3.1-3.5 GHz Evaluation Board

Absolute Maximum Ratings

Parameter	Value
Breakdown Voltage (V_{D0})	145 V
Gate Voltage Range (V_G)	-7 to 0 V
Drain Current (I_D)	12 A
Gate Current (I_G)	-28.8 to 33.6 mA
Power Dissipation (P_D)	117 W
RF Input Power, CW, T = 25 °C (P_{IN})	44.5 dBm
Channel Temperature (T_{CH})	275 °C
Mounting Temperature (30 Seconds)	320 °C
Storage Temperature	-40 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value
Drain Voltage (V_D)	36 V (Typ.)
Drain Quiescent Current (I_{DQ})	360 mA (Typ.)
Peak Drain Current (I_D)	6 A (Typ.)
Gate Voltage (V_G)	-2.9 V (Typ.)
Channel Temperature (T_{CH})	250 °C (Max.)
Power Dissipation, CW (P_D)	86 W (Max)
Power Dissipation, Pulse (P_D)	144 W (Max)

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

RF Characterization – Load Pull Performance at 3.1 GHz ⁽¹⁾

Test conditions unless otherwise noted: $T_A = 25$ °C, $V_D = 36$ V, $I_{DQ} = 360$ mA

Symbol	Parameter	Min	Typical	Max	Units
G_{LIN}	Linear Gain		18.4		dB
P_{3dB}	Output Power at 3 dB Gain Compression		130.0		W
DE_{3dB}	Drain Efficiency at 3 dB Gain Compression		64.6		%
PAE_{3dB}	Power-Added Efficiency at 3 dB Gain		62.7		%
G_{3dB}	Gain at 3 dB Compression		15.4		dB

Notes:

- $V_{DS} = 36$ V, $I_{DQ} = 360$ mA; Pulse: 100 μ s, 20%

RF Characterization – Load Pull Performance at 3.5 GHz ⁽¹⁾

Test conditions unless otherwise noted: $T_A = 25$ °C, $V_D = 36$ V, $I_{DQ} = 360$ mA

Symbol	Parameter	Min	Typical	Max	Units
G_{LIN}	Linear Gain		18.7		dB
P_{3dB}	Output Power at 3 dB Gain Compression		136.0		W
DE_{3dB}	Drain Efficiency at 3 dB Gain Compression		62.7		%
PAE_{3dB}	Power-Added Efficiency at 3 dB Gain		61.0		%
G_{3dB}	Gain at 3 dB Compression		15.7		dB

Notes:

- $V_{DS} = 36$ V, $I_{DQ} = 360$ mA; Pulse: 100 μ s, 20%

RF Characterization – Performance at 3.3 GHz ^(1, 2)

Test conditions unless otherwise noted: $T_A = 25\text{ }^\circ\text{C}$, $V_D = 36\text{ V}$, $I_{DQ} = 360\text{ mA}$

Symbol	Parameter	Min	Typical	Max	Units
G_{LIN}	Linear Gain	15.0	16.0		dB
P_{3dB}	Output Power at 3 dB Gain Compression	100.0	120.0		W
DE_{3dB}	Drain Efficiency at 3 dB Gain Compression	50.0	52.0		%
G_{3dB}	Gain at 3 dB Compression	12.0	13.0		dB

Notes:

- Performance at 3.3 GHz in the 3.1 to 3.5 GHz Evaluation Board
- $V_{DS} = 36\text{ V}$, $I_{DQ} = 360\text{ mA}$; Pulse: 100 μs , 20%

RF Characterization – Narrow Band Performance at 3.50 GHz ⁽¹⁾

Test conditions unless otherwise noted: $T_A = 25\text{ }^\circ\text{C}$, $V_D = 36\text{ V}$, $I_{DQ} = 360\text{ mA}$

Symbol	Parameter	Typical
VSWR	Impedance Mismatch Ruggedness	10:1

Notes:

- $V_{DS} = 36\text{ V}$, $I_{DQ} = 360\text{ mA}$, CW at P_{3dB}

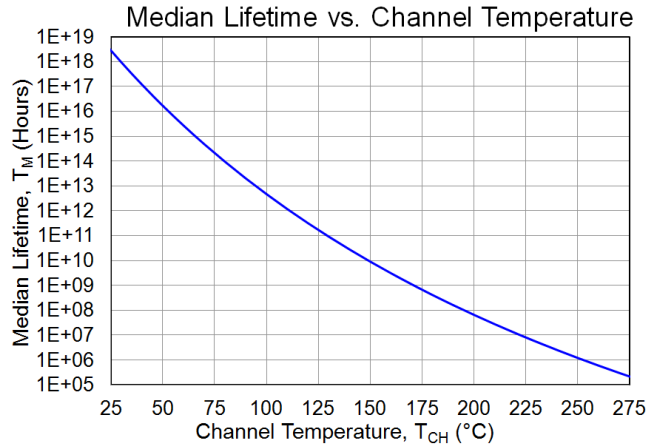
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC})	Vd = 36V, DC at 85°C Case CW	1.62	°C/W
Channel Temperature (T_{CH})		225	°C
Thermal Resistance (θ_{JC})	Vd = 32 V, DC at 85°C Case 100 usec, 20% duty cycle	0.90	°C/W
Channel Temperature (T_{CH})		175.5	°C
Thermal Resistance (θ_{JC})	Vd = 32 V, DC at 85°C Case 100 usec, 10% duty cycle	0.81	°C/W
Channel Temperature (T_{CH})		167	°C
Thermal Resistance (θ_{JC})	Vd = 32 V, DC at 85°C Case 300 usec, 20% duty cycle	1.03	°C/W
Channel Temperature (T_{CH})		189	°C
Thermal Resistance (θ_{JC})	Vd = 32 V, DC at 85°C Case 300 usec, 10% duty cycle	0.97	°C/W
Channel Temperature (T_{CH})		183	°C

Notes:

Thermal resistance measured to bottom of package, CW.

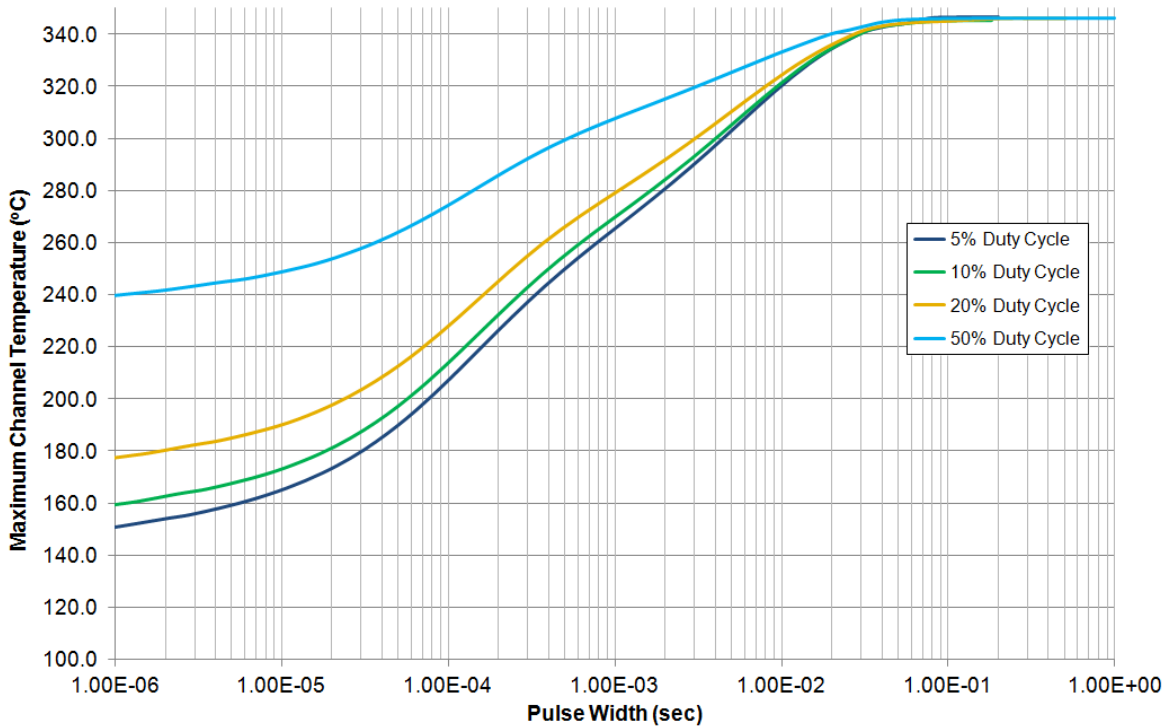
Median Lifetime



Maximum Channel Temperature

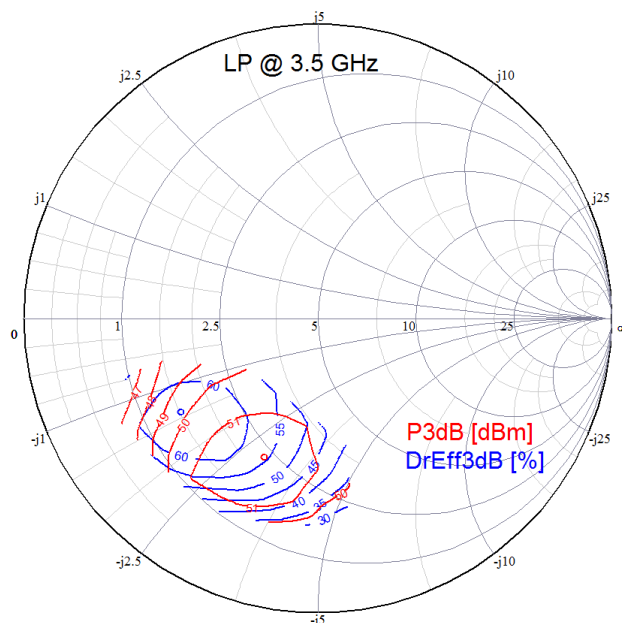
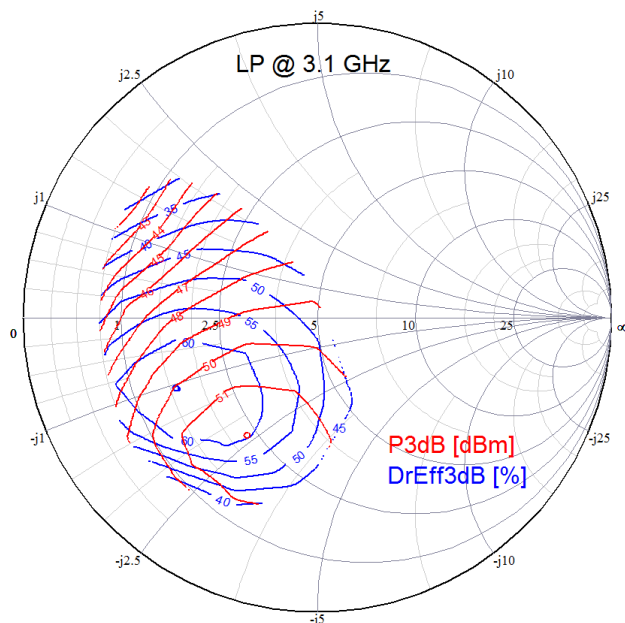
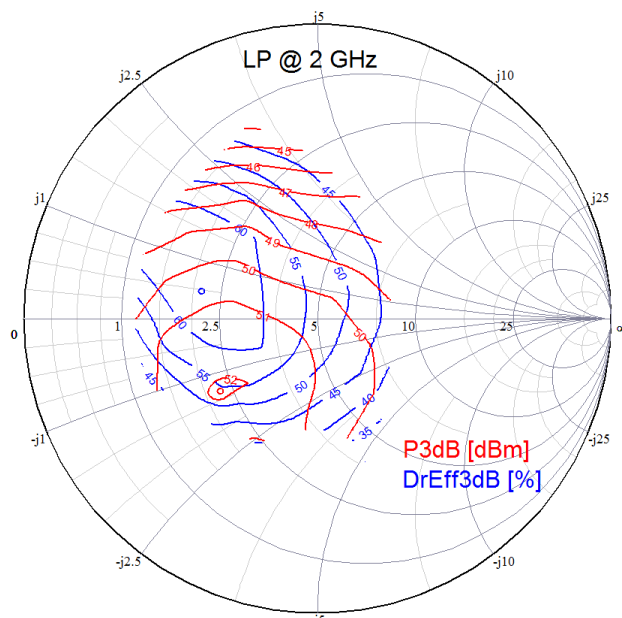
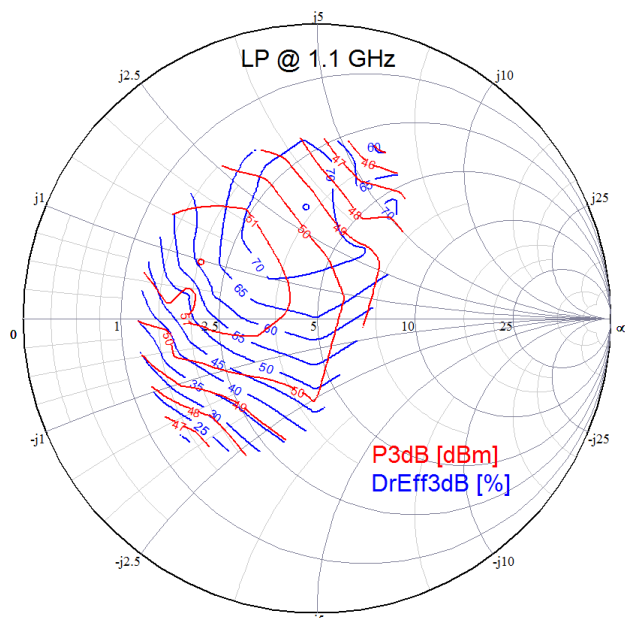
$T_{BASE} = 85^\circ\text{C}$, $P_D = 144\text{ W}$

Maximum Channel Temperature vs. Pulse Width



Load Pull Smith Charts (1, 2)

RF performance that the device typically exhibits when placed in the specified impedance environment. The impedances are not the impedances of the device, they are the impedances presented to the device via an RF circuit or load-pull system. The impedances listed follow an optimized trajectory to maintain high power and high efficiency.

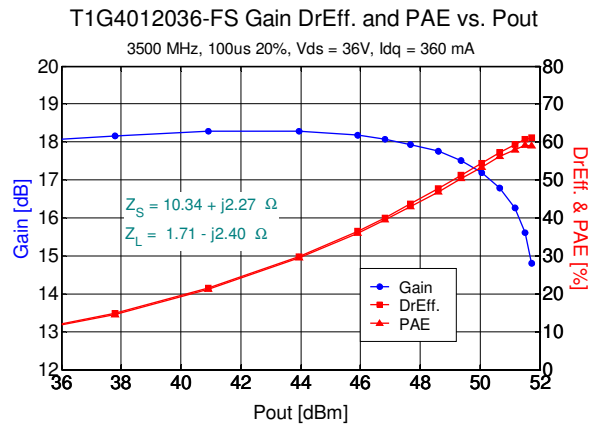
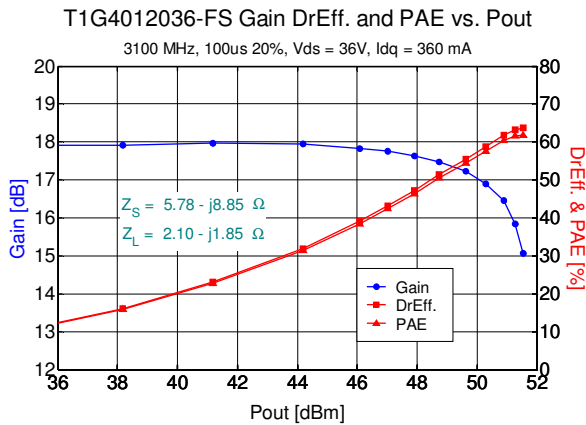
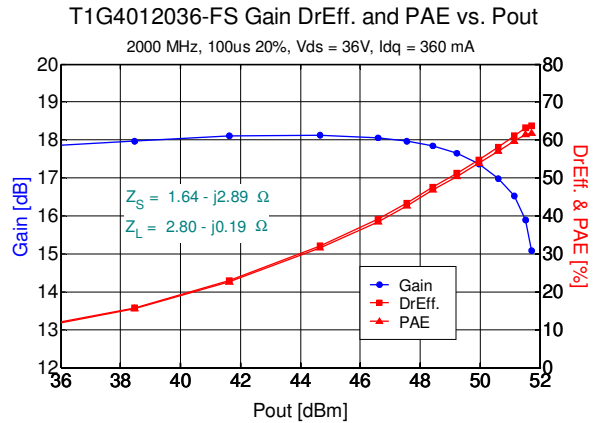
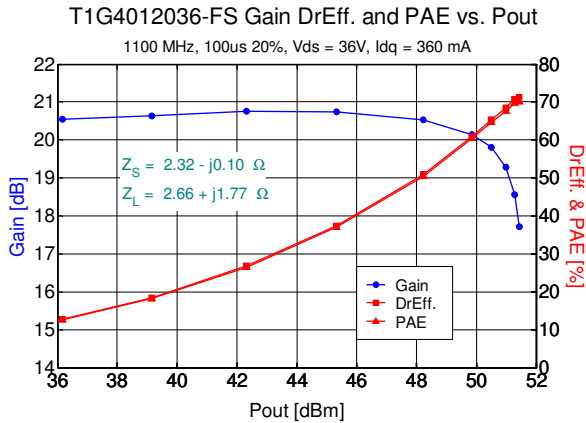


Notes:

1. Test Conditions: $V_{DS} = 36\text{ V}$, $I_{DQ} = 360\text{ mA}$
2. Test Signal: Pulse Width = 100 μsec , Duty Cycle = 20%

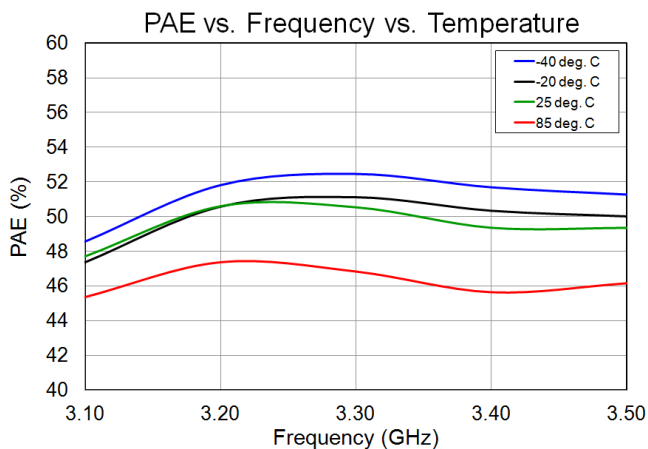
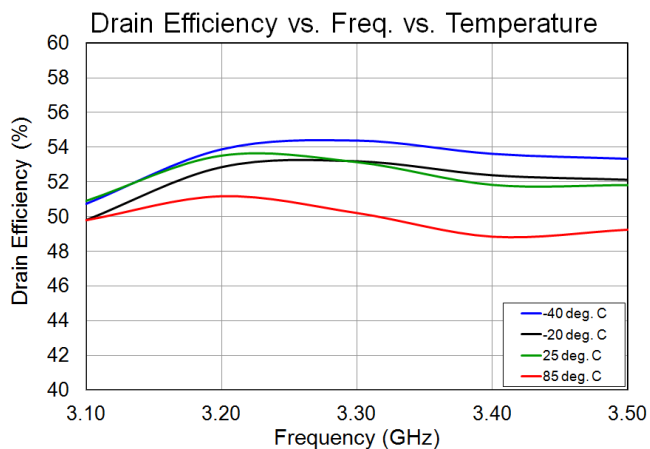
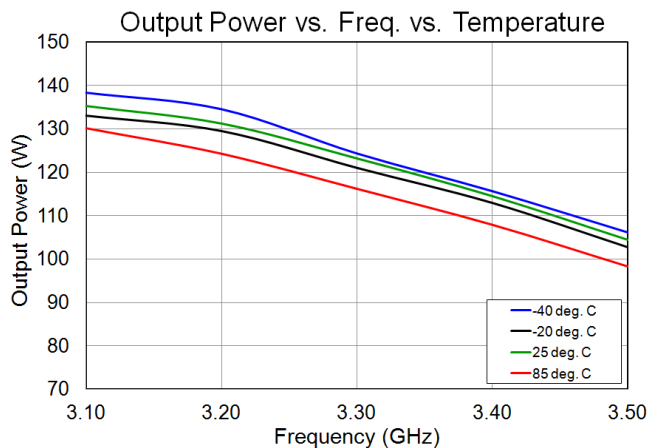
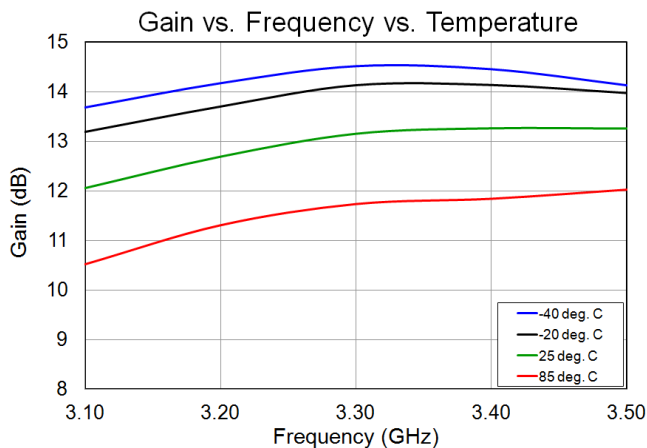
Typical Performance

Performance is based on compromised impedance point and measured at DUT reference plane.



Performance Over Temperature (1, 2)

Performance measured in TriQuint's 3.1 GHz to 3.5 GHz Evaluation Board at 3 dB compression.

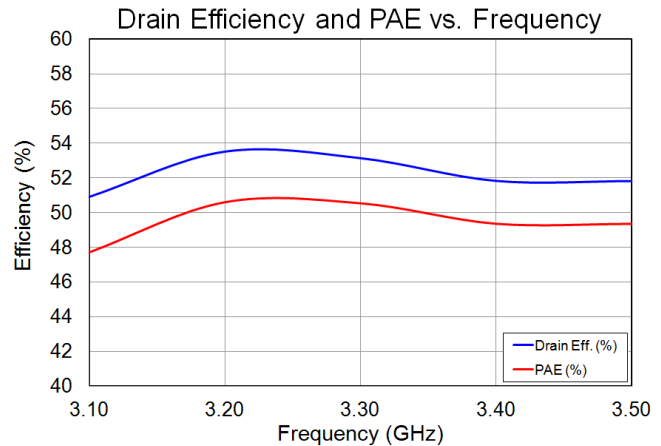
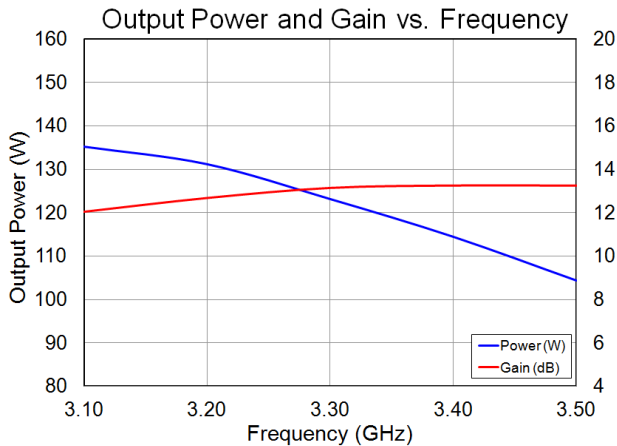


Notes:

1. Test Conditions: $V_{DS} = 36\text{ V}$, $I_{DQ} = 360\text{ mA}$
2. Test Signal: Pulse Width = 100 μs , Duty Cycle = 20%

Evaluation Board Performance (1, 2)

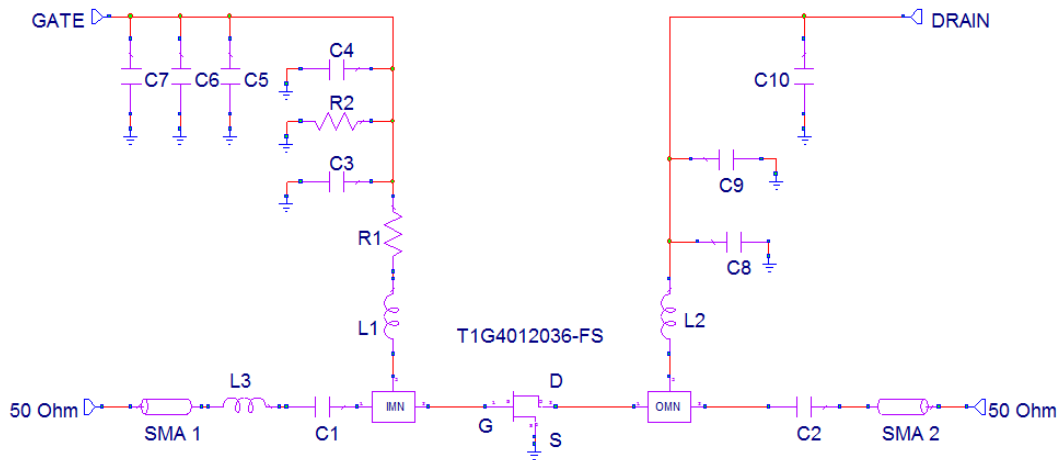
Performance at 3 dB Compression



Notes:

1. Test Conditions: $V_{DS} = 36\text{ V}$, $I_{DQ} = 360\text{ mA}$
2. Test Signal: Pulse Width = 100 μs , Duty Cycle = 20 %

Application Circuit



Bias-up Procedure

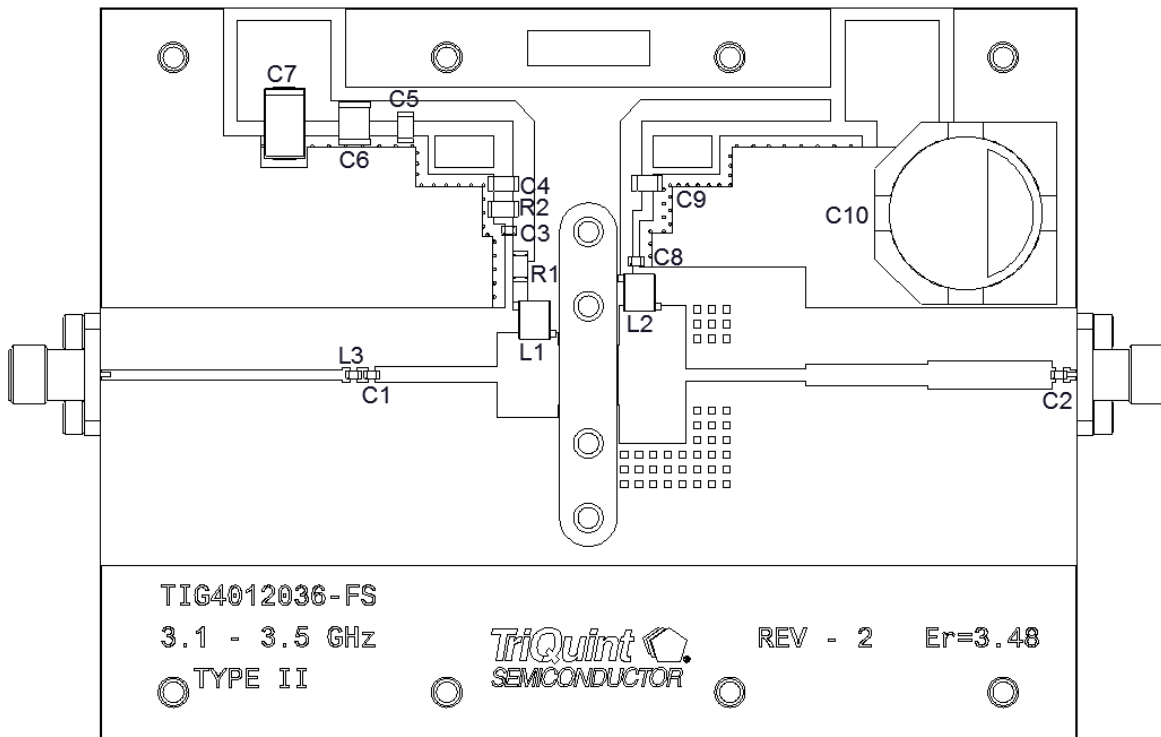
- Set gate voltage (V_G) to -5.0V
- Set drain voltage (V_D) to 36 V
- Slowly increase V_G until quiescent I_D is 360 mA.
- Apply RF signal

Bias-down Procedure

- Turn off RF signal
- Turn off V_D and wait 1 second to allow drain capacitor dissipation
- Turn off V_G

Evaluation Board Layout

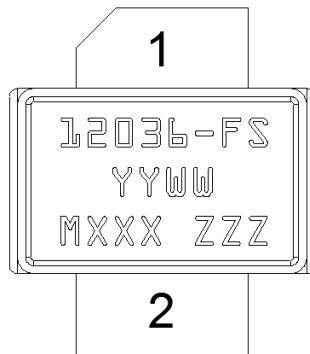
Top RF layer is 0.020" thick Rogers RO4350B, $\epsilon_r = 3.48$. The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances.



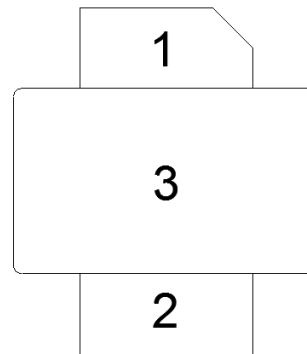
Bill of Materials

Reference Design	Value	Qty	Manufacturer	Part Number
L1	12.55 nH	1	Coilcraft	1606-10_L
L2	12.5 nH	1	Coilcraft	A04T_L
L3	1.6 nH	1	Coilcraft	0603HC-1N6X_L
R1	51 ohms	1	Vishay/Dale	CRCW120651R0FKEA
R2	1000 ohms	1	Vishay/Dale	CRCW12061K00FKTA
C1	1.8 pF	1	ATC	600S1R8BT
C2, C3	15 PF	2	ATC	600S150JT250XT
C4, C9	1000 pF	2	ATC	800B102JT50XT
C5	0.01 uF	1	Kemet	C1206C103KRAC7800
C6	1 uF	1	Allied	18121C105KAT2A
C7	22 uF	1	Sprague	T4910D
C8	2400 pF	1	Murata	C08BL242X-5UN-X0T
C10	220 uF	1	United Chemi-Con	EMVY500ADA221MJA0G

Pin Layout



TOP VIEW



BOTTOM VIEW

Note:

The T1G4012036-FS will be marked with the “12036” designator and a lot code marked below the part designator. The “YY” represents the last two digits of the calendar year the part was manufactured, the “WW” is the work week of the assembly lot start, the “MXXX” is the production lot number, and the “ZZZ” is an auto-generated serial number.

Pin Description

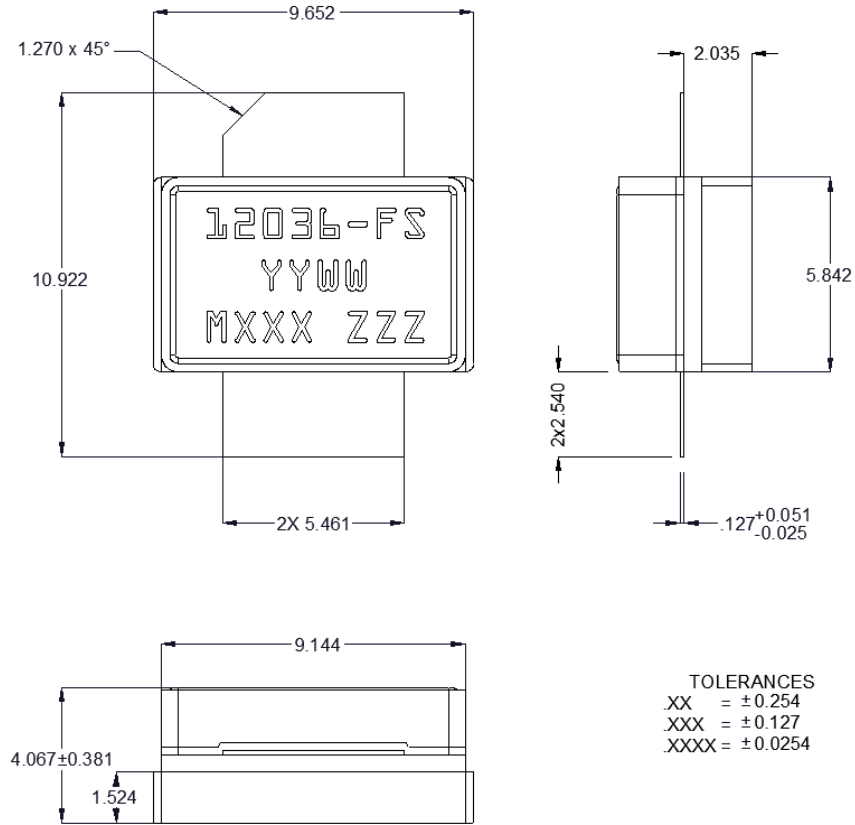
Pin	Symbol	Description
1	V_D / RF OUT	Drain voltage / RF Output matched to 50 ohms; see EVB Layout on page 9 as an example.
2	V_G / RF IN	Gate voltage / RF Input matched to 50 ohms; see EVB Layout on page 9 as an example.
3	Flange	Source connected to ground; see EVB Layout on page 9 as an example.

Notes:

Thermal resistance measured to bottom of package

Mechanical Information

All dimensions are in millimeters.



Note:

This package is lead-free/RoHS-compliant. The plating material on the leads is NiAu. It is compatible with both lead-free (maximum 260 °C reflow temperature) and tin-lead (maximum 245 °C reflow temperature) soldering processes.

Product Compliance Information

ESD Sensitivity Ratings



Caution! ESD-Sensitive Device

ESD Rating: Class 1B
 Value: Passes ≥ 500 V to $< 1,000$ V max.
 Test: Human Body Model (HBM)
 Standard: JEDEC Standard JESD22-A114

MSL Rating

Level 3 at $+260$ °C convection reflow
 The part is rated Moisture Sensitivity Level 3 at 260 °C per JEDEC standard IPC/JEDEC J-STD-020.

ECCN

US Department of Commerce EAR99

Solderability

Compatible with the latest version of J-STD-020, Lead free solder, 260 ° C

RoHS Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Recommended Soldering Temperature Profile

