T1G4020036-FS

DC – 3.5 GHz, 50 V, 2 x 200 W GaN RF Transistor

Product Overview

The Qorvo T1G4020036-FS is a 2 x 200 W (P_{3dB}) discrete GaN on SiC HEMT which operates from DC to 3.5 GHz. The device is in an industry standard air cavity package and is ideally suited for IFF, avionics, military and civilian radar, and test instrumentation. The device can support both pulsed and linear operations.

Lead-free and ROHS compliant

Evaluation boards are available upon request.

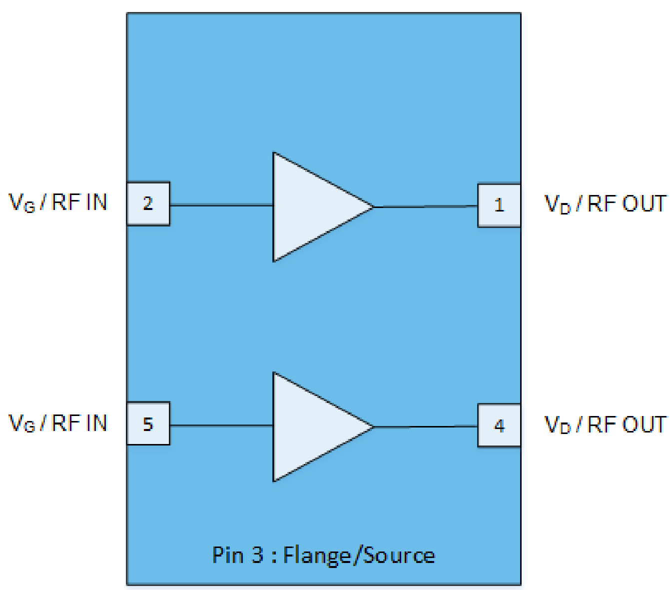
4-lead NI-650 Package (Earless)

Key Features

- Frequency: DC to 3.5 GHz
- Output Power (P_{3dB})[1]: 200 W
- Linear Gain[1]: 18.1 dB
- Typical PAE_{3dB}[1]: 67.6%
- Operating Voltage: 50 V
- CW and Pulse capable

Note 1: @ 2.8 GHz Load Pull (Half of device)

Functional Block Diagram



Applications

- Military and civilian radar
- Professional and military radio communications
- Test instrumentation
- Wideband or narrowband amplifiers
- Jammers

Ordering info

Part No.	Description
T1G4020036-FS	DC – 3.5 GHz, 50 V, 200 W GaN RF Transistor, Earless
T1G4020036-FS-EVB1	2.9 – 3.3 GHz EVB

Absolute Maximum Ratings [1]

Parameter	Rating	Units
Breakdown Voltage, BV_{DG}	+145	V
Gate Voltage Range, V_G	–7 to +2	V
Drain Current, I_{DMAX}	24	A
Power Dissipation, CW, P_{DISS}	236	W
RF Input Power, CW, T = 25 °C	+47.5	dBm
Channel Temperature, T_{CH}	275	°C
Mounting Temperature (30 Seconds)	320	°C
Storage Temperature	−65 to +150	°C

Notes:

1. Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions [1]

Parameter	Min	Typ	Max	Units
Operating Temp. Range	−40	+25	+85	°C
Drain Voltage Range, V_D	+32	+50	+55	V
Drain Bias Current, I_{DQ}	–	520	–	mA
Drain Current, I_D[4]	–	12	–	A
Gate Voltage, V_G[3]	–	−2.8	–	V
Channel Temperature (T_{CH})	–	–	250	°C
Power Dissipation (P_D)[2,4]	–	–	374	W
Power Dissipation (P_D), CW[2]	–	–	211	W

Notes:

1. Electrical performance is measured under conditions noted in the electrical specifications table. Specifications are not guaranteed over all recommended operating conditions.
2. Package base at 85 °C
3. To be adjusted to desired I_{DQ}
4. Pulsed, 100us PW, 20% DC

Measured Load Pull Performance – Power Tuned [1]

Parameter	Typical Values				Units
Frequency, F	2.4	2.8	3.2	3.6	GHz
Output Power at 3dB compression, P_{3dB}	53.1	53.0	52.8	52.9	dBm
Power Added Efficiency at 3dB compression, PAE_{3dB}	54.1	54.7	57.5	54.9	%
Gain at 3dB compression, G_{3dB}	15.6	15.1	15.9	16.0	dB

Notes:

1. Test conditions unless otherwise noted: T_A = 25 °C, V_D = 50 V, I_{DQ} = 260 mA (half device)
2. Pulsed, 100 us Pulse Width, 10% Duty Cycle.

Measured Load Pull Performance – Efficiency Tuned [1]

Parameter	Typical Values				Units
Frequency, F	2.4	2.8	3.2	3.6	GHz
Output Power at 3dB compression, P_{3dB}	50.1	50.2	50.5	50.5	dBm
Power Added Efficiency at 3dB compression, PAE_{3dB}	72.9	67.6	66.5	65.8	%
Gain at 3dB compression, G_{3dB}	17.5	18.4	17.4	18.1	dB

Notes:

1. Test conditions unless otherwise noted: T_A = 25 °C, V_D = 50 V, I_{DQ} = 260 mA (half device)
2. Pulsed, 100 us Pulse Width, 10% Duty Cycle.

RF Characterization – 2.9 – 3.3 GHz EVB Performance at 2.9 GHz [1]

Parameter	Min	Typ	Max	Units
Linear Gain, G_{LIN}	–	16.1	–	dB
Output Power at 3dB compression point, P3dB	162	190	–	W
Drain Efficiency at 3dB compression point, DEFF3dB	40.0	47.0	–	%
Gain at 3dB compression point, G3dB	12.0	13.1	–	dB
Gate Leakage[2] V_D = +10 V, V_G = −3.8 V	−63.4			mA

Notes:
1. V_D = +36 V, I_{DQ} = 520 mA (combined), Temp = +25 °C, Pulse Width = 100 us, Duty Cycle = 20%
2. Gate leakage per path

RF Characterization – Mismatch Ruggedness at 2.9 GHz [1, 2, 3]

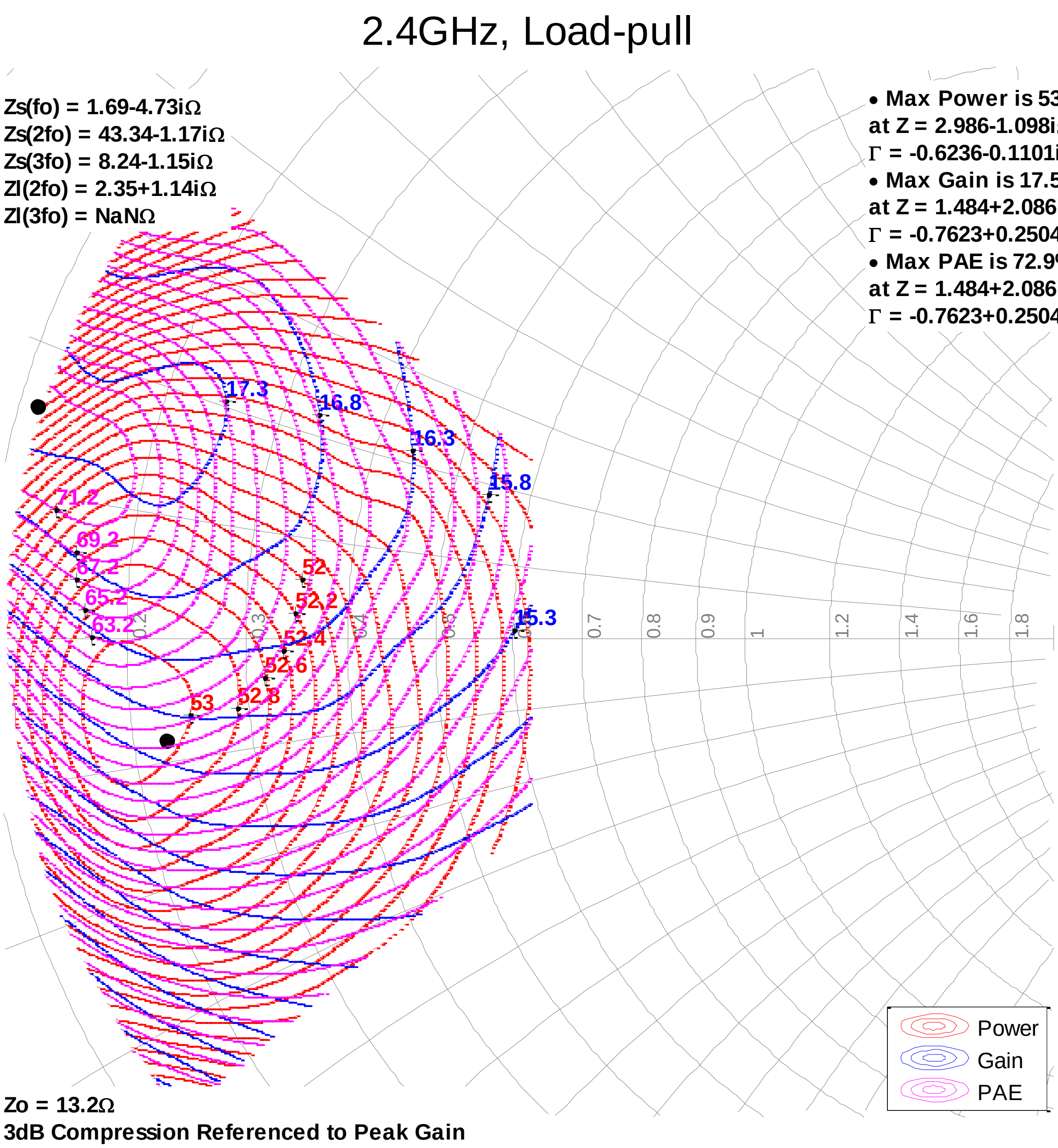
Symbol	Parameter	dB Compression	Typical
VSWR	Impedance Mismatch Ruggedness	3	10:1

Notes:
1. Test conditions unless otherwise noted: T_A = 25 °C, V_D = 36 V, I_{DQ} = 520 mA (combined)
2. Input drive power is determined at pulsed 3dB compression under matched condition at EVB output connector.
3. Pulse: 100us, 20% Duty cycle.

Measured Load-Pull Smith Charts [1, 2, 3]

Notes:

1. Test Conditions: V_D = 50 V, I_{DQ} = 260 mA, 100 us Pulse Width, 10% Duty Cycle, Temp = 25°C.
2. The performance shown below is for only half of the device out of the two independent amplification paths.
3. See page 15 for load pull reference planes where the performance was measured.



Measured Load-Pull Smith Charts [1, 2, 3]

Notes:
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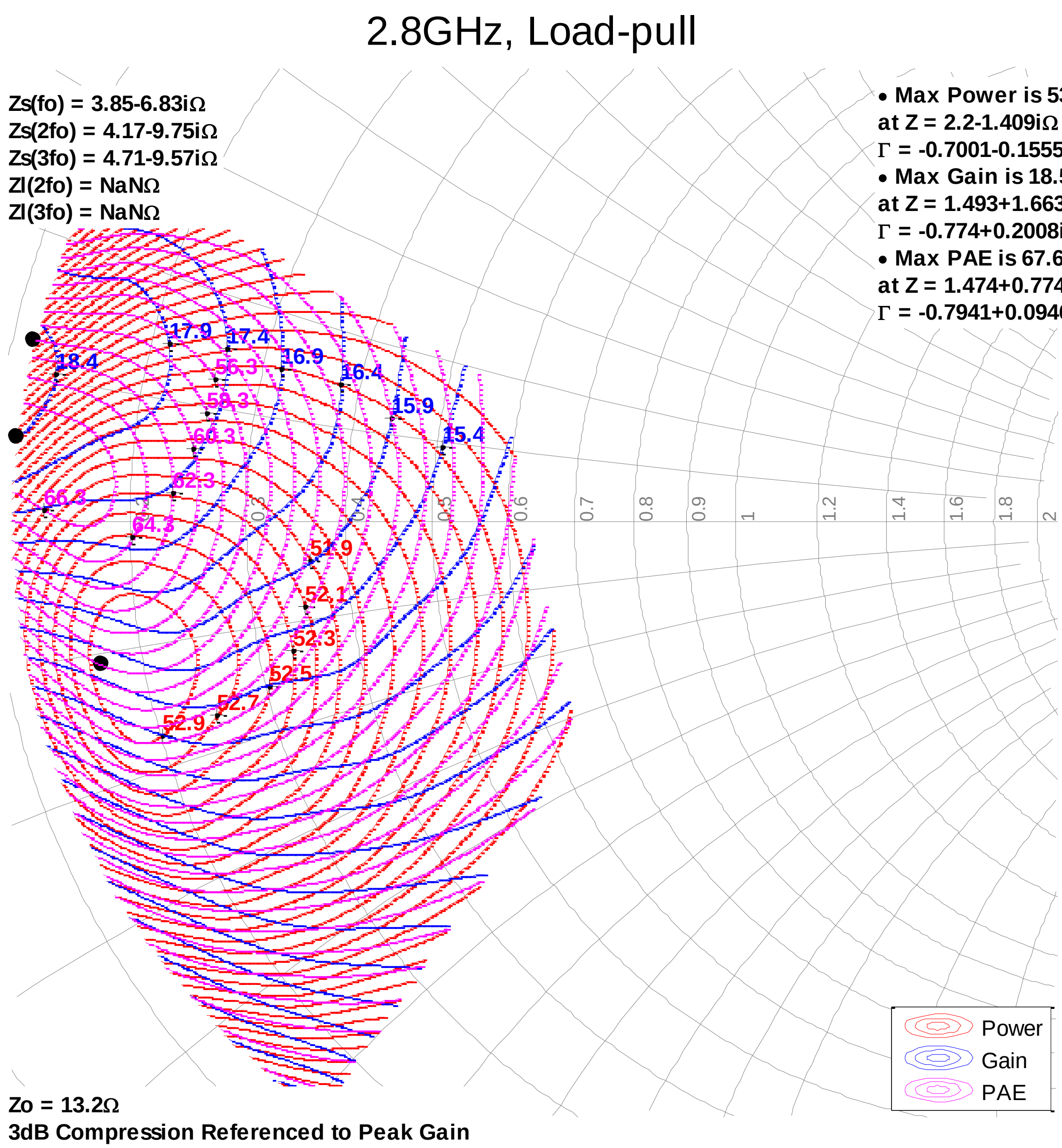

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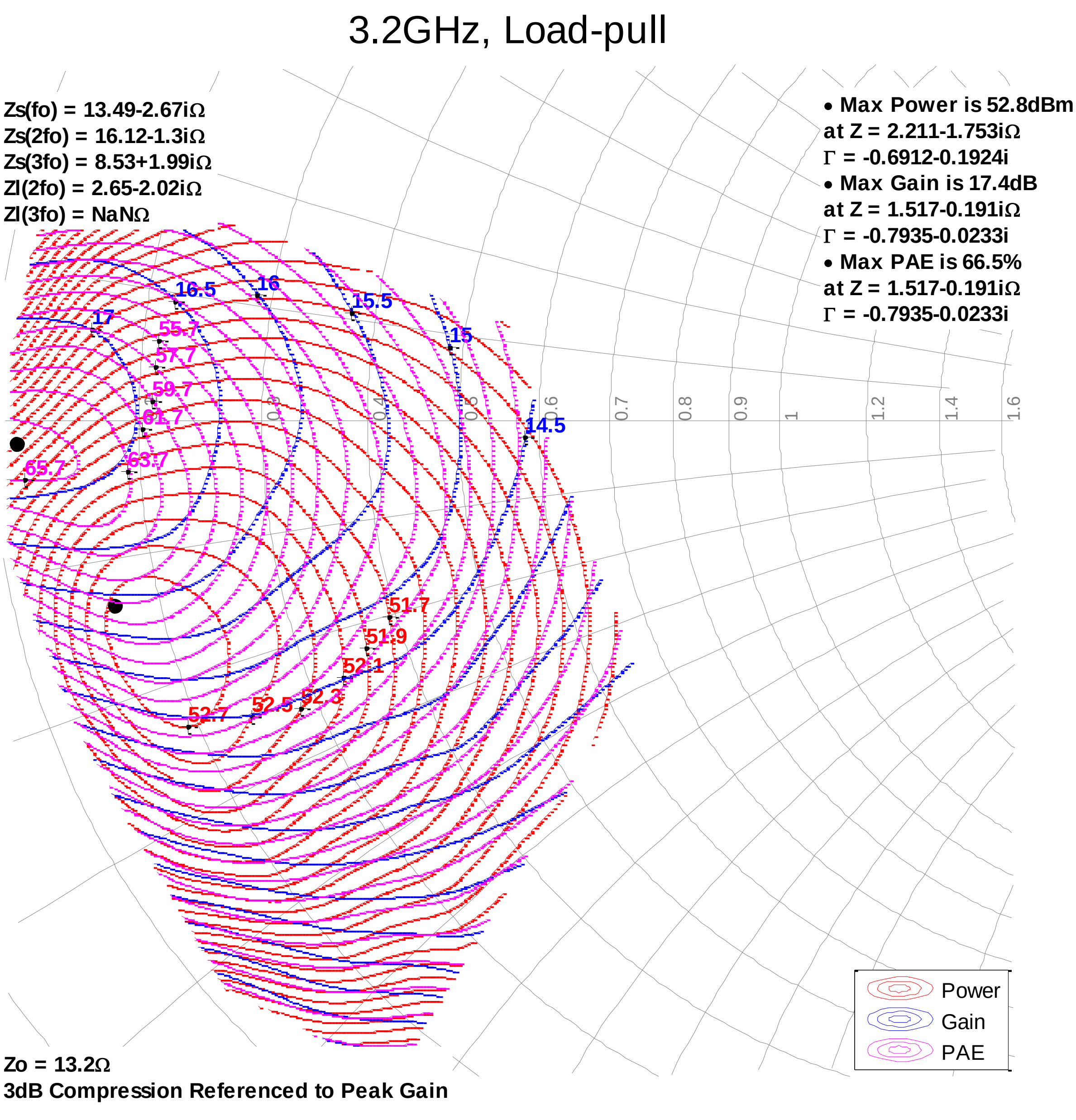

Measured Load-Pull Smith Charts [1, 2, 3]

Notes:
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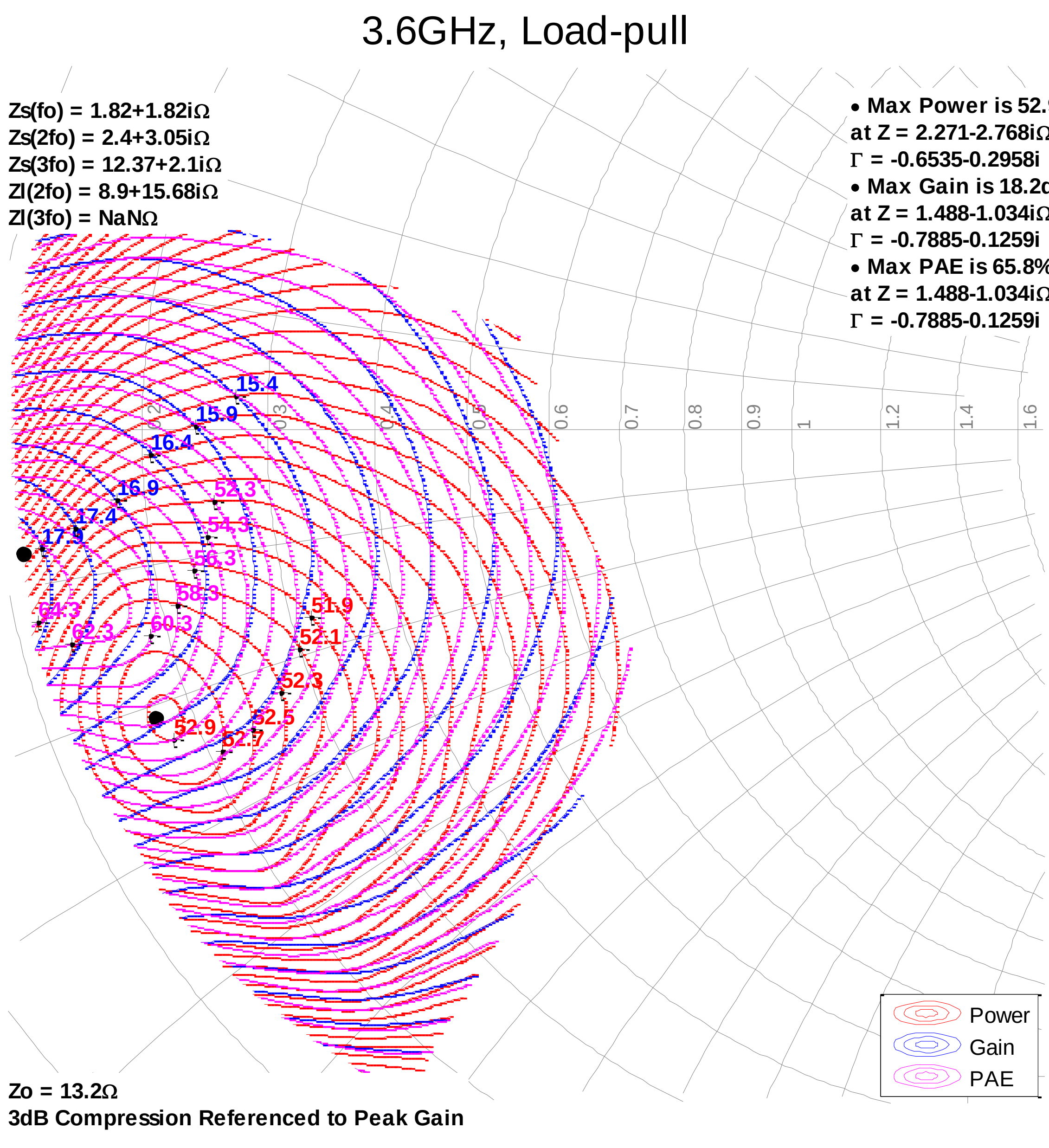

Typical Measured Performance – Load-Pull Drive-up [1, 2]

Notes:
1. Test Conditions: V_D = 50 V, I_{DQ} = 260 mA, 100 us Pulse Width, 10% Duty Cycle, Temp = 25°C.
2. The performance shown below is for only half of the device out of the two independent amplification paths.
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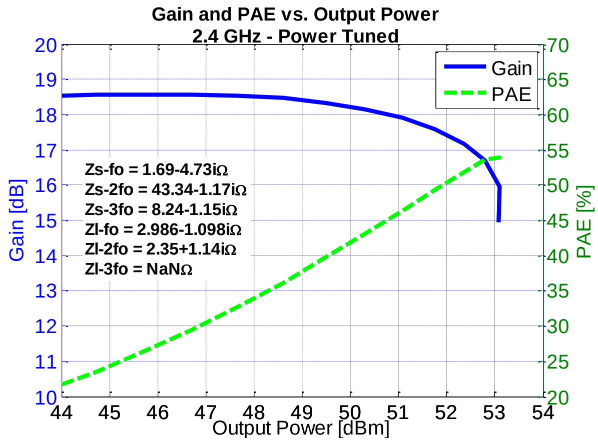

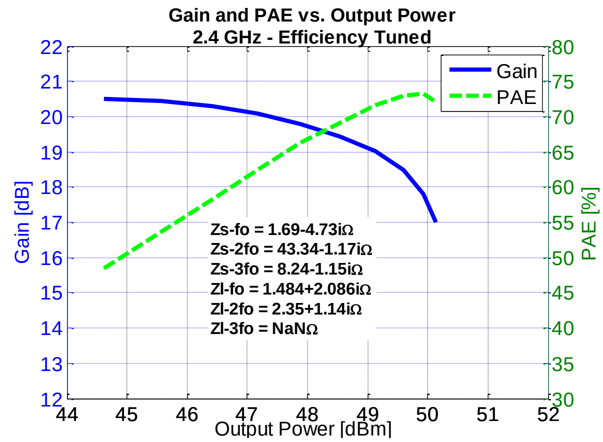

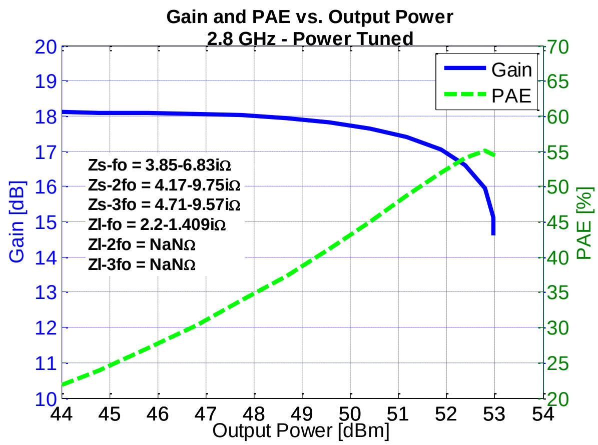

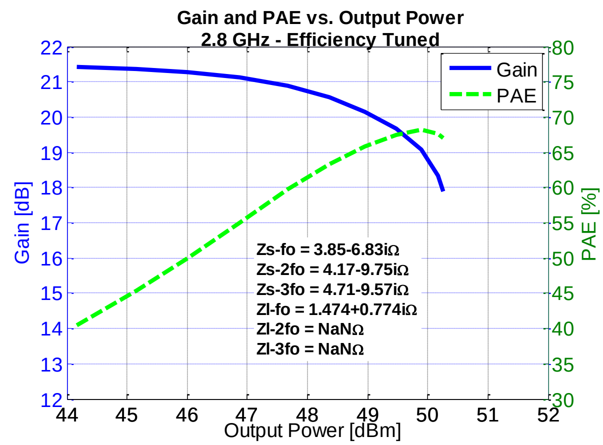

Typical Measured Performance – Load-Pull Drive-up [1, 2]

Notes:

1. Test Conditions: V_D = 50 V, I_{DQ} = 260 mA, 100 us Pulse Width, 10% Duty Cycle, Temp = 25°C.
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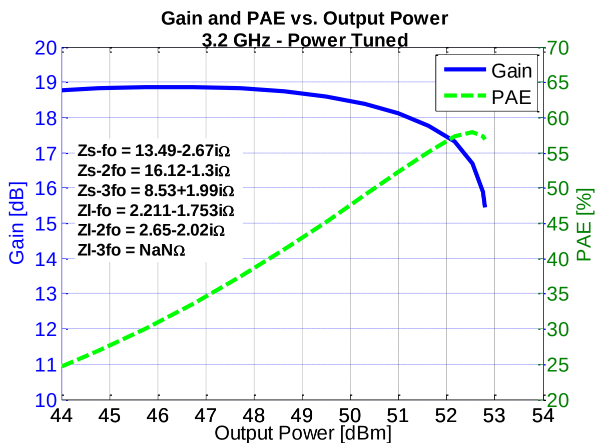
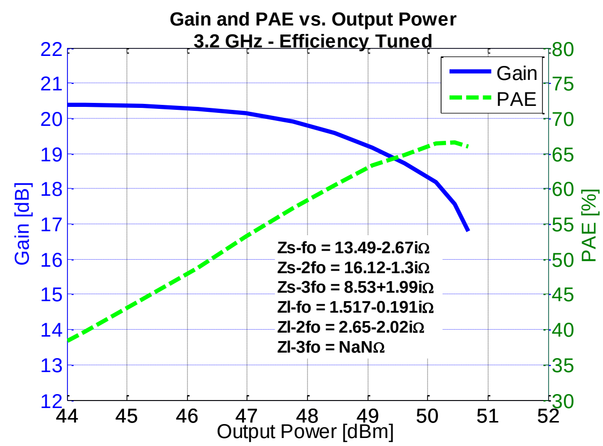
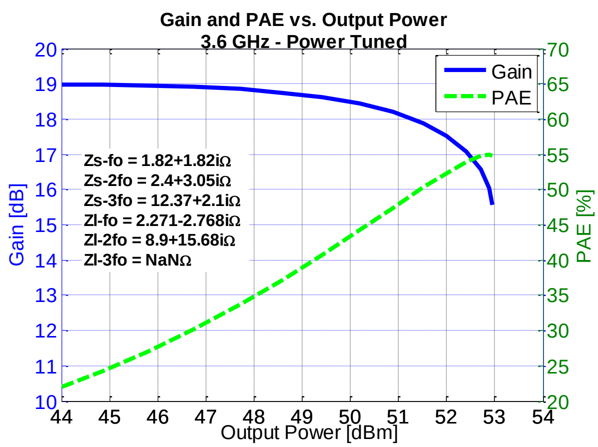
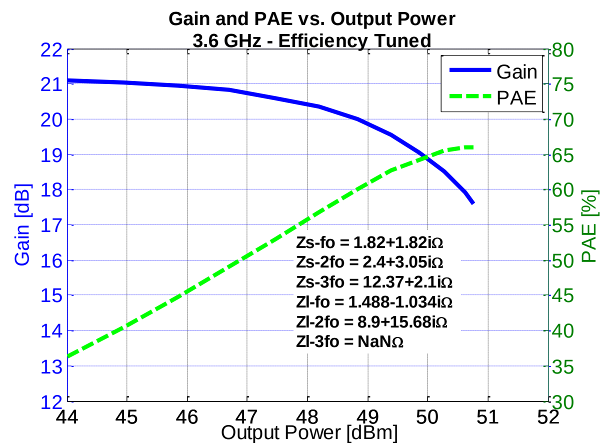


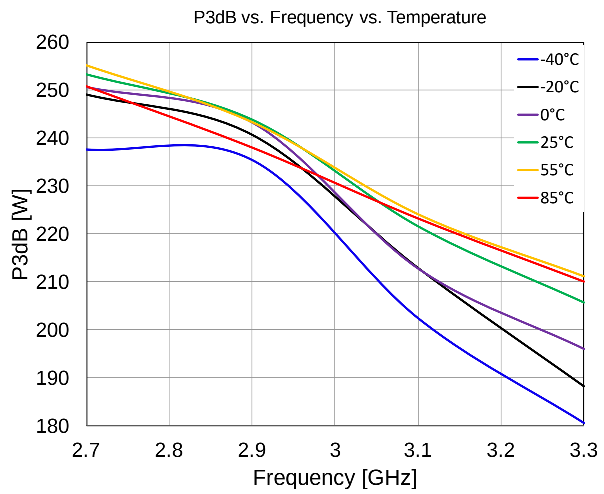


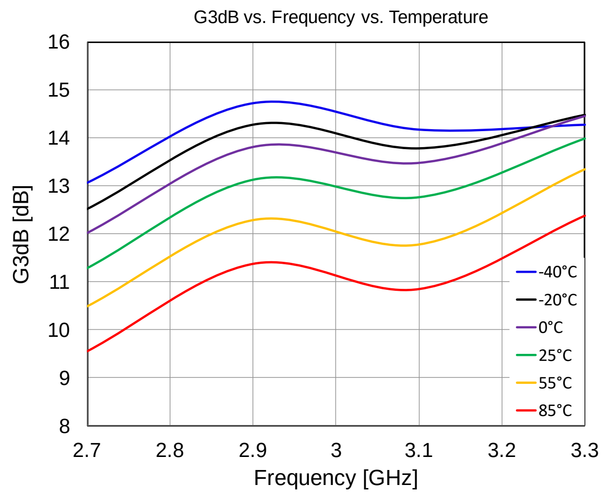


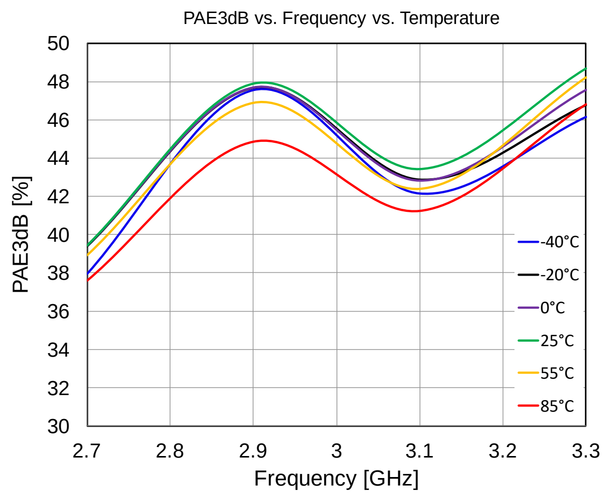


Power Driveup Performance Over Temperatures Of 2.9 – 3.3 GHz EVB [1]

Notes:
1. Test Conditions: V_D = 36 V, I_{DQ} = 520 mA, 100 us Pulse Width, 20% Duty Cycle.

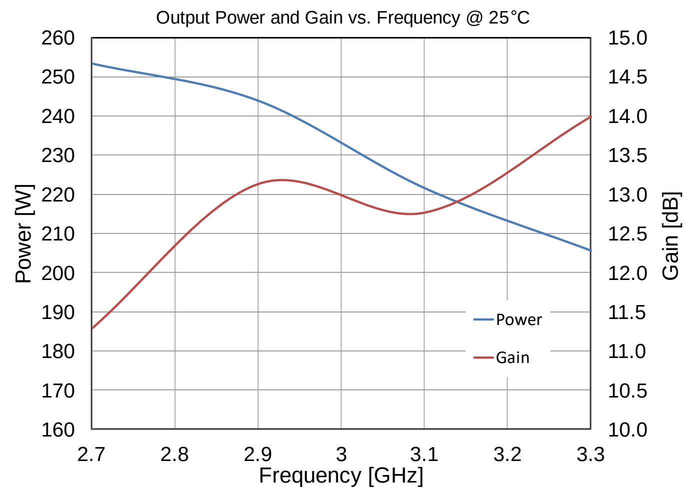


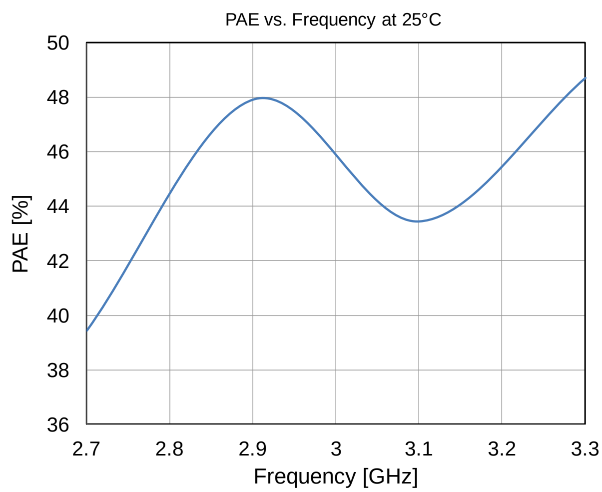




Power Driveup Performance At 25°C Of 2.9 – 3.3 GHz EVB [1]

Notes:
1. Test Conditions: V_D = 36 V, I_{DQ} = 520 mA, 20 us Pulse Width, 20% Duty Cycle.





Thermal and Reliability Information - CW (1)

Parameter	Test Conditions	Value	Units
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	P_{DISS} = 288 W, Tbaseplate = 85°C	0.58	ºC/W
Channel Temperature, T_{CH}		253	°C
Thermal Resistance, Peak IR Surface	P_{DISS} = 230 W, Tbaseplate = 85°C	0.56	ºC/W
Channel Temperature, T_{CH}		213	°C
Thermal Resistance, Peak IR Surface	P_{DISS} = 173 W, Tbaseplate = 85°C	0.52	ºC/W
Channel Temperature, T_{CH}		175	°C
Thermal Resistance, Peak IR Surface	P_{DISS} = 115 W, Tbaseplate = 85°C	0.50	ºC/W
Channel Temperature, T_{CH}		142	°C

Notes:

1. Based on expected carrier amplifier efficiency of Doherty.
2. P_{OUT} assumes 25% peaking amplifier contribution of total average Doherty rated power.
3. Thermal resistance is measured to package backside.
4. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

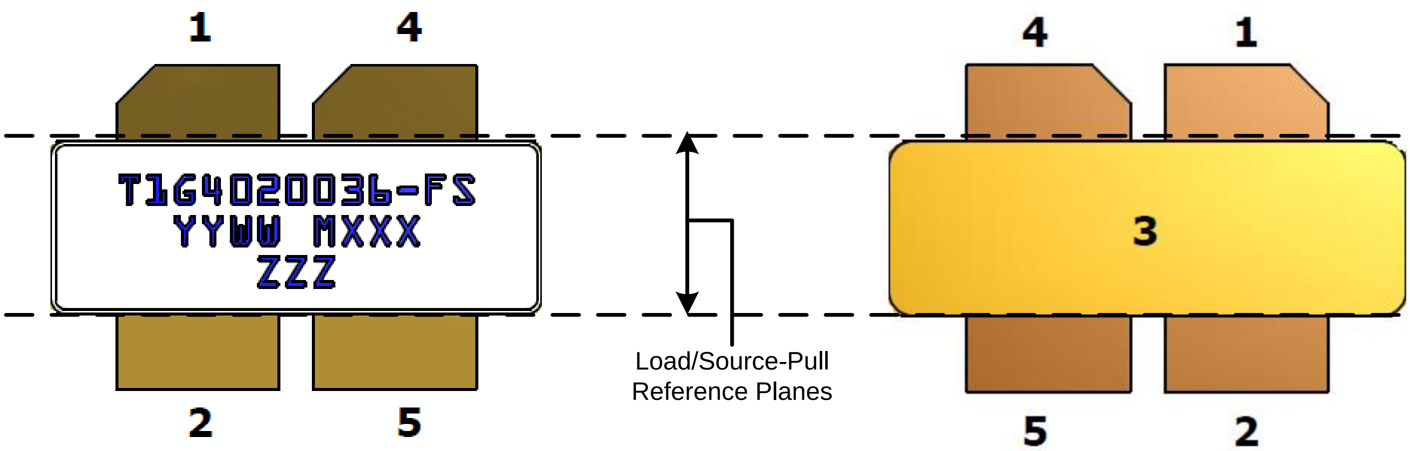
Thermal and Reliability Information - Pulsed (1)

Parameter	Test Conditions	Value	Units
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	P_{DISS} = 230.4 W, Tbaseplate = 85°C Pulse Width = 100 uS Duty Cycle = 5%	0.35	ºC/W
Channel Temperature, T_{CH}		166	°C
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	P_{DISS} = 230.4 W, Tbaseplate = 85°C Pulse Width = 100 uS Duty Cycle = 10%	0.36	°C/W
Channel Temperature, T_{CH}		168	°C
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	P_{DISS} = 230.4 W, Tbaseplate = 85°C Pulse Width = 300 uS Duty Cycle = 20%	0.38	ºC/W
Channel Temperature, T_{CH}		173	°C
Thermal Resistance, Peak IR Surface Temperature at Average Power (θ_{JC})	P_{DISS} = 230.4 W, Tbaseplate = 85°C Pulse Width = 300 uS Duty Cycle = 50%	0.44	ºC/W
Channel Temperature, T_{CH}		187	°C

Notes:

1. Based on expected carrier amplifier efficiency of Doherty.
2. P_{OUT} assumes 25% peaking amplifier contribution of total average Doherty rated power.
3. Thermal resistance is measured to package backside.
4. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

Pin Configuration and Description [1]

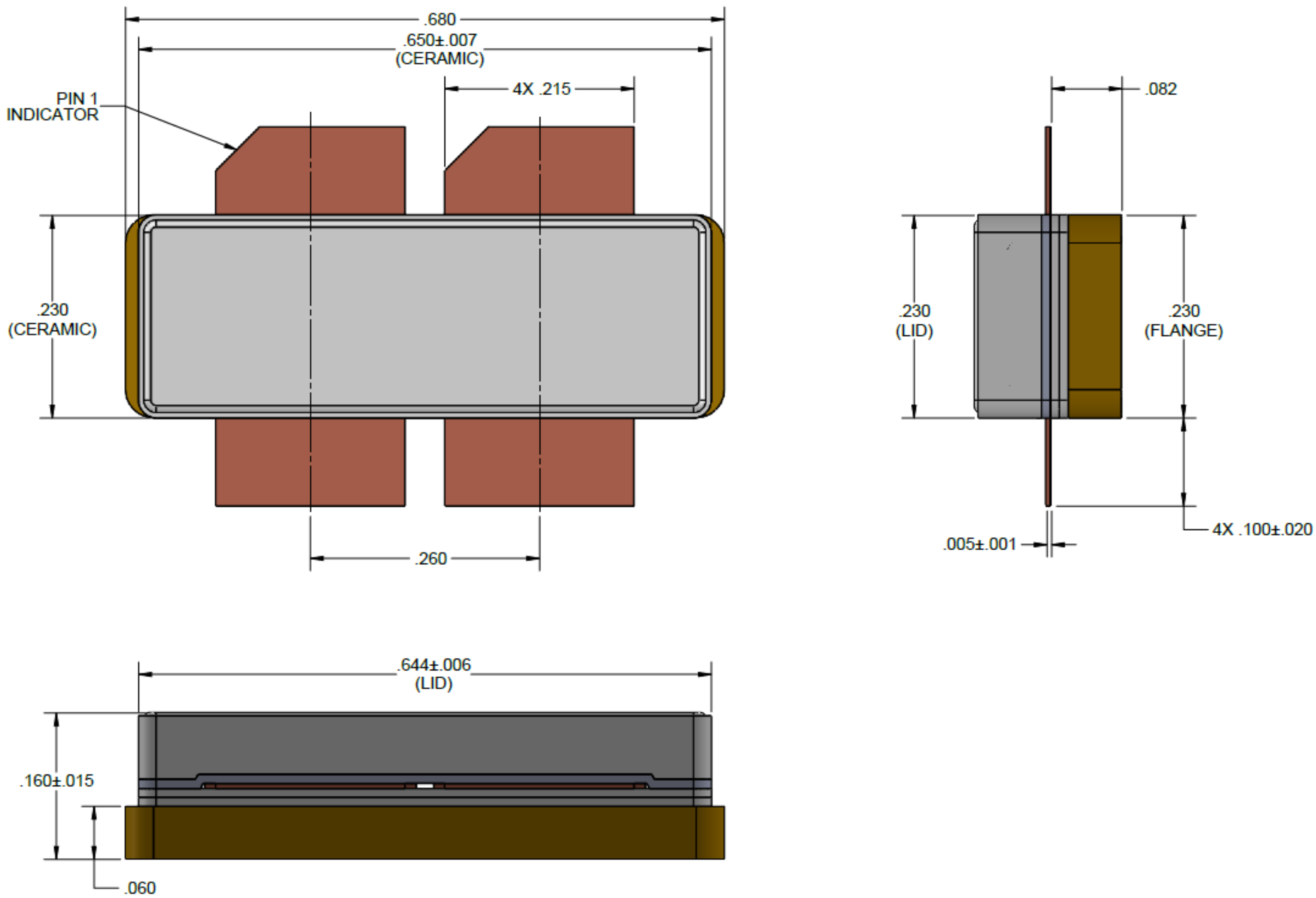


Note:

1- The T1G4020036-FS will be marked with the "20036" designator and a lot code marked below the part designator. The "YY" represents the last two digits of the calendar year the part was manufactured, the "WW" is the work week of the assembly lot start, the "MXXX" is the production lot number, and the "ZZZ" is an auto-generated serial number.

Pin	Symbol	Description
2, 5	RF IN / V_G	Gate
1, 4	RF OUT / V_D	Drain
3	Source	Source / Ground / Backside of part

Mechanical Drawing [1]



Note:

1- MATERIAL:
PACKAGE BASE: CERAMIC / METAL
PACKAGE LID: CERAMIC

2- ALL DIMENSIONS ARE IN INCHES. DIMENSION TOLERANCE IS ± 0.005 INCHES, UNLESS NOTED OTHERWISE.

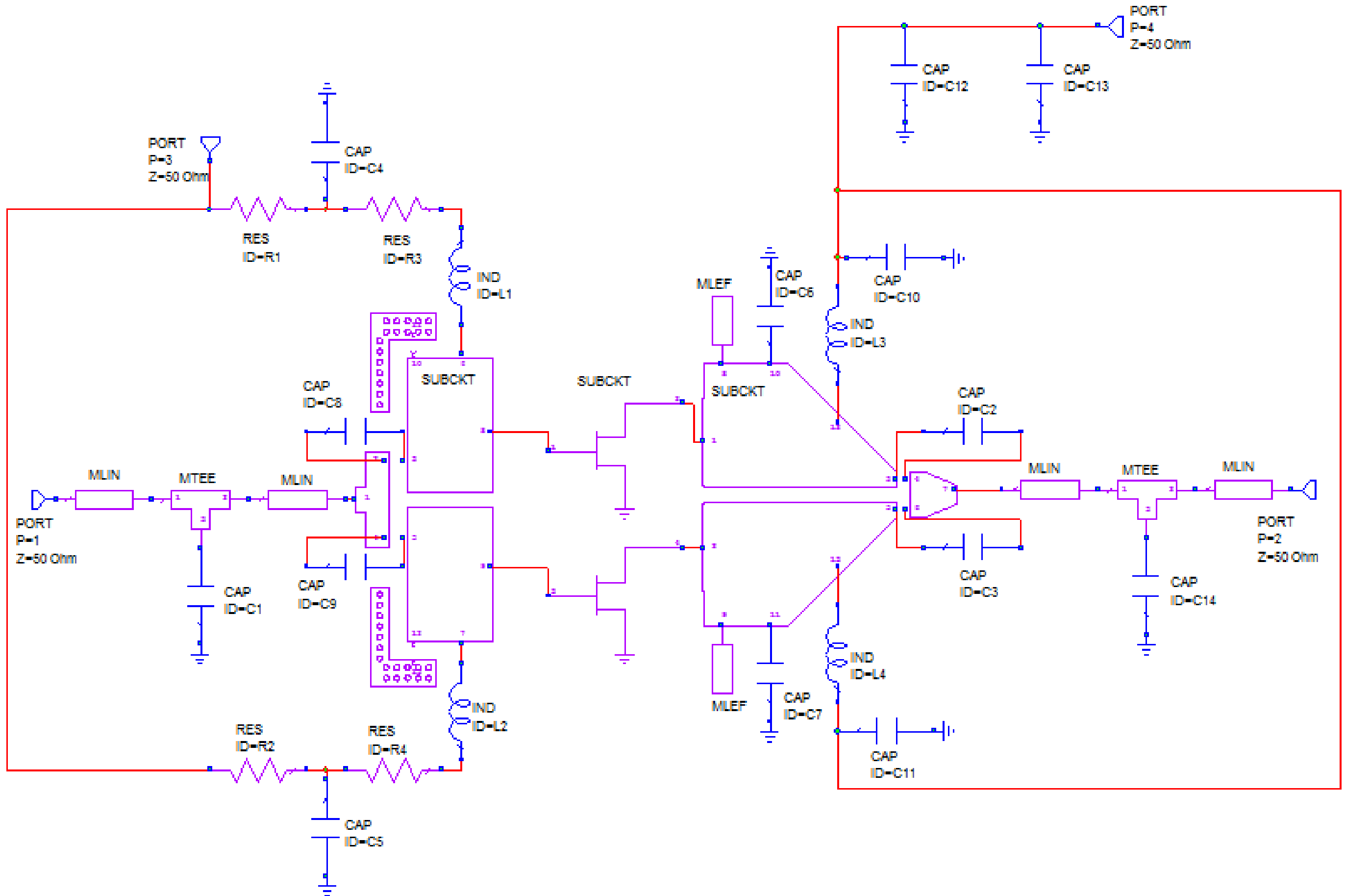
3- PACKAGE METAL BASE AND LEADS ARE GOLD PLATED.

4- PART IS EPOXY SEALED.

5- PARTS MEETS INDUSTRY NI650 FOORPRINT.+

6- BODY DIMENSIONS DO NOT INCLUDE EPOXY RUNOUT WHICH CAN BE UP TO .020 PER SIDE.

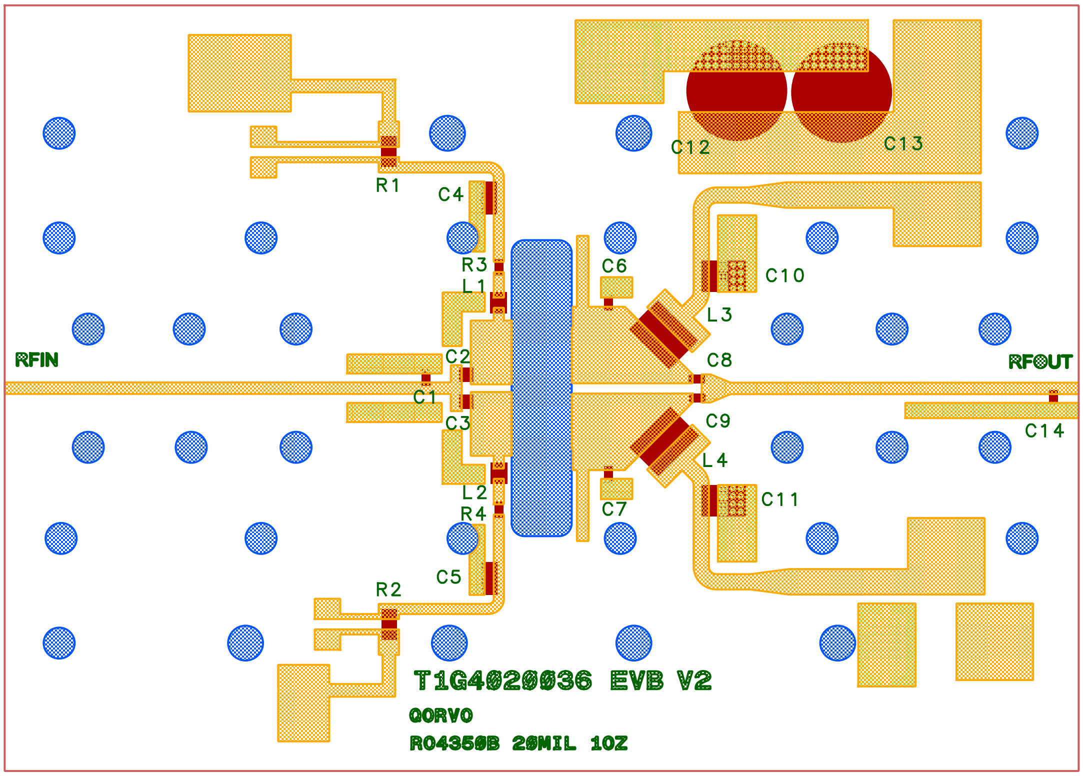
2.9 – 3.3 GHz Application Circuit - Schematic



Bias-up Procedure	Bias-down Procedure
1. Set V_G to -5 V.	1. Turn off RF signal.
2. Set I_D current limit to 4 A.	2. Turn off V_D
3. Apply 36 V V_D.	3. Wait 2 seconds to allow drain capacitor to discharge.
4. Slowly adjust V_G until I_D is set to 520 mA.	4. Turn off V_G
5. Apply RF.	

2.9 – 3.3 GHz Application Circuit - Layout

PCB material is RO4350B 0.020" thick.



2.9 – 3.3 GHz Application Circuit – Bill of Material

Reference Design	Value	Qty	Manufacturer	Part Number
C4, C5	10uF, 6.3V	2	TDK	C1632X5R0J106M130AC
C10, C11	1uF, 100V	2	AVX	18121C105KAT2A
C12, C13	220uF, 50V	2	United Chemi-Con	EMVY500ADA221MJA0G
C2, C3	2.7pF	2	ATC	600F2R7AT250X
C8, C9	5.6pF	2	ATC	600S5R6AT250X
C1	1.6pF	1	ATC	600S1R6AT250X
C6, C7	0.5pF	2	ATC	600S0R5AT250X
C14	0.8pF	1	ATC	600S0R8AT250X
R3, R4	10Ohms	2	Vishay	CRCW060310R0FKEA
R1, R2	0.001Ohms	2	Stackpole Electronics	CSNL1206FT1L00
L1, L2	22nH	2	Coilcraft	0805CS-220X_E_
L3, L4	6.6nH	2	Coilcraft	GA3093-AL_
Connectors	SMA	2	Gigalane	1101055

Recommended Solder Temperature Profile