Application note

How to evaluate and improve Triacs immunity to EFT bursts

Introduction

For ensuring user's safety, the designers are asked for complying their appliances to worldwide, regional and/or local standards. Especially, the electro-technical appliances must avoid any possible mechanical bodily harms, electrical shock or fire ignition, and even more, during nominal operation and in some degraded modes. Therefore, designers need to prevent any risk for the user in case of spurious activation coming from external electrical perturbances.

Mechanical contacts switching and circuits opening on inductive loads are the main sources of such external electrical disturbances coming from other appliances connected near on the power grid.

When submitted to such events, electrical fast transient bursts (EFT bursts) are applied to the appliances power and control lines. When an appliance embeds Triacs for controlling alternative current loads, it is then necessary to take care about those Triacs immunity to EFT bursts.

The present document will first describe a method for evaluating a single Triac intrinsic immunity to EFT bursts. Then it will provide explanations on the SCR and Triac internal silicon structures which will allow the reader to better understand the relationship between the type of Triac and its proper immunity; while explaining the effect of external filtering components as well. This will guide the designer in the Triac choice. Finally, tips for even enhancing the Triac overall immunity will be described.

1 Reminder on standards

Electrical perturbances applied to the appliances are in practice all different in current and voltage waveforms but have all a similar signature. This is the reason why the IEC (international electro-mechanical comity) was able to define an EFT burst model which can be used to verify an application conformance to EFT bursts immunity.

The measurement method, the dedicated tooling and the maximum levels for EFT bursts immunity checking have been described in the IEC 61000-4-4 standard which is one chapter of the IEC 61000 standards dedicated to the systems EMC (electro-magnetic compatibility). Many of the appliance specific product standards directly, or through regional / local declination, refer to this IEC 61000-4-4 standard. Those ones require to strictly comply, or even precise when and up to which level a given specific system needs to comply with. It applies to complete systems and not to alone sub-assemblies such as printed circuit boards or single electronic components.

In more details, the IEC 61000-4-4 standard describes the evaluation method through:

- The physical position of the equipment under test (EUT), especially its vertical distance referred to a ground reference plane
- The distance between the EFT busts generator and the EUT
- The connections to the ground reference plane
- The coupling / decoupling network to use for submitting the EFT burst stress in a standardized way and regardless the power grid actual impedance
- The EFT bursts waveforms (each spike rising/falling characteristics, repetition frequencies, polarities…)
- The duration of the test

In addition, the standard defines some levels as reference acceptance criteria for coupling to power or signal lines.

As an example, for electro-domestic appliances which are submitted to the IEC 60335-1 standard, a level 4 is required for the power lines which is corresponding to 4 kV EFT bursts peak voltage, applied for a two minutes duration. This must not create any over-heating which could lead to fire, neither expose the user to any mechanical bodily harm or electrical shock.

2 EFT bursts immunity evaluation of a single Triac

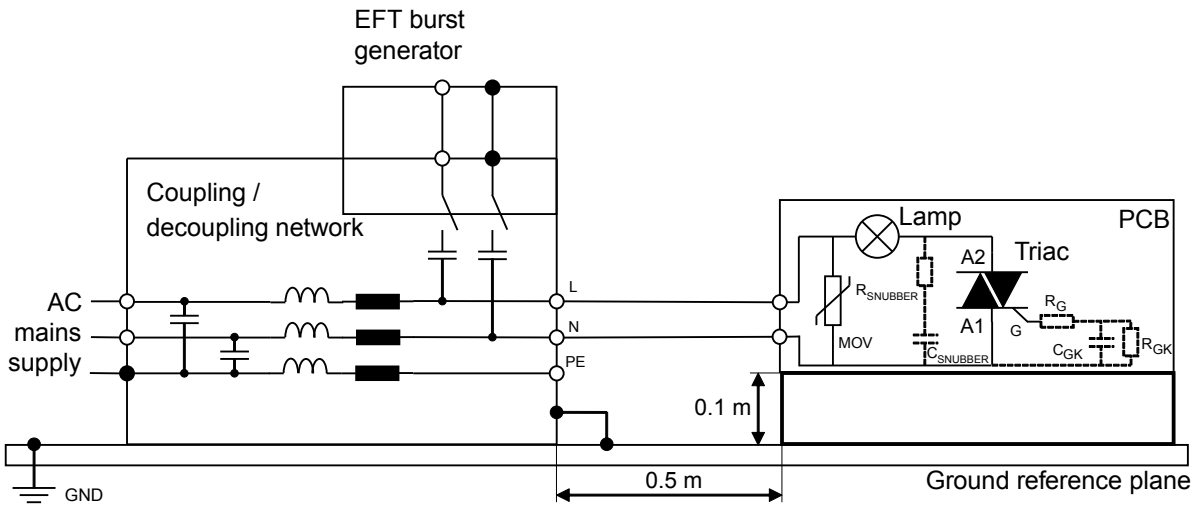
The IEC 61000-4-4 applies to complete equipment assemblies. However, evaluating a single Triac immunity to EFT bursts does make sense to choose the right part number.

Indeed, in case a Triac is controlling an AC load which could impact the user safety in case of spurious ignition, getting a high intrinsic Triac immunity will help ensuring the user safety at system level.

This is the reason why measuring and comparing the immunity to EFT bursts at Triac level, for different Triac part numbers and/or for different external filtering passive components will help the designers for choosing the best solution according to their robustness requirements and design constraints.

To proceed to such an evaluation, the circuit schematic as shown on the Figure 1 is used. The EFT bursts are superimposed to the AC mains voltage by capacitive coupling. Bursts are generated during 2 minutes between L and ground or N and ground in positive and negative polarities. The Triac is placed on a specific PCB which remains identical when comparing different part numbers. This PCB has no ground plane neither protected shield, so it does not contain any PE connection as, again, the evaluation is concerning a single Triac and not a complete system assembly.

Figure 1. EFT burst Triac immunity test setup



The Triac is placed in series with an incandescence lamp whose role is to visually witness any spurious Triac ignition while applying the EFT stress.

For all the couplings and polarities configurations, the EFT bursts voltage is progressively increased until the lamp is starting to flash. The last voltage level with no lamp ignition is retained. Finally, the lowest EFT burst voltage value from the four testing configurations (L+|GND, L-|GND, N+|GND, N-|GND) gives the Triac immunity level.

For an overall evaluation accounting for any manufacturing dispersion, this testing procedure is repeated on several samples coming from different production batches. This results in a Triac overall part number immunity performance value.

A MOV (metal-oxide varistor) is systematically placed at the input circuit to avoid the Triac ignition by breakover. Indeed, the EFT burst voltage level is expected to be higher than 1 kV, so higher than any common Triac V_{DSM} parameter, whereas the present evaluation goal is to measure the immunity to fast transient but not to high voltage where any Triac is assumed to trigger by breakover.

The immunity of a SCR (silicon controlled rectifiers) or a Triac (triode for alternative current) can also be evaluated when assisted by external EMI filtering passive components, like a snubber or a gate filter.

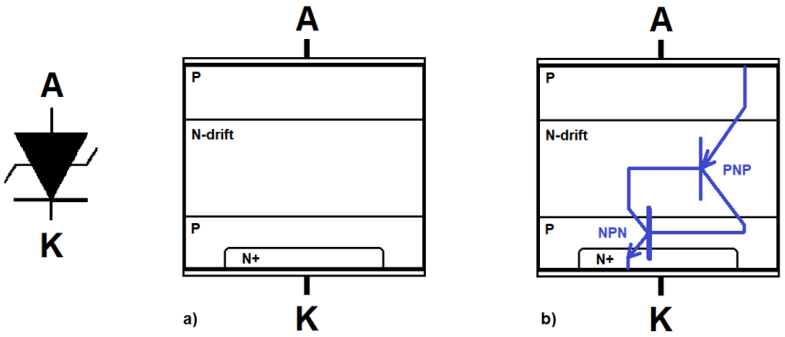
The measurement is performed at room temperature because the immunity to EFT is mainly wanted at OFF-state. The measurement could be performed at higher ambient temperature while the physical setup would remain compatible with the positioning referenced to the ground reference plane.

Most of the Triacs datasheets include a static dV/dt parameter. This parameter is a good first input to simply compare some Triacs performances in terms of immunity. However, as the EFT bursts may occur at lower temperature than the dV/dt specification and is a question of bursts repetitions bringing a kind of integrative phenomenon, the static dV/dt parameter and immunity to EFT bursts cannot be so directly correlated.

3 Triac choice for best immunity

The basic structure of any crowbar type of semiconductor device is made of four silicon types layers. Most of this kind of components are diffused on a N-type substrate due to higher electron mobility characteristics in this wide drift region. As a result, the four layers order, from anode (A) to cathode (K), is usually PNPN as described on the Figure 2 a).

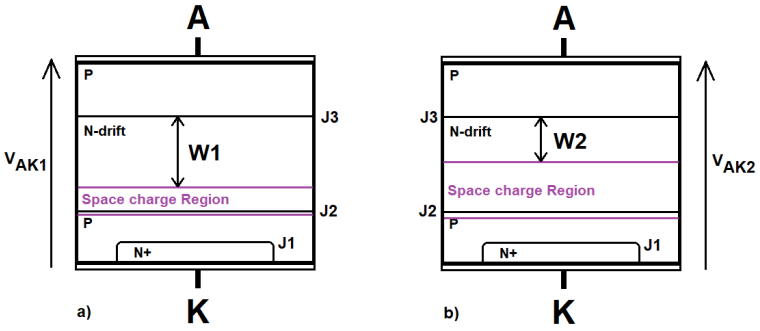
Figure 2. PNPN description



The SCRs (silicon controlled rectifiers) and Triacs (triode for alternative current) are using this basic structure with the addition of a gate terminal.

The crowbar structure can also be seen like two bipolar junction transistors (bjt), one PNP and one NPN, with each base terminal connected to the collector terminal of its associated internal transistor, as shown on the Figure 2 b). At ON-state, those both bjt will saturate each other.

Figure 3. Crowbar structure



At off-state, with $V_{AK} > 0$, J_2 is the PN junction which is sustaining the A-K voltage. Higher the voltage is and wider the space charge region is. In the meantime, higher the voltage is and lower W will be. As illustrated on the Figure 3, applying $V_{AK2} > V_{AK1}$ will lead to W2 < W1.

As W is corresponding to the effective PNP base width which defines the actual PNP transistor current gain, the structure triggering will be easier at higher voltage due to the higher PNP current gain. This explains why a lower gate current is required for triggering a SCR or a Triac when the applied voltage is high prior to the gate current ignition. Historically linked to the curve tracers setup, the I_{GT} parameter is given in the ST SCRs or Triacs datasheets for V_{AK} (or V_{A2A1}) equal to 12 V which is a low voltage compared to AC mains peak voltage, so can be considered as a worse case. For instance, when a Triac is used as an AC switch in a 230 V / 50 Hz application, the specified I_{GT} will ensure the triggering at:

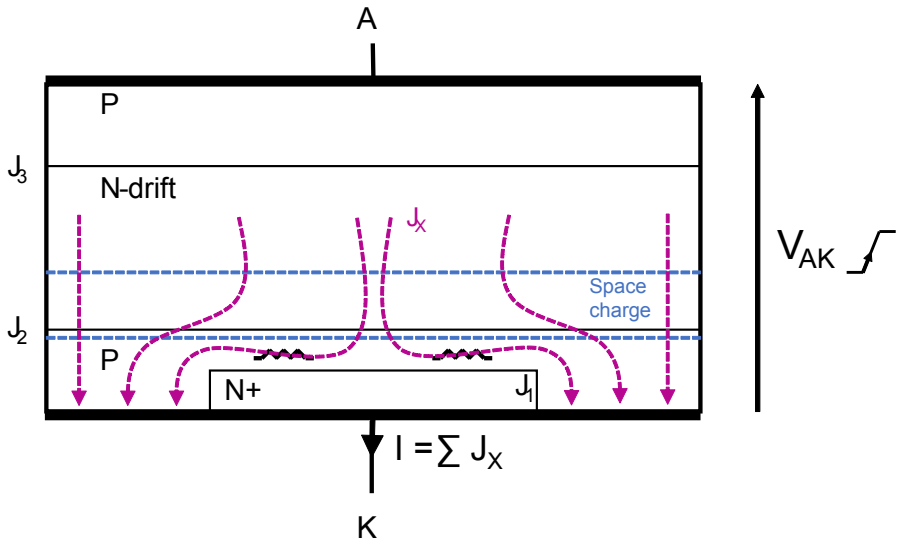
$$t = \frac{1}{2\pi \cdot 50}\text{asin}\left(\frac{12}{230\sqrt{2}}\right) \cong 100\ \mu s$$ after the zero AC mains voltage crossing in worse case.

This is well fitting to the common Triac usages.

Besides, as its space charge region width is lower at low voltage, the J_2 junction capacitance will be higher at low A-K voltage. This junction capacitance is not constant and is a non-linear decreasing function of the A-K voltage. Therefore, still considering the off-state, a capacitive current is internally generated across J_2, which can be considered as a capacitor at off-state, when a positive A-K voltage slope is applied. And this capacitive current will be higher at lower A-K voltage due to higher capacitance. This relies on the following theoretical equation:

$i_{C\_J2} = C_{J2}(v_{AK}) \cdot \frac{dv_{AK}}{dt}$, *where* $C_{J2}(v_{AK})$ is a non-linear decreasing function of A-K voltage.

Figure 4. Illustration of the capacitive current densities flowing in the P region below the N+ region



Now, considering the internal capacitive current densities generated at the J_2 junction when an A-K transient voltage is applied as shown on the Figure 4; as long as the J_1 junction has not reached its proper forward conduction voltage, the part of the capacitive current generated under the N+ region needs to flow through the P region in order to join the cathode terminal. As the P region area located under the N+ region can be considered as a resistance, the sum of capacitive current densities flowing there will lead to apply a voltage drop across the J_1 junction. As soon as the J_1 is polarized, the corresponding NPN internal transistor will be activated and then will activate its associated PNP transistor. Consequently, the crowbar structure will trigger.

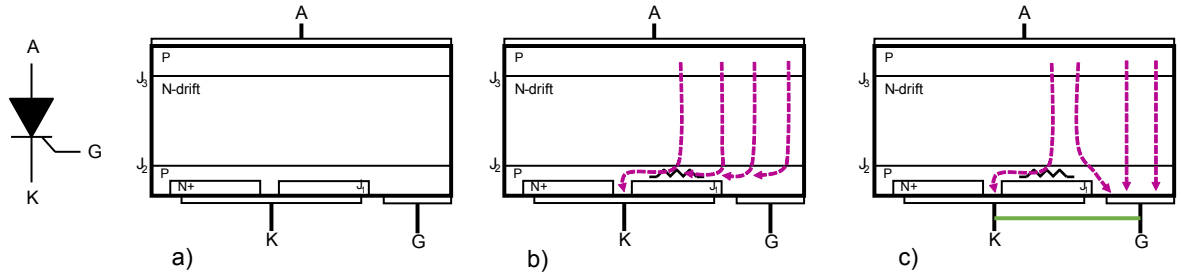
This is describing the triggering phenomenon of a silicon crowbar structure by dV/dt.

It must be said that the J_2 current would be even higher in case of the silicon temperature is increased due to higher electron-hole pairs generation in the space charge region and higher carriers lifetime.

All the above description explains why the dV/dt performance is specified in the ST SCRs and Triacs datasheets with a voltage slope starting from zero, reaching a high maximum applied voltage, usually $\frac{2}{3}$ of V_{DRM}, and for the maximum junction temperature.

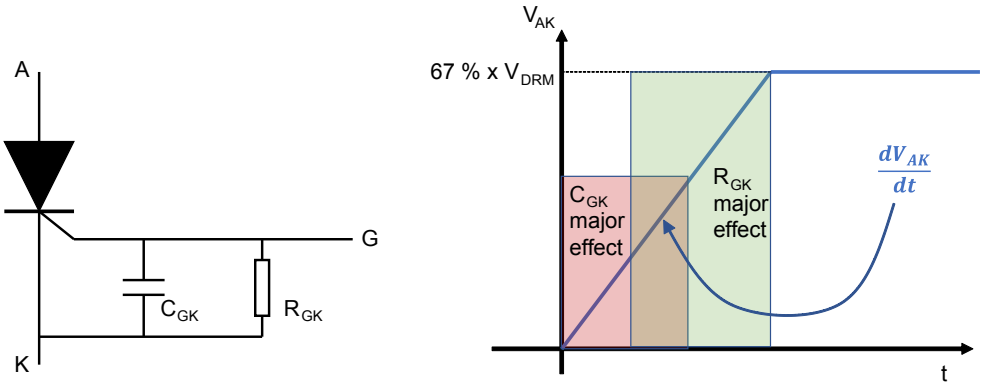
The triggering by dV/dt mechanism was described for a simple crowbar structure. As an enhancement the SCRs and Triacs allow the triggering by the application of a gate current. This feature is achieved by adding a gate terminal connected to the P region on the same side than the cathode, like shown on the Figure 5 a). The Figure 5 b) illustrates the capacitive current densities created in the gate region when a positive A-K voltage transient is applied and when the gate is not connected (open). It can be observed that those current densities are adding a significant current flow across the P region equivalent resistor located under the N+ region leading to polarize the J_1 junction earlier. This will trigger the structure for a lower applied dV/dt than in an equivalent simple crowbar configuration with no gate. Finally, on the Figure 5 c), a similar behavior is shown but with the gate terminal externally connected to the cathode terminal. This time, the capacitive current densities generated in the gate area are collected by the gate terminal and no more contribute to the J_1 polarization.

Figure 5. a) typical SCR structure, b) capacitive current density at gate open, c) capacitive current density with G-K short-circuited



This is explaining why adding an external impedance between the gate and cathode terminals will improve the immunity of a SCR against voltage fast transients. For sure, directly connecting the G-K terminals makes no sense as the triggering through the gate feature would be consequently lost. But placing a capacitor instead is particularly efficient especially for low A-K voltage with high slope when it can then be considered as a wire; in combination with a gate to cathode resistor which will enhance the efficiency at higher A-K voltage. This resistor will also help to discharge the G-K capacitor especially for the very sensitive SCRs. So, connecting a capacitor in parallel to a resistor across the gate-to-cathode of a SCR is a common way to enhance its immunity to fast transients, as shown on the Figure 6.

Figure 6. Gate-to-Cathode capacitor and resistor enhance the SCR dV/dt performance

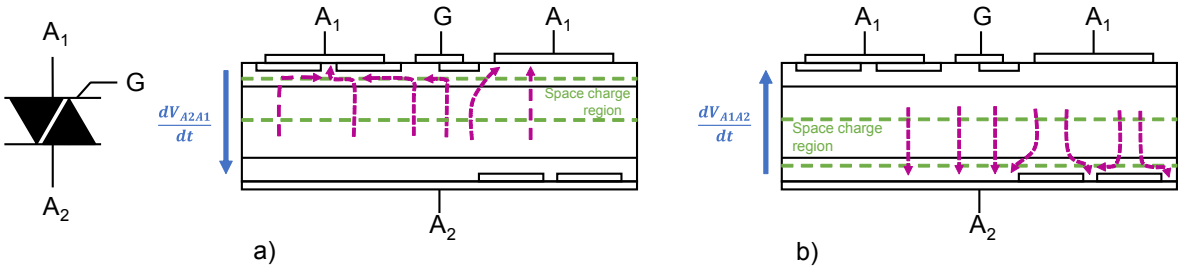


However, connecting capacitor directly across gate-to-cathode for a Triac is not recommended for reliability reasons as referred in the AN4030 (“Gate to cathode capacitor, impact on Triac immunity and reliability”). As it will be described in a following chapter, it is better to share the gate resistor and place the capacitor in between to form a called R-C-R T-filter whose efficiency will remain high.

It must be noticed here that dV/dt parameter of most of the ST SCRs and Triacs is specified in datasheet at gate open because, as demonstrated above, it is well corresponding to the worse case. Only the very sensitive devices, means very low gate triggering current in the range of few tenths of µA, are specified with a G-K resistor added to the parameter measurement conditions description.

Now moving to the Triac structure which is basically made of two SCRs placed in back-to-back configuration, it is easy to understand through the Figure 7 that the capacitive current generated in the gate area will have a lower impact in negative polarity than in positive one as the gate area is located on the A_1 terminal side.

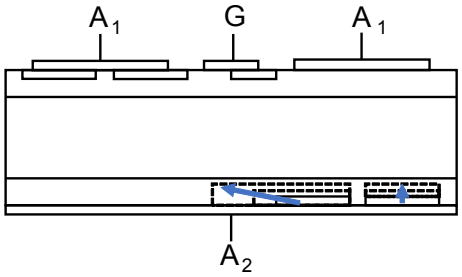
Figure 7. a) illustration of the current flow when positive voltage slope is applied between A_2 and A_1, b) between A_1 and A_2



Indeed, when a positive voltage slope is applied from terminal A_2 to terminal A_1, as illustrated on the Figure 7 a), the current densities generated in the gate area need to flow through the N+ area to reach the A_1 terminal. By opposition, if a positive voltage slope is applied from A_1 to A_2, as illustrated on Figure 7 b), the current densities generated in the gate area can straight ahead reach the A_2 terminal with no contribution to the structure triggering.

However, for triggering the Triac structure in the negative polarity (V_{A2} - V_{A1} < 0) while maintaining the required gate current as low as possible, the backside NPN equivalent transistor gain must be increased. This is usually achieved by diffusing more in depth the N+ layer and/or by increasing the area of the backside N+ layer under the gate as shown on the Figure 8. Those technics are even reinforced when designing a device specified in the fourth quadrant (V_{A2A1} < 0 with I_G > 0), refer to AN4993 (“How to implement an SCR or a Triac in hybrid relay applications”) for Triac quadrants definition.

Figure 8. A_2 side N+ layer size and depth increase to achieve lower I_{GT} in the 3rd and 4th quadrants



It can be deduced from the Figure 8 that the reverse dV/dt performance will be affected when looking for lower I_{GT}, and even more when the triggering is required on the fourth quadrant.

Therefore, getting a high dV/dt performance while keeping a low I_{GT} value is the result of a compromise. Higher the I_{GT} parameter is and higher the dV/dt parameter will be too. In addition, for the same I_{GT} value, a three quadrants Triac offers a better immunity to fast transients than a four-quadrants one.

A high I_{GT} value requires to design a higher power circuit for the gate drive, which is increasing the solution size and cost.

Additionally, a direct connection to MCU is convenient with limited I_{GT} Triac.

Therefore, the solution robustness will come from a trade-off between the Triac choice, especially its proper dV/dt and I_{GT} parameters balancing, the sizing of the auxiliary power supply, the gate driver and the count of EMI additional filtering passive devices and parasitic passive of assembly (for example: parasitic capacitor of PCB tracks or parasitic inductor of application wires).

For an optimized starting point, it is better to choose, when possible, a less sensitive Triac (I_{GT} ≥ 35 mA), with no capability in the 4th quadrant. The ST T-series, H-series and 8H-Triacs series 35 mA three-quadrants Triacs are typically designed for reaching such a very high immunity robustness, while offering high commutation and thermal performances at 150 °C of maximum junction temperature.

4 Enhancing EFT burst Triac robustness

There are many ways for designing auxiliary power supplies compatible with the control of a three-quadrants Triac (in Q_1 / Q_3 or Q_2 / Q_3) with no need of the triggering capability in the fourth quadrant. It can be achieved by using a capacitive power supply or a buck-boost converter with $+V_{dd}$ connected to the line. Or, for an isolated version, fly-back or push-pull converters are commonly used. The pulse transformers offer the triggering in Q_2 / Q_3 in an isolated configuration as well.

For additional information concerning the auxiliary power supplies commonly used for controlling the Triac gate, the reader can refer to the following ST application notes:

- AN3168: Non-insulated SCR / Triac control circuits
- AN4564: Is a positive power supply mandatory for my application, or could a negative output work also?
- AN436: Triac control by pulse transformer

Except for specific topologies where positive power supply ($-V_{ss}$ connected to the line) remains mandatory, it is then possible to use three quadrants Triacs which offer higher intrinsic immunity compared to four quadrants ones as previously demonstrated.

Considering the choice for three quadrants is done, the power consumption for the gate depends on the V_{dd} voltage level. Indeed, any Triac is controlled by a current applied to its gate. Considering a constant gate current, the consumption will basically be:

$$P_{gate} = V_{dd} \cdot I_g.$$

As a result, it is better from a Triac gate driver power consumption point of view to adopt a low power supply voltage, 5 V or even 3.3 V for instance.

Knowing that a Triac gate triggering current (I_{GT}) parameter depends on its junction temperature with higher value at low temperature and considering that the triggering must be ensured at low temperature in the application, designers will have to dimension the gate resistor accordingly. A gross and safe design is made by applying twice the I_{GT} parameter, even if an approximative 1.6 factor runs in many cases. This can be fine-tuned by using $I_{GT} = f(T_j)$ datasheets curves. It comes that the power consumption is:

$$P_{gate} \approx 2 \cdot V_{dd} \cdot I_{GT},$$

showing that in addition to the power supply voltage level the choice of the Triac in terms of gate triggering current is key.

As enhancement this chapter will first cover tips for reducing the gate driver power consumption while keeping high I_{GT} with intrinsic high immunity level Triacs and/or remaining with relatively high auxiliary power supply voltage. Then, especially when lower gate triggering current (≤ 10 mA) must be kept, different ways for implementing EMI filters around the Triac will be described. Finally, a short part will be dedicated to cautious to take on the gate driver components themselves. This last part will also shortly discuss about the specific case of the photo-Triac.

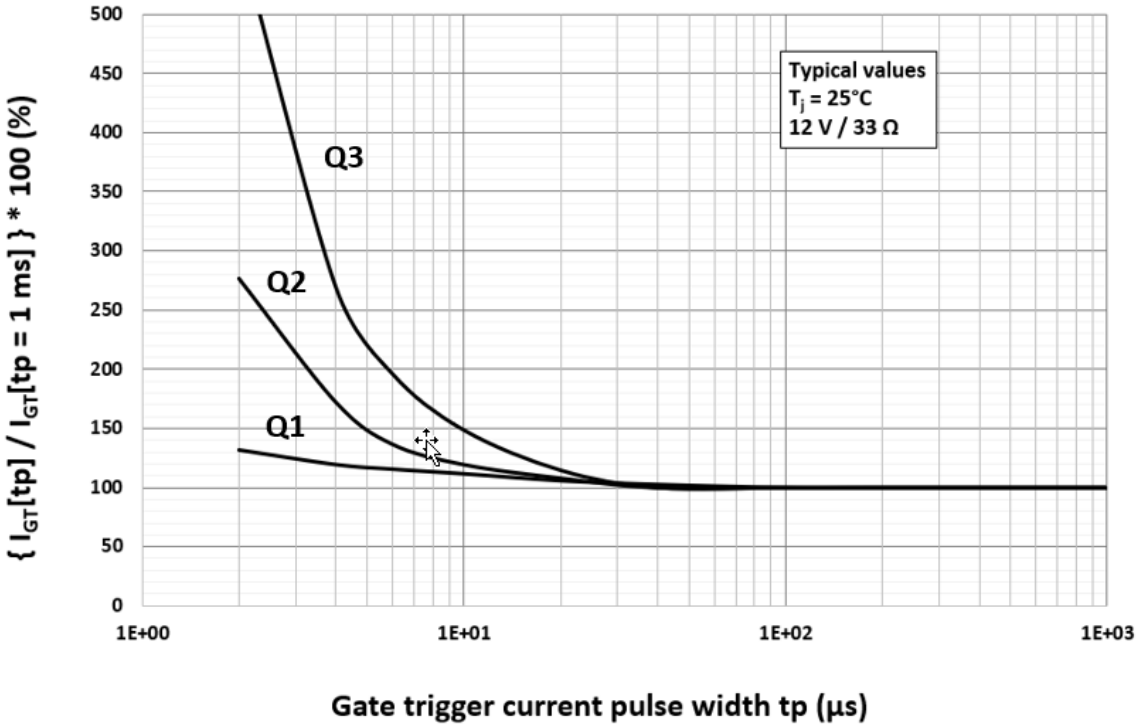
4.1 Pulsed gate current

Pulsing the gate current instead of applying a constant one will reduce the gate power consumption. There are two main ways for implementing such a pulsed gate signal. The first one consists of applying a constant PWM (pulse width modulation) signal, the second consists of applying a single gate current pulse at each AC mains semi-cycle. The second method for sure requires the controller to be equipped with a synchronization to the AC mains voltage zero crossing (ZVS).

PWM signal and ZVS have become easier to implement with the generalization of the micro-controllers using, which are offering more and more analog and digital features at reasonable cost.

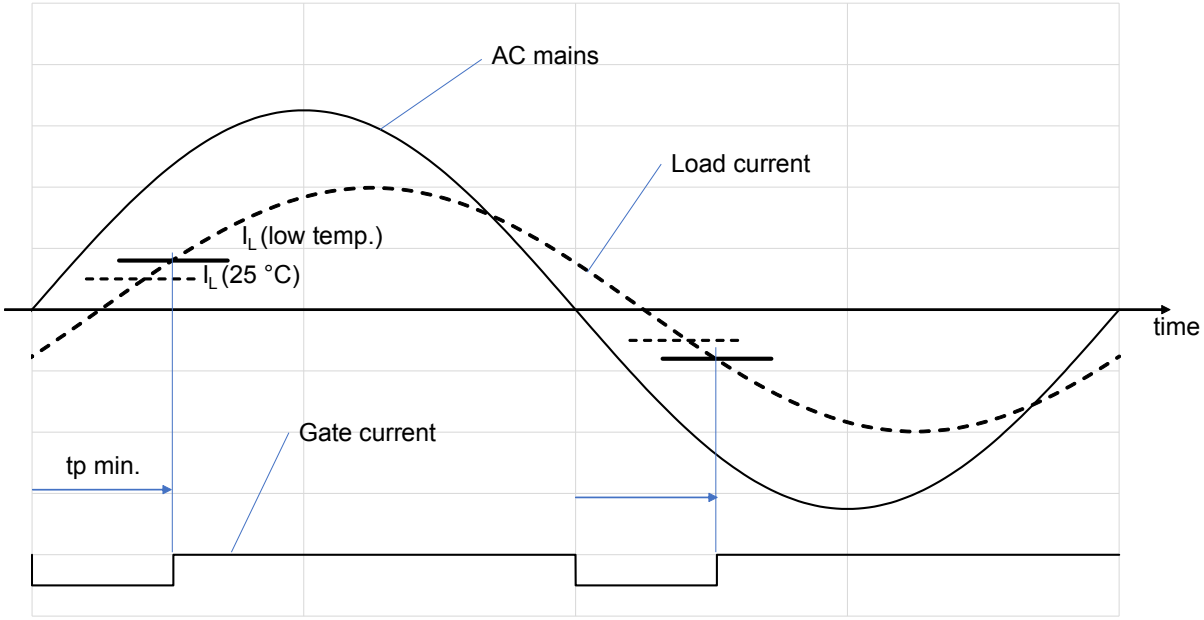
In standard gate triggering current characterization conditions, means 12 V supply and serial resistor of 32 Ω, a Triac typically triggers in less than 20 – 30 µs as illustrated in the Figure 9. Therefore, considering a PWM frequency of 10 kHz for instance, a duty cycle of 0.3 will comfortably ensure the triggering in any case, assuming the current level has been correctly set. In the meantime, the power consumption will then be reduced by 70 % which brings a significant gain.

Figure 9. **Typical required I_G depending on gate pulse signal duration and triggering quadrant**



In case a ZVS is available at the controller level, it is possible to reduce even more the gate pulse duration. This time, the pulse duration will depend on the current-voltage shift of the AC load which the Triac is controlling and the rate of the load current rising. Indeed, to make sure that the Triac remains triggered after the gate current has been cut, the current flowing from its A_2 to A_1 terminals must be higher than its proper latching current (I_L) parameter which is usually in the range of few tenth of mA. As I_L depends on the junction temperature with higher value at lower temperature, like for I_{GT}, designers will have to use the $I_L = f(T_j)$ datasheet curve for fine tuning the gate pulse duration. The Figure 10 illustrates such a setting with a high inductive low power load.

Figure 10. Minimum gate pulse duration (t_p) illustration for inductive low power load, accounting for latching current at low temperature



Implementing a ZVS allows also to avoid any Triac ignition at high AC mains voltage. Indeed, with high power resistive or capacitive kinds of loads, the anode current slope at triggering under high voltage is critical for the Triac due to internal current focalization at the ignition instant. This is referring to the dI/dt at turn-on absolute maximum rating specified in the datasheets which must not be exceeded.

To be noticed that ignition near the zero crossing reduces the interference emissions at switching on as well. This can help designers to comply with conducted noise standards.

Finally, both ZVS and PWM features can be combined to get an optimum gate control at low power consumption, while using a very high intrinsic immunity level Triac.

4.2 Snubber and gate filter

The AN437 application note from ST (“how to design snubber circuit for turn-off improvement”) describes how to dimension a snubber for aiding the turn-off commutation or limit the overvoltage at turn-off for the very inductive low rms current loads.

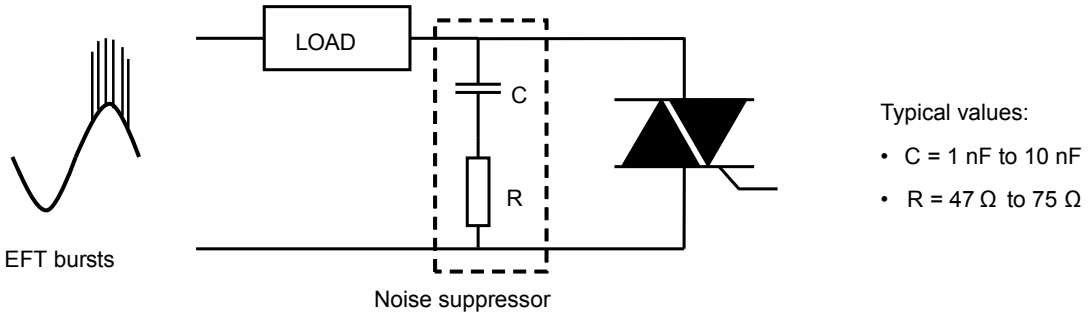
Implementing a snubber is usually recommended when using sensitive low I_{GT} Triacs in combination with highly inductive loads. Non sensitive Triacs (I_{GT}≥ 35 mA) are often called snubberless as their commutation capability is high, even with high reapplied voltage slope at switching off (generally up to 20 V/µs).

When a snubber is in place for commutation aiding, it automatically improves the Triac immunity.

It must be noticed that such a snubber is necessarily composed with a capacitor and a resistor. Indeed, in case of Triac triggering at high AC mains voltage on a resistive kind of load, a snubber with no resistor could dramatically increase the anode dI/dt at turn-on due to the capacitor discharge through the Triac with no current limitation.

In case of resistive kinds of loads, the reapplied voltage is low because the load current is in phase with the AC mains voltage. So, there is no need for snubber commutation aiding circuit, even if using sensitive Triacs, while nevertheless immunity enhancement may be required. In this case, a snubber can be added which will play here the role of noise suppressor. As shown on the Figure 11, based on the past cumulative ST experience, 1 to 10 nF for the capacitor and 47 to 75 Ω for the resistor values have experimentally proven their efficiency.

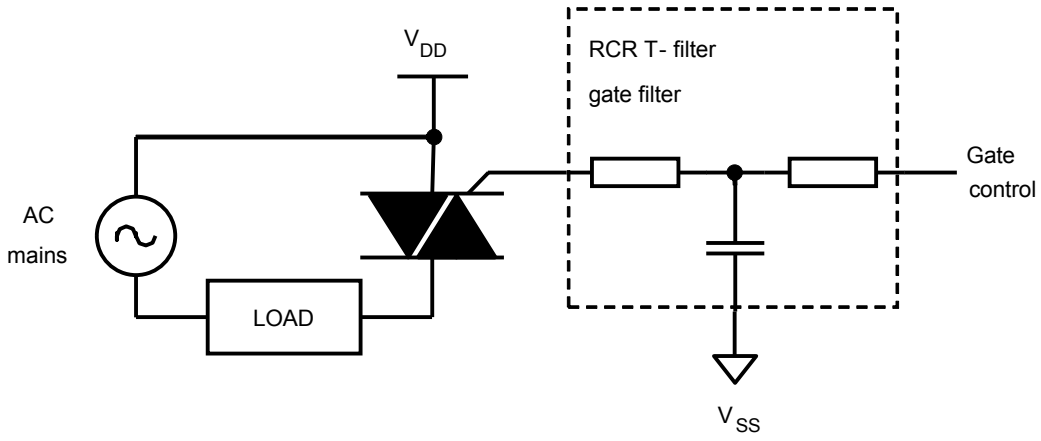
Figure 11. Typical components values for a high voltage snubber used as a noise suppressor



As the snubber circuit is connected across the Triac A_2 and A_1 terminals, the capacitor must sustain the AC mains voltage at Triac off-state leading to bulky high creepage capacitor. In addition, such a RC snubber remains active at OFF-state leading to unwanted power consumption in stand-by mode. Contrarily, a filter connected across the gate and A_1 terminal does not require to be high voltage as the internal gate to cathode electrical potentials cannot overpass 10-20 V typically. And such a voltage is supposed to occur rarely, only during surge stress for instance. Nominal gate to cathode voltage is around 1-2 V. As a consequence, in case the immunity level can be reached with a gate filter and with no high voltage snubber, optimized size and BOM (bill of material) is reached.

It is not recommended to implement a capacitor directly connected between gate and A_1 terminal, especially for long-term reliability when the device is submitted to repetitive or spurious high dI/dt at turn-on. The reader can refer to the ST AN4030 (“Gate to cathode capacitor, impact on Triac immunity and reliability”) for additional information. This is the reason why the gate resistor is splitted into two resistors with the capacitor placed in the middle forming a R-C-R T-filter as illustrated on the Figure 12.

Figure 12. Illustration of a gate RCR T-filter configuration



A value of 50 Ω between the capacitor and the Triac gate has demonstrated good immunity improvements with no robustness risk. The second resistor, placed between the gate driver and the filtering capacitor, will be calculated to deliver the right gate current level according to the auxiliary power supply voltage. The filtering components will have to be placed close to the Triac on the PCB (printed circuit board) layout.

4.3 Driver cautiousness

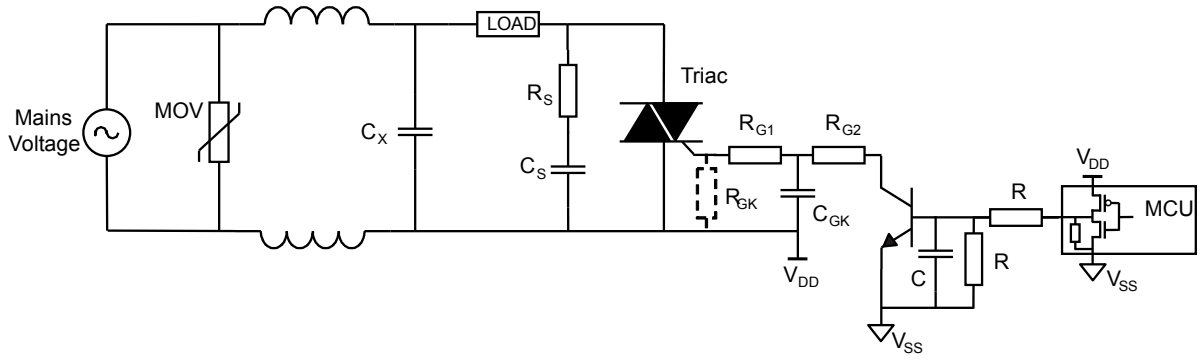
Independently of the Triac immunity, if its gate driver is spuriously activated due to EFT bursts, the Triac will trigger. This is the reason why it is necessary to care about the driver immunity as well to reach a perfect overall level.

In case of sensitive Triacs the gate can be directly connected to a microcontroller.

In any case the microcontroller needs to prevent from unwanted latching.

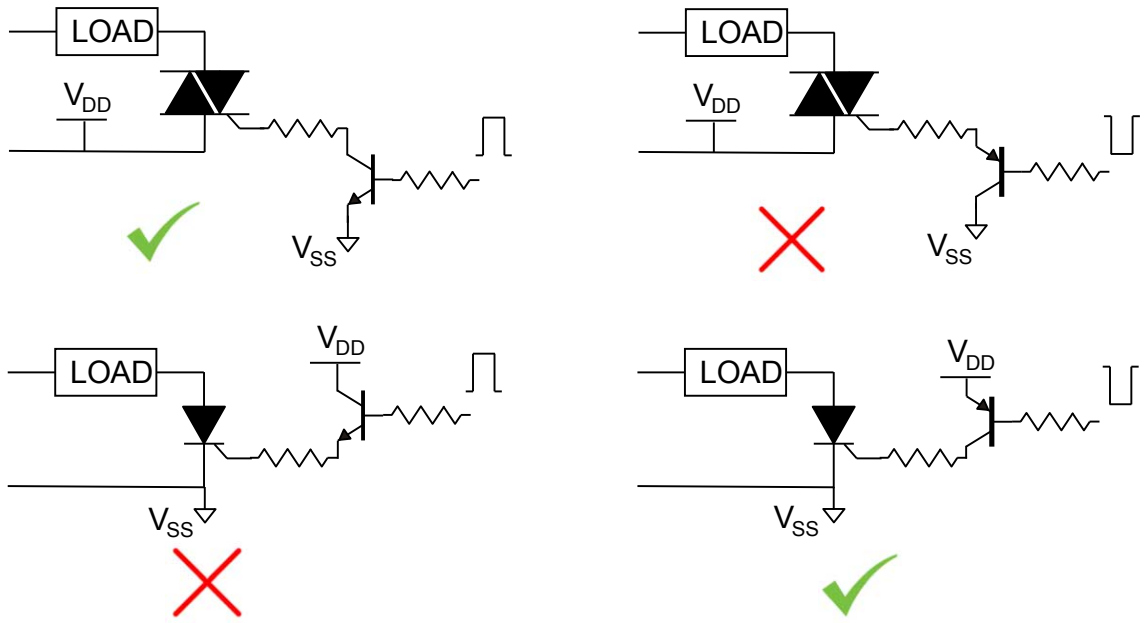
For non-sensitive Triacs, a buffer made of a simple low voltage bipolar transistor, is commonly placed between the digital signal and the gate supply as shown on the Figure 13.

Figure 13. Common way to drive a Triac with a microcontroller and an intermediate buffer



In this case, in addition to preventing from microcontroller latching, it is necessary to avoid the activation of the bjt by noises through its proper base terminal. For that, in addition to parameter the microcontroller GPIOs with push-down resistor (or push-pull depending on the circuit), the amplifying transistor emitter-base is usually equipped with a RC filter. It is also recommended, as a generic cautious method, to connect the emitter terminal to the as stable potential as possible. For instance, using a NPN bipolar transistor with its emitter connected to V_{SS} is better than using a PNP which would have its emitter potential floating between the V_{DD} and V_{SS} ones. Referring to the illustration on the Figure 14, the inverse situation applies to the SCR gate control.

Figure 14. Better choice for bipolar transistor type according to the requested gate control and for avoiding emitter floating potentials



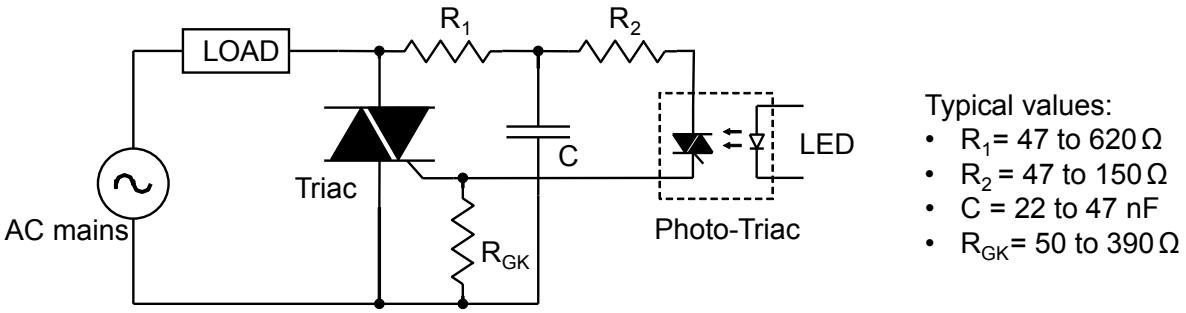
A very simple Triac driver is the photo-Triac. Indeed, it offers the insulation; and the power for the gate current is delivered by the AC mains without any need for auxiliary power supply. It can offer an embedded automatic zero voltage crossing synchronization. Those reasons make this method attractive.

However, for igniting a photo-Triac through its embedded LED, its internal structure cannot be vertical (from bottom to the top silicon sides) but requires to be lateral. This is the reason why its voltage drop at ON-state is relatively high and it cannot be used as a power Triac. The triggering through photons instead of direct gate current also explains why the structure requires to be sensitive.

It must be noticed that a photo-Triac is not supposed to heat as it delivers only the power Triac gate current during a limited pulse duration. This is the reason why most of the photo-Triac dV/dt specifications are given at 25 °C of junction temperature. This makes confusing the comparison with the immunity of a paired power Triac whose dV/dt is specified at maximum junction temperature, while the overall immunity to EFT bursts can apply when both devices are at OFF-state with same junction (equals to ambient) temperature.

Consequently, for driving a power load, a combination of a sensitive photo-Triac and a power Triac is needed. And as the photo-Triac is connected to the power Triac gate terminal, it becomes easy to understand that the overall immunity depends first on the photo-Triac one.

Figure 15. Typical circuit for high immunity configuration with photo-Triac driver



A usual way to improve such an assembly immunity is to build a high voltage snubber connected across both devices. A low voltage filtering is not possible as the photo-Triac is connected to the line through the load and the internal gate access is not possible by construction. A limiting gate resistor in series with the photo-Triac is required to limit the current inside it in case of triggering at peak mains AC voltage. The power-Triac ignition instant will depend on the gate resistance and its proper I_{GT}. Therefore, there is a voltage drop across the switch at each AC mains semi-cycle zero voltage crossing which results from the immunity requirement. But such repetitive voltage spikes are a source of noises emission. As a result, implementing a robust photo-Triac circuit in addition to complying to emission standards is not so obvious. Reader can refer to the ST application note AN5114 (“controlling a Triac with phototriac”) for deeper details. It is to be noticed that the requirement for a high voltage snubber increases the leakage at OFF-state, which can make harder to comply with the required stand-by power consumption limits at system level. Especially when several Triacs with their proper photo-Triac are embedded.

5 Experimental measurements

As shown on the Table 1, experimental tests were performed on the ST T-series, H-series and 8H-Triacs series Triacs with using the method described in the Section 2 EFT bursts immunity evaluation of a single Triac. Thanks to their optimized design, the low sensitivity part numbers (I_{GT} = 35 mA) performance exceeded 6 kV with no need for implementing any external filtering components. The performance of the higher sensitivity ones (I_{GT} = 10 mA) is similar (around 3.3 kV) with using a high voltage snubber or with using a low voltage R-C-R T-filter. This is due to the optimized internal silicon design, especially the equilibrium between the top and bottom sides in terms of sensitivity to direct and reverse dV/dt, making the gate filter particularly efficient. Finally, the same performance with 10 mA T-series compared to 35 mA ones can be achieved with combining a high voltage snubber with a low voltage gate filter.

Table 1. ST T-series, H-series and 8H-Triacs series Triacs immunity to EFT bursts at 5 kHz with effect of snubber and T-filter on the sensitive versions (I_{GT} = 10 mA)

Series	P/N	I_{GT} (mA)	Packages	Snubber		R-C-R gate T-filter			EFT burst level (kV)
				$R_{(SNUBBER)}$ (Ω)	$C_{(SNUBBER)}$ (nF)	R_G (Ω)	C_{GK} (nF)	R_{GK} (Ω)	
T-series H-series 8H-Triacs	Txx35T-8x Txx35H-6x Txx35H-8x	35	TO-220FP TO-220 Ins. TO-220 D²PAK	-	-	-			> 6.0
T-series	Txx10T-8x	10		-	-	-	-	-	1.0
				47	1	-	-	-	1.8
				-	-	50	1	50	3.3
				47	1	50	1	50	> 6.0

It must be noticed that those tests were done without any EMI input filter which may be present in a final application. Implementing a simple X-cap. across L-N at the appliance input enhances the Triac immunity and can be necessary for preventing other devices like ICs (integrated circuits) from latching. In this case a 3 kV of immunity at the Triac alone level will probably already be sufficient for the global system immunity.

6 Conclusion

This document has described a method for comparing different Triac references each other and, after a short internal structure behavior explanation, provided some tips for optimizing a Triac based circuit immunity to EFT bursts, while using a low consumption auxiliary gate power supply.

It was shown that the ST 35 mA of I_{GT} T-series, H-series and 8H-Triacs series intrinsic immunity is very high; and the sensitive 10 mA three quadrants T-series can reach a high level using only simple low voltage R-C-R T-filter on the gate.

Finally, it must be noticed that applying such described methods for enhancing the immunity to EFT bursts prevents from most of the possible external sources. However, when spurious ignitions still occur in an application due to fast transients while the circuit immunity design has properly been done, it is by experience often due to internal load or cabling faults. So, the quality and reliability of those devices are for sure parts of the overall robustness.

Related application notes:

- AN437: How to design snubber circuit for turn-off improvement
- AN4030: Gate to cathode capacitor, impact on Triac immunity and reliability
- AN5114: Controlling a Triac with a phototriac
- AN4993: How to implement an SCR or a Triac in hybrid relay applications
- AN3168: Non-insulated SCR / Triac control circuits
- AN4564: Is a positive power supply mandatory for my application, or could a negative output work also?
- AN436: Triac control by pulse transformer

Revision history

Table 2. **Document revision history**

Date	Revision	Changes
15-Jun-2021	1	Initial release.

Contents