QorIQ Communications Platforms

T Series—QorIQ T2080 and T2081 communication processors

The 28 nm QorIQ T2080 and T2081 communications processors bring the architectural innovations of the T series flagship T4240, such as the 1.8 GHz dual-threaded e6500 core, into an eight virtual core mid-range platform at reduced power and price points.

OVERVIEW

The T2080 processor is primarily intended to succeed our successful P3041 and P2041 mid-range series of quad-core devices as a control plane or integrated control and data plane processor. It provides an excellent migration path, as it offers 2x or better in core capability, cache size, SerDes bandwidth and Ethernet connectivity within a similar power budget. It also provides a value engineering opportunity for P4080 customers, as T2080 provides equivalent performance at much lower price and power.

The T2081 is a smaller package version of the T2080, which is pin compatible with the quad-core T1042. This provides T1042 customers an easy upgrade to higher performance if processing requirements increase. It also enables customers to reuse a single board for two different product performance levels.

TARGET MARKETS AND APPLICATIONS

The T2080 and T2081 processors are targeted at mid-range control plane applications or mixed control and data plane applications. The highly efficient eight virtual core device achieves up to 1.8 GHz even while maintaining a short seven-stage pipeline for better latency response to unpredictable control plane code branches. Advanced virtualization technology facilitates safe partitioning of control and data plane applications within the device.

- **Enterprise equipment:** Modular Ethernet switches, services cards, UTM equipment, enterprise storage, data center
- **Service provider:** Core and edge routers, broadband access, metro Ethernet, optical networking
- **Wireless infrastructure:** Mobile backhaul, NICs, channel cards, control cards in LTE, WCDMA, GSM, WiMAX
- **Aerospace and defense:** ruggedized or highly secure routers, avionics networking, instrumentation panels, military SBCs
- **Industrial computing:** SBCs, factory automation, test and measurement

E6500 CORE

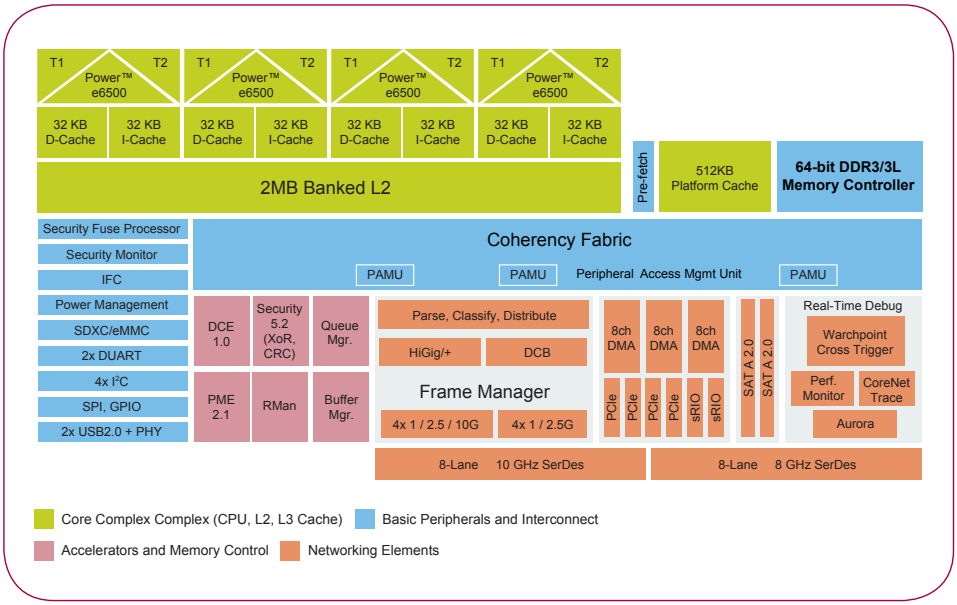
The T2080 and T2081 processors are based on the 64-bit e6500 core, built on Power Architecture® technology, and run up to 1.8 GHz. The e6500 core also offers higher aggregate instructions per clock at lower power with an innovative "fused core" approach to threading. The e6500's fully resourced dual threads provide 1.7 times the performance of a single thread.

The four e6500 dual-threaded cores share a low-latency backside 2 MB L2 cache, allowing efficient sharing of code and data. Each e6500 core implements the NXP AltiVec technology-based SIMD engine, dramatically boosting the performance of media and networking algorithms, offering native inline programming and using less power than a separate DSP.

VIRTUALIZATION

TThe T2080 and T2081 processors include support for hardware-assisted virtualization. The e6500 core offers an extra core privilege level (hypervisor) and hardware offload of logical to real address translation. In addition, the T2080 and T2081 include platform-level enhancements such as SR-IOV and I/O virtualization with DMA memory protection through IOMMUs and configurable "storage profiles," which provide isolation of I/O buffers between guest environments. Virtualization software for the T2080 and T2081 processors includes kernel virtualization model (KVM), Linux® containers and the NXP hypervisor.

QorIQ T2080 COMMUNICATIONS PROCESSOR



T2080 VS. T2081 DIFFERENCES

	T2080	T2081
SerDes	16	8
PCIe	2x Gen3 + 2x Gen2	1x Gen3 + 3x Gen2
SRIO	2 + RMan	No
SATA	2	No
Aurora	Yes	No
10 Gb/s MACs	Up to four, with XFI, XAUI, HiGig	Up to 2x XFI
1 Gb/s MACs	Up to eight	Up to seven
Package	25 x 25mm, 896 pins, 0.8 mm pitch	23 x 23mm, 780 pins, 0.8 mm pitch, pin compatible with T1042

DATA PATH ACCELERATION ARCHITECTURE (DPAA)

The T2080 and T2081 processors integrate the QorIQ DPAA, an innovative multicore infrastructure for scheduling work to cores (physical and virtual), hardware accelerators and network interfaces. The FMAN, a primary element of the DPAA, parses headers from incoming packets and classifies and selects data buffers with optional policing and congestion management. The FMAN passes its work to the QMAN, which assigns it to cores or accelerators with a multi-level scheduling hierarchy, while maintaining packet ordering. The BMAN manages allocation and de-allocation of packet buffers. The T2080 and T2081's implementation of DPAA offers accelerators for cryptography, deep packet inspection and compression decompression.