# T2G6000528-Q3

## 10 W, 28 V, DC – 6 GHz, GaN RF Power Transistor

## Product Overview

The Qorvo T2G6000528-Q3 is a 10W ($P_{3dB}$) discrete GaN on SiC HEMT which operates from DC to 6 GHz. The device features advanced field plate techniques to optimize power and efficiency at high drain bias operating conditions. This optimization can potentially lower system costs in terms of fewer amplifier line-ups and lower thermal management costs.

Lead-free and ROHS compliant

Evaluation boards are available upon request.

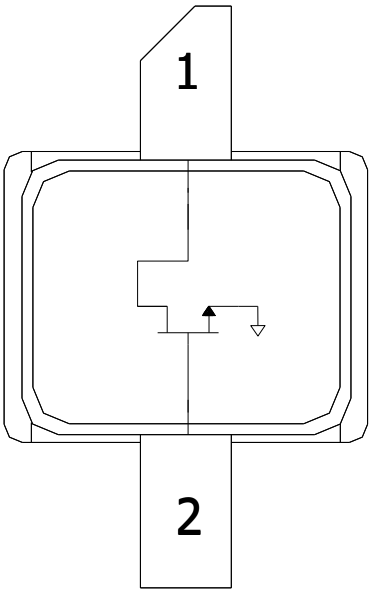

## Key Features

- Frequency: DC to 6 GHz
- Output Power ($P_{3dB}$)[1]: 9.5 W
- Linear Gain[1]: 18 dB
- Typical $DE_{3dB}$[1]: 70%
- Operating Voltage: 28 V
- Low thermal resistance package
- Pulse capable

Notes:

1. @ 3.0 GHz

## Functional Block Diagram




## Applications

- Military Radar
- Civilian Radar
- Professional and military radio communications
- Test Instrumentation
- Wideband or narrowband amplifiers
- Jammers

## Ordering Information

| Part Number | Description |
|---|---|
| 1099997 | T2G6000528-Q3, Qty. 100 |
| 1099999 | T2G6000528-Q3 3.0 – 3.5 GHz EVB |
| 1125393 | T2G6000528-Q3 1.9 – 3.2 GHz EVB |
| 1139251 | T2G6000528-Q3 5.0 – 6.0 GHz EVB |
| T2G6000528Q3EVB03 | T2G6000528-Q3 3.5 – 4.3 GHz EVB |

## Absolute Maximum Ratings[1]

| Parameter | Rating | Units |
|---|---|---|
| Breakdown Voltage ($BV_{DG}$) | +100 | V |
| Gate Voltage ($V_G$) | -7 to +2 | V |
| Drain Current ($I_D$) | 2.5 | A |
| Gate Current Range ($I_G$) | See page 4 | mA |
| Power Dissipation ($P_D$)[2] | 15 | W |
| RF Input Power ($RF_{IN}$)[3] | 34 | dBm |
| Mounting Temperature (30 seconds) | 320 | °C |
| Storage Temperature | -65 to +150 | °C |

Notes:
1. Operation of this device outside the parameter ranges given above may cause permanent damage.
2. Pulsed CW: Pulse Width = 500 µs, Duty Cycle = 20%
3. Signal Type: CW, T = 25 °C

## Recommended Operating Conditions[1]

| Parameter | Min | TYP | Max | Units |
|---|---|---|---|---|
| Operating Temperature | -40 | +25 | +85 | °C |
| Drain Voltage ($V_D$) | +12 | +28 | +40 | V |
| Drain Bias Current ($I_{DQ}$) | - | 50 | - | mA |
| Drain Current ($I_D$) | - | 650 | - | mA |
| Gate Voltage ($V_G$)[4] | - | -2.7 | - | V |
| Power Dissipation ($P_D$)[2] | - | - | 11 | W |
| Power Dissipation ($P_D$)[3] | - | - | 12.5 | W |

Notes:
1. Electrical performance is measured under conditions noted in the electrical specifications table. Specifications are not guaranteed over all recommended operating conditions.
2. Signal Type: CW, Package base at 85°C
3. Pulsed CW: Pulse Width = 100 µs, Duty Cycle = 20% Package base at 85°C
4. To be adjusted to desired $I_{DQ}$

## Pulsed Characterization – Load Pull Performance – Power Tuned[1]

| Parameters | Typical Values | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| Frequency | 1.0 | 2.0 | 3.0 | 4.0 | 5.0 | 6.0 | GHz |
| Linear Gain ($G_{LIN}$) | 18.1 | 20.8 | 18.1 | 16.6 | 14.8 | 14.5 | dB |
| Output Power at 3dB Compression ($P_{3dB}$) | 7.6 | 9.1 | 9.5 | 10 | 11 | 10 | W |
| Drain Efficiency at 3dB Compression ($DE_{3dB}$) | 54.3 | 61.5 | 53.7 | 60.0 | 60.6 | 58.8 | % |
| Gain at 3dB Compression ($G_{3dB}$) | 15.1 | 17.8 | 15.1 | 13.6 | 11.8 | 11.5 | dB |

Notes:
1. Test conditions unless otherwise noted: $V_D$ = +28 V, $I_{DQ}$ = 50 mA, $T_A$ = +25 °C

## Pulsed Characterization – Load Pull Performance – Efficiency Tuned[1]

| Parameters | Typical Values | | | | | | Unit |
|---|---|---|---|---|---|---|---|
| Frequency | 1.0 | 2.0 | 3.0 | 4.0 | 5.0 | 6.0 | GHz |
| Linear Gain ($G_{LIN}$) | 22.3 | 21.2 | 18.7 | 17.3 | 15.3 | 15.2 | dB |
| Output Power at 3dB Compression ($P_{3dB}$) | 5.4 | 7.8 | 5.9 | 7.8 | 7.8 | 6.6 | W |
| Drain Efficiency at 3dB Compression ($DE_{3dB}$) | 81.9 | 72.2 | 69.6 | 66.1 | 70.7 | 66.8 | % |
| Gain at 3dB Compression ($G_{3dB}$) | 19.3 | 18.2 | 15.7 | 14.3 | 12.3 | 12.2 | dB |

Notes:
1. Test conditions unless otherwise noted: $V_D$ = +28 V, $I_{DQ}$ = 50 mA, $T_A$ = +25 °C

## RF Characterization – 3.0 – 3.5 GHz EVB Performance at 3.3 GHz[1]

| Parameters | Min | Typical | Max | Units |
|---|---|---|---|---|
| Linear Gain ($G_{LIN}$) | 15.5 | 17.4 | - | dB |
| Output Power at 3dB Compression ($P_{3dB}$) | 8.9 | 9.7 | - | W |
| Power-Added-Efficiency at 3dB Compression ($DE_{3dB}$) | 50 | 53.0 | - | % |
| Gain at 3dB Compression ($G_{3dB}$) | 12.5 | 14.4 | - | dB |
| Gate Leakage ($I_{G-Leak}$)[2] | -0.1 | - | -2.75 | mA |

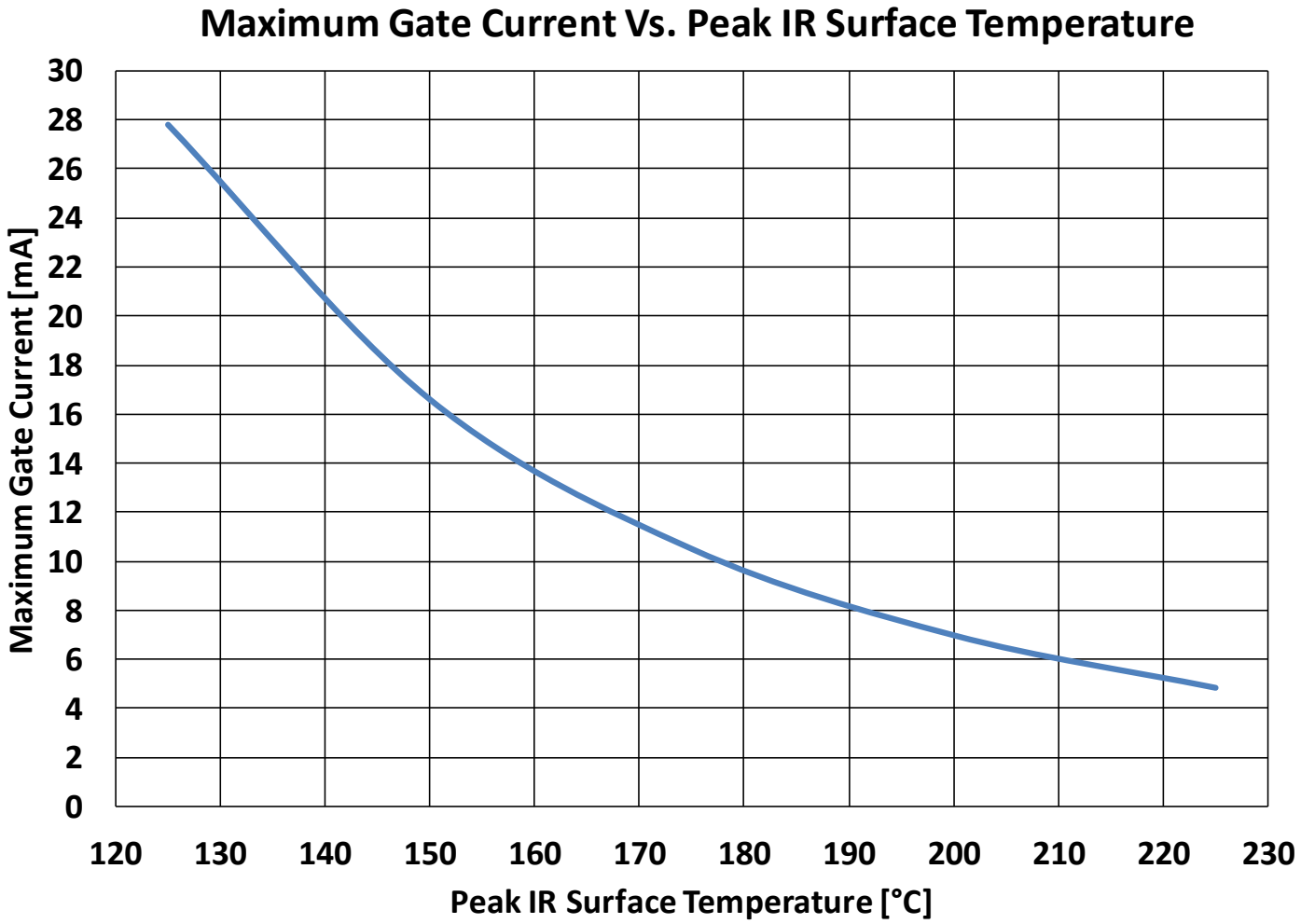
Notes:
1. Test conditions unless otherwise noted: $V_D$ = +28 V, $I_{DQ}$ = 50 mA, $T_A$ = +25 °C, Pulsed Width = 100 µs, Duty Cycle = 20%
2. $V_D$ = 10 V, $V_G$ = -3.7 V, Signal Type: DC

## RF Characterization – Mismatch Ruggedness at 3.5 GHz[1]

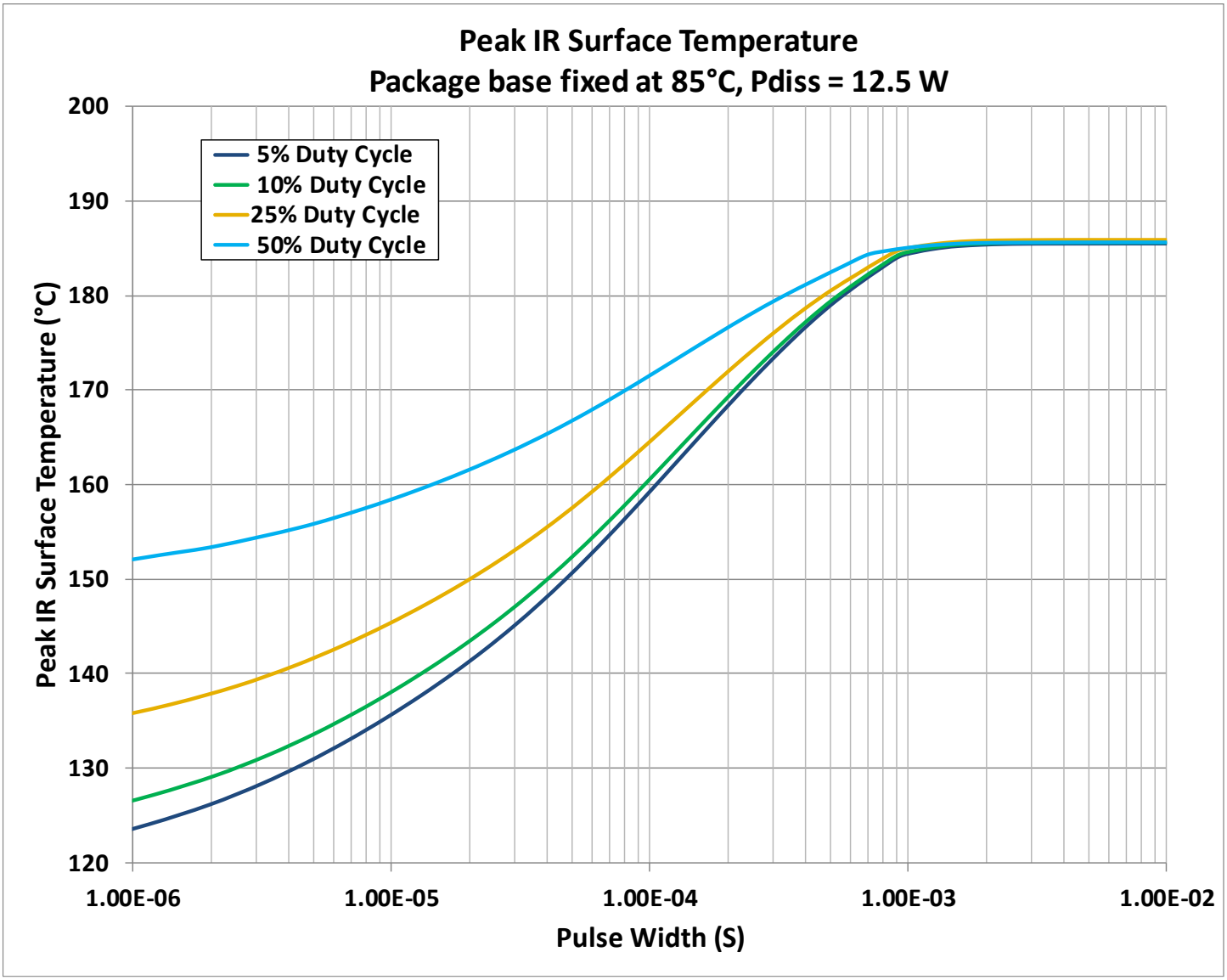
| Symbol | Parameter | dB Compression | Typical |
|---|---|---|---|
| VSWR | Impedance Mismatch Ruggedness | 3 | 10:1 |

Notes:
1. Test conditions unless otherwise noted: $V_D$ = +28 V, $I_{DQ}$ = 50 mA, $T_A$ = +25 °C, Pulse Width = 100 µs, Duty Cycle = 20%
2. Driving input power is determined at pulsed compression under matched condition at EVB output connector.

## Maximum Gate Current



## Thermal and Reliability Information – Pulsed

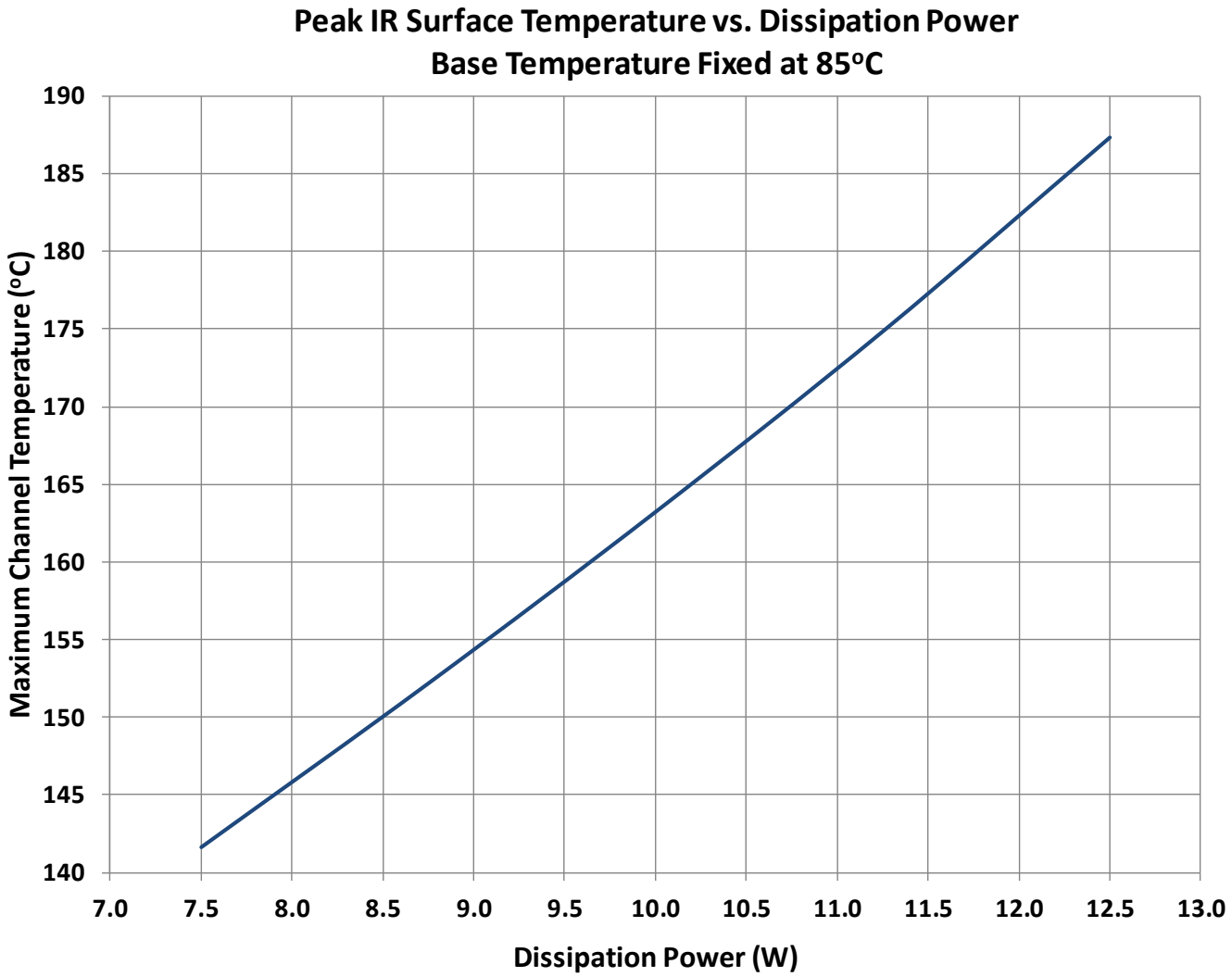



| Parameter | Conditions | Values | Units |
|---|---|---|---|
| Thermal Resistance, IR[1] ($\theta_{JC}$) | 85 °C back side temperature<br>12.5 W $P_D$, Pulse Width = 100 µs, Duty Cycle = 5% | 5.9 | °C/W |
| Peak IR Surface Temperature[1] ($T_{CH}$) | | 159 | °C |
| Thermal Resistance, IR[1] ($\theta_{JC}$) | 85 °C back side temperature<br>12.5 W $P_D$, Pulse Width = 100 µs, Duty Cycle = 10% | 6.1 | °C/W |
| Peak IR Surface Temperature[1] ($T_{CH}$) | | 161 | °C |
| Thermal Resistance, IR[1] ($\theta_{JC}$) | 85 °C back side temperature<br>12.5 W $P_D$, Pulse Width = 100 µs, Duty Cycle = 25% | 6.3 | °C/W |
| Peak IR Surface Temperature[1] ($T_{CH}$) | | 164 | °C |
| Thermal Resistance, IR[1] ($\theta_{JC}$) | 85 °C back side temperature<br>12.5 W $P_D$, Pulse Width = 100 µs, Duty Cycle = 50% | 7.0 | °C/W |
| Peak IR Surface Temperature[1] ($T_{CH}$) | | 172 | °C |

Notes:

1. Refer to the following document GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

## Thermal and Reliability Information – Pulsed




| Parameter | Conditions | Values | Units |
|---|---|---|---|
| Thermal Resistance, IR[1] ($\theta_{JC}$) | 85 °C back side temperature 7.5 W $P_D$ | 7.6 | °C/W |
| Peak IR Surface Temperature[1] ($T_{CH}$) | | 142 | °C |
| Thermal Resistance, IR[1] ($\theta_{JC}$) | 85 °C back side temperature 8.75 W $P_D$ | 7.7 | °C/W |
| Peak IR Surface Temperature[1] ($T_{CH}$) | | 152 | °C |
| Thermal Resistance, IR[1] ($\theta_{JC}$) | 85 °C back side temperature 10.0 W $P_D$ | 7.8 | °C/W |
| Peak IR Surface Temperature[1] ($T_{CH}$) | | 163 | °C |
| Thermal Resistance, IR[1] ($\theta_{JC}$) | 85 °C back side temperature 11.25 W $P_D$ | 8.0 | °C/W |
| Peak IR Surface Temperature[1] ($T_{CH}$) | | 175 | °C |
| Thermal Resistance, IR[1] ($\theta_{JC}$) | 85 °C back side temperature 12.5 W $P_D$ | 8.2 | °C/W |
| Peak IR Surface Temperature[1] ($T_{CH}$) | | 187 | °C |

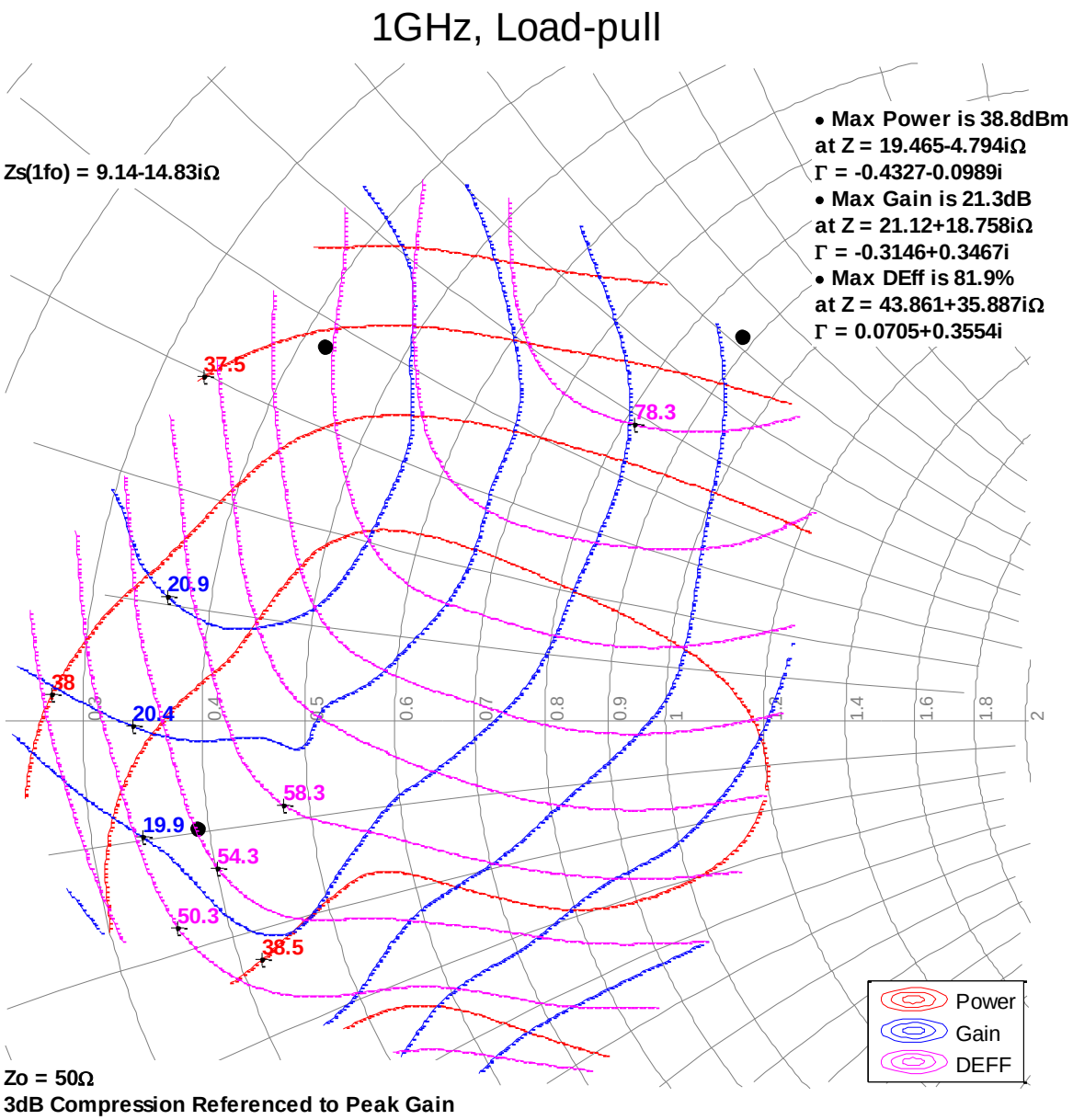
Notes:

1. Refer to the following document GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

## Load Pull Contours[1, 2]

Notes:

1. $V_D$ = 28 V, $I_{DQ}$ = 50 mA, Pulse Width = 100 µs. Duty Cycle = 20%. Performance is at 3dB gain compression referenced to peak gain.
2. See page 20 for load-pull and source-pull reference planes. 50 Ω load-pull TRL fixtures are built with 20 mils RO4350B material.



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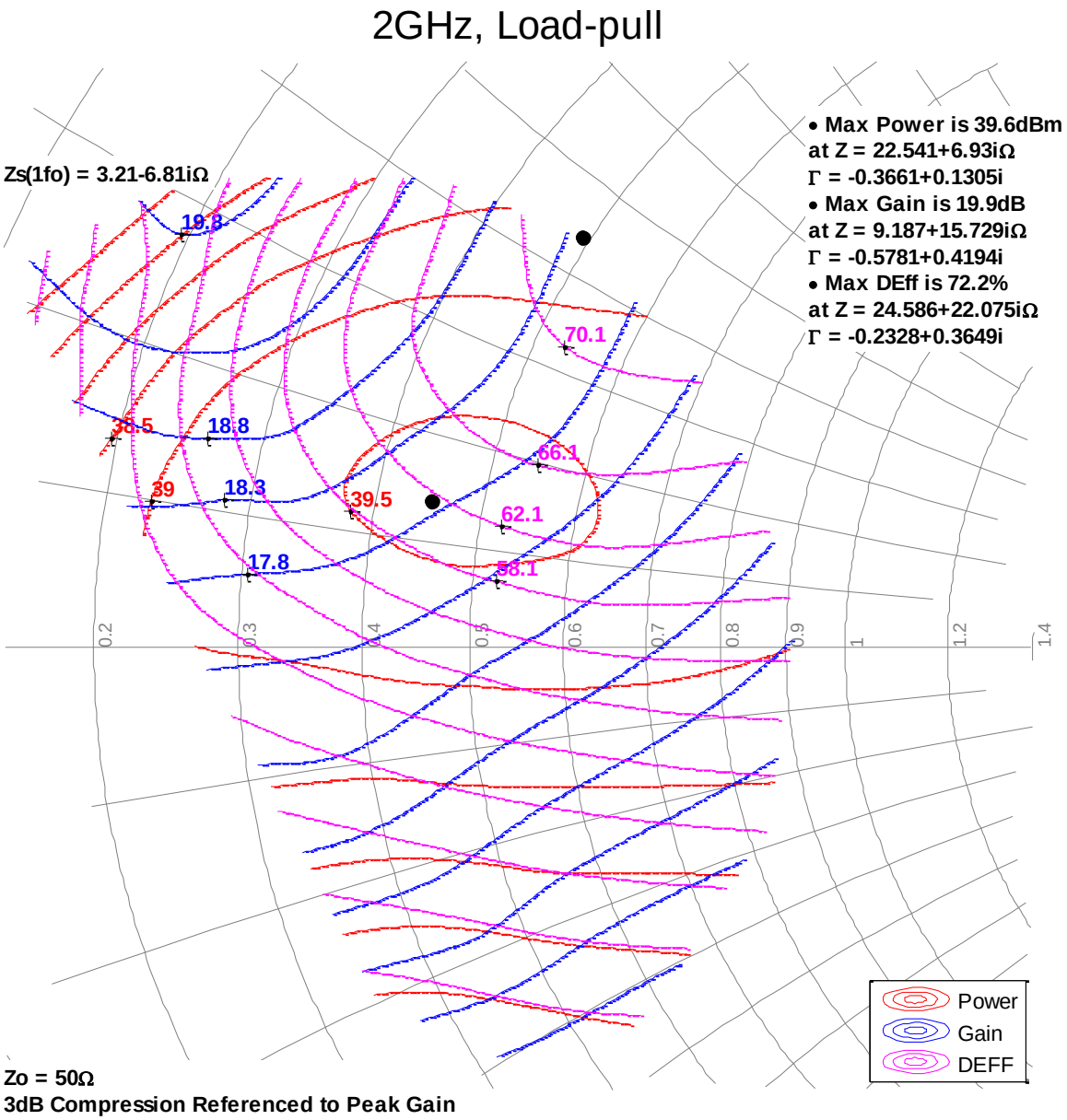

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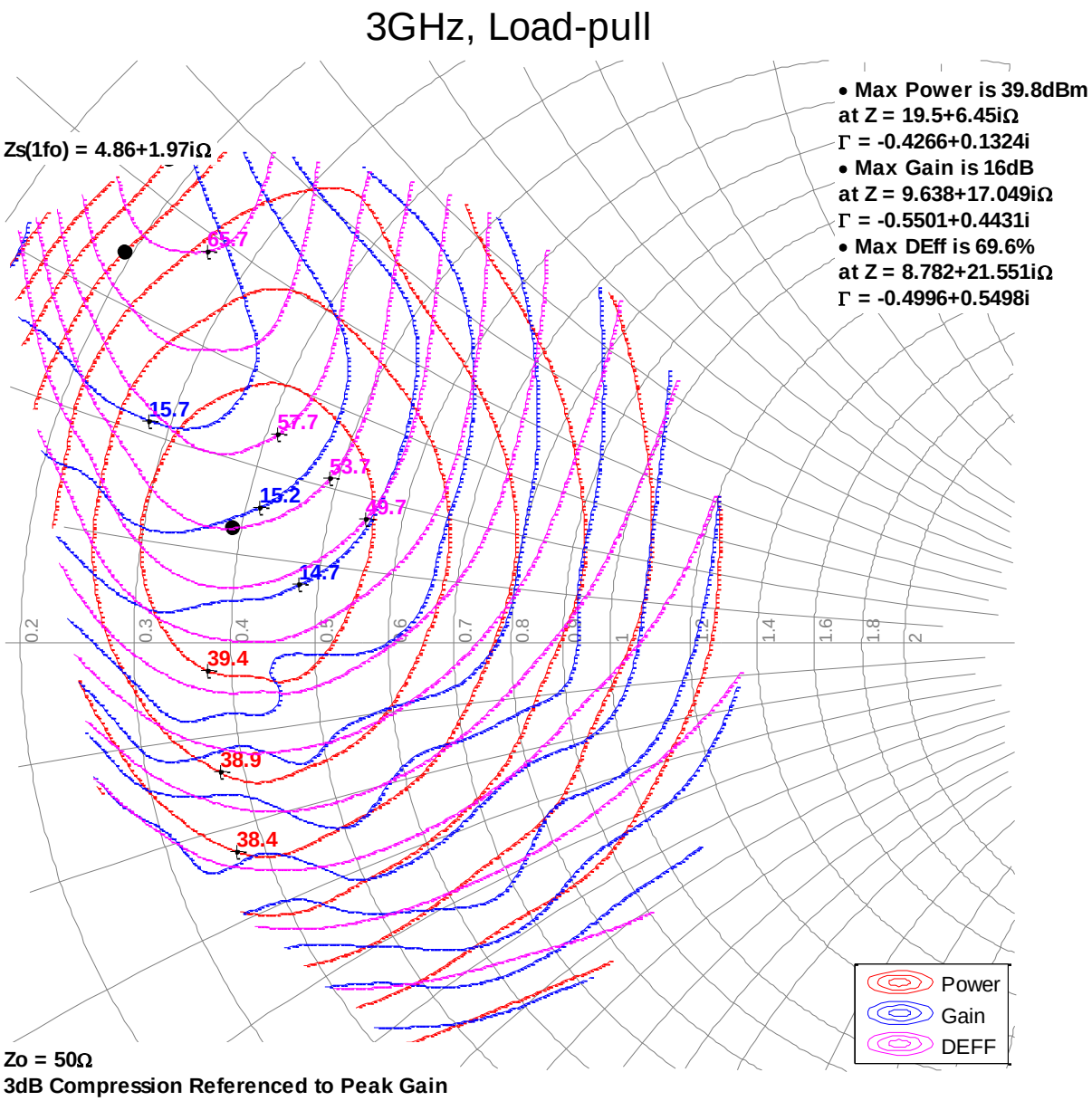

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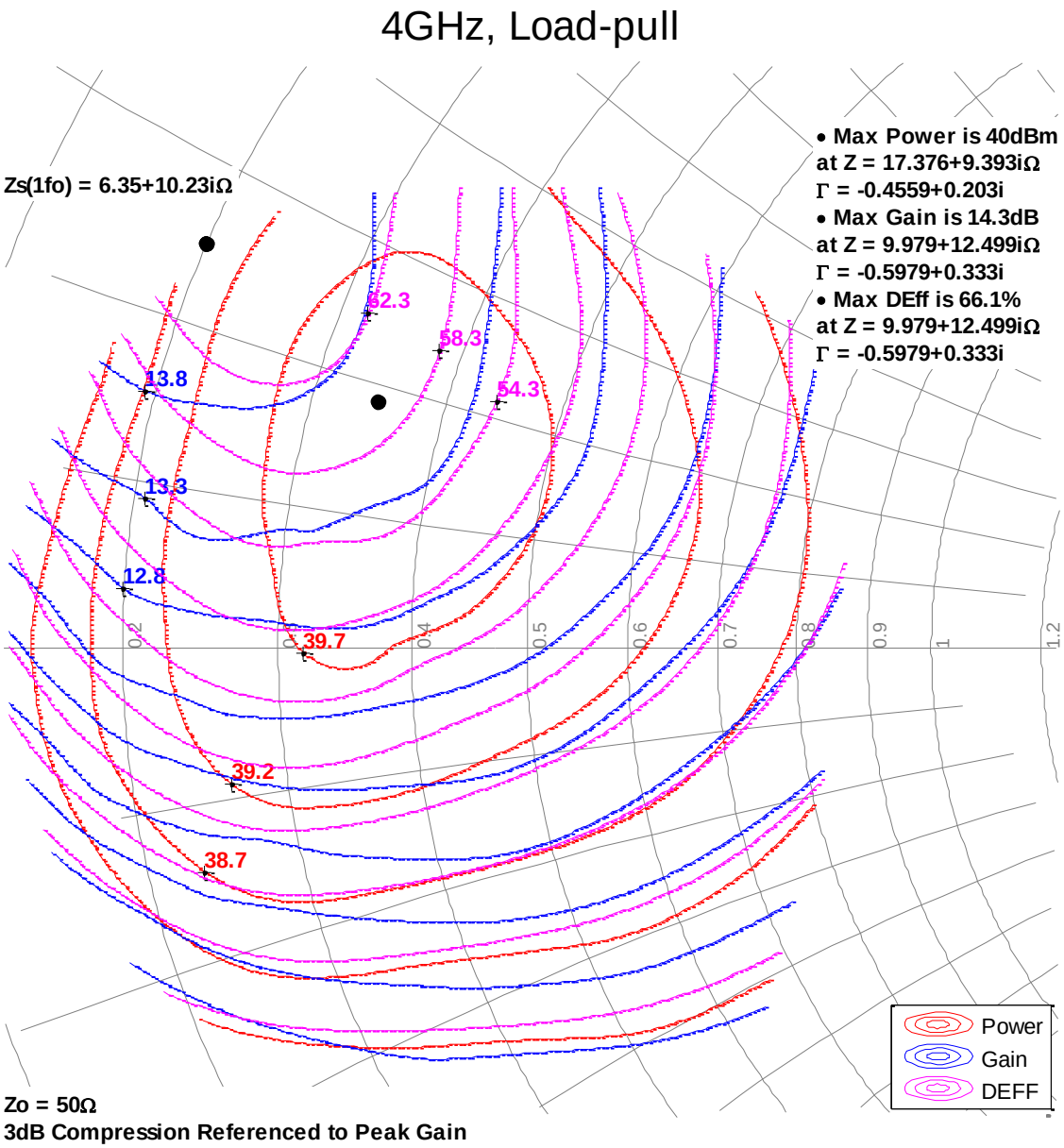

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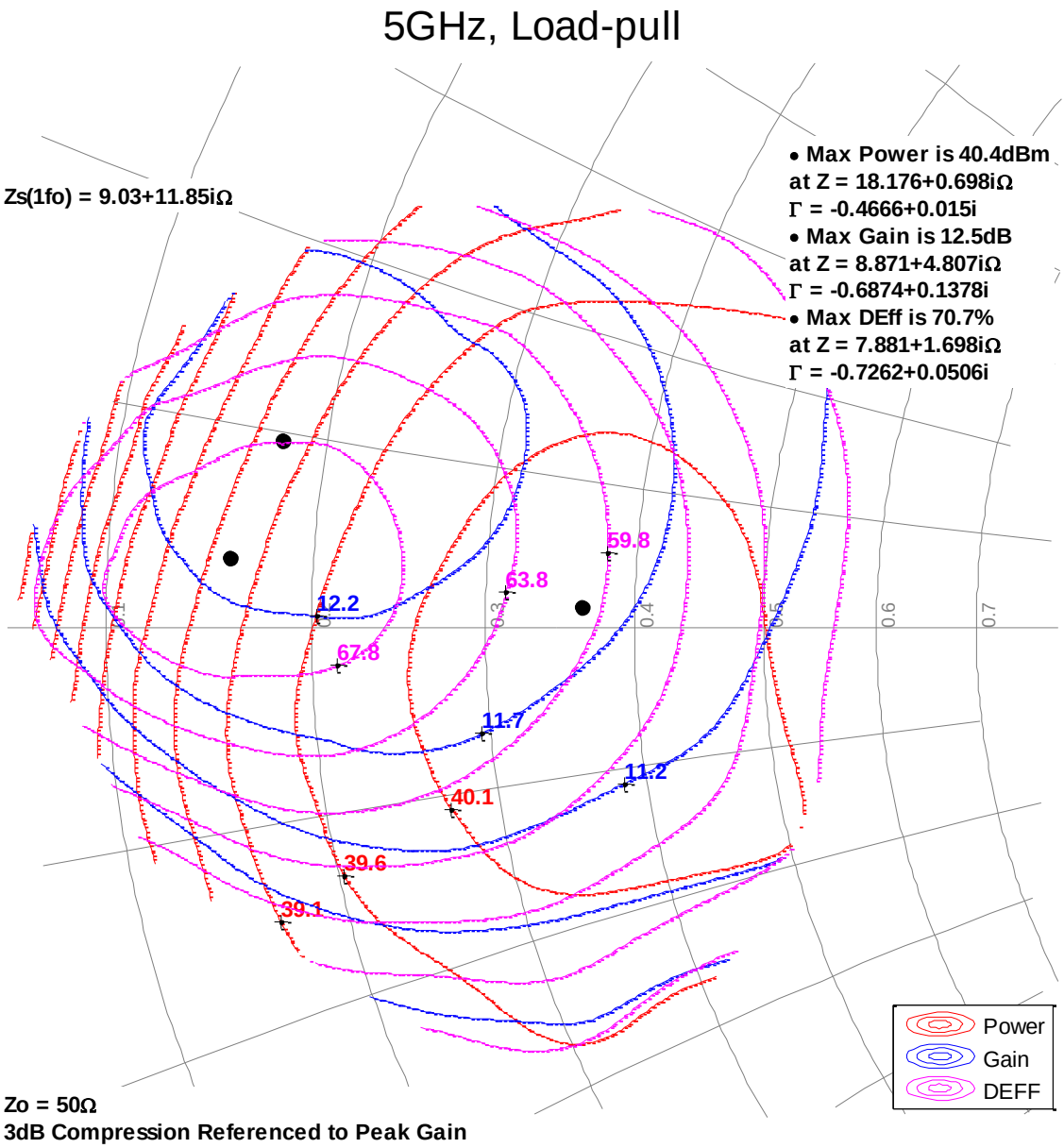

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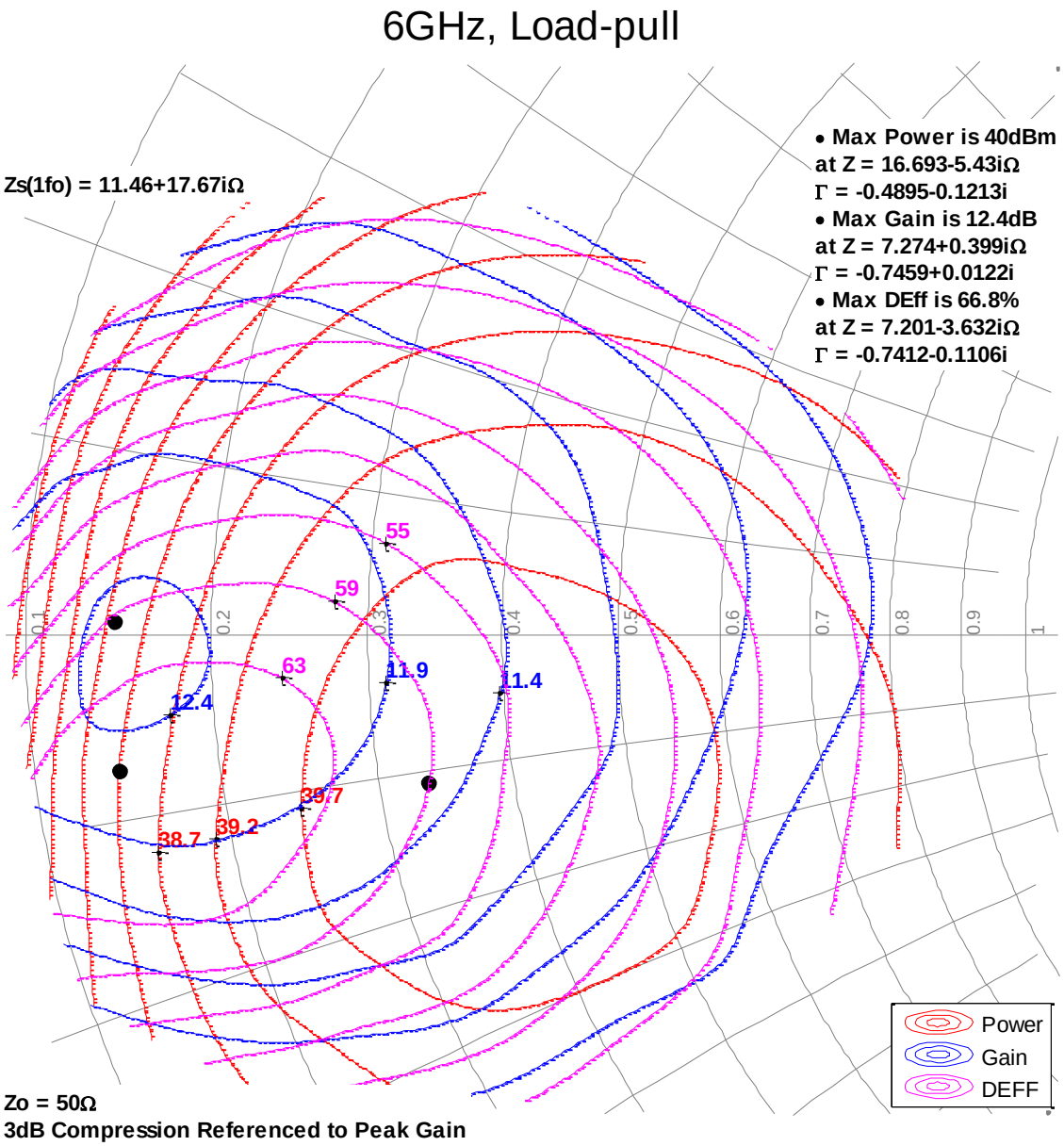
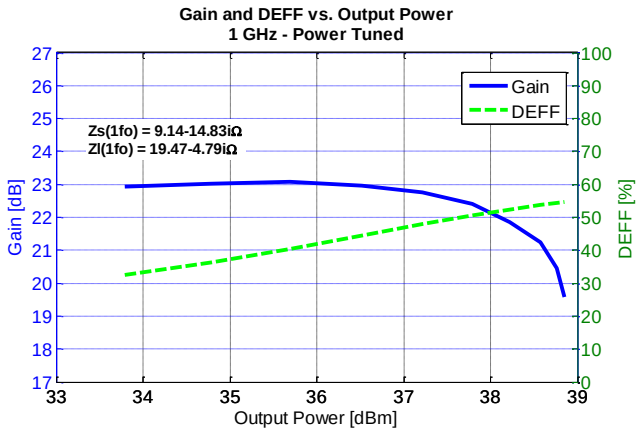
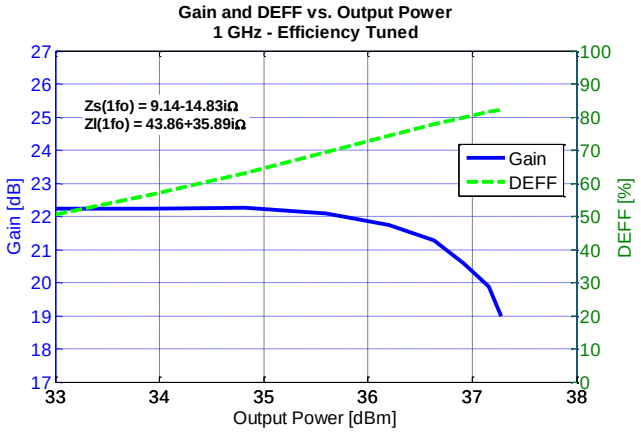


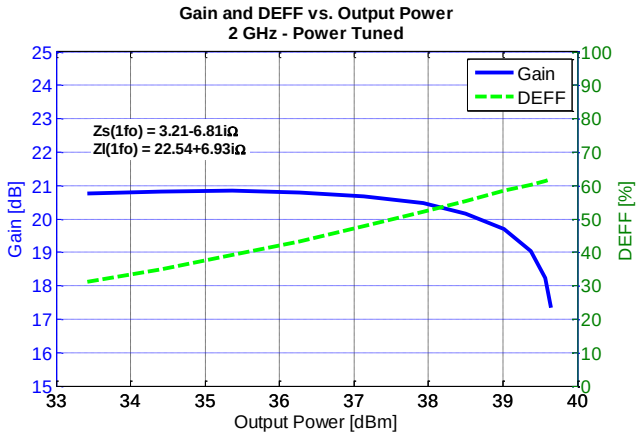
## Typical Performance – Load-Pull Drive-up[1, 2]

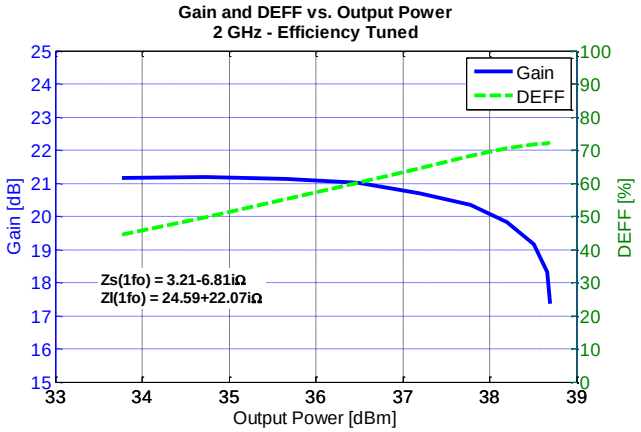
Notes:

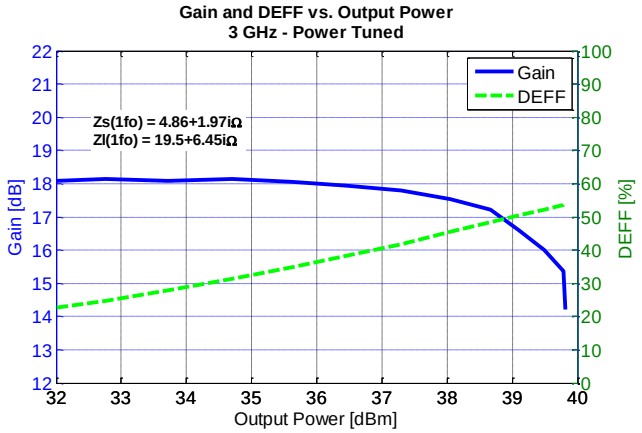
1. Pulse Width = 100 µs, Duty Cycle = 20%, $V_D$ = 28 V, $I_{DQ}$ = 50 mA
2. See page 20 for load-pull and source-pull reference planes where the performance was measured.

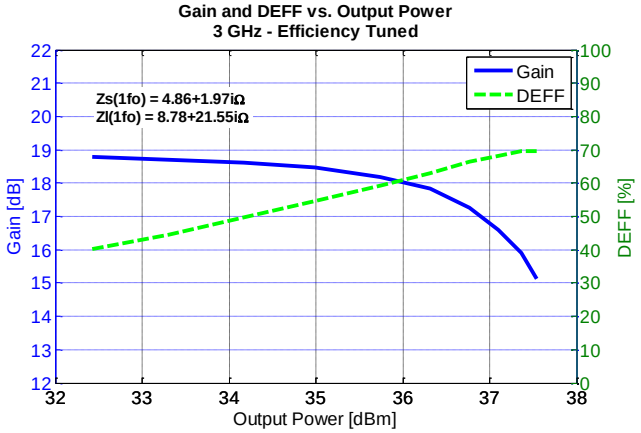


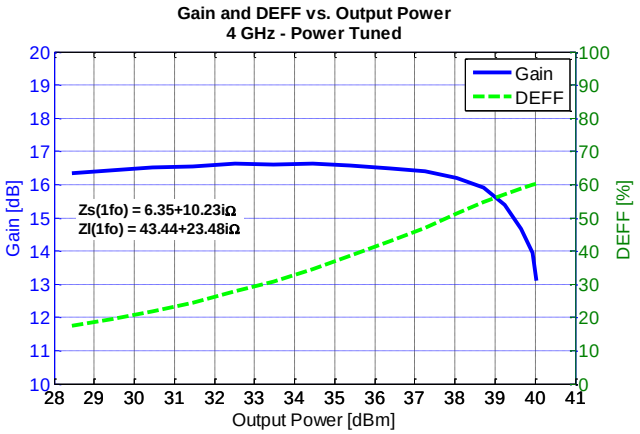



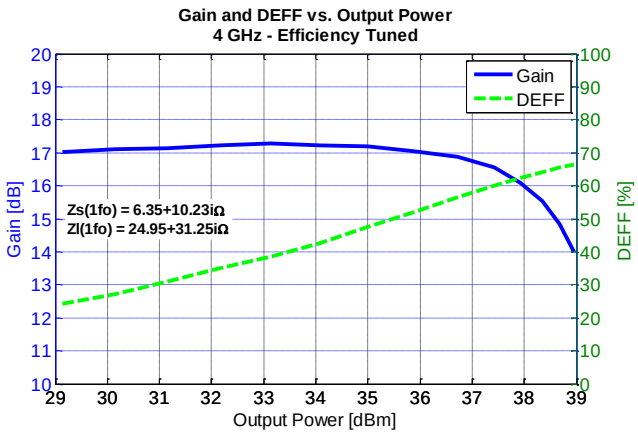



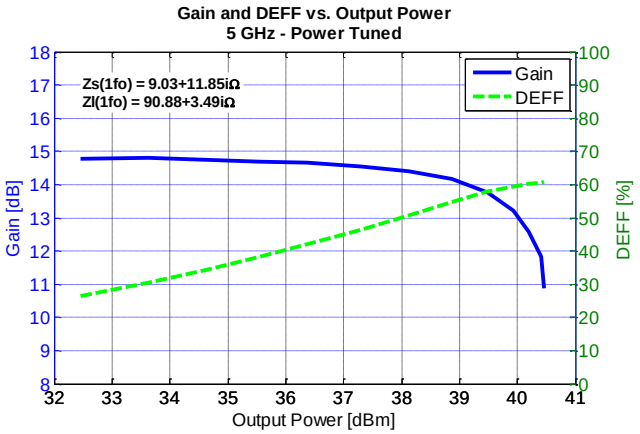
## Typical Performance – Load-Pull Drive-up[1, 2]

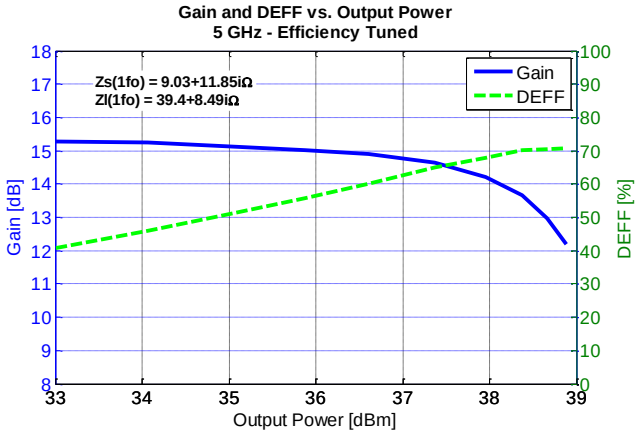
Notes:

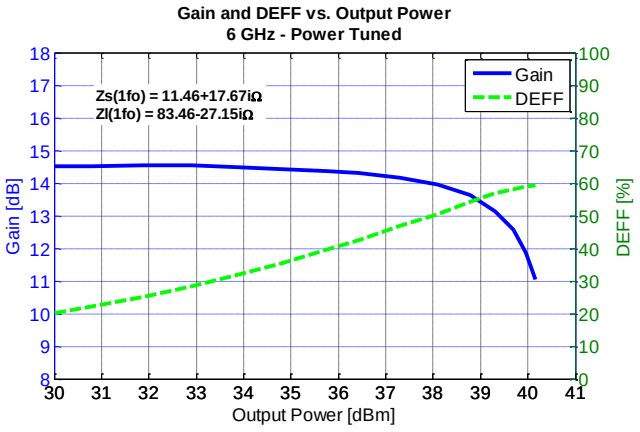
1. Pulse Width = 100 µs, Duty Cycle = 20%, $V_D$ = 28 V, $I_{DQ}$ = 50 mA
2. See page 20 for load-pull and source-pull reference planes where the performance was measured.

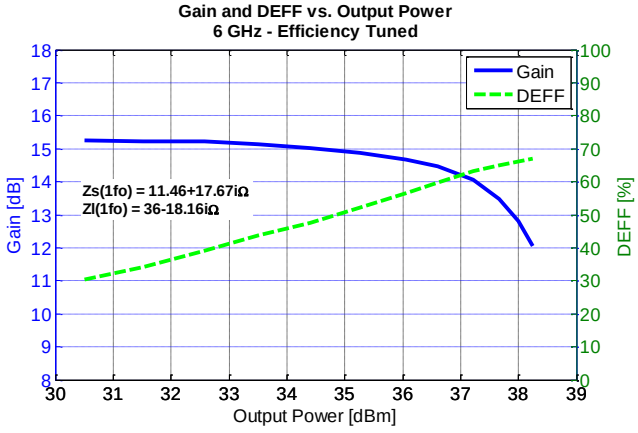


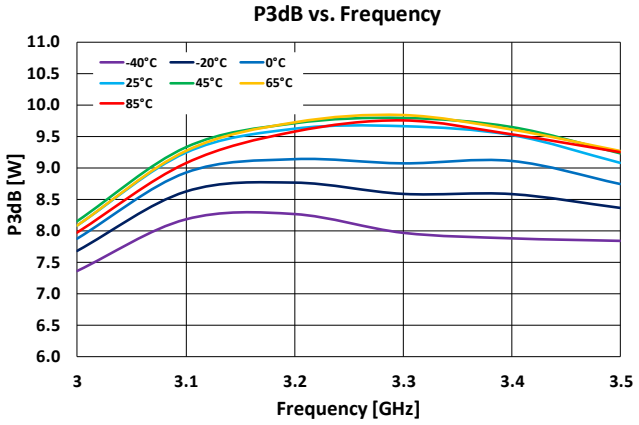



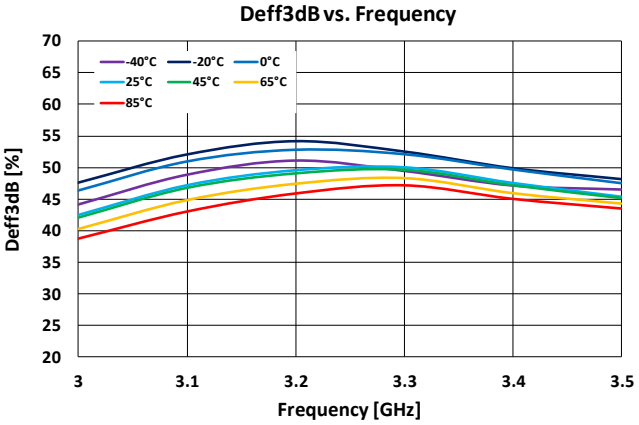



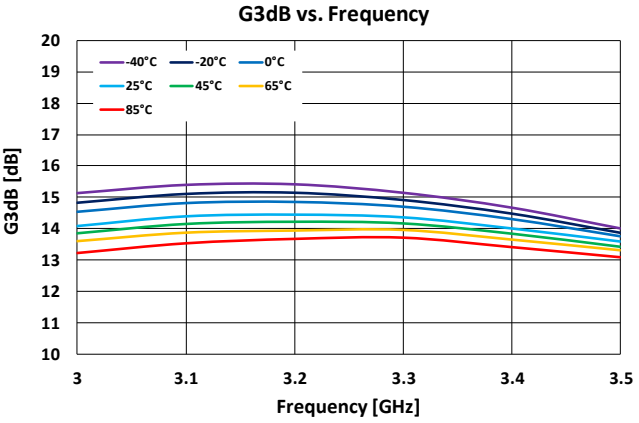
## Power Drive-Up Performance Over Temperatures of 3.0 – 3.5 GHz EVB[1]

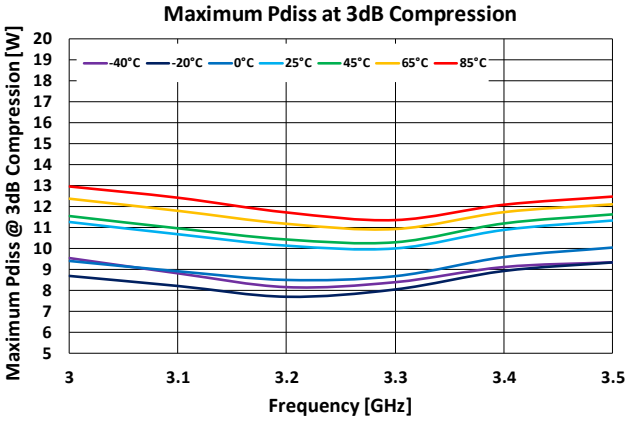
Notes:

1. Pulse Width = 100 µs, Duty Cycle = 20%, $V_D$ = 28 V, $I_{DQ}$ = 50 mA



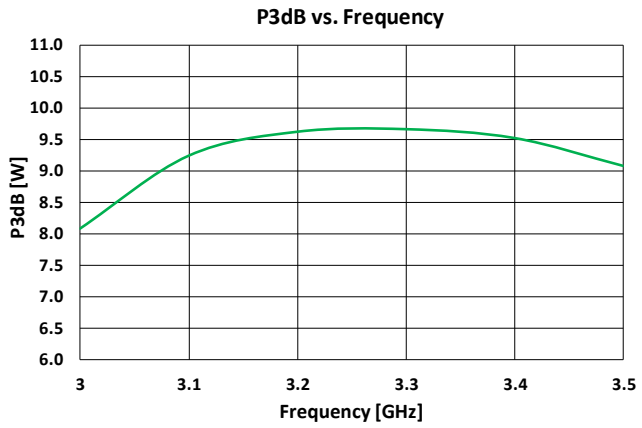



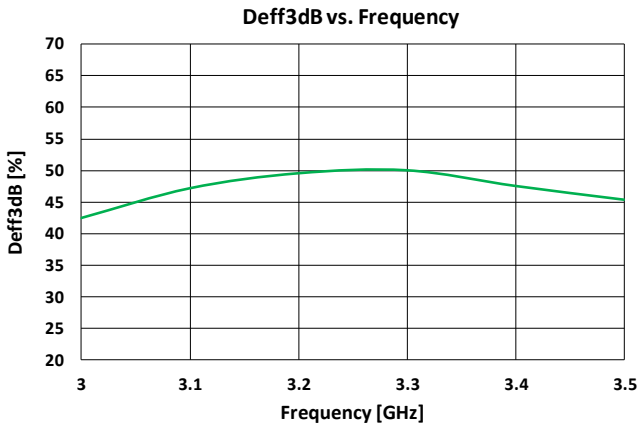



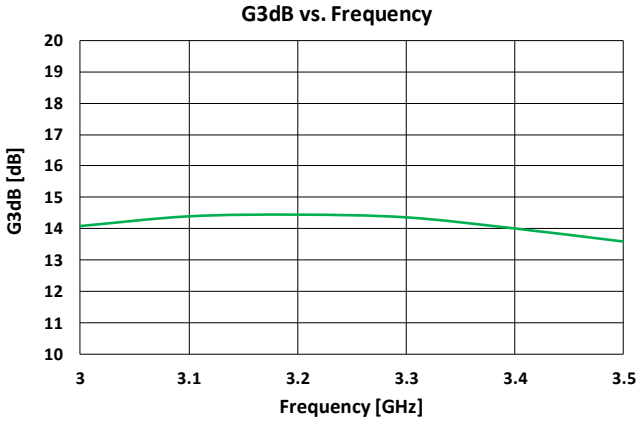
## Power Drive-Up Performance at 25 °C of 3.0 – 3.5 GHz EVB[1]

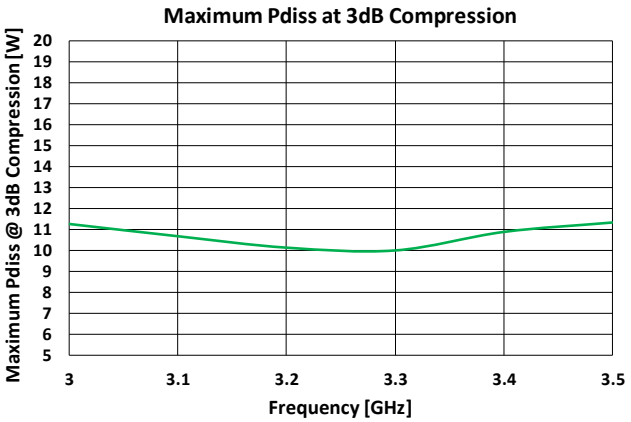
Notes:

1. Pulse Width = 100 µs, Duty Cycle = 20%, $V_D$ = 28 V, $I_{DQ}$ = 50 mA



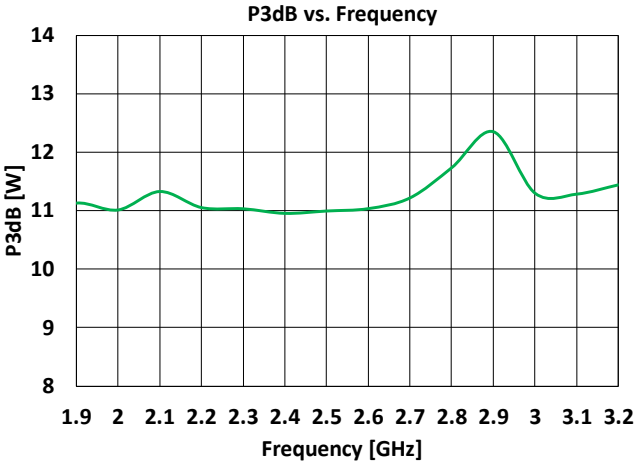



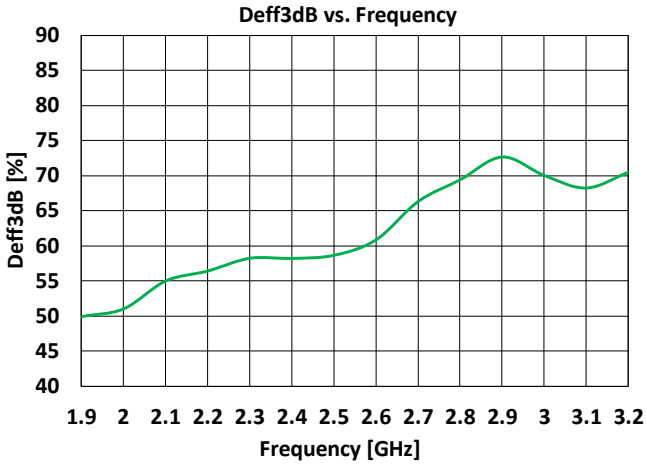



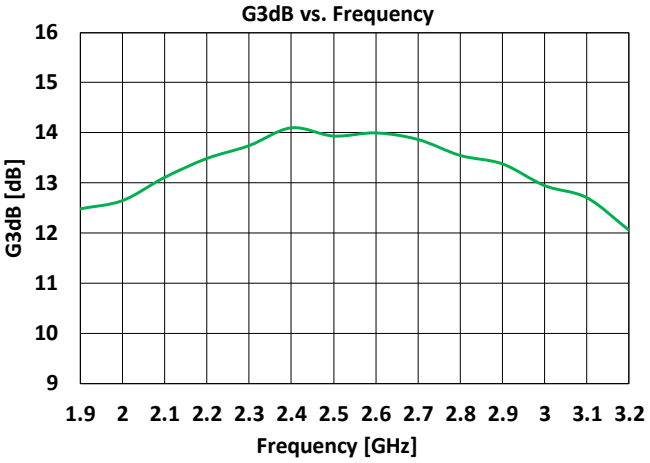
## Power Drive-Up Performance at 25 °C of 1.9 – 3.2 GHz EVB[1]

Notes:

1. Pulse Width = 100 µs, Duty Cycle = 20%, $V_D$ = 28 V, $I_{DQ}$ = 50 mA



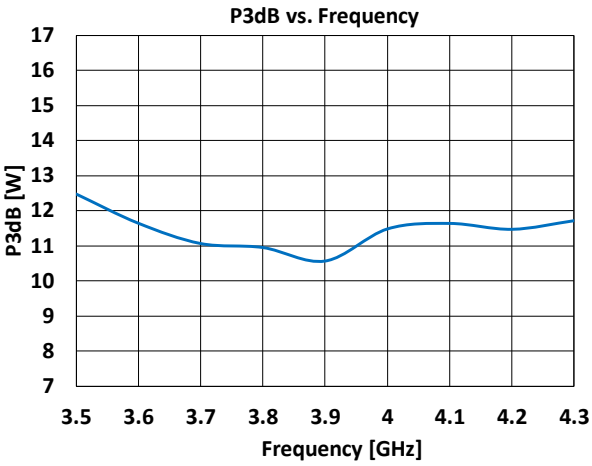



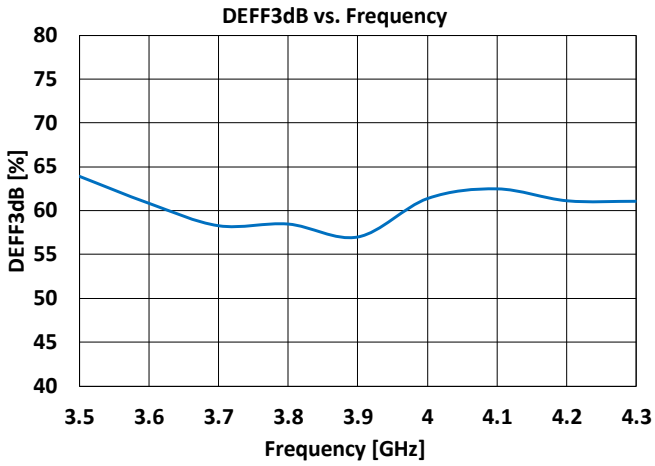



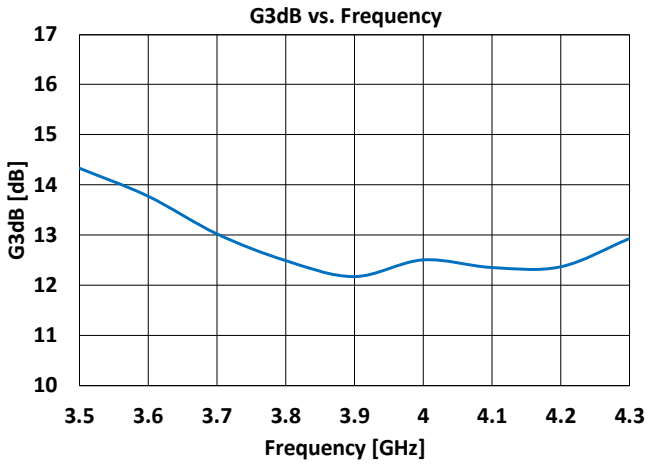
## Power Drive-Up Performance at 25 °C of 3.5 – 4.3 GHz EVB[1]

Notes:

1. Pulse Width = 100 µs, Duty Cycle = 20%, $V_D$ = 28 V, $I_{DQ}$ = 50 mA



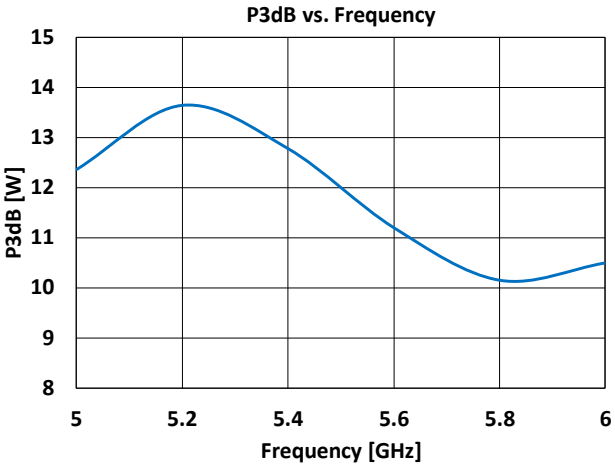



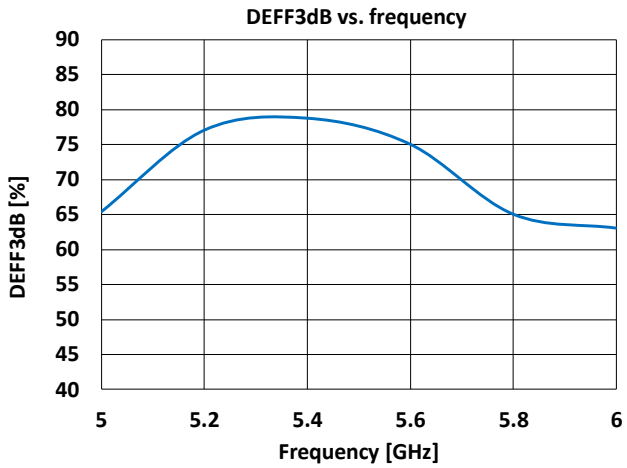



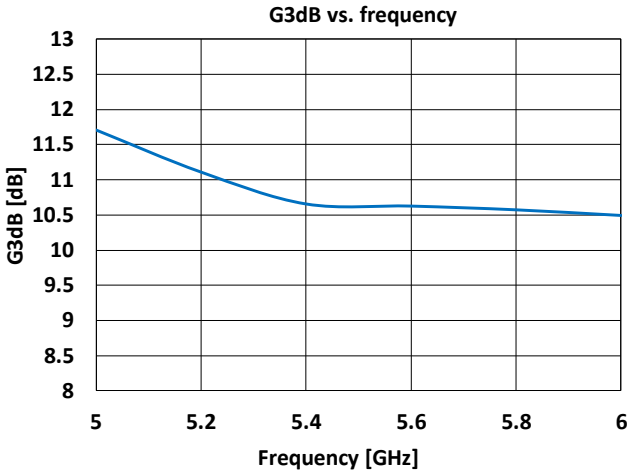
## Power Drive-Up Performance at 25 °C of 5 – 6 GHz EVB[1]

Notes:

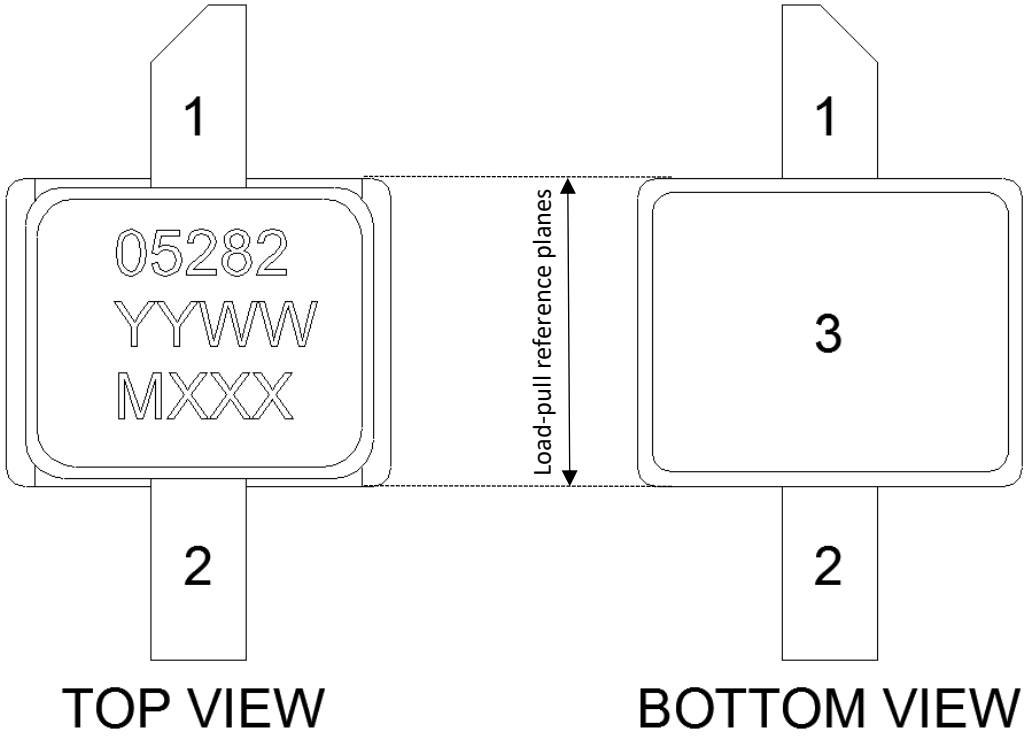
1. Pulse Width = 100 µs, Duty Cycle = 20%, $V_D$ = 32 V, $I_{DQ}$ = 50 mA



## Pin Configuration and Package Marking[1]

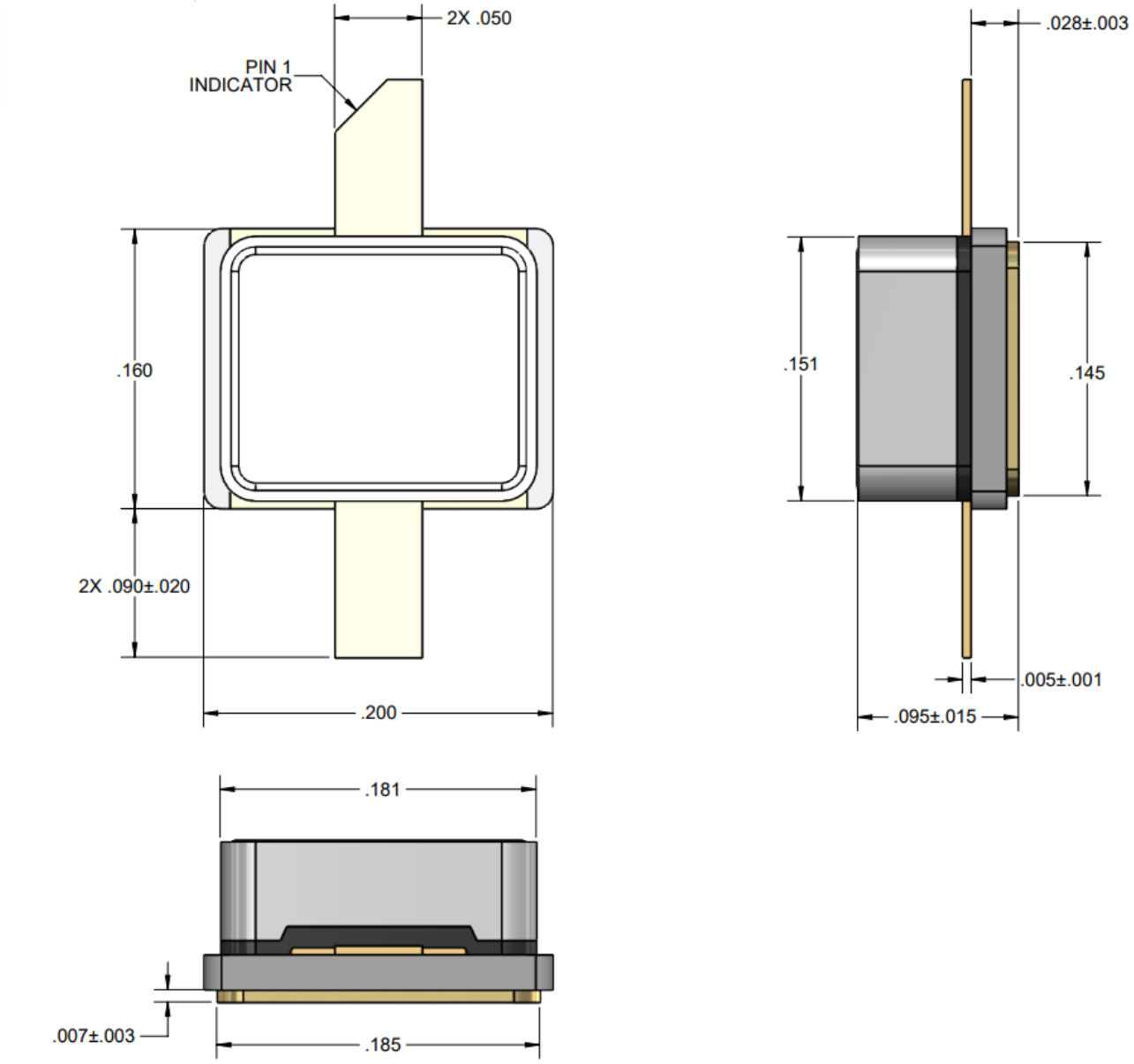



| Pin | Symbol | Description |
|---|---|---|
| 1 | $V_D$ / $RF_{OUT}$ | Gate Voltage / RF Input |
| 2 | $V_G$ / $RF_{IN}$ | Drain Voltage / RF Output |
| 3 | GND | Package base/ Ground |

Notes:

1. The T2G6000528-Q3 will be marked with the “05282” designator and a lot code marked below the part designator. The “YY” represents the last two digits of the calendar year the part was manufactured, the “WW” is the work week of the assembly lot start, the “MXXX” is the production lot number.

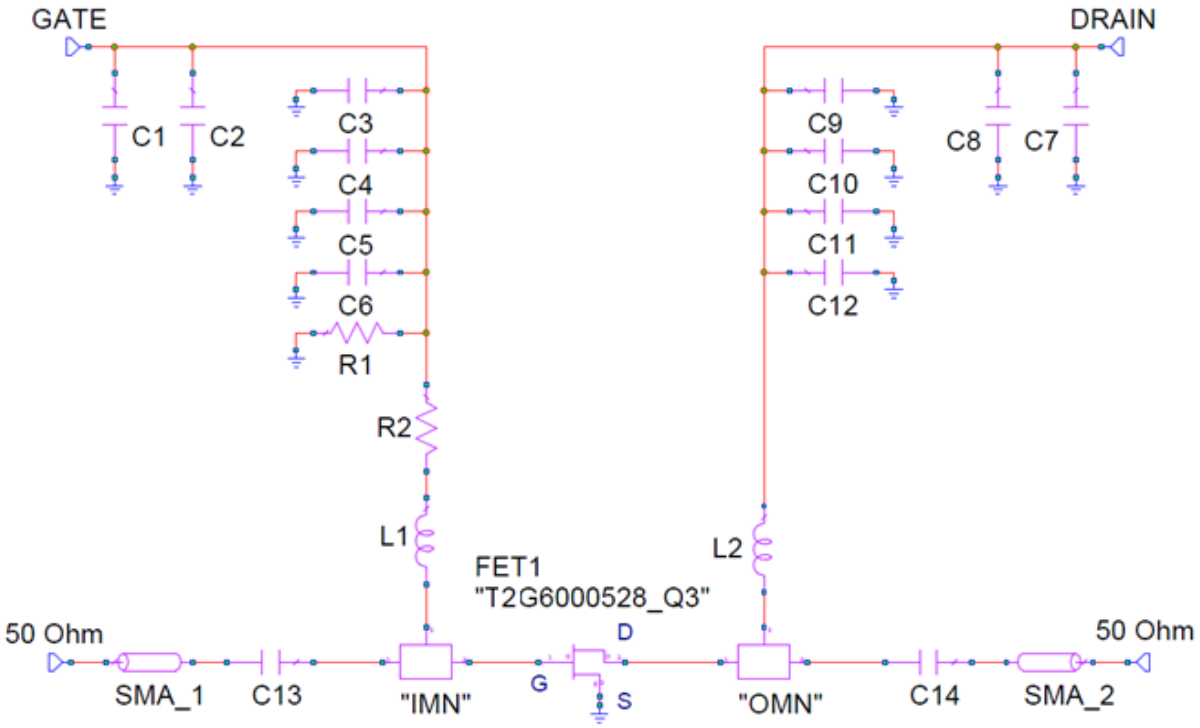
## Package Dimensions[1, 2, 3, 4, 5, 6]




Notes:

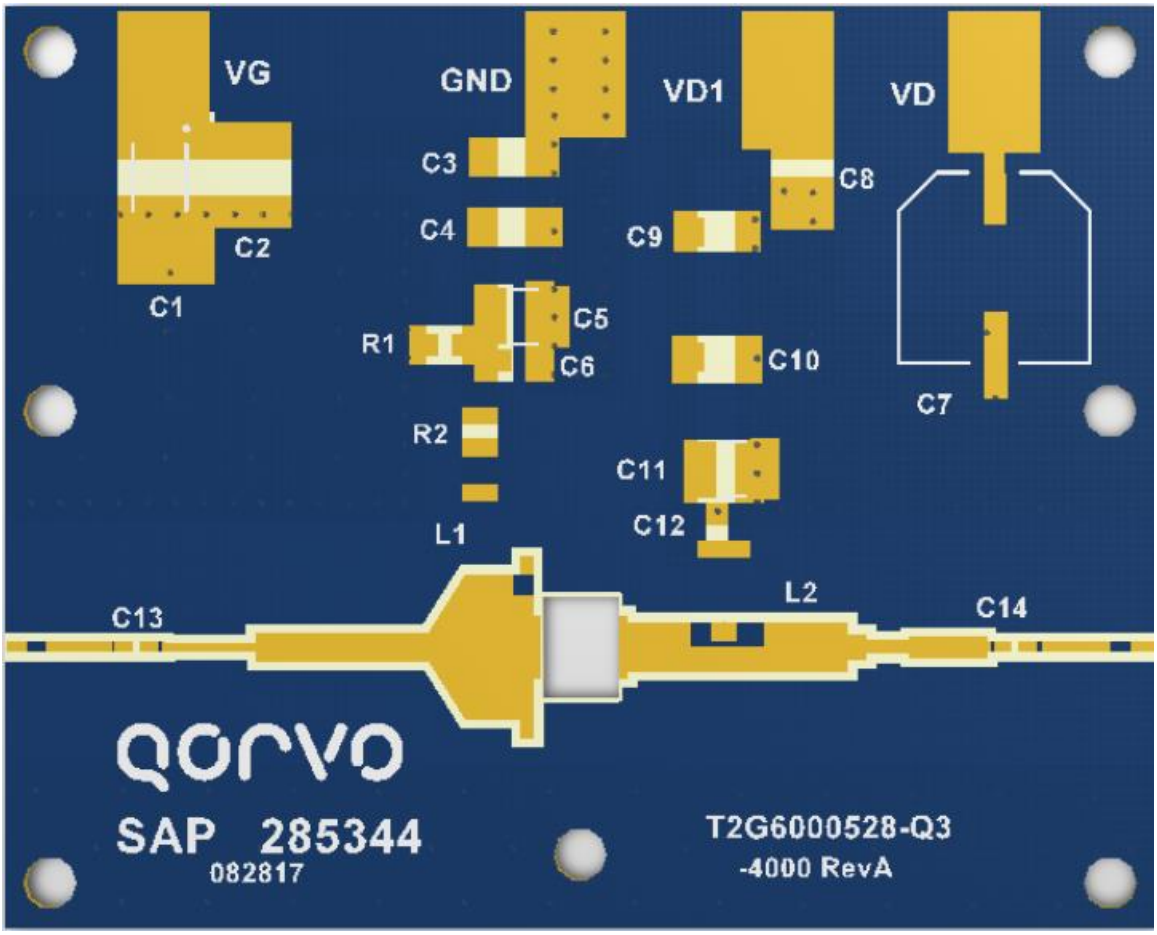
1. Unless otherwise specified, dimensions are in inches.
2. Material:
   Package Base: Ceramic/Metal
   Package Lid: Ceramic
3. Package exposed metal base and leads are gold plated.
4. Part is epoxy sealed.
5. Part meets industry NI200 footprint.
6. Body Dimensions do not include lid shift or epoxy run out which can be up to 0.020 per side.

## Schematic of 3.0 – 3.5 GHz EVB




| Bias-up Procedure | Bias-down Procedure |
|---|---|
| 1. Set $V_G$ to -4 V | 1. Turn off RF signal. |
| 2. Set $I_D$ current limit to 60 mA. | 2. Turn off $V_D$. |
| 3. Set $V_D$ to 28 V. | 3. Wait 2 seconds to allow drain capacitor to discharge |
| 4. Slowly adjust $V_G$ until $I_D$ is set to 50 mA. | 4. Turn off $V_G$ |
| 5. Set $I_D$ current limit to 0.7 A. | |
| 6. Apply RF. | |

## Layout of 3.0 – 3.5 GHz EVB[1, 2, 3]



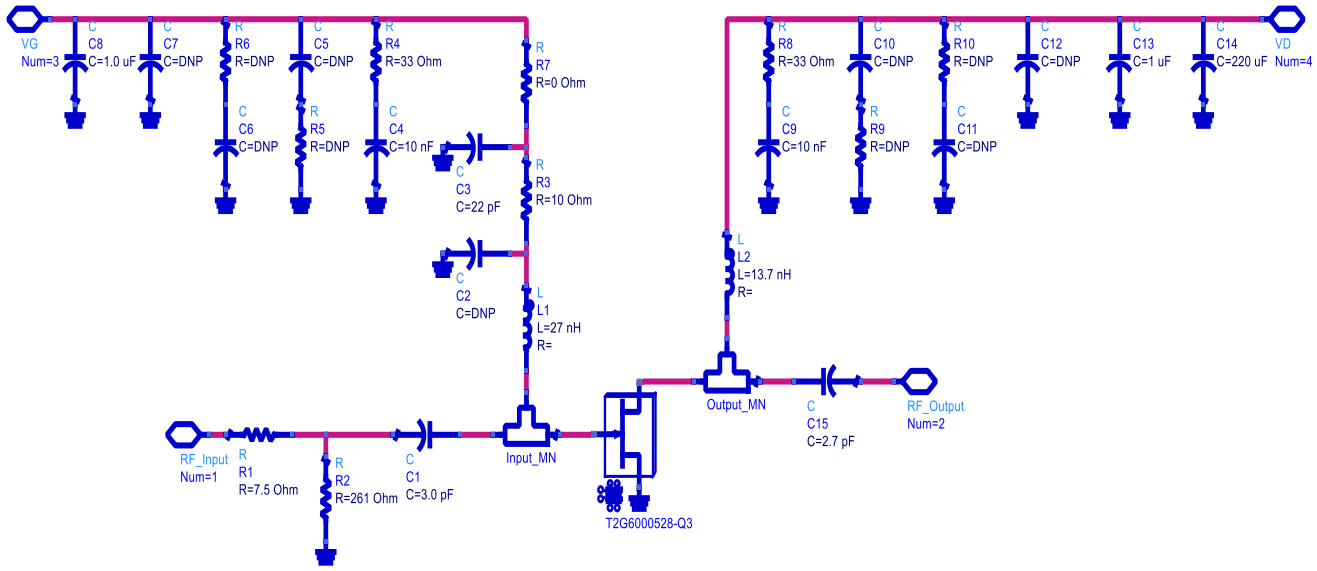

Notes:

1. PCB Material: RO4350B, 20 mil thickness, 1 oz copper cladding
2. Overall size is 2 x 2.5 inch$^2$.
3. Connect 28 V to $V_D$ port and insert a current sensor for current measurement between $V_{D1}$ and $V_D$ ports.

## Bill of Material – 3.0 – 3.5 GHz EVB

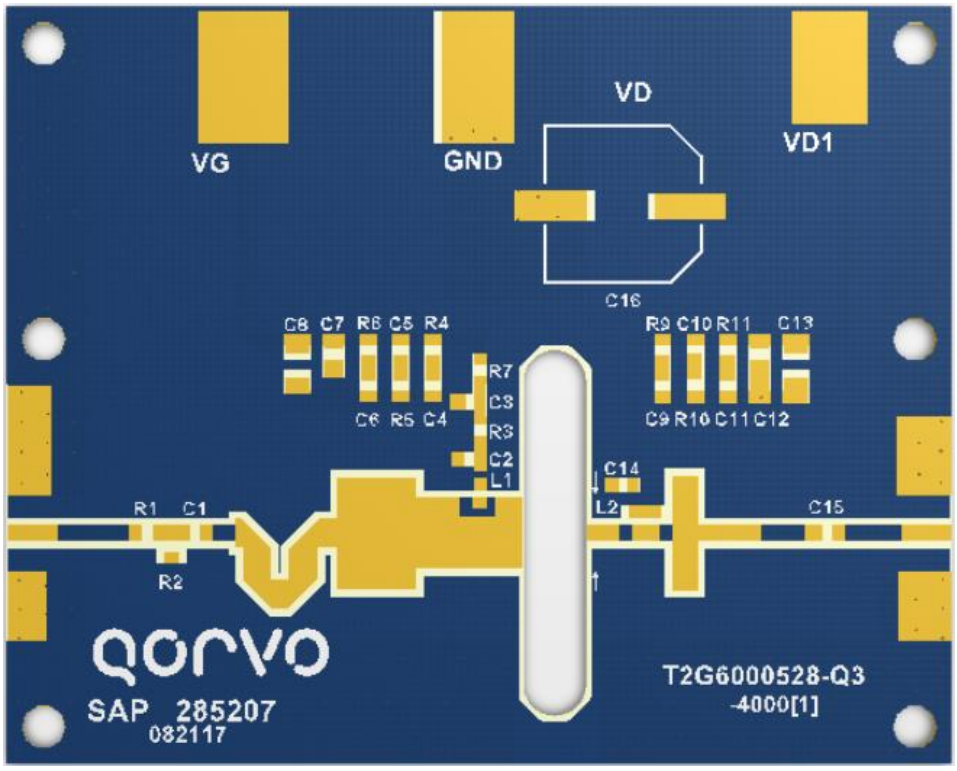
| Ref Des | Value | Qty | Manufacturer | Part Number |
|---|---|---|---|---|
| C1, C7 | 22 uF | 2 | Sprague | T491D |
| C2, C8 | 1 uF | 2 | Kemet | 1812C105KAT2A |
| C3, C9 | 0.1 uF | 2 | Kemet | C1206C104KRAC7800 |
| C4, C10 | 0.01 uF | 2 | Kemet | C1206C103KRAC7800 |
| C5, C11 | 100 pF | 2 | ATC | 100B101 |
| C6, C12 | 2400 pF | 2 | DLI | C08BL242C5UNC0B |
| C13, C14 | 27 pF | 2 | ATC | 600L270JT200 |
| R1 | 1000 ohm | 1 | Vishay Dale | CRCW0805100F100 |
| R2 | 12 ohm | 1 | Vishay Dale | RM73B2B120J |
| L1, L2 | 9.85 nH | 2 | Coilcraft | 16069JLB |

## Schematic of 1.9 – 3.2 GHz EVB




| Bias-up Procedure | Bias-down Procedure |
|---|---|
| 2. Set $V_G$ to -4 V | 3. Turn off RF signal. |
| 4. Set $I_D$ current limit to 60 mA. | 4. Turn off $V_D$. |
| 5. Set $V_D$ to 28 V. | 5. Wait 2 seconds to allow drain capacitor to discharge |
| 6. Slowly adjust $V_G$ until $I_D$ is set to 50 mA. | 7. Turn off $V_G$ |
| 8. Set $I_D$ current limit to 0.7 A. | |
| 9. Apply RF. | |

## Layout of 1.9 – 3.2 GHz EVB[1, 2, 3]



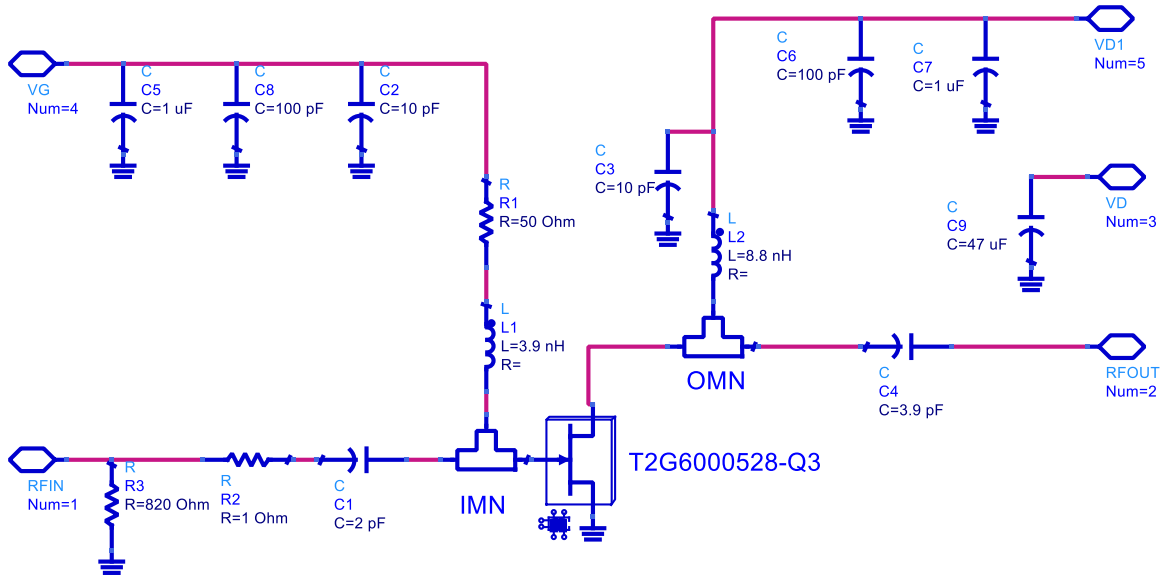

Notes:

1. PCB Material: RO4350B, 20 mil thickness, 1 oz copper cladding
2. Overall size is 2 x 2.5 inch$^2$.
3. Connect 28 V to $V_D$ port and insert a current sensor for current measurement between $V_{D1}$ and $V_D$ ports.

## Bill of Material – 1.9 – 3.2 GHz EVB

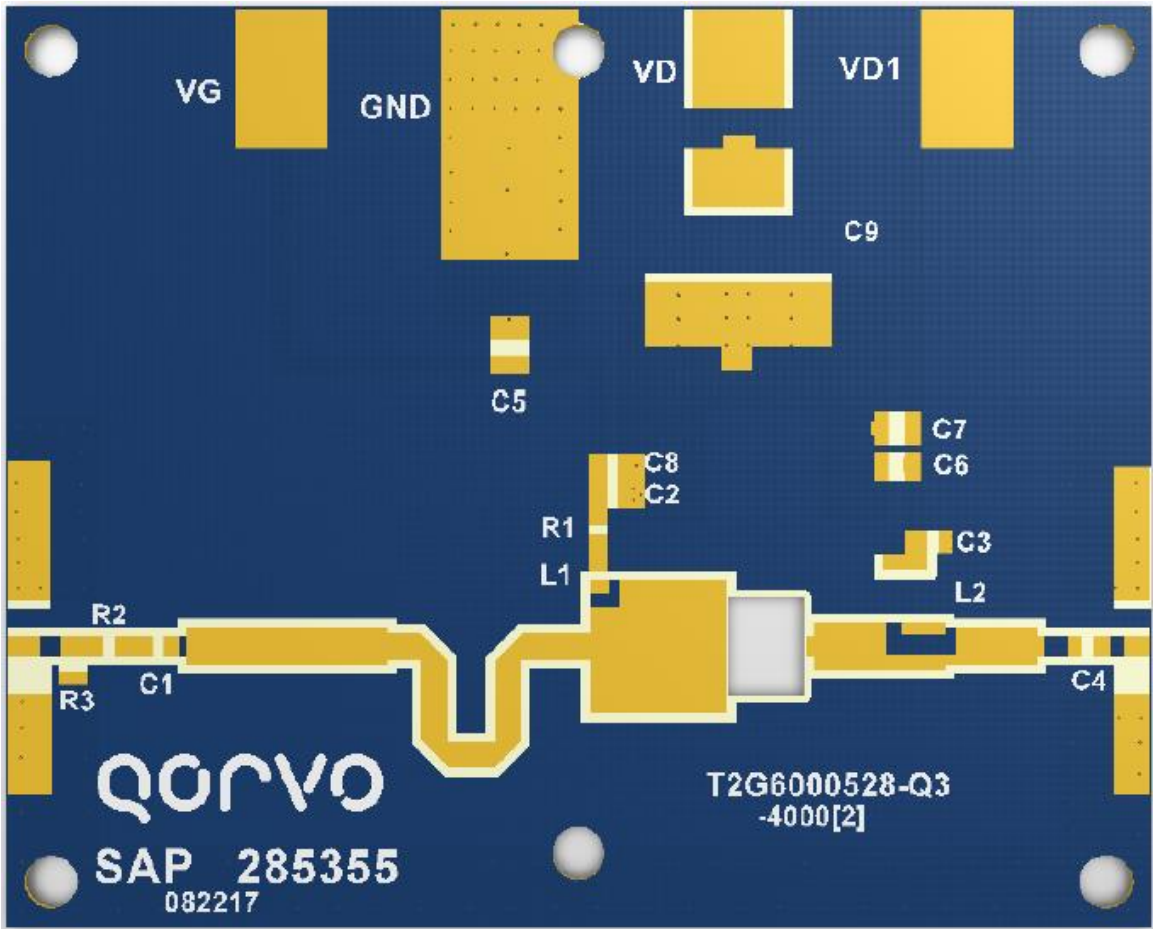
| Ref Des | Value | Qty | Manufacturer | Part Number |
|---|---|---|---|---|
| C1 | 3.0 pF | 1 | PPI | 0603N3R0AW251X |
| C3, C14 | 22 pF | 2 | ATC | 600S220FT250XT |
| C4, C9 | 10 nF | 2 | Capax | 0603X103K101S |
| C8, C13 | 1 uF | 2 | TTI | C1206T105J5RACTU |
| C15 | 2.7 pF | 1 | ATC | 600S2R7AW250XT |
| C16 | 47 uF | 1 | Panasonic | EEETG1K470UP |
| L1 | 27 nH | 1 | Coilcraft | 0603CS-27NXGEW |
| L2 | 13.7 nH | 1 | Coilcraft | 0807SQ-14NJLB |
| R1 | 7.5 Ohm | 1 | TTI | CRCW06037R50FKEA |
| R2 | 270 Ohm | 1 | TTI | RK73B1JTTD271J |
| R3 | 10 Ohm | 1 | TTI | CRCW060310R0JNTA |
| R4, R9 | 33.2 Ohm | 2 | TTI | CRCW060333R2FKTA |
| R7 | 0 Ohm | 1 | TTI | ERJ-3GEY0R00V |
| C5, C6, C7, C10, C11, C12, R5, R6, R10, R11 | DNP | | | |

## Schematic of 3.5 – 4.3 GHz EVB




| Bias-up Procedure | Bias-down Procedure |
|---|---|
| 3. Set $V_G$ to -4 V | 5. Turn off RF signal. |
| 6. Set $I_D$ current limit to 60 mA. | 6. Turn off $V_D$. |
| 7. Set $V_D$ to 28 V. | 7. Wait 2 seconds to allow drain capacitor to discharge |
| 8. Slowly adjust $V_G$ until $I_D$ is set to 50 mA. | 10. Turn off $V_G$ |
| 11. Set $I_D$ current limit to 0.7 A. | |
| 12. Apply RF. | |

## Layout of 3.5 – 4.3 GHz EVB[1, 2, 3]



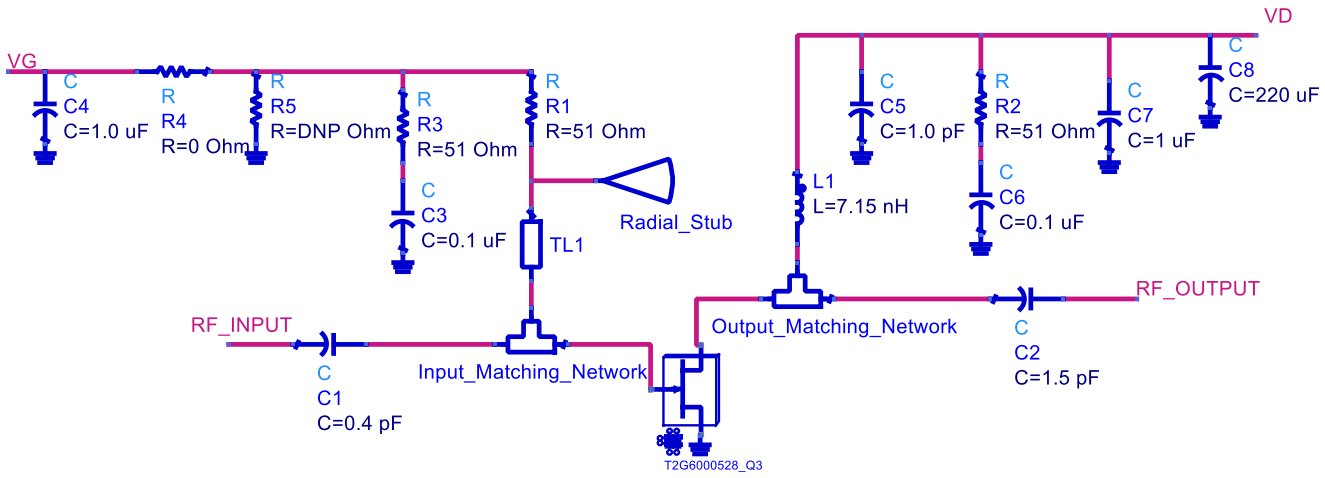

Notes:

1. PCB Material: RO4350B, 20 mil thickness, 1 oz copper cladding
2. Overall size is 2 x 2.5 inch$^2$.
3. Connect 28 V to $V_D$ port and insert a current sensor for current measurement between $V_{D1}$ and $V_D$ ports.

## Bill of Material – 3.5 – 4.3 GHz EVB

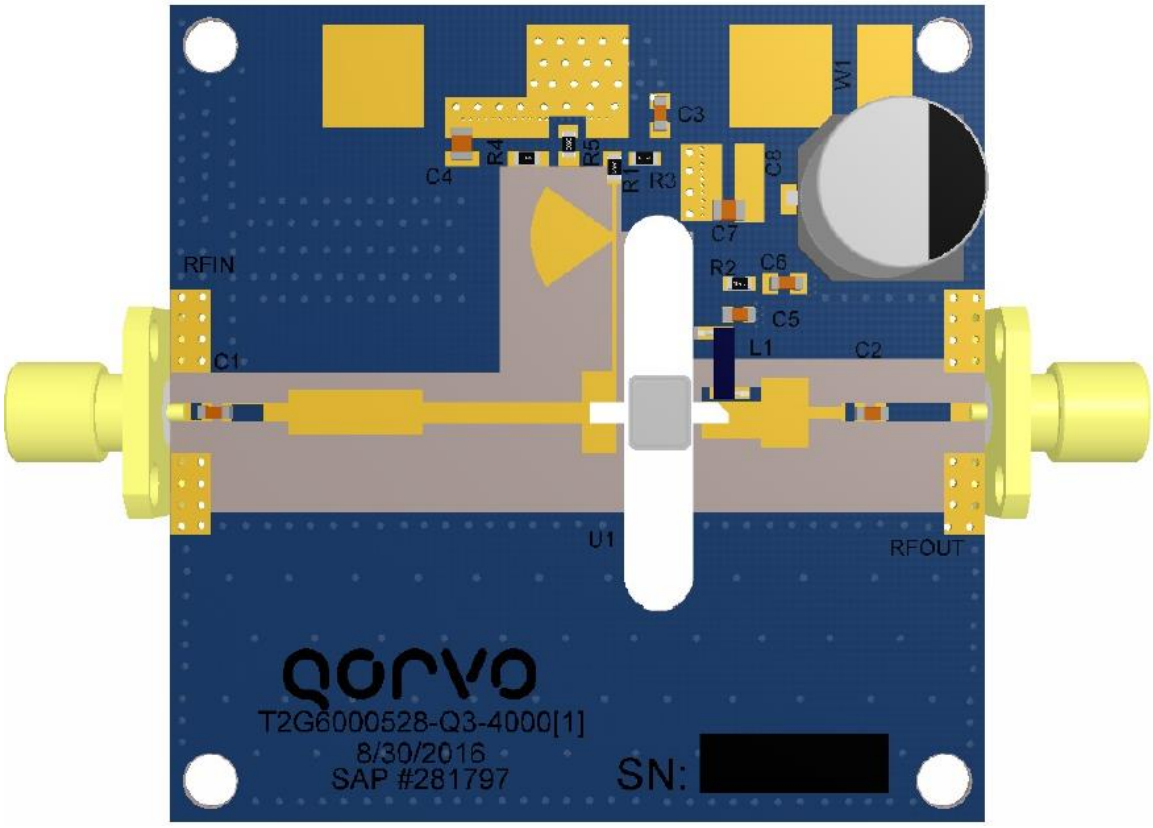
| Ref Des | Value | Qty | Manufacturer | Part Number |
|---|---|---|---|---|
| C1 | 2 pF | 1 | ATC | 600S2R0AT250X |
| C4 | 3.9 pF | 1 | ATC | 600S3R9AT250X |
| C2, C3 | 10 pF | 2 | ATC | 600S100FT250XT |
| C6, C8 | 100 pF | 2 | Capax | 0603G101J201S |
| C5, C7 | 1 uF | 2 | TTI | C0805C105K5RACTU |
| C9 | 47 uF | 1 | Digikey | EEETG1K470UP |
| L1 | 3.9 nH | 1 | Coilcraft | 0603CS-3N9XJEW |
| L2 | 8.8 nH | 1 | Coilcraft | 1606-8GLB |
| R1 | 50 Ohm | 1 | Vishay | CRCW060350R0FKEA-ND |
| R2 | 1 Ohm | 1 | Vishay | RC1608F1R0CS |
| R3 | 866 Ohm | 1 | Vishay | CRCW0603866RFKEA |

## Schematic of 5 – 6 GHz EVB




| Bias-up Procedure | Bias-down Procedure |
|---|---|
| 4. Set $V_G$ to -4 V | 7. Turn off RF signal. |
| 8. Set $I_D$ current limit to 60 mA. | 8. Turn off $V_D$. |
| 9. Set $V_D$ to 32 V. | 9. Wait 2 seconds to allow drain capacitor to discharge |
| 10. Slowly adjust $V_G$ until $I_D$ is set to 50 mA. | 13. Turn off $V_G$ |
| 14. Set $I_D$ current limit to 0.7 A. | |
| 15. Apply RF. | |

## Layout of 5.0 – 6.0 GHz EVB[1, 2, 3]




Notes:

1. PCB Material: RO4350B, 20 mil thickness, 1 oz copper cladding
2. Overall size is 2 x 2 inch$^2$.
3. Connect 32 V to $V_D$ port.

## Bill of Material – 5.0 – 6.0 GHz EVB

| Ref Des | Value | Qty | Manufacturer | Part Number |
|---|---|---|---|---|
| C1 | 0.4 pF | 1 | ATC | 600S0R4AT250X |
| C2 | 1.5 pF | 1 | ATC | 600S1R5AT250X |
| C5 | 1 pF | 1 | ATC | 600S1R0BT250XT |
| C3, C6 | 0.1 uF | 2 | TTI | C0603C104K5RAC |
| C4, C7 | 1 uF | 2 | Digikey | CGA4J3X7S2A105K125AB |
| C8 | 220 uF, 50 V | 1 | Panasonic | EEE-FK1H221GP |
| L1 | 5.6 nH | 1 | Coilcraft | 1606-6GLC |
| R1, R2, R3 | 51 Ohm | 3 | Vishay | CRCW060351R1FKTA |
| R4 | 0 Ohm | 1 | Vishay | CRCW06030000Z0EA |
| R5 | DNP | 1 | | |

## Recommended Solder Temperature Profile