

## Product Overview

The T2G6001528-Q3 is an 18W ( $P_{3dB}$ ) discrete GaN on SiC HEMT which operates from DC to 6.0 GHz. The device is constructed with Qorvo's proven TQGaN25 process, which features advanced field plate techniques to optimize power and efficiency at high drain bias operating conditions. This optimization can potentially lower system costs in terms of fewer amplifier line-ups and lower thermal management costs.

Lead free and RoHS compliant.

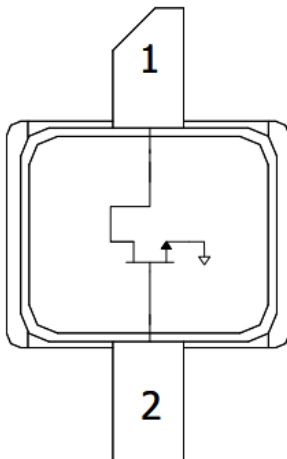
Evaluation boards are available upon request.



## Key Features

- Operating Frequency Range: DC – 6.0 GHz
- Operating Drain Voltage: 28 V
- Output Power ( $P_{3dB}$ ): 19 W at 5.2 GHz
- Low thermal resistance package

## Functional Block Diagram



## Applications

- Military Radar
- Civilian Radar
- Professional and military radio communications
- Test Instrumentation
- Wideband/Narrowband Amplifiers
- Jammers

## Ordering Information

| Part Number       | Description                    |
|-------------------|--------------------------------|
| T2G6001528-Q3     | Packaged Part Flangeless       |
| T2G6001528-Q3EVB1 | 5.0 – 6.0 GHz Evaluation Board |
| T2G6001528-Q3EVB2 | 1.8 – 2.6 GHz Evaluation Board |

### Absolute Maximum Ratings

| Parameter                         | Rating         |
|-----------------------------------|----------------|
| Breakdown Voltage ( $V_{DG}$ )    | +100 V         |
| Gate Voltage Range ( $V_G$ )      | -7 to +2 V     |
| Drain Current ( $I_D$ )           | 5 A            |
| Gate Current ( $I_G$ )            | -5 to 14 mA    |
| Power Dissipation ( $P_D$ )       | 28 W           |
| Peak RF Input Power, CW           | +36 dBm        |
| Channel Temperature ( $T_{CH}$ )  | +275 °C        |
| Mounting Temperature (30 seconds) | 320 °C         |
| Storage Temperature               | -40 to +150 °C |

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to device may reduce device reliability.

### Recommended Operating Conditions<sup>(1)</sup>

| Parameter                            | Min | Typ  | Max  | Units |
|--------------------------------------|-----|------|------|-------|
| Gate Voltage ( $V_G$ )               | -   | -2.9 | -    | V     |
| Drain Voltage ( $V_D$ )              | -   | +32  | -    | V     |
| Quiescent Drain Current ( $I_{DQ}$ ) | -   | 50   | -    | mA    |
| Peak Drain Current ( $I_D$ )         | -   | 1.4  | -    | A     |
| Channel Temperature ( $T_{CH}$ )     | -   | -    | 225  | °C    |
| Power Dissipation, CW $P_D^{(2)}$    | -   | -    | 20.9 | W     |
| Power Dissipation, Pulse $P_D^{(3)}$ | -   | -    | 22.5 | W     |

<sup>1</sup> Electrical specification are measured at specified test conditions.

Specifications are not guaranteed over all recommended operating conditions.

<sup>2</sup> Package at 85 °C

<sup>3</sup> 100uS Pulse Width, 20 % Duty Cycle, package at 85 °C

### RF Characterization – Load Pull Performance at 3.0 GHz<sup>(1)</sup>

| Parameter   | Min | Typ  | Max | Units |
|---|-----|------|-----|-------|
| Linear Gain ( $G_{LIN}$ )                                       | -   | 16.5 | -   | dB    |
| Output Power at 3 dB Gain Compression ( $P_{3dB}$ )             | -   | 19.6 | -   | W     |
| Drain Efficiency at 3 dB Gain Compression ( $DE_{3dB}$ )        | -   | 69.6 | -   | %     |
| Power Added Efficiency at 3 dB Gain Compression ( $PAE_{3dB}$ ) | -   | 66.4 | -   | %     |
| Gain at 3 dB Compression ( $G_{3dB}$ )                          | -   | 13.5 | -   | dB    |

Notes:

1. Test conditions unless otherwise noted:  $T_A = 25$  °C,  $V_D = 28$  V,  $I_{DQ} = 50$  mA, Pulse: 100uS, 20%

### RF Characterization – Load Pull Performance at 6.0 GHz<sup>(1)</sup>

| Parameter   | Min | Typ  | Max | Units |
|---|-----|------|-----|-------|
| Linear Gain ( $G_{LIN}$ )                                       | -   | 11.3 | -   | dB    |
| Output Power at 3 dB Gain Compression ( $P_{3dB}$ )             | -   | 19.0 | -   | W     |
| Drain Efficiency at 3 dB Gain Compression ( $DE_{3dB}$ )        | -   | 66.0 | -   | %     |
| Power Added Efficiency at 3 dB Gain Compression ( $PAE_{3dB}$ ) | -   | 56.2 | -   | %     |
| Gain at 3 dB Compression ( $G_{3dB}$ )                          | -   | 8.3  | -   | dB    |

Notes:

1. Test conditions unless otherwise noted:  $T_A = 25$  °C,  $V_D = 28$  V,  $I_{DQ} = 50$  mA, Pulse: 100uS, 20%

## RF Characterization – Performance at 5.2 GHz<sup>(1,2)</sup>

| Parameter  | Min  | Typ  | Max | Units |
|--|------|------|-----|-------|
| Linear Gain ( $G_{LIN}$ )                                | -    | 10.5 | -   | dB    |
| Output Power at 3 dB Gain Compression ( $P_{3dB}$ )      | -    | 17.3 | -   | W     |
| Drain Efficiency at 3 dB Gain Compression ( $DE_{3dB}$ ) | -    | 48.0 | -   | %     |
| Gain at 3 dB Compression ( $G_{3dB}$ )                   | -    | 7.5  | -   | dB    |
| Gate Leakage, $V_D = 10$ V, $V_G = -3.7$ V               | -5.5 | -    | -   | mA    |

Notes:

1. Performance at 5.2 GHz in the 5.0 - 6.0 GHz Evaluation Board
2. Test conditions unless otherwise noted:  $T_A = 25$  °C,  $V_D = 28$  V,  $I_{DQ} = 50$  mA, Pulse: 100 $\mu$ s, 20%

## RF Characterization – Mismatch Ruggedness at 3.50 GHz<sup>(1,2)</sup>

| Symbol | Parameter                     | dB Compression | Typical |
|--------|-------------------------------|----------------|---------|
| VSWR   | Impedance Mismatch Ruggedness | 1              | 10:1    |

Notes:

1. Test conditions unless otherwise noted:  $T_A = +25$  °C,  $V_D = +28$  V,  $I_{DQ} = 50$  mA
2.  $V_{DS} = 28$  V,  $I_{DQ} = 50$  mA, CW at  $P_{1dB}$

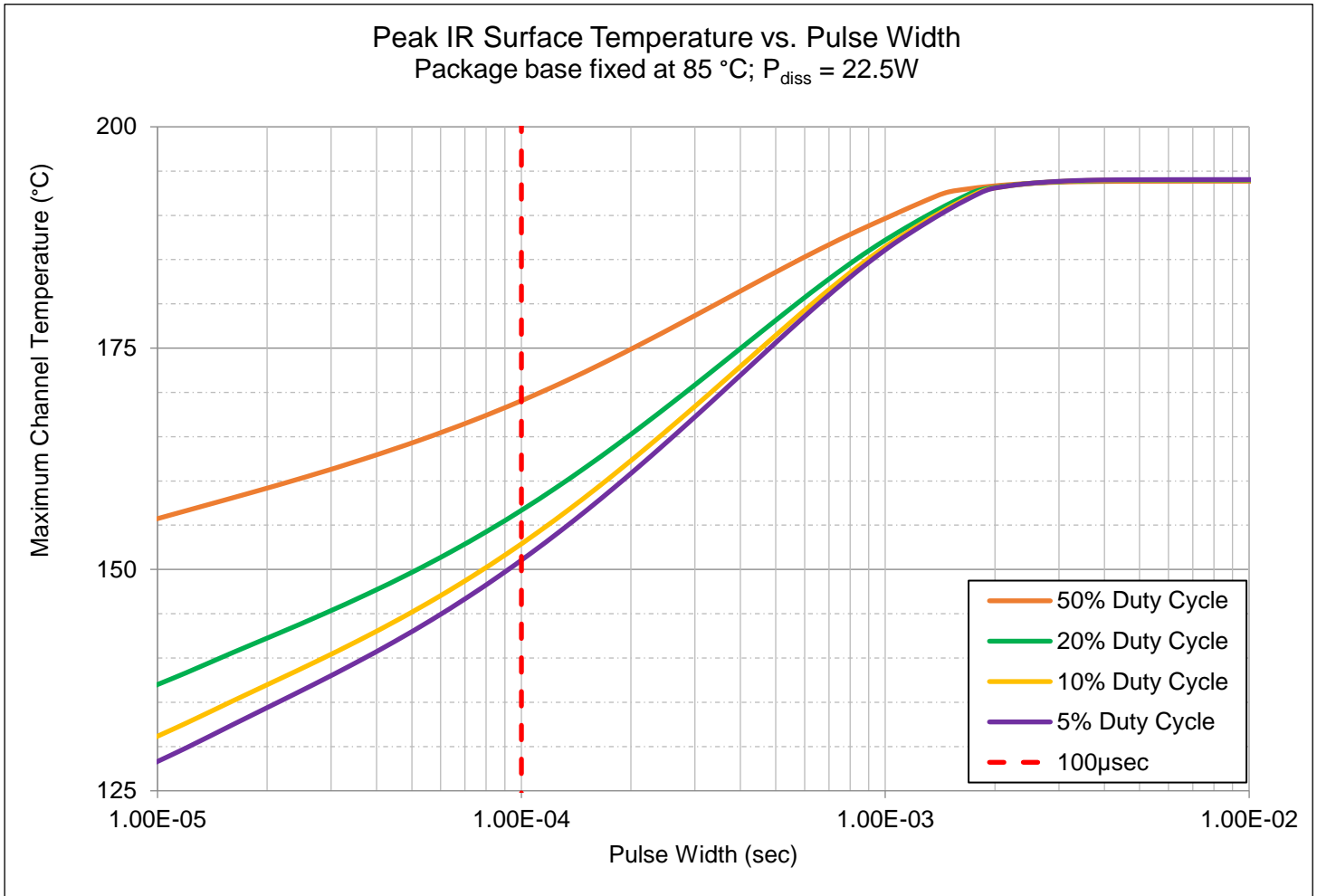
## Thermal Information<sup>(1,2)</sup>

| Parameter           | Test Conditions                                | Values | Units |
|---------------------|--|--------|-------|
| Thermal Resistance  | $P_{DISS} = 22.5$ W, Pulse Width = 100 $\mu$ s | 3.2    | °C/W  |
| Channel Temperature | Duty Cycle = 20%, $T_{CASE} = 85$ °C           | 156.8  | °C    |

Notes:

1. Thermal resistance is measured to package backside.
2. Refer to the following document: [GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates](#)

### Maximum Channel Temperature

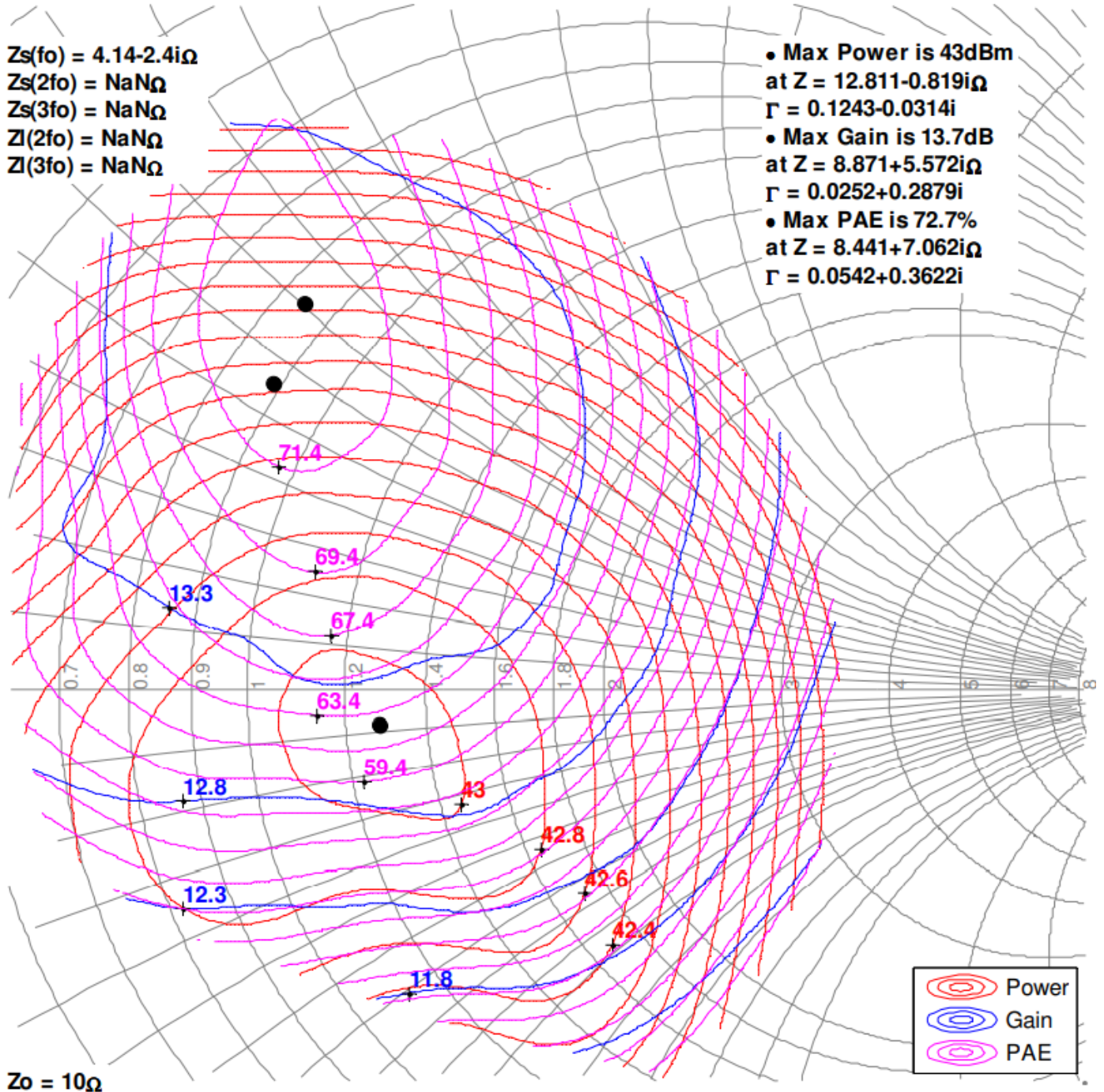


### Load Pull Contours<sup>(1,2,3,4,5)</sup>

Notes:

1. The impedances shown are those presented to the device at load pull reference planes. See page 13.
2. Test Conditions:  $V_{DS} = 28\text{ V}$ ,  $I_{DQ} = 50\text{ mA}$
3. Test Signal: Pulse Width = 100  $\mu\text{sec}$ , Duty Cycle = 20%
4. NaN indicates the value was not set during load pull.
5.  $Z_0$  is the characteristic impedance of load pull fixtures.

### 3GHz, Load-pull

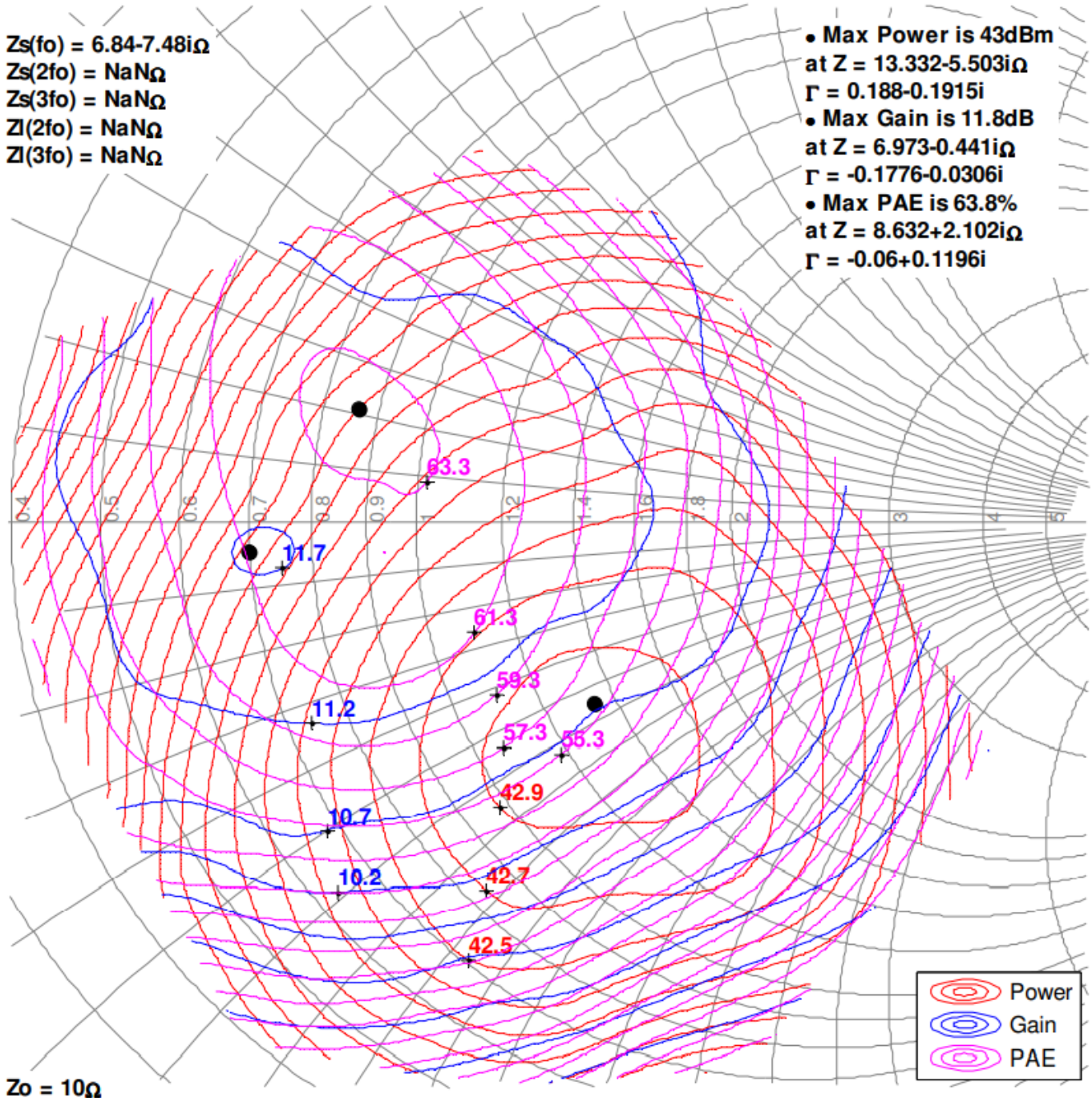


Load Pull Contours<sup>(1,2,3,4,5)</sup>

Notes:

1. The impedances shown are those presented to the device at load pull reference planes. See page 13.
2. Test Conditions:  $V_{DS} = 28\text{ V}$ ,  $I_{DQ} = 50\text{ mA}$
3. Test Signal: Pulse Width = 100  $\mu\text{sec}$ , Duty Cycle = 20%
4. NaN indicates the value was not set during load pull.
5.  $Z_0$  is the characteristic impedance of load pull fixtures.

4GHz, Load-pull



Load Pull Contours<sup>(1,2,3,4,5)</sup>

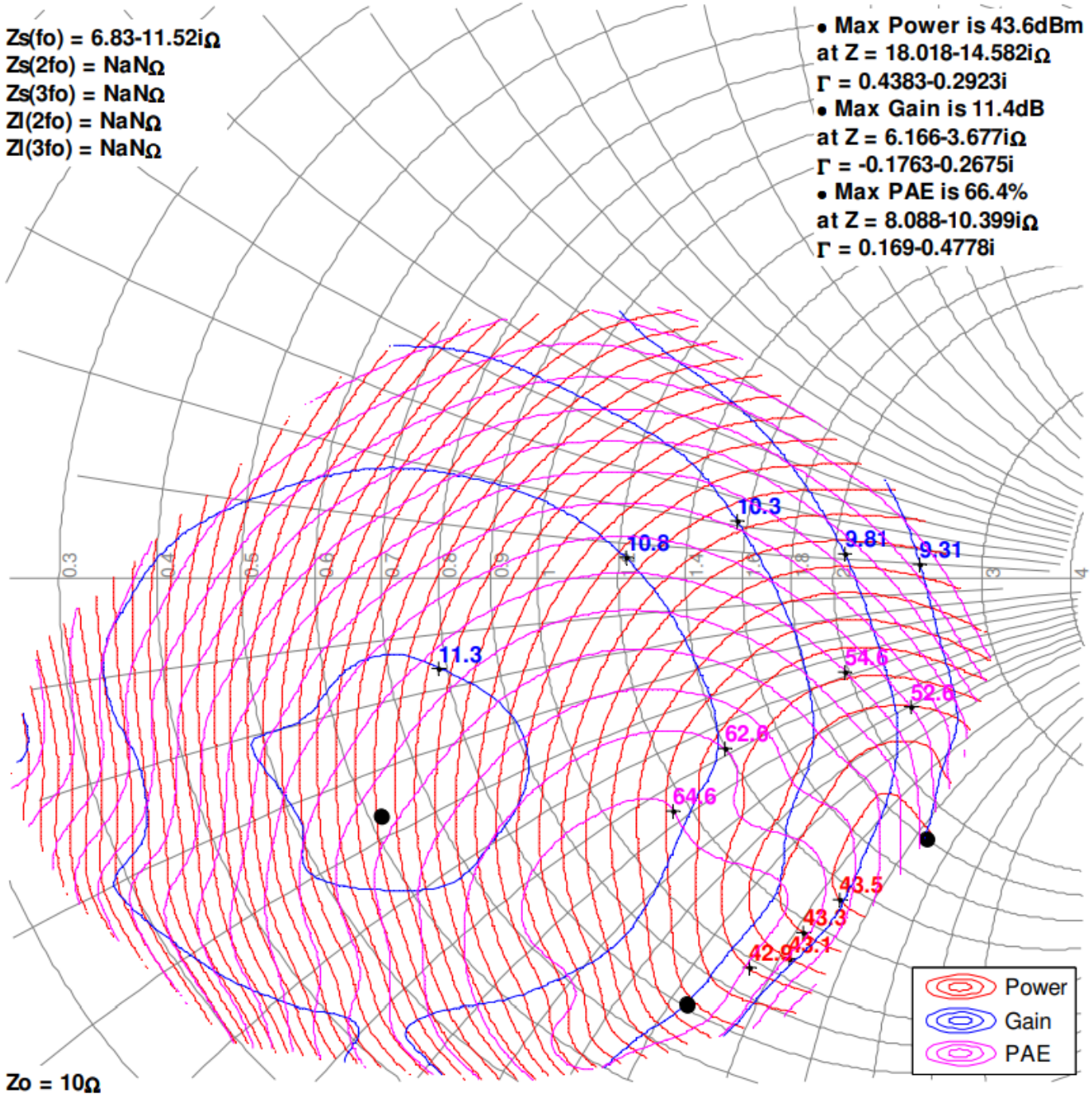
Notes:

1. The impedances shown are those presented to the device at load pull reference planes. See page 13.
2. Test Conditions:  $V_{DS} = 28\text{ V}$ ,  $I_{DQ} = 50\text{ mA}$
3. Test Signal: Pulse Width = 100  $\mu\text{sec}$ , Duty Cycle = 20%
4. NaN indicates the value was not set during load pull.
5.  $Z_0$  is the characteristic impedance of load pull fixtures.

5GHz, Load-pull

$Z_s(f_0) = 6.83-11.52i\Omega$   
 $Z_s(2f_0) = \text{NaN}\Omega$   
 $Z_s(3f_0) = \text{NaN}\Omega$   
 $Z_l(2f_0) = \text{NaN}\Omega$   
 $Z_l(3f_0) = \text{NaN}\Omega$

- Max Power is 43.6dBm at  $Z = 18.018-14.582i\Omega$   
 $\Gamma = 0.4383-0.2923i$
- Max Gain is 11.4dB at  $Z = 6.166-3.677i\Omega$   
 $\Gamma = -0.1763-0.2675i$
- Max PAE is 66.4% at  $Z = 8.088-10.399i\Omega$   
 $\Gamma = 0.169-0.4778i$



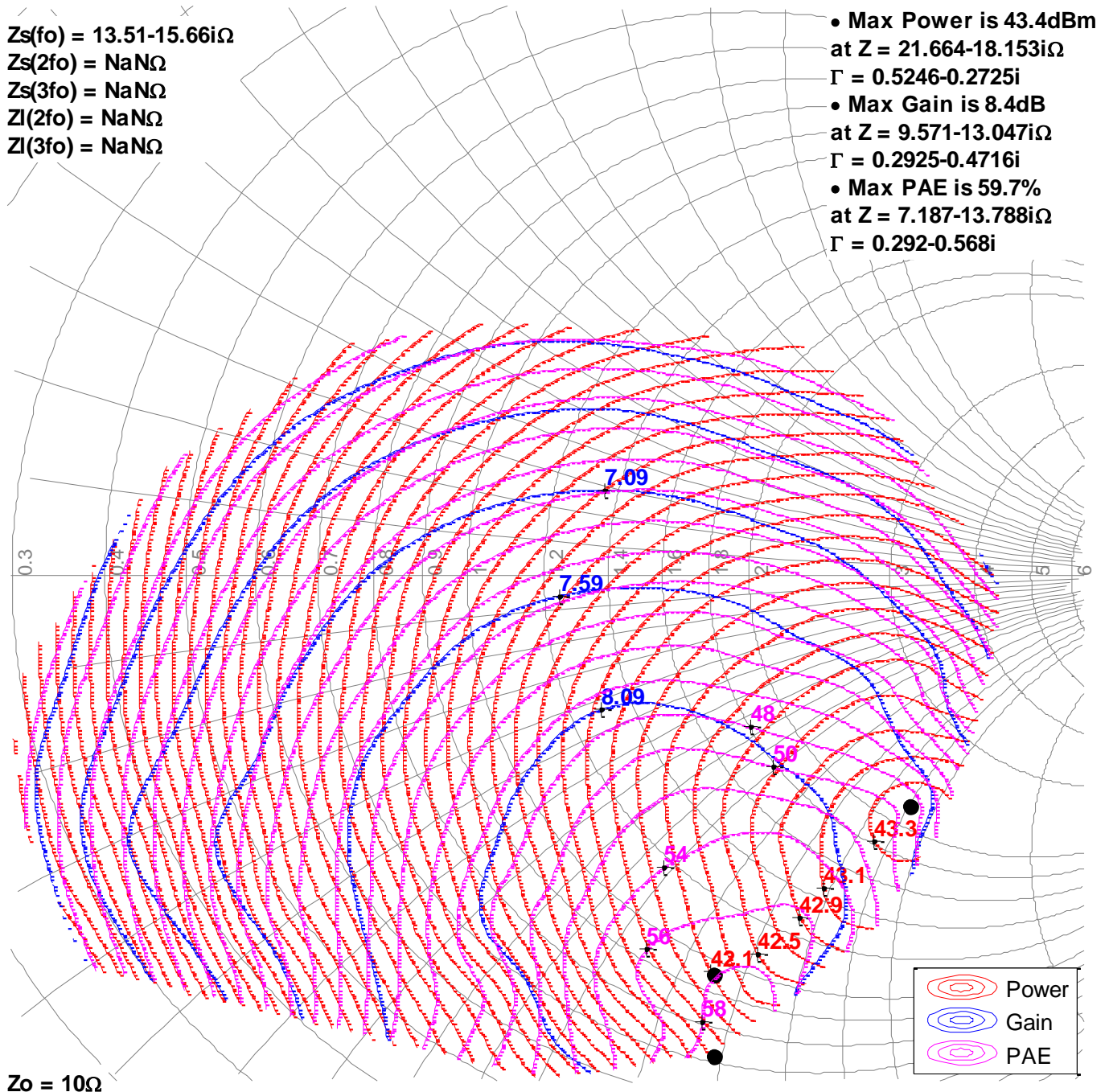
$Z_0 = 10\Omega$

### Load Pull Contours<sup>(1,2,3,4,5)</sup>

Notes:

1. The impedances shown are those presented to the device at load pull reference planes. See page 13.
2. Test Conditions:  $V_{DS} = 28\text{ V}$ ,  $I_{DQ} = 50\text{ mA}$
3. Test Signal: Pulse Width = 100  $\mu\text{sec}$ , Duty Cycle = 20%
4. NaN indicates the value was not set during load pull.
5.  $Z_0$  is the characteristic impedance of load pull fixtures.

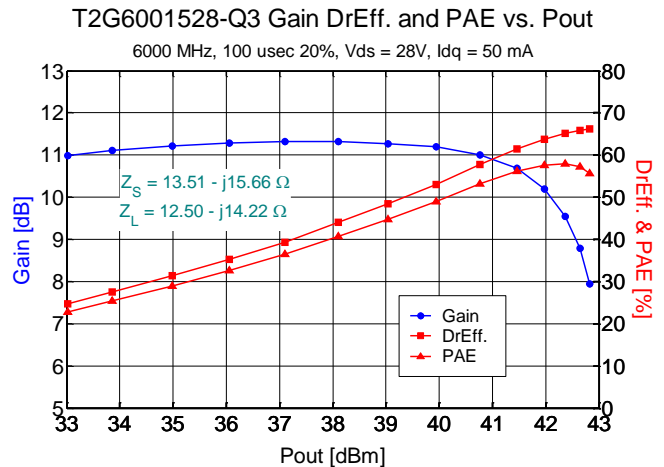
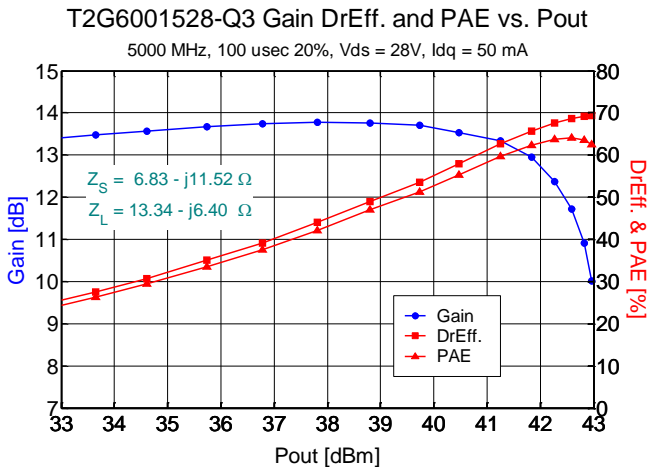
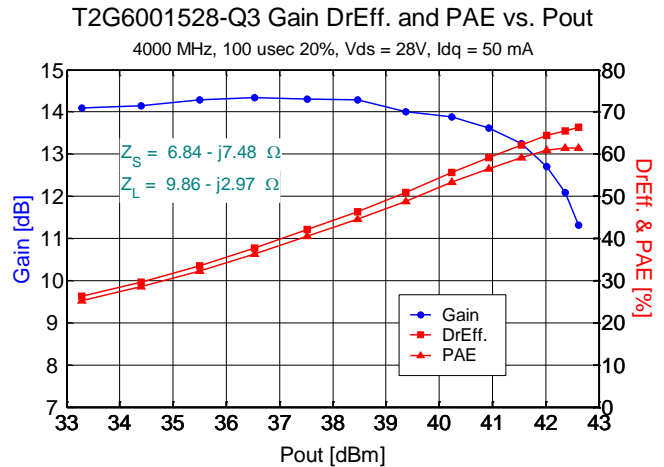
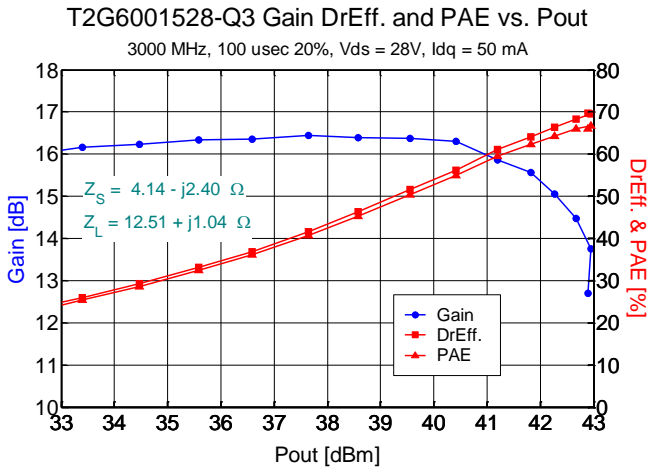
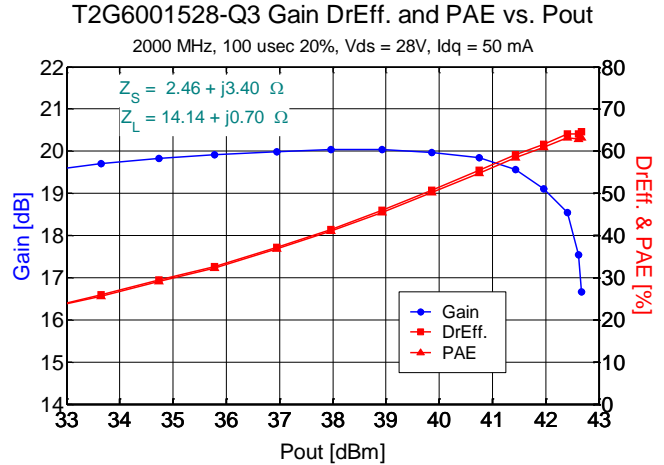
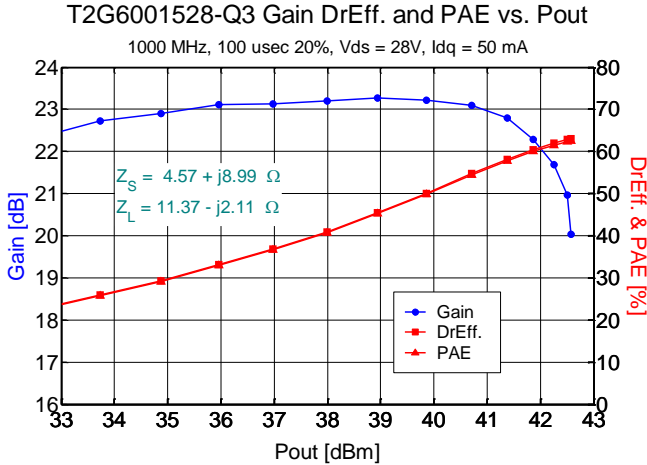
### 6GHz, Load-pull





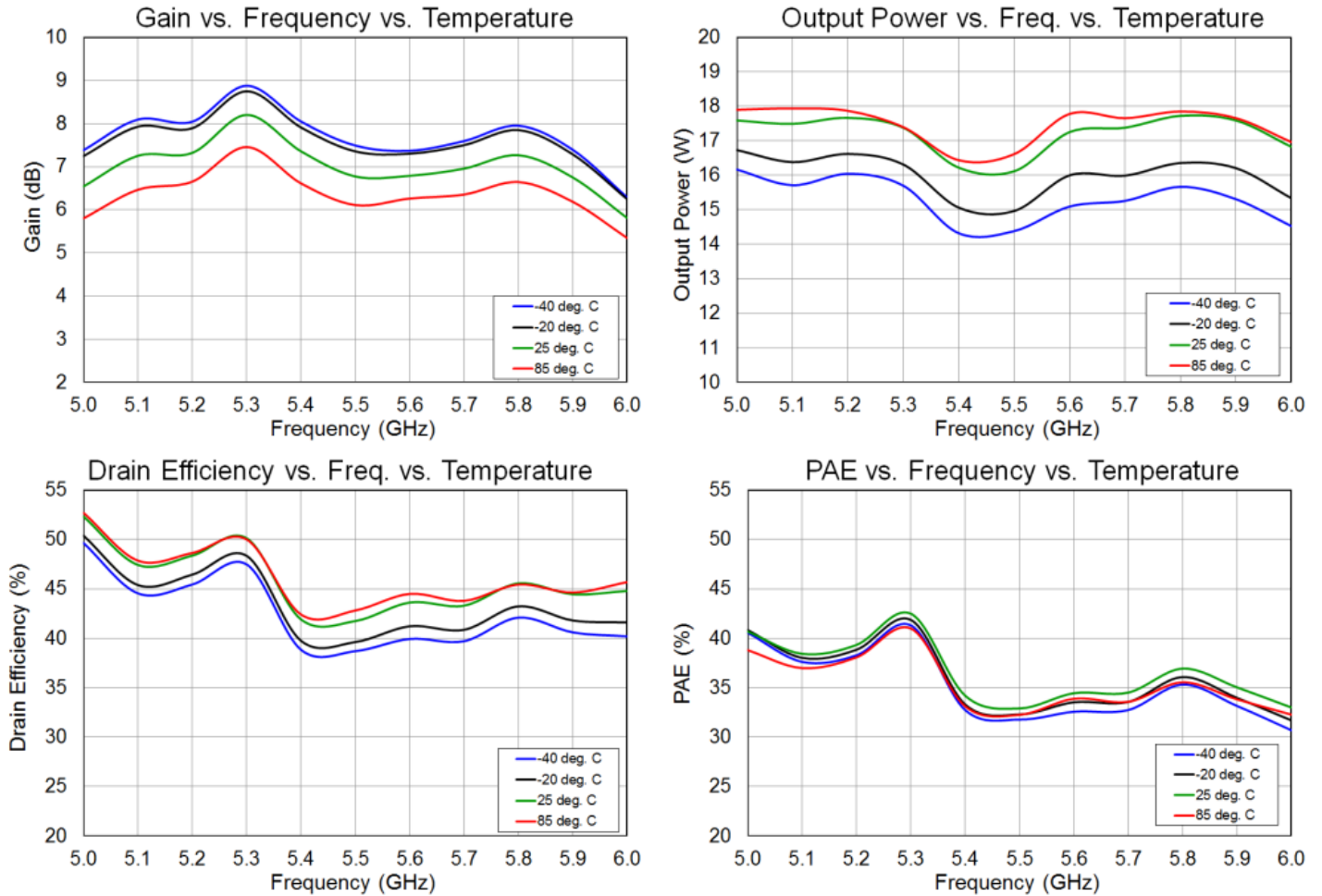
## Typical Performance

Performance is based on compromised impedance point and measured at DUT reference planes. See page 13.



### Performance Over Temperature<sup>(1,2)</sup>

Performance measured in Qorvo's 5.0 GHz to 6.0 GHz Evaluation Board at 3dB Compression.

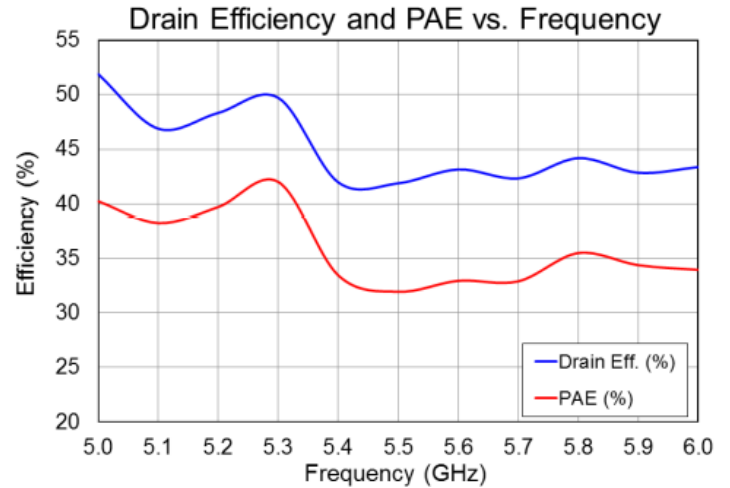
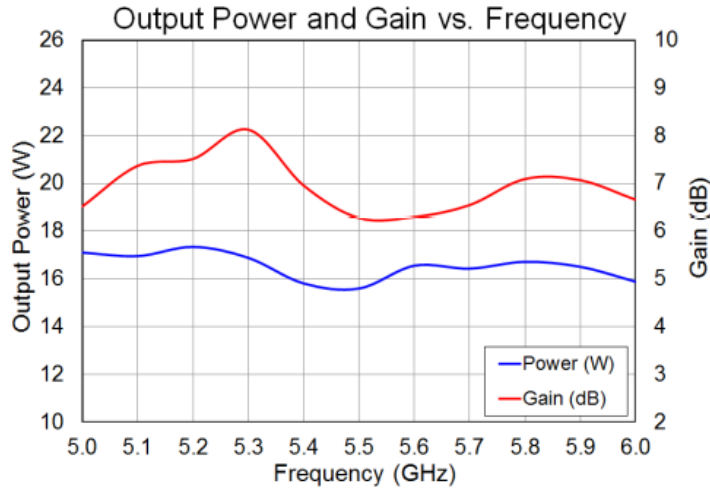


Note:

1. Test Conditions:  $V_{DS} = 28 \text{ V}$ ,  $I_{DQ} = 50 \text{ mA}$
2. Test Signal: Pulse Width = 100  $\mu\text{s}$ , Duty Cycle = 20%

### T2G6001528-Q3-EVB1 Performance Plots – 5.0 – 6.0 GHz Reference Design<sup>(1,2)</sup>

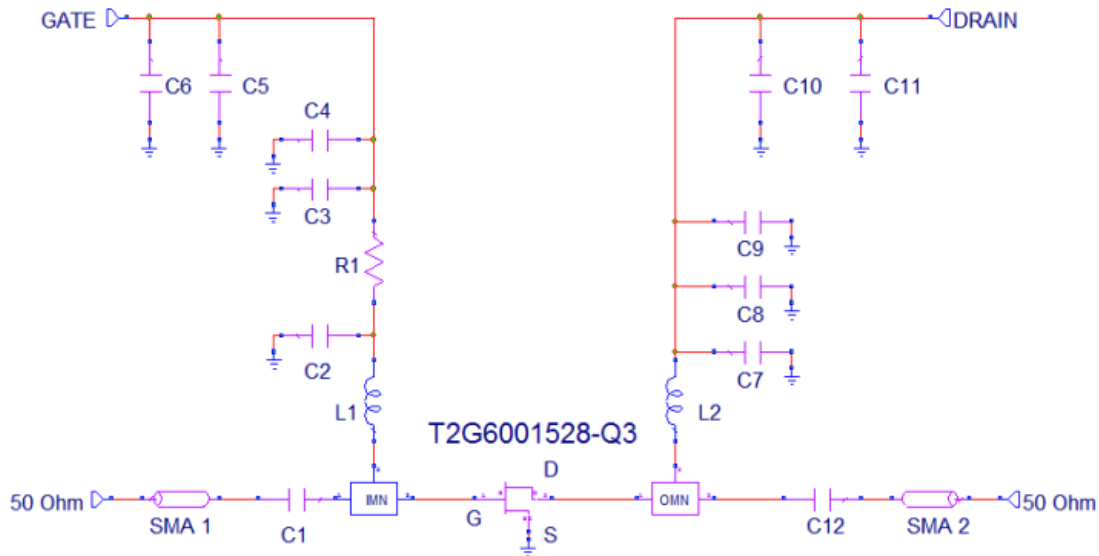
Performance at 3 dB Compression



Notes:

1. Test Conditions:  $V_{DS} = 28\text{ V}$ ,  $I_{DQ} = 50\text{ mA}$
2. Test Signal: Pulse Width =  $100\text{ }\mu\text{s}$ , Duty Cycle = 20%

### Application Circuit



### Biasing Procedure

#### Bias On

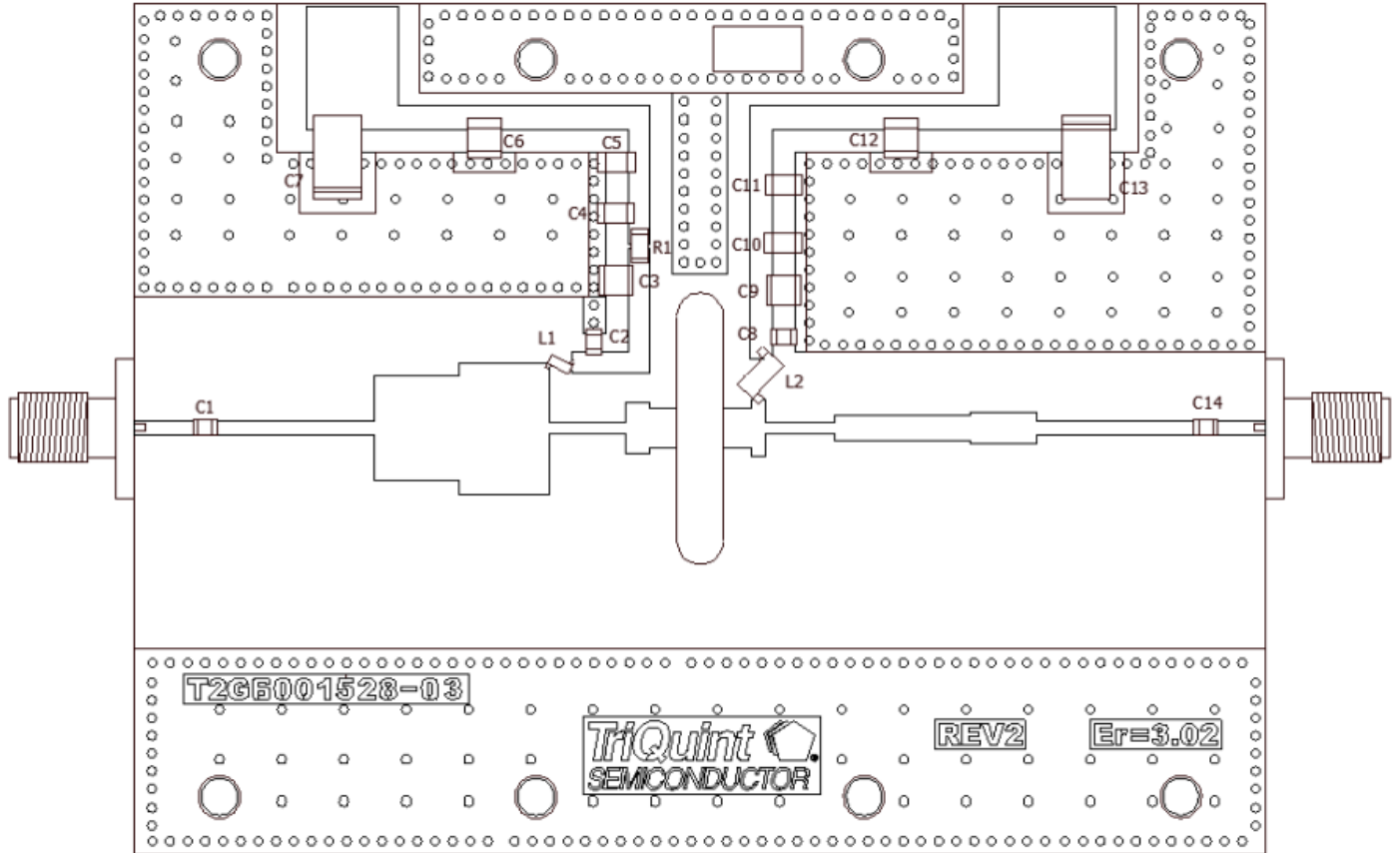
1. Turn ON  $V_G$  to  $-5\text{ V}$ .
2. Turn ON  $V_D$  to  $+28\text{ V}$ .
3. Slowly adjust  $V_G$  until  $I_D = 50\text{ mA}$ .
4. Turn ON RF.

#### Bias Off

1. Turn OFF RF.
2. Adjust  $V_G$  to  $-5\text{ V}$ .
3. Turn OFF  $V_D$ .
4. Wait two (2) seconds to allow drain capacitors to discharge.
5. Turn OFF  $V_G$ .

### T2G6001528-Q3EVB1 Layout – 5.0 – 6.0 GHz Reference Design

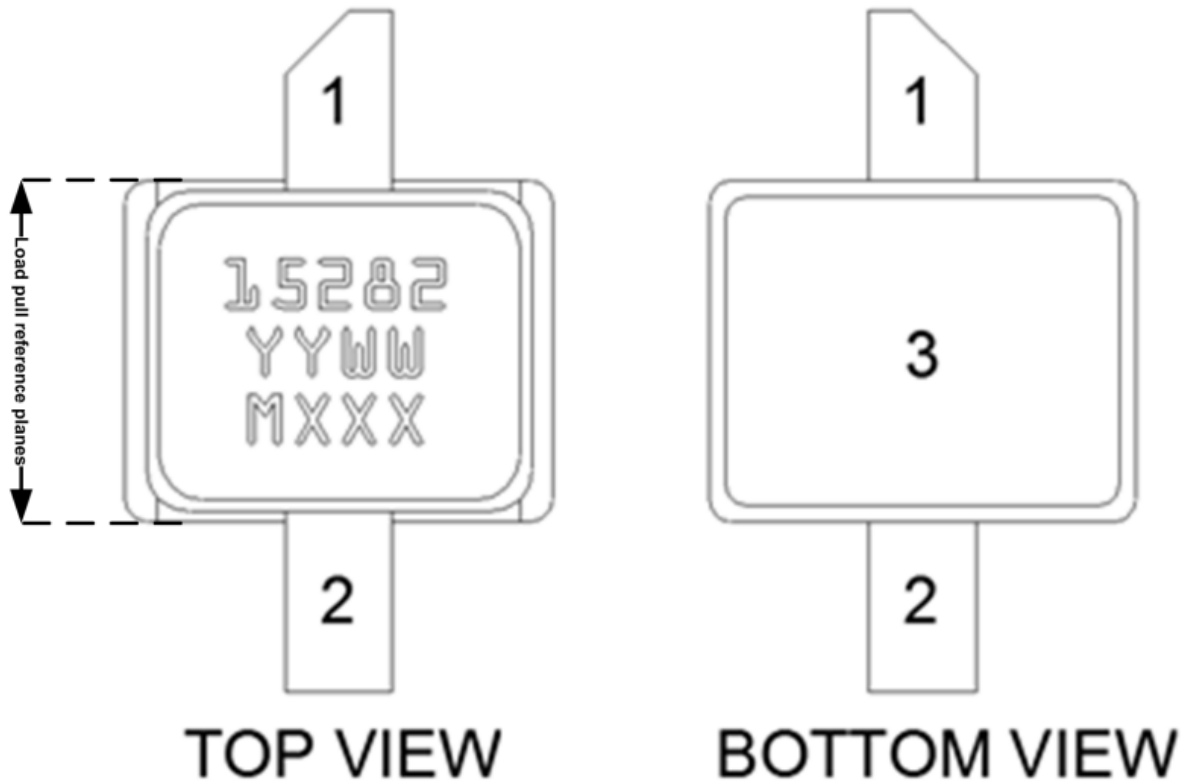
Top RF Layer is 0.020" thick Rogers RO3203,  $\epsilon_r = 3.02$ . The pad pattern shown has been developed and tested for optimized assembly at Qorvo Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances.



### T2G6001528-Q3EVB1 Bill of Materials – 5.0 – 6.0 GHz Reference Design

| Reference Des. | Value         | Description | Manuf.          | Part Number       |
|----------------|---------------|-------------|-----------------|-------------------|
| C1, C14        | 100 pF        | -           | ATC             | 100A101JW500XC    |
| C2, C8         | 2400 pF       | -           | Dielectric Labs | C08BL242X-5UN-XOB |
| C3, C9         | 100 pF        | -           | ATC             | 100B101GT500X     |
| C4, C10        | 0.01 $\mu$ F  | -           | Kemet           | C1206C103K1RACTU  |
| C5, C11        | 0.1 $\mu$ F   | -           | Kemet           | C1206C104K1RACTU  |
| C6, C12        | 1.0 $\mu$ F   | -           | AVX             | 1812C105KAT2A     |
| C7, C13        | 22 $\mu$ F    | -           | Sprague         | 226K035AT         |
| L1             | 5.4 nH        | -           | Coilcraft       | 0906-5JL          |
| L2             | 9.85 nH       | -           | Coilcraft       | 1606-9JLB         |
| R1             | 12.1 $\Omega$ | -           | Vishay          | CRC120612R1FKEA   |

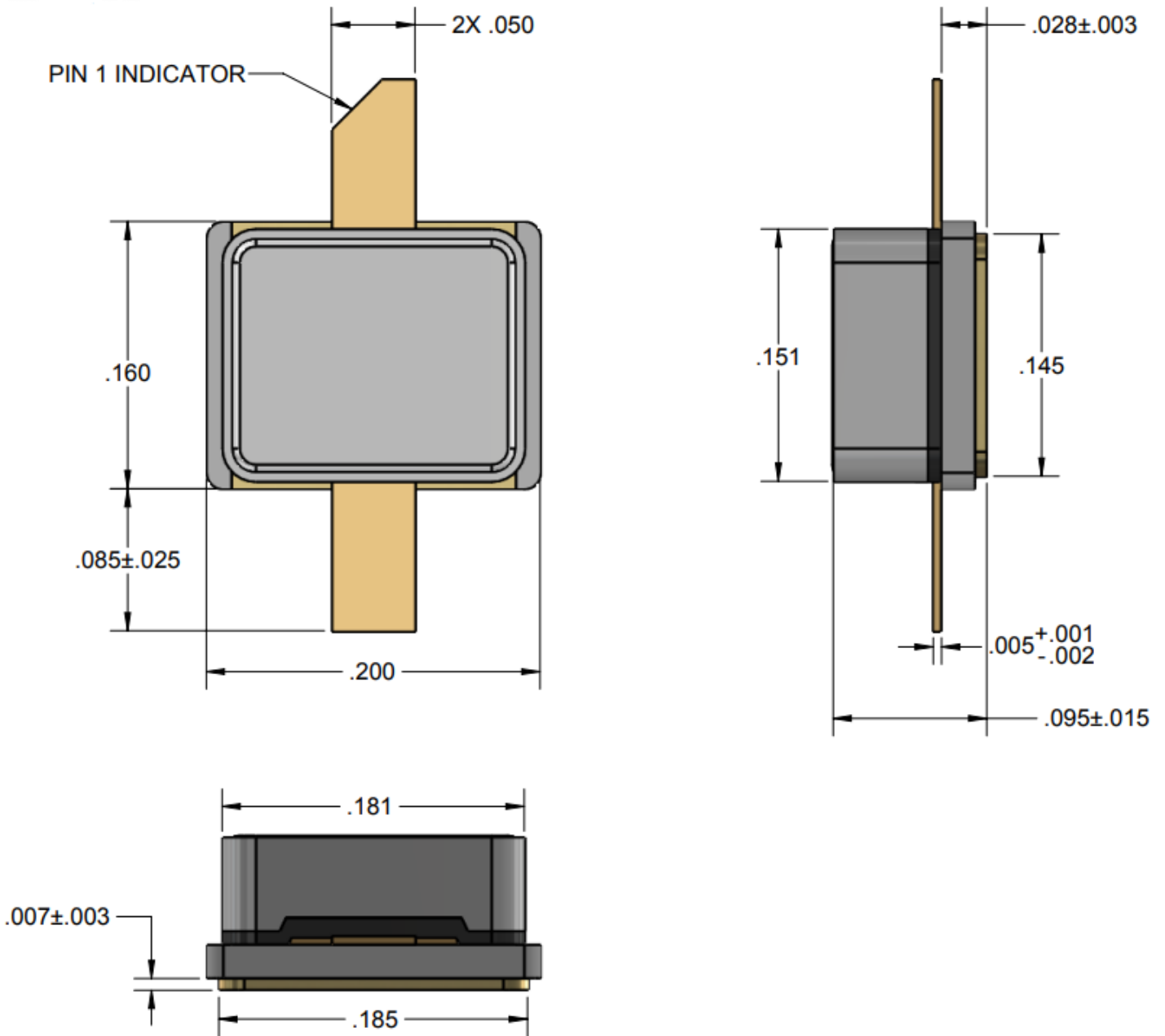
### Pin Configuration and Description<sup>(1)</sup>



| Pin Number | Label            | Description   |
|------------|------------------|---|
| 1          | $V_D / RF_{OUT}$ | Drain voltage / RF Output matched to 50 $\Omega$ ; see EVB Layout on page 10 as an example. |
| 2          | $V_G / RF_{IN}$  | Gate voltage / RF Input matched to 50 $\Omega$ ; see EVB Layout on page 10 as an example.   |
| 3          | Flange           | Source connected to ground; see EVB Layout on page 10 as an example.                        |

- Note:
- The T2G6001528-Q3 will be marked with the “15282” designator and a lot code marked below the part designator. The “YY” represents the last two digits of the calendar year the part was manufactured, the “WW” is the work week of the assembly lot start, and the “MXXX” is the production lot number.

Package Marking and Dimensions<sup>(1)</sup>



Notes:

1. Unless otherwise noted, tolerance is  $.XXX \pm .005$ ".
2. Material:  
Package Base: Ceramic/Metal  
Package Lid: Ceramic
3. Package exposed metallization is gold plated.
4. Part is epoxy sealed.
5. Parts meet industry NI-200 footprint
6. Body dimensions do not include lid shift or epoxy run out which can be up to 20 mils per side.

### Recommended Solder Temperature Profile

