# T2G6003028-FS

**30 W, 28V DC – 6 GHz, GaN RF Power Transistor**

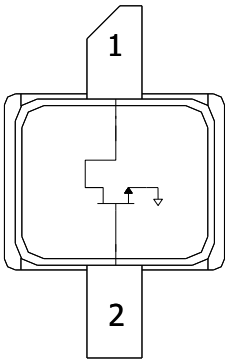
## Product Overview

The Qorvo T2G6003028-FS is a 30W ($P_{3dB}$) discrete GaN on SiC HEMT which operates from DC to 6 GHz. The device is constructed with Qorvo's proven QGaN25 process, which features advanced field plate techniques to optimize power and efficiency at high drain bias operating conditions. This optimization can potentially lower system costs in terms of fewer amplifier line-ups and lower thermal management costs.

Lead-free and ROHS compliant

Evaluation boards are available upon request.


## Functional Block Diagram




## Key Features [1]

- Frequency: DC to 6 GHz
- Output Power ($P_{3dB}$): 42.7 W
- Linear Gain: >14 dB
- Operating Voltage: 28 V
- Low thermal resistance package
- Pulse capable

Note 1: @ 3 GHz

## Applications

- Military radar
- Civilian radar
- Professional and military radio communications
- Test instrumentation
- Wideband or narrowband amplifiers
- Jammers

## Pin Configuration

| Pin No. | Label |
|---|---|
| 1 | $V_D$ / RF OUT |
| 2 | $V_G$ / RF IN |
| 3 | Flange/Source |

## Ordering info

| Part No. | Description |
|---|---|
| T2G6003028-FS | Packaged part<br>Flangeless |
| T2G6003028-FSEVB | 5.4 – 5.9 GHz<br>Evaluation Board |
| T2G6003028-FSEVB2 | 1.3 – 1.9 GHz Evaluation Board |

## Absolute Maximum Ratings

| Parameter | Rating | Units |
|---|---|---|
| Breakdown Voltage, $BV_{DG}$ | 100 | V |
| Gate Voltage Range, $V_G$ | -7 to +2 | V |
| Drain Current, $I_{DMAX}$ | 5.5 | A |
| Gate Current Range, $I_G$ | -10 to 28 | mA |
| Power Dissipation, Pulsed, $P_{DISS}$ [2] | 47.5 | W |
| RF Input Power, CW, T = 25°C ($P_{IN}$) | 40 | dBm |
| Channel Temperature ($T_{CH}$) | 275 | °C |
| Mounting Temperature (30 Seconds) | 320 | °C |
| Storage Temperature | −40 to +150 | °C |

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

## Recommended Operating Conditions [1, 2]

| Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|
| Drain Voltage Range, $V_D$ | 12 | | 40 | V |
| Drain Bias Current, $I_{DQ}$ | | 200 | | mA |
| Gate Voltage, $V_G$ | – | −3.0 | – | V |

## Electrical Specifications [1, 2]

| Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|
| Linear Gain, $G_{LIN}$ | 12 | 14 | – | dB |
| Output Power at 3dB compression point, P3dB | 43.0 | 44.6 | – | W |
| Drain Efficiency at 3dB compression point, DEFF3dB | 45.0 | 54.0 | – | % |
| Gain at 3dB compression point, G3dB | 9.0 | 11.0 | – | dB |
| Gate Leakage ($V_D$ = +10 V, $V_G$ = −3.7 V) | -11 | – | – | mA |

Notes:
1. Performance at 5.6 GHz in the 5.4 to 5.9 GHz Evaluation Board
2. $V_{DS}$ = 28 V, $I_{DQ}$ = 200 mA; Pulse: 100µs, 20%

## RF Characterization – Mismatch Ruggedness at 5.6 GHz [1]

| Symbol | Parameter | dB Compression | Typical |
|---|---|---|---|
| VSWR | Impedance Mismatch Ruggedness | 3 | 10:1 |

Notes:
1. $P_{1dB}$ CW Input Power under matched condition.

## Power-Matched Load Pull Performance

Test conditions unless otherwise noted: T = 25°C.

| Parameter | Typical Value | | | | | | Units |
|---|---|---|---|---|---|---|---|
| Frequency (F) | 1 | 2 | 3 | 4 | 5 | 6 | GHz |
| Drain Voltage ($V_D$) | 28 | 28 | 28 | 28 | 28 | 28 | V |
| Bias Current ($I_{DQ}$) | 200 | 200 | 200 | 200 | 200 | 200 | mA |
| Output P3dB ($P_{3dB}$) | 45.7 | 46 | 46.3 | 46.5 | 46.8 | 46.2 | dBm |
| PAE @ $P_{3dB}$ ($PAE_{3dB}$) | 64.9 | 64.2 | 68.1 | 54.6 | 55.9 | 54.7 | % |
| Gain @ P3dB ($G_{3dB}$) | 19.9 | 15.7 | 11.3 | 10.1 | 10.7 | 12.1 | dB |

Notes:

1. $V_D$ = 28 V, $I_{DQ}$ = 200 mA, Pulse Width = 100 uS, Duty Cycle = 20%
2. Characteristic Impedance ($Z_o$) = 10 Ω. See pg. 14 for Load Pull Reference Planes.

## Efficiency-Matched Load Pull Performance

Test conditions unless otherwise noted: T = 25°C.

| Parameter | Typical Value | | | | | | Units |
|---|---|---|---|---|---|---|---|
| Frequency (F) | 1 | 2 | 3 | 4 | 5 | 6 | GHz |
| Drain Voltage ($V_D$) | 28 | 28 | 28 | 28 | 28 | 28 | V |
| Bias Current ($I_{DQ}$) | 200 | 200 | 200 | 200 | 200 | 200 | mA |
| Output P3dB ($P_{3dB}$) | 43.1 | 43.1 | 44.6 | 44.1 | 44.9 | 45.7 | dBm |
| PAE @ $P_{3dB}$ ($PAE_{3dB}$) | 73 | 76 | 46.1 | 65.1 | 69.5 | 60 | % |
| Gain @ P3dB ($G_{3dB}$) | 19.7 | 16.2 | 11.7 | 10.8 | 12.4 | 12.9 | dB |

Notes:

1. $V_D$ = 28 V, $I_{DQ}$ = 200 mA, Pulse Width = 100 uS, Duty Cycle = 20%.
2. Characteristic Impedance ($Z_o$) = 10 Ω. See pg. 14 for Load Pull Reference Planes.

## Thermal Information – CW [1, 2]

| Parameter | Test Conditions | Value | Units |
|---|---|---|---|
| Thermal Resistance, IR² ($\theta_{JC}$) | $P_D$ = 30 W, Tbase = 85°C | 2.51 | °C/W |
| Maximum Channel Temperature, $T_{CH}$ | | 160.65 | °C |
| Thermal Resistance, IR² ($\theta_{JC}$) | $P_D$ = 35 W, Tbase = 85°C | 2.58 | °C/W |
| Maximum Channel Temperature, $T_{CH}$ | | 175.20 | °C |
| Thermal Resistance, IR² ($\theta_{JC}$) | $P_D$ = 40 W, Tbase = 85°C | 2.67 | °C/W |
| Maximum Channel Temperature, $T_{CH}$ | | 191.68 | °C |
| Thermal Resistance, IR² ($\theta_{JC}$) | $P_D$ = 45 W, Tbase = 85°C | 2.75 | °C/W |
| Maximum Channel Temperature, $T_{CH}$ | | 208.73 | °C |

Notes:
1. Thermal resistance calculated to bottom of package.
2. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

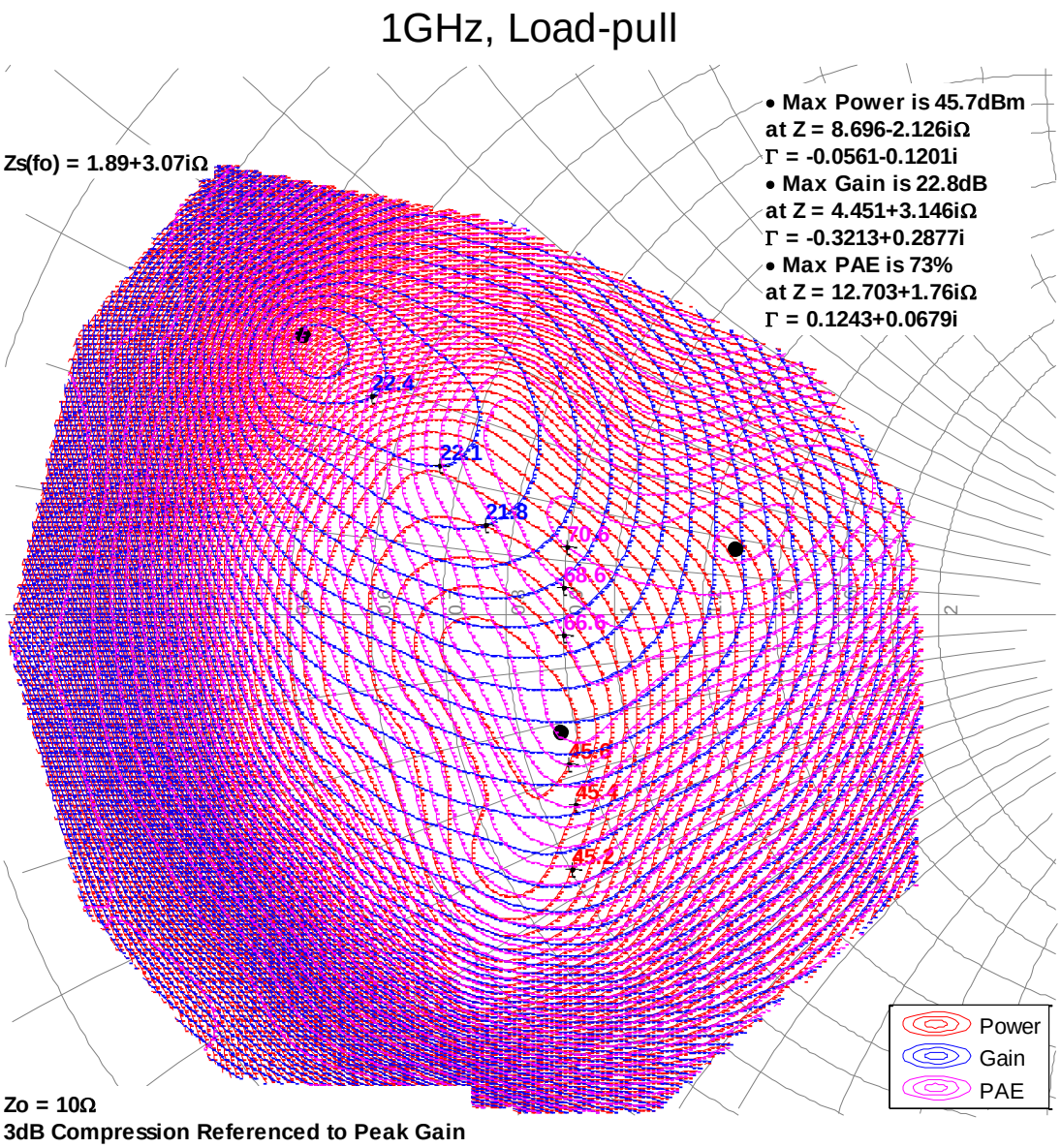
## Thermal Information – Pulsed [1, 2]

| Parameter | Test Conditions | Value | Units |
|---|---|---|---|
| Thermal Resistance, IR² ($\theta_{JC}$) | $P_D$ = 40 W, Tbase = 85°C<br>Pulse Width = 100 uS<br>Duty Cycle = 5% | 1.56 | °C/W |
| Peak Channel Temperature,$T_{CH}$ | | 147.37 | °C |
| Thermal Resistance, IR² ($\theta_{JC}$) | $P_D$ = 40 W, Tbase = 85°C<br>Pulse Width = 100 uS<br>Duty Cycle = 10% | 1.62 | °C/W |
| Peak Channel Temperature, $T_{CH}$ | | 149.83 | °C |
| Thermal Resistance, IR² ($\theta_{JC}$) | $P_D$ = 40 W, Tbase = 85°C<br>Pulse Width = 100 uS<br>Duty Cycle = 20% | 1.77 | °C/W |
| Peak Channel Temperature, $T_{CH}$ | | 155.89 | °C |
| Thermal Resistance, IR² ($\theta_{JC}$) | $P_D$ = 40 W, Tbase = 85°C<br>Pulse Width = 100 uS<br>Duty Cycle = 50% | 2.07 | °C/W |
| Peak Channel Temperature, $T_{CH}$ | | 167.69 | °C |

Notes:
1. Thermal resistance calculated to bottom of package.
2. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

## Load Pull Contours [1, 2, 3]

Notes:
1. Test Conditions: $V_{DS}$ = 28 V, $I_{DQ}$ = 200 mA
2. Test Signal: Pulse Width = 100 µsec, Duty Cycle = 20%
3. See pg. 14 for load pull reference planes.



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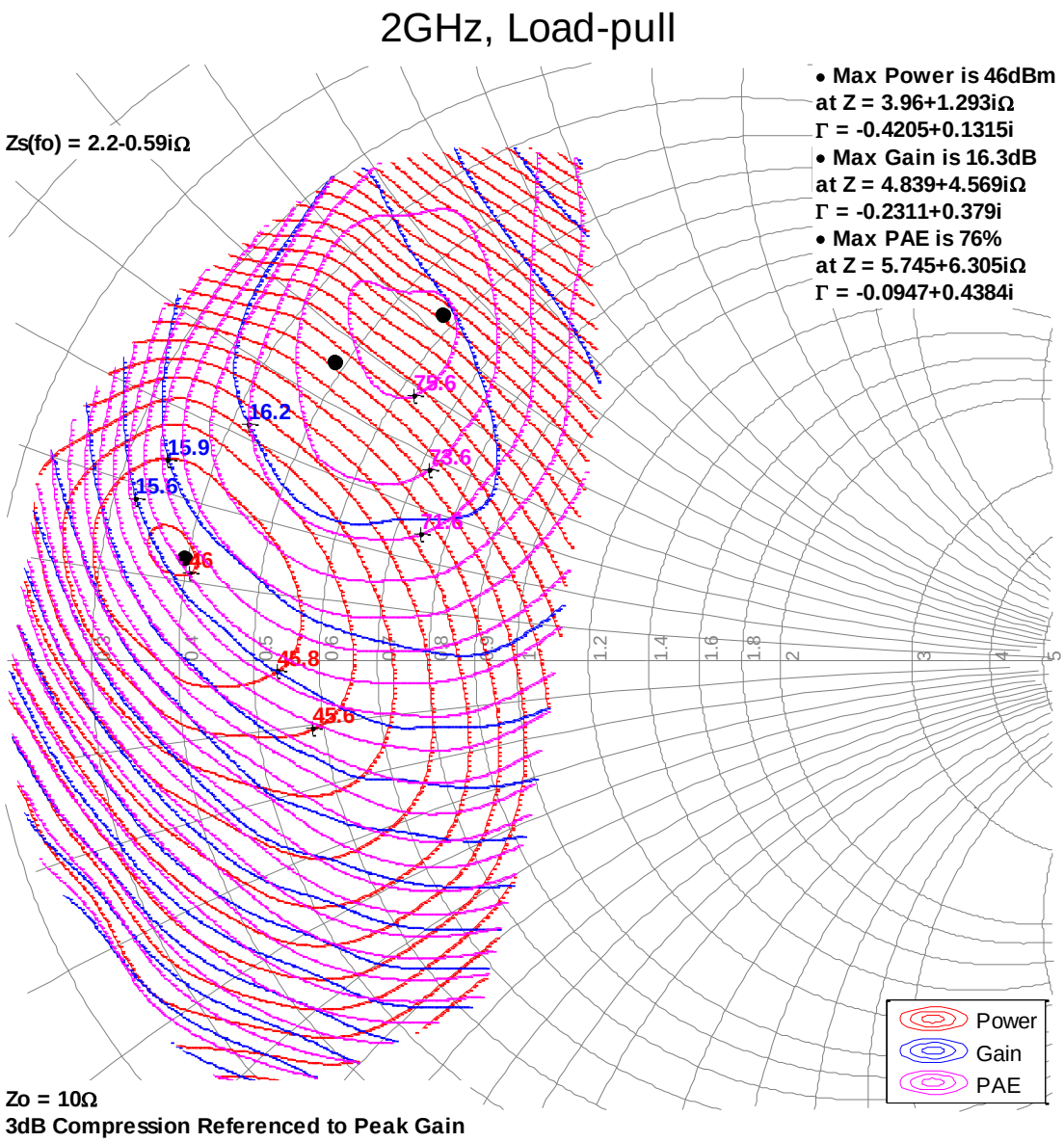

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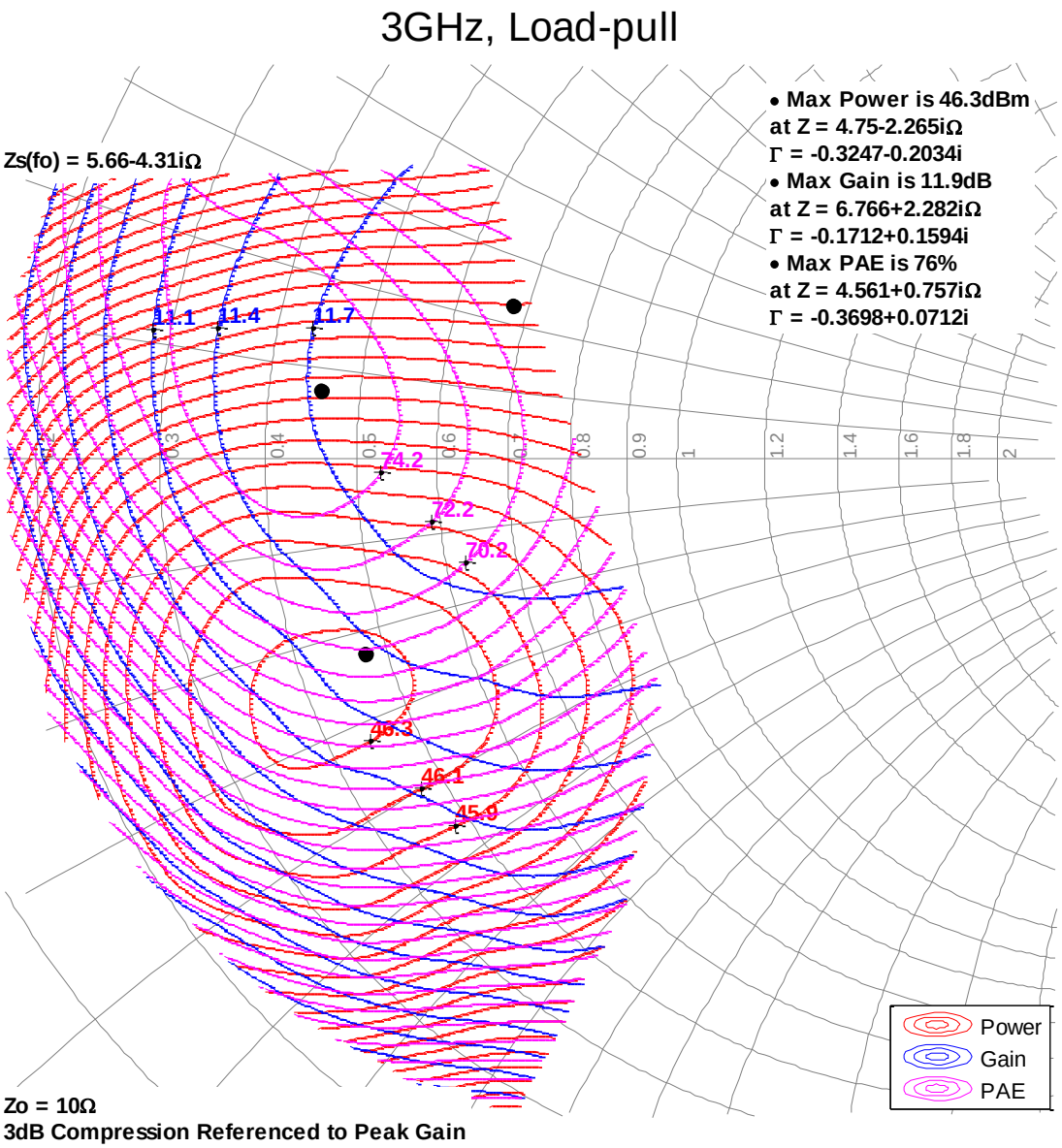

## Load Pull Contours [1, 2, 3]

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2. Test Signal: Pulse Width = 100 µsec, Duty Cycle = 20%
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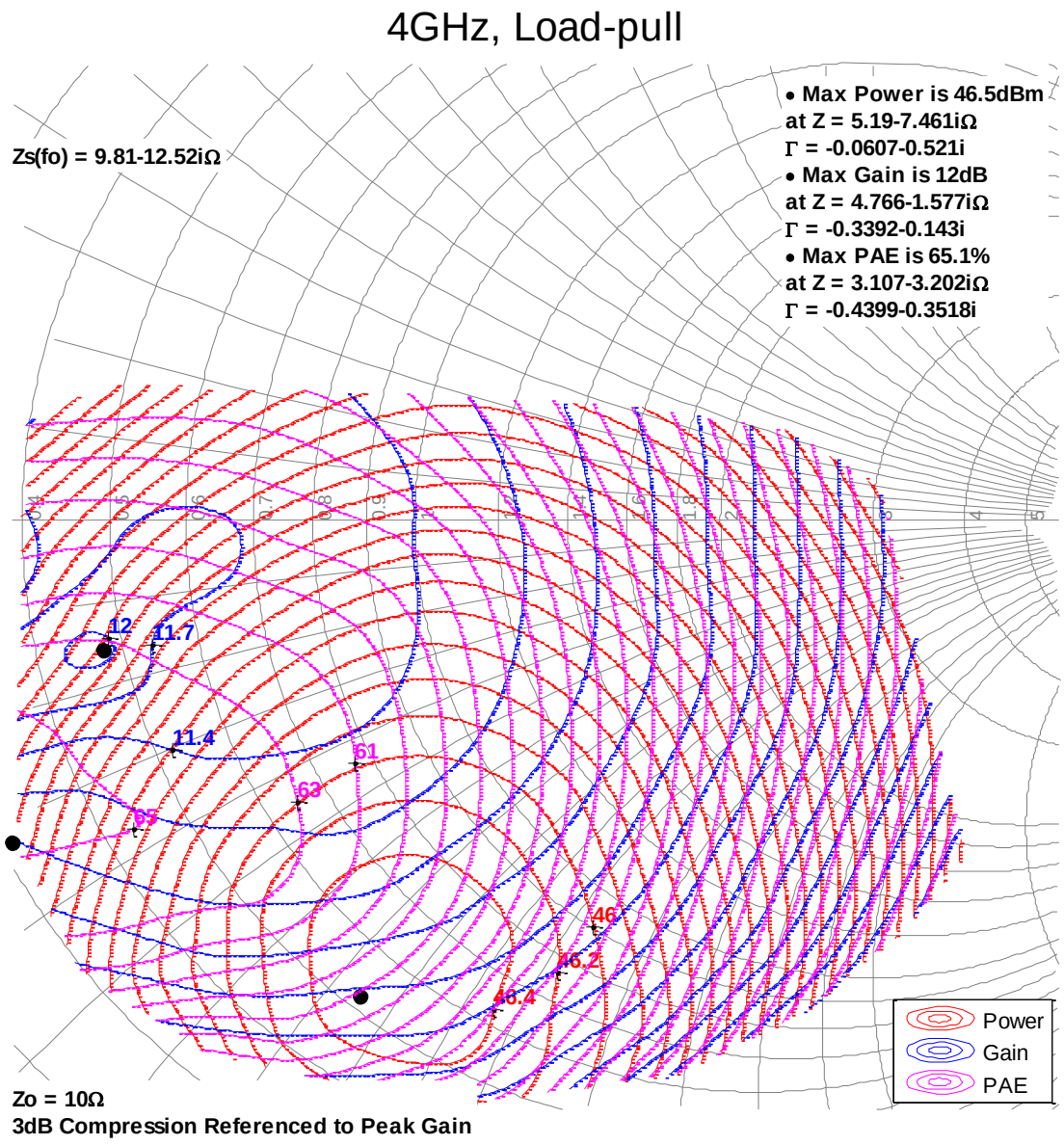

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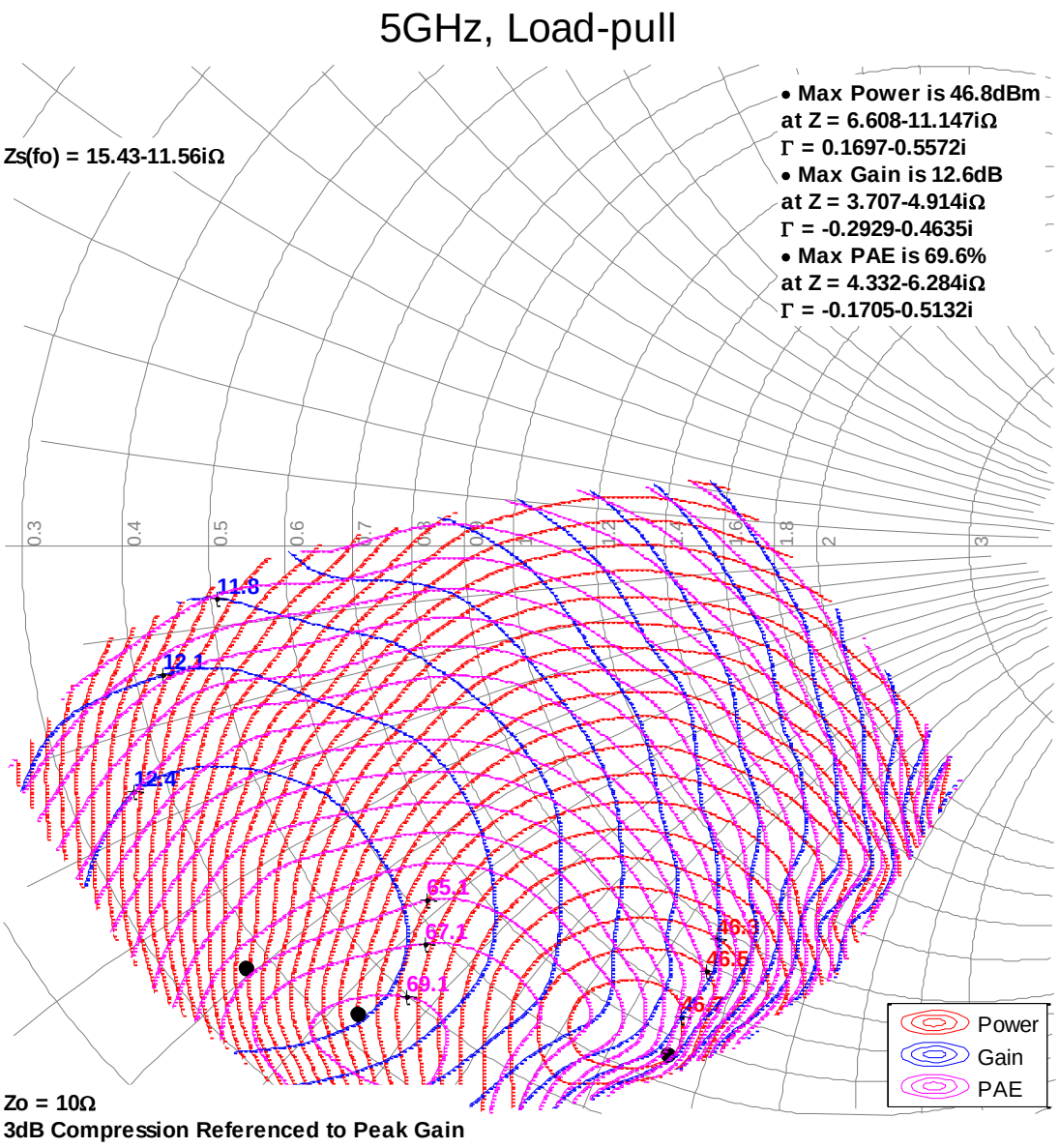

## Load Pull Contours [1, 2, 3]

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2. Test Signal: Pulse Width = 100 µsec, Duty Cycle = 20%
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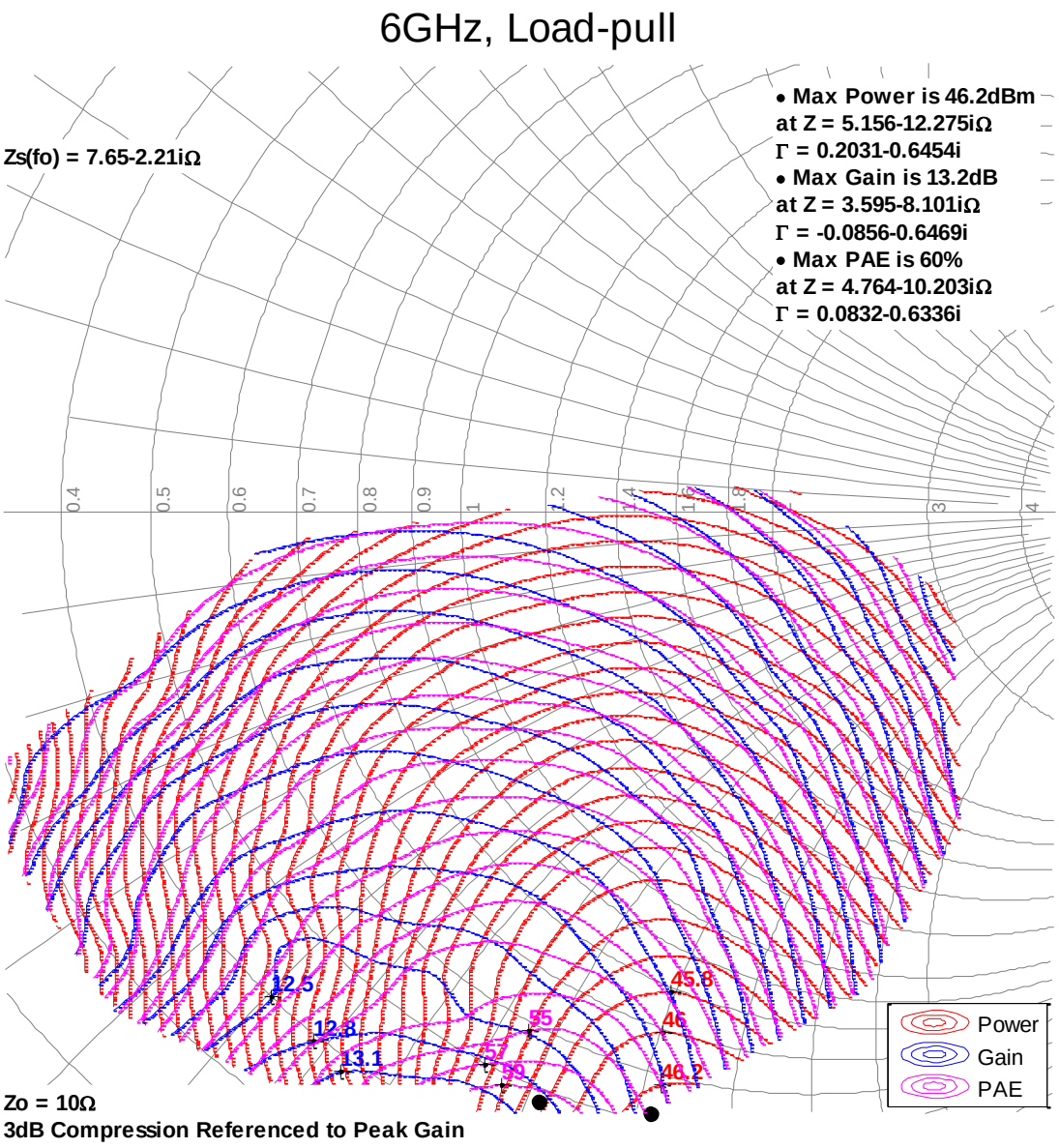
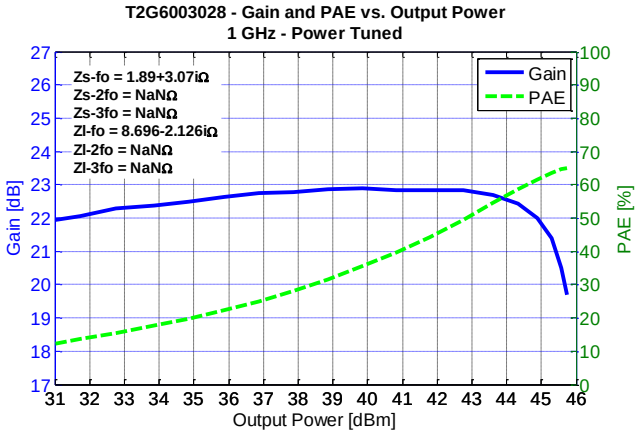
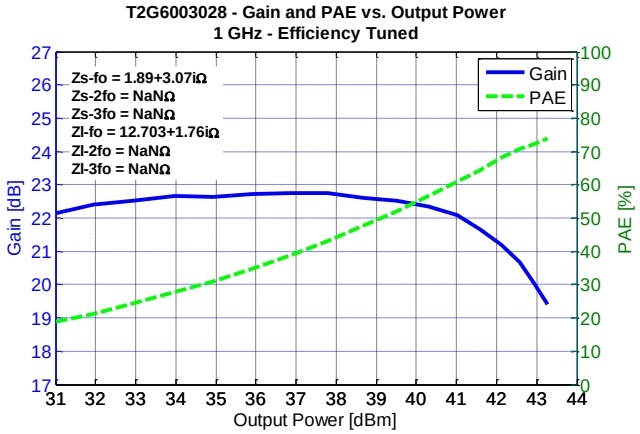


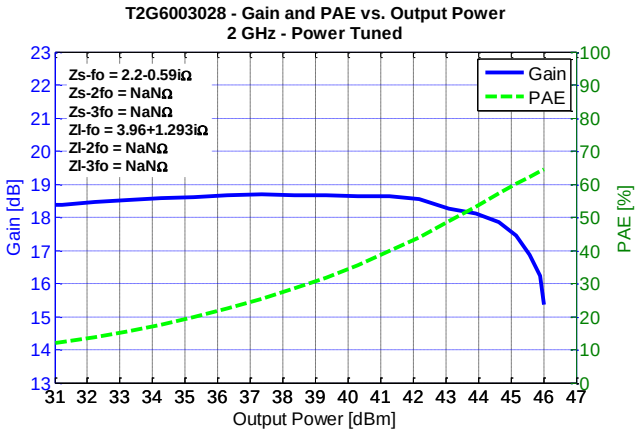
## Load Pull Drive-up [1, 2]

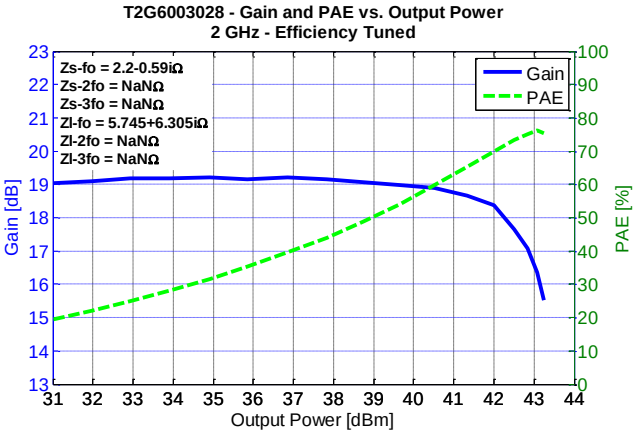
Notes:

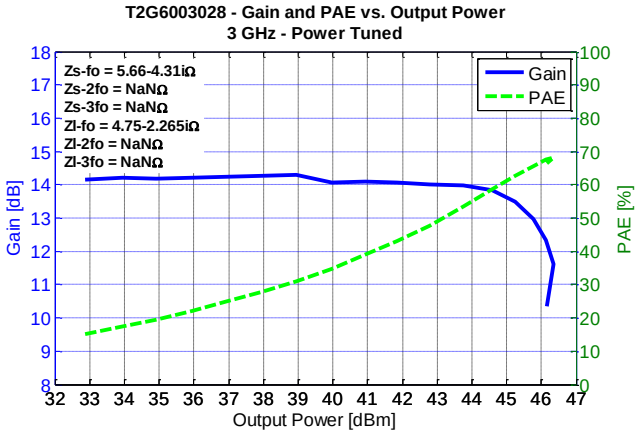
1. Vd = 28 V, Idq = 200 mA, Pulse Width = 100 uS, Duty Cycle = 20%
2. NaN means the parameter is either unavailable or undefined.

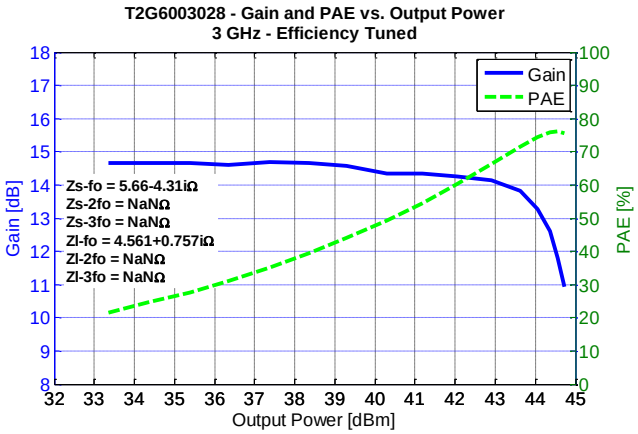


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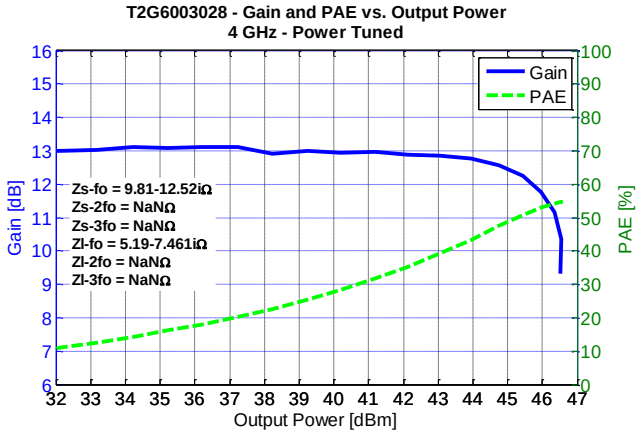
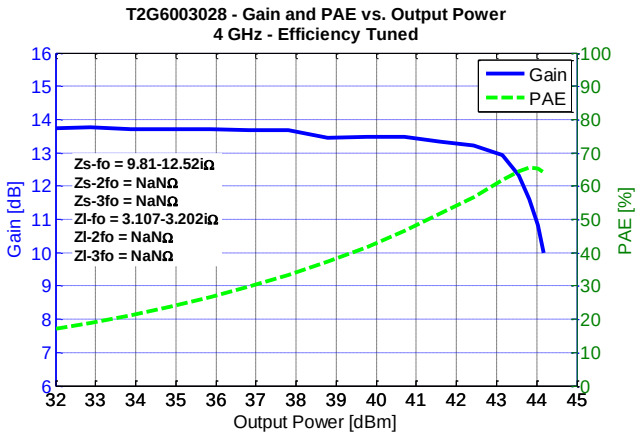
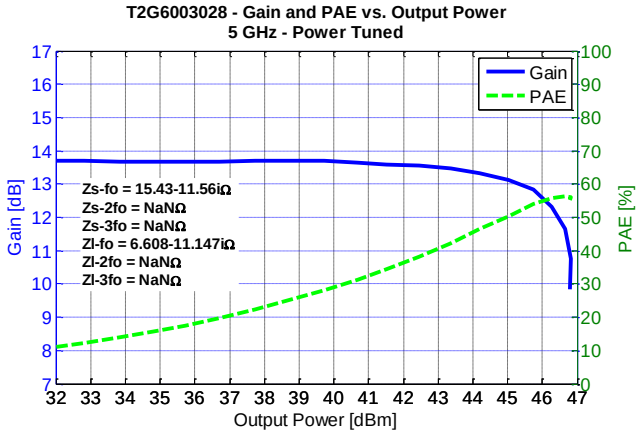
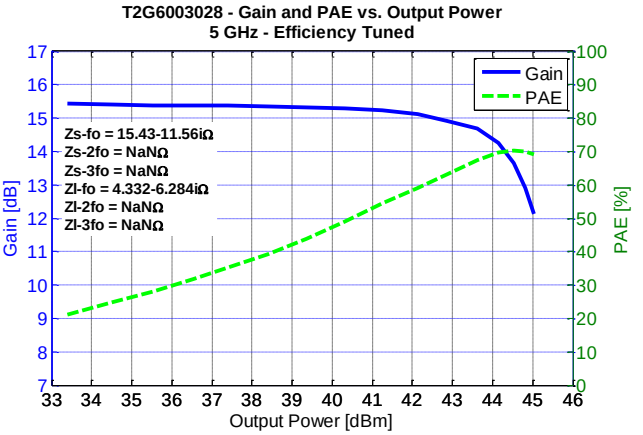
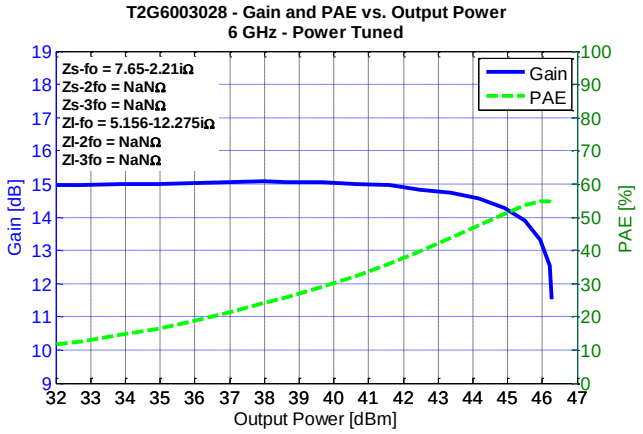
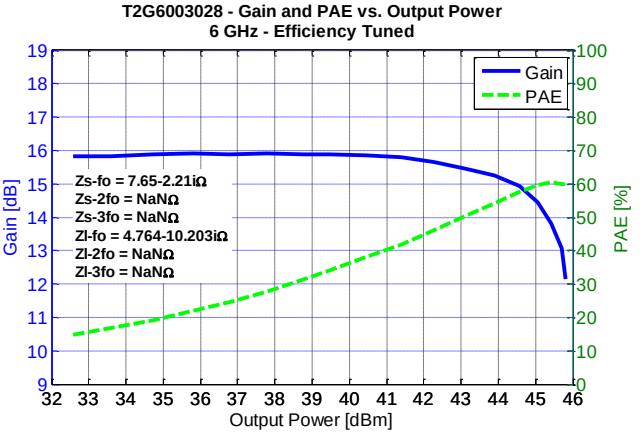


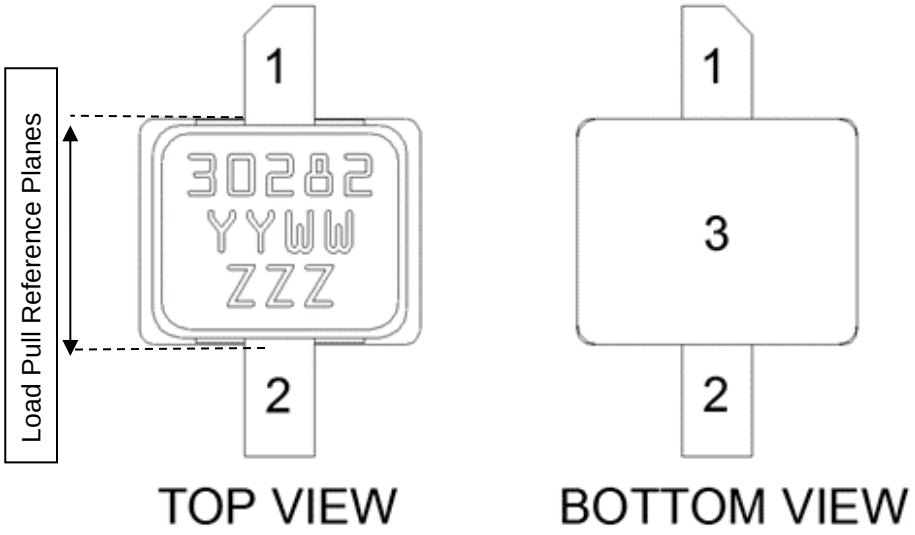



## Package Marking and Pin Configuration [1]

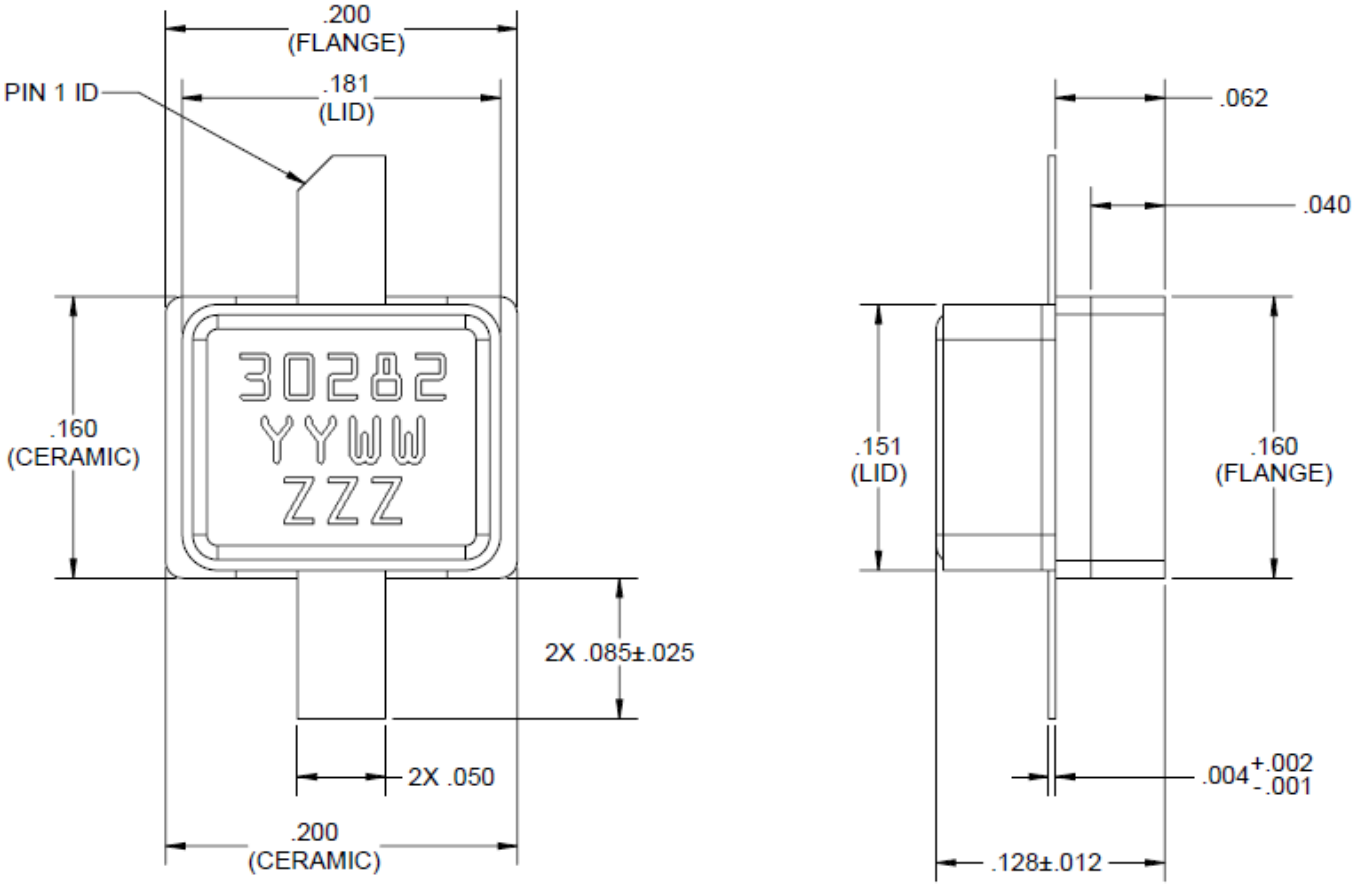



Note:
The T2G6003028-FS will be marked with the “30282” designator and a lot code marked below the part designator. The “YY” represents the last two digits of the calendar year the part was manufactured, the “WW” is the work week of the assembly lot start, and the “ZZZ” is an auto-generated number.

| Pin | Symbol | Description |
|---|---|---|
| 1 | $V_D$ / RF OUT | Drain voltage / RF Output matched to 50 ohms; see EVB Layout on page 17 as an example. |
| 2 | $V_G$ / RF IN | Gate voltage / RF Input matched to 50 ohms; see EVB Layout on page 17 as an example. |
| 3 | Flange | Source connected to ground; see EVB Layout on page 17 as an example. |

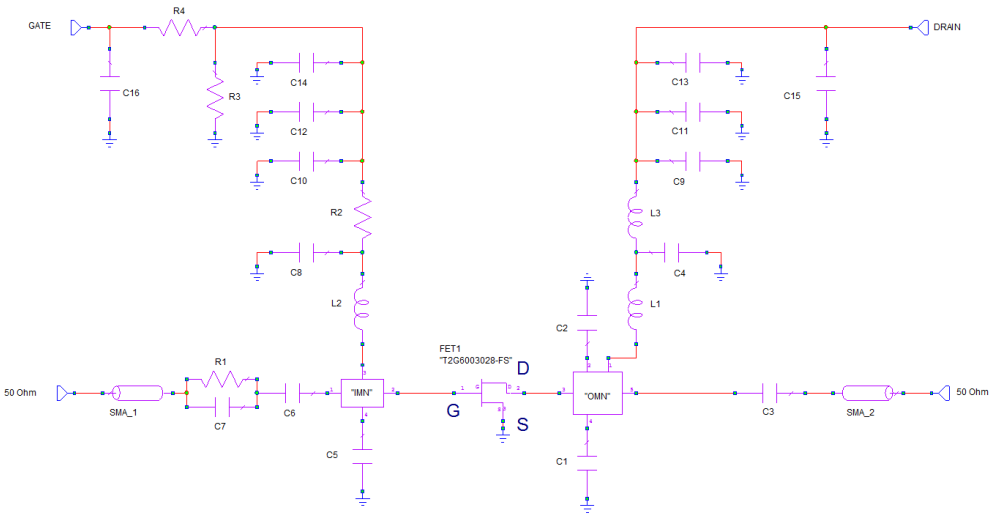
Notes:
Thermal resistance measured to bottom of package

## Package Dimensions




Notes:
1. Material:
   Package Base: Ceramic/Metal
   Package Lid: Ceramic
2. Package exposed matellization is gold plated
3. Part is epoxy sealed
4. Part meets industry NI200 footprint
5. Body dimensions do not include lid shift or epoxy run out which can be up to 0.020 per side.
6. Dimensions are in inches. General tolerance is ±0.005”.

## Application Circuit

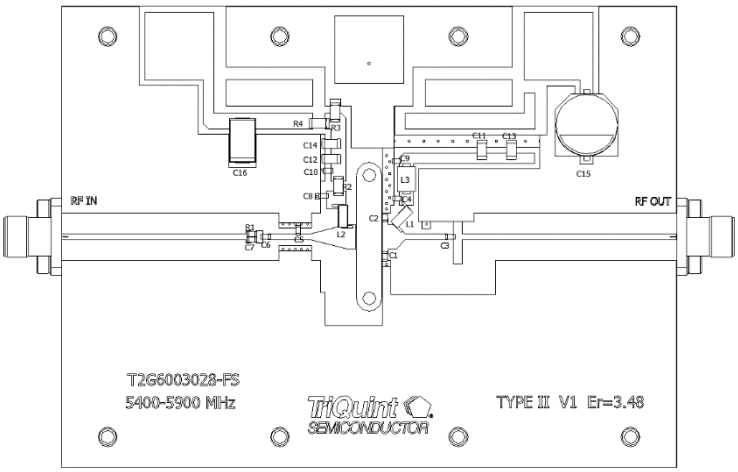



## Bias Procedure

| Bias-up Procedure | Bias-down Procedure |
|---|---|
| 1. Set $V_G$ to -5 V. | 1. Turn off RF signal. |
| 2. Set $I_D$ current limit to 220 mA. | 2. Turn off $V_D$ |
| 3. Apply 28 V $V_D$. | 3. Wait 1 seconds to allow drain capacitor to discharge. |
| 4. Slowly adjust $V_G$ until $I_D$ is set to 200 mA. | 4. Turn off $V_G$ |
| 5. Set $I_D$ to 2.8 A. | |
| 6. Apply RF signal | |

## 5.4 – 5.9 GHz Evaluation Board– Layout [1, 2, 3]

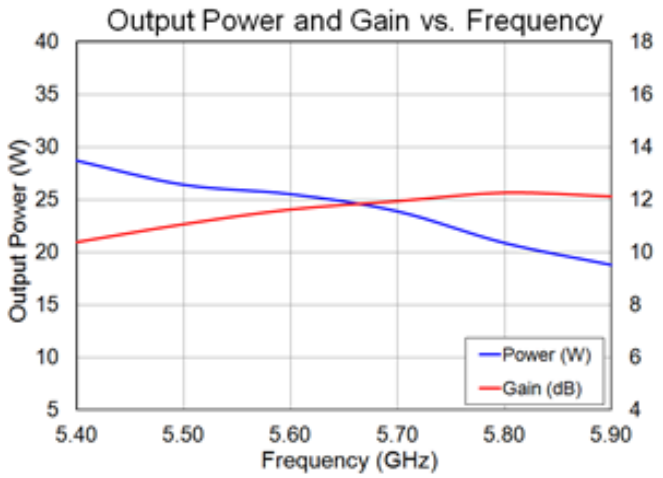
Notes:
1. Top RF layer is 0.020” thick Rogers RO4350B, $\varepsilon_r$ = 3.48
2. The pad pattern shown has been developed and tested for optimized assembly at Qorvo Semiconductor.
3. The PCB land pattern has been developed to accommodate lead and package tolerances

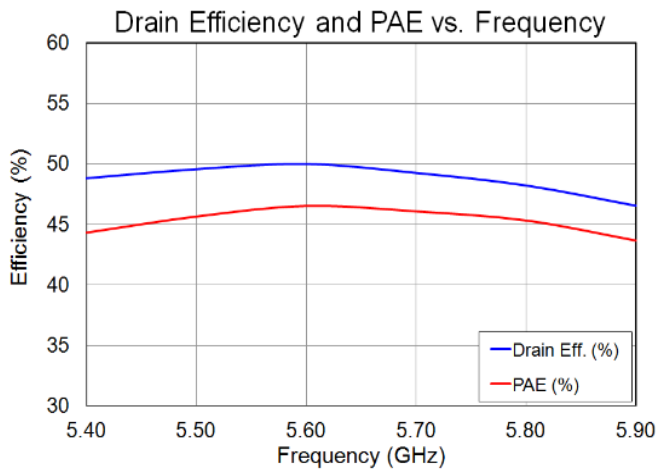



## 5.4 – 5.9 GHz Application Circuit – Bill of Materials EVB1

| Ref Des | Qty | Description | Mfg Name | Mfg Part # |
|---|---|---|---|---|
| C1 | 1 | 0.3 pF | ATC | ATC600S0R3 |
| C2 | 1 | 0.2 pF | ATC | ATC600S0R2 |
| L1, L2 | 2 | 8.8 NH | COILCRAFT | 1606-8 |
| C3, C4, C6, C7, C8 | 5 | 3 pF | ATC | ATC600S3R0 |
| C5 | 1 | 0.4 pF | ATC | ATC600S0R5 |
| R1 | 1 | 97.6 Ohms | Venkel | CR0604-16w-97R6FT |
| R2 | 1 | 4.7 Ohms | Newark | 37C0064 |
| R3 | 1 | 330 Ohms | Newark | TNPW1206330RBT9ET1-E3 |
| R4 | 1 | 50 Ohms | ATC | CRCW120651R0FKEA |
| C9, C10 | 2 | 220 pF | AVX | AVX06035C22KAT2A |
| C11, C12 | 2 | 2200 pF | Vitramon | VJ1206Y222KXA |
| C13, C14 | 2 | 22000 pF | Vitramon | VJ1206Y223KXA |
| C15 | 1 | 220 uF | United Chemi-Con | EMVY500ADA221MJA0G |
| C16 | 1 | 1.0 uF | Allied | 541-1231 |
| L3 | 1 | 48 Ohm | Ferrite, Laird Tech. | 28F0121-0SR-10 |

## Evaluation Board Performance [1, 2, 3]



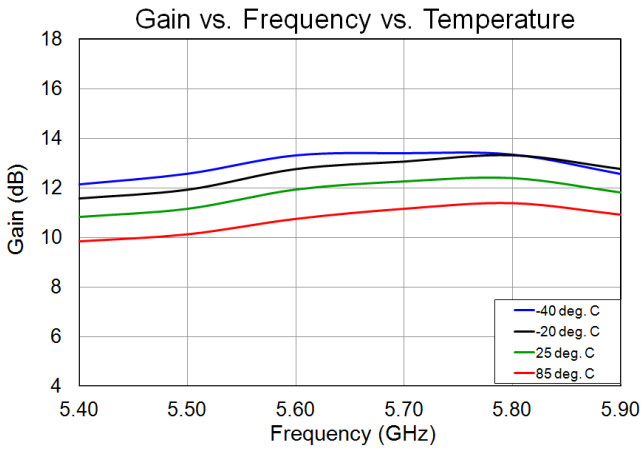



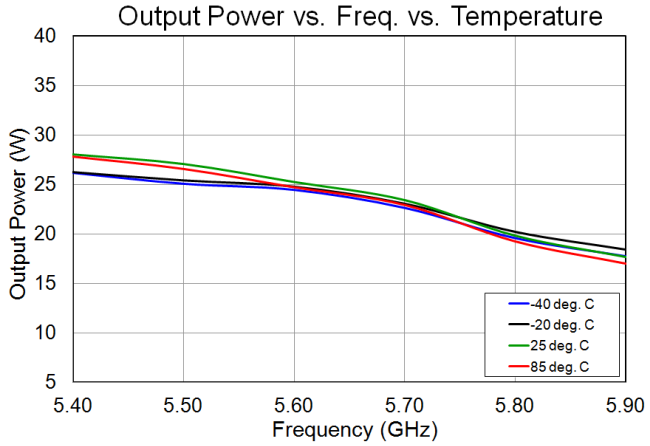

Notes:

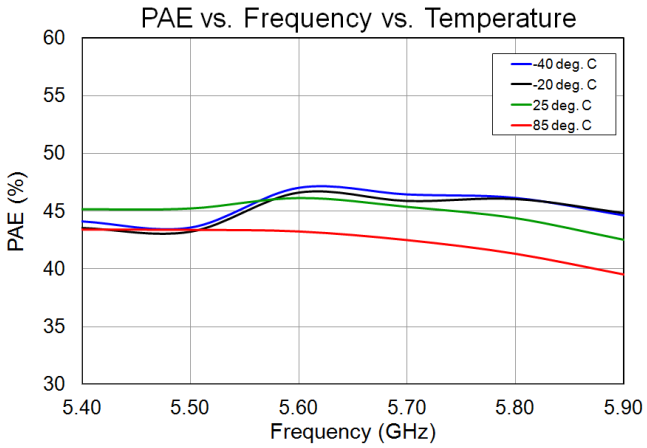
1. Test Conditions: $V_{DS}$ = 28 V, $I_{DQ}$ = 200 mA
2. Test Signal: Pulse Width = 100 µs, Duty Cycle = 20 %
3. Performance at 3dB compression.

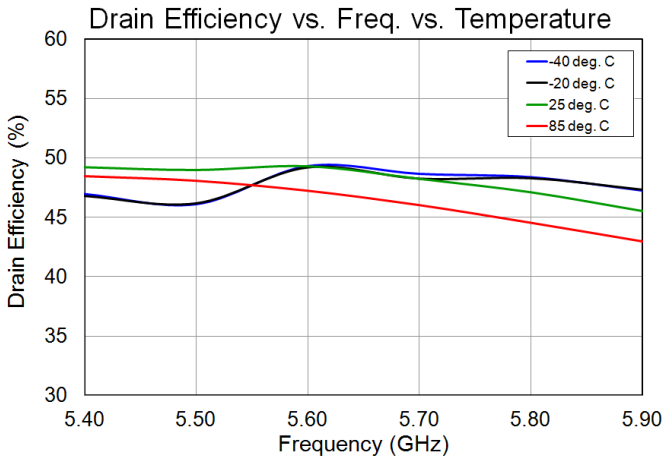
## Performance over Temperatures of 5.4 – 5.9 GHz EVB [1, 2]

Notes:
1. Test Conditions: $V_D$ = 28 V, $I_{DQ}$ = 200 mA, 100 us Pulse Width, 20% Duty Cycle.
2. Performance at 3dB compression.



## Recommended Solder Temperature Profile