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T4160

QorIQ T4160/T4080 Data Sheet

Features

- Eight e6500 cores built on Power Architecture® technology and arranged as clusters of four e6500 cores sharing a 2 MB L2 cache (one cluster of four e6500 cores on T4080)
- 1.0 MB CoreNet platform cache (CPC)
- Hierarchical interconnect fabric
  - CoreNet fabric supporting coherent and non-coherent transactions with prioritization and bandwidth allocation amongst CoreNet end-points
  - 1.6 Tbps coherent read bandwidth
- Two 64-bit DDR3 SDRAM memory controllers
  - DDR3 and DDR3L with ECC and interleaving support
- Data Path Acceleration Architecture (DPAA) incorporating acceleration for the following functions:
  - Packet parsing, classification, and distribution (Frame Manager 1.1)
  - Queue management for scheduling, packet sequencing, and congestion management (Queue Manager 1.1)
  - Hardware buffer management for buffer allocation and de-allocation (Buffer Manager 1.1)
  - Cryptography Acceleration (SEC 5.0)
  - RegEx Pattern Matching Acceleration (PME 2.0)
  - Decompression/Compression Acceleration (DCE 1.0)
  - DPAA chip-to-chip interconnect via RapidIO Message Manager (RMan 1.0)
- 24 SerDes lanes at up to 10 GHz
- Ethernet interfaces
  - Up to two 10 Gbps Ethernet MACs
  - Up to 13 1 Gbps Ethernet MACs
  - Combinations of 1 Gbps, 2.5 Gbps, and 10 Gbps Ethernet MACs
  - IEEE Std 1588™ support
- High-speed peripheral interfaces
  - Three PCI Express 2.0/3.0 controllers running at up to 8 Gbps with one controller supporting end-point, single-root I/O virtualization (SR-IOV)
  - Two Serial RapidIO 2.0 controllers running at up to 5 Gbaud
  - Interlaken look-aside interface for TCAM connection
- Additional peripheral interfaces
  - Two Serial ATA (SATA 2.0) controllers
  - Two high-speed USB 2.0 controllers with integrated PHY
  - Enhanced secure digital host controller (SD/MMC/eMMC)
  - Enhanced Serial peripheral interface (eSPI)
  - Four I2C controllers
  - Four 2-pin UARTs or two 4-pin DUARTs
  - Integrated flash controller supporting NAND and NOR flash
- Three 8-channel DMA engines
- 1932 FC-PBGA package, 45 mm x 45 mm, 1mm pitch

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1 Overview

The T4160 and T4080 QorIQ integrated multicore communications processor combines 8 and 4 respectively, dual-threaded cores built on Power Architecture® technology with high-performance data path acceleration and network and peripheral bus interfaces required for networking, telecom/datacom, wireless infrastructure, and military/aerospace applications.

This chip can be used for combined control, data path, and application layer processing in routers, switches, gateways, and general-purpose embedded computing systems. Its high level of integration offers significant performance benefits compared to multiple discrete devices, while also simplifying board design.

This figure shows the block diagram of the T4160.

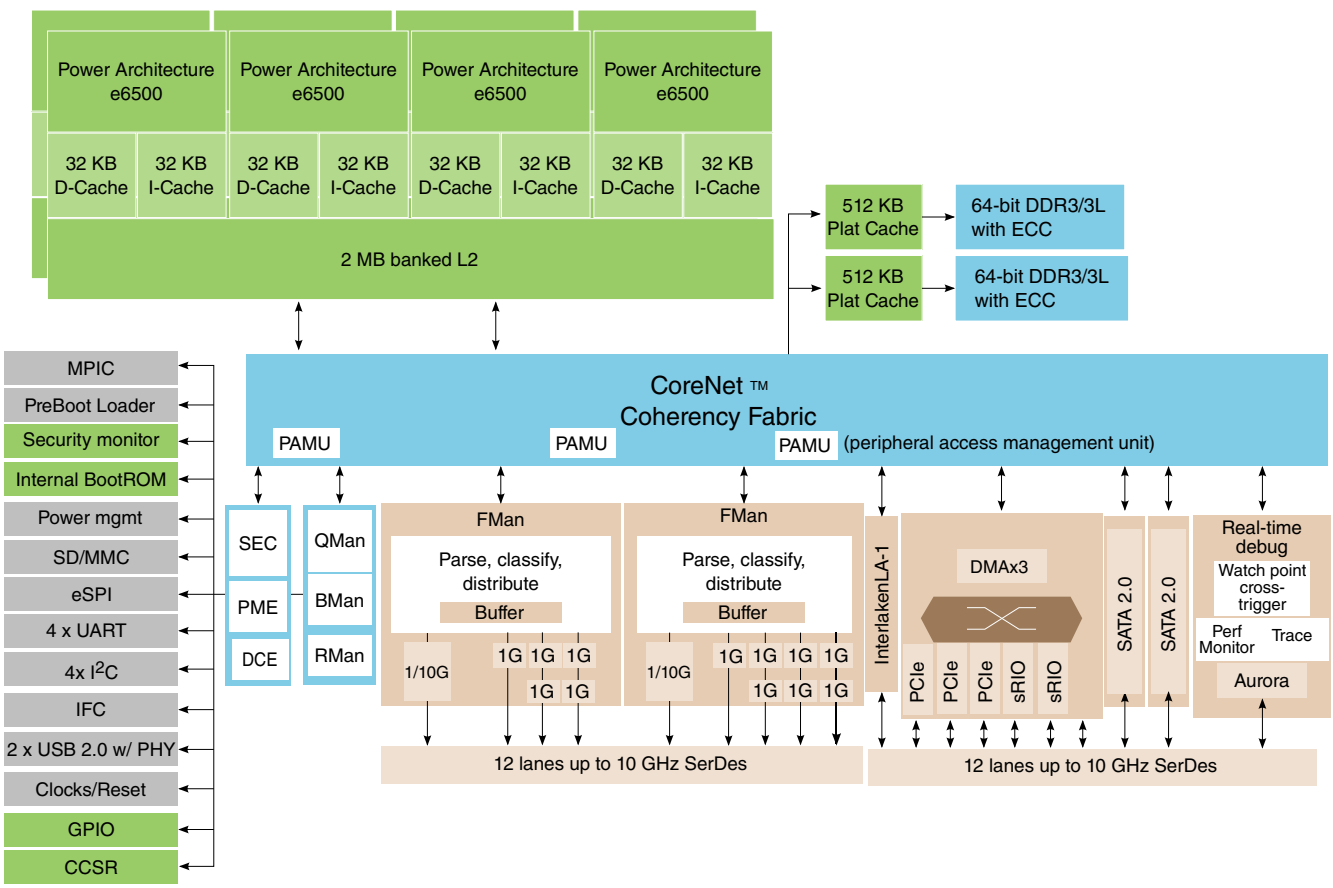

Figure 1. T4160 Block diagram

This figure shows the block diagram of the T4080.

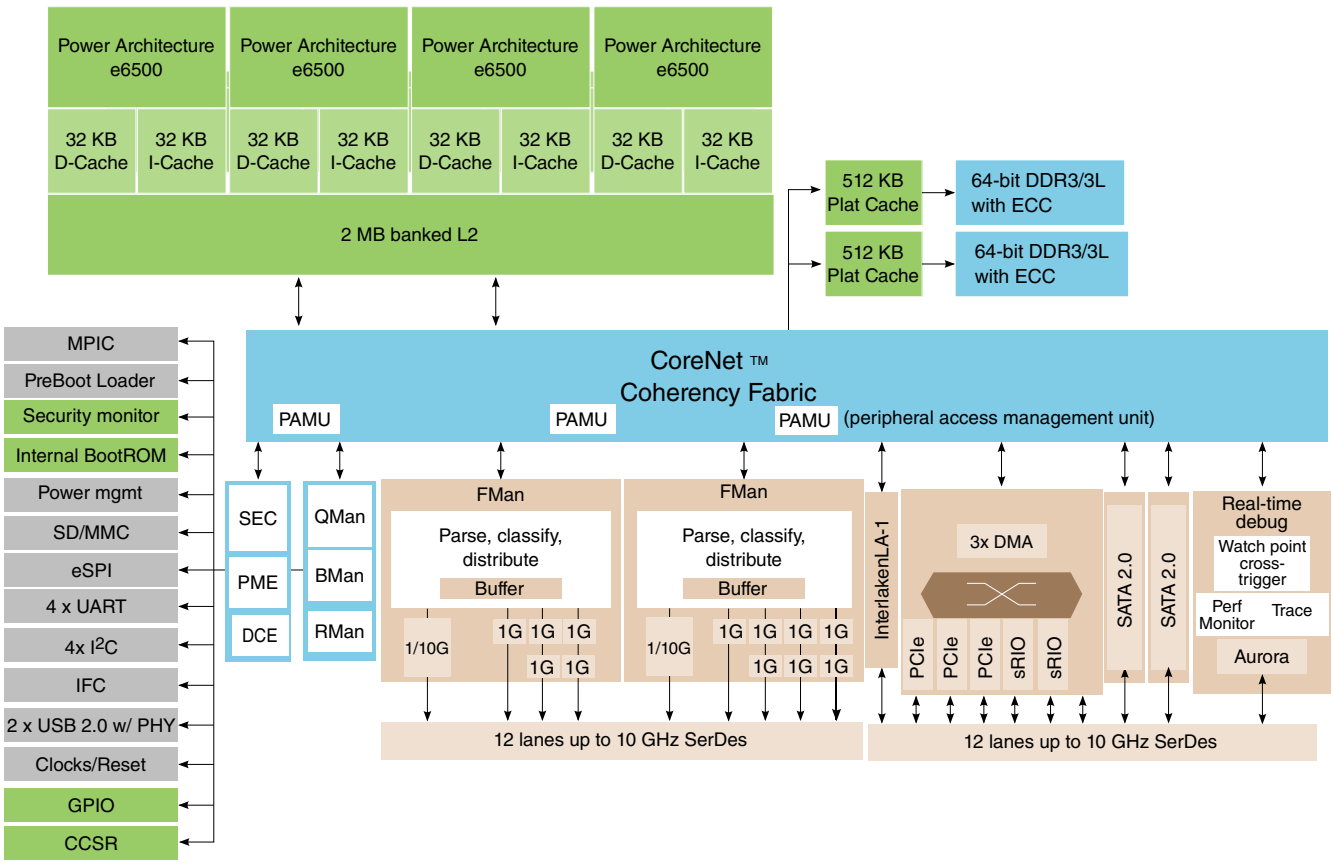

Figure 2. T4080 Block diagram

2 Pin assignments

2.1 1932 ball layout diagrams

This figure shows the complete view of the T4160 and T4080 ball map diagram. Figure 4, Figure 5, Figure 6, and Figure 7 show quadrant views.

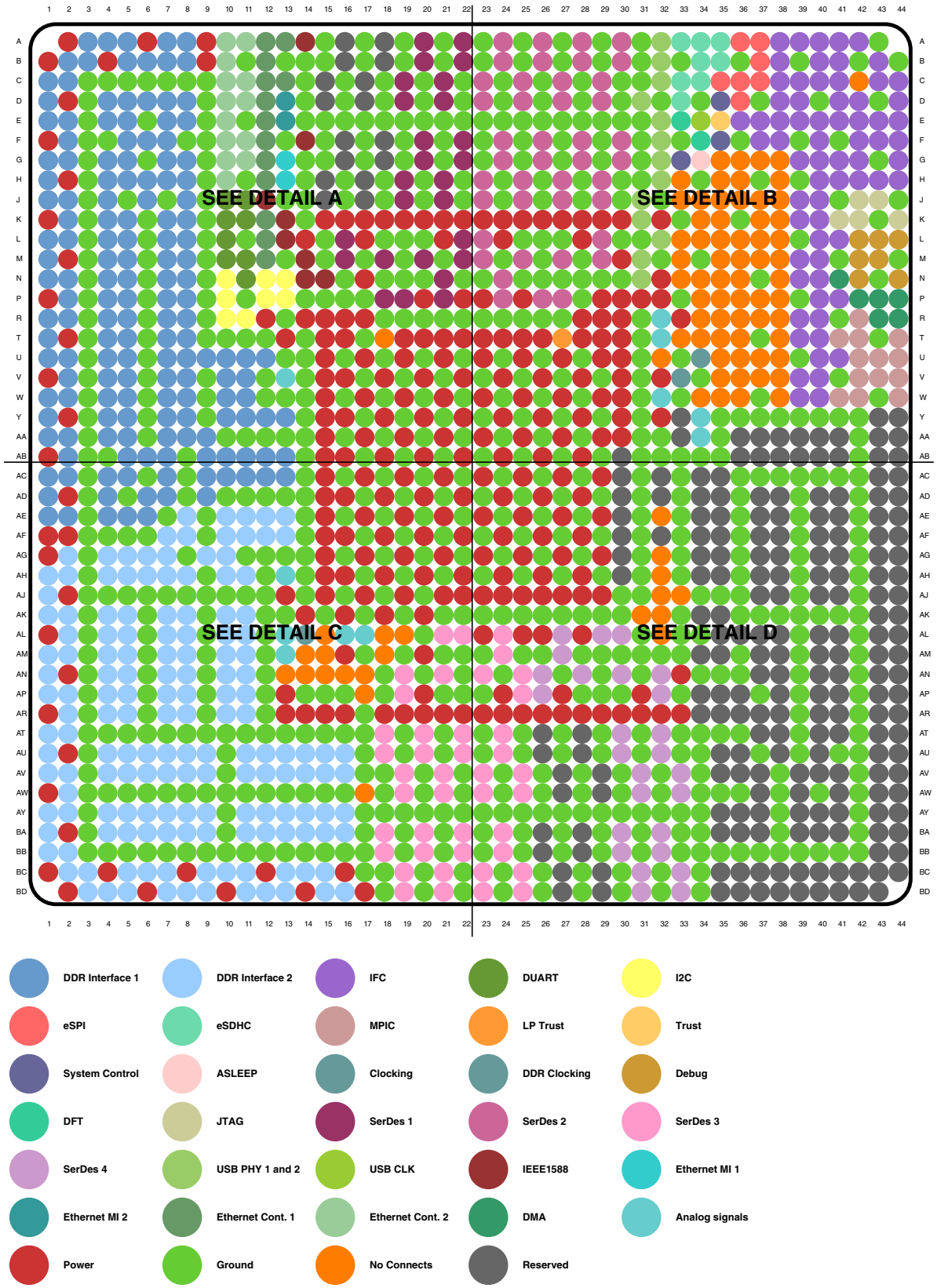

Figure 3. Complete BGA Map for the T4160

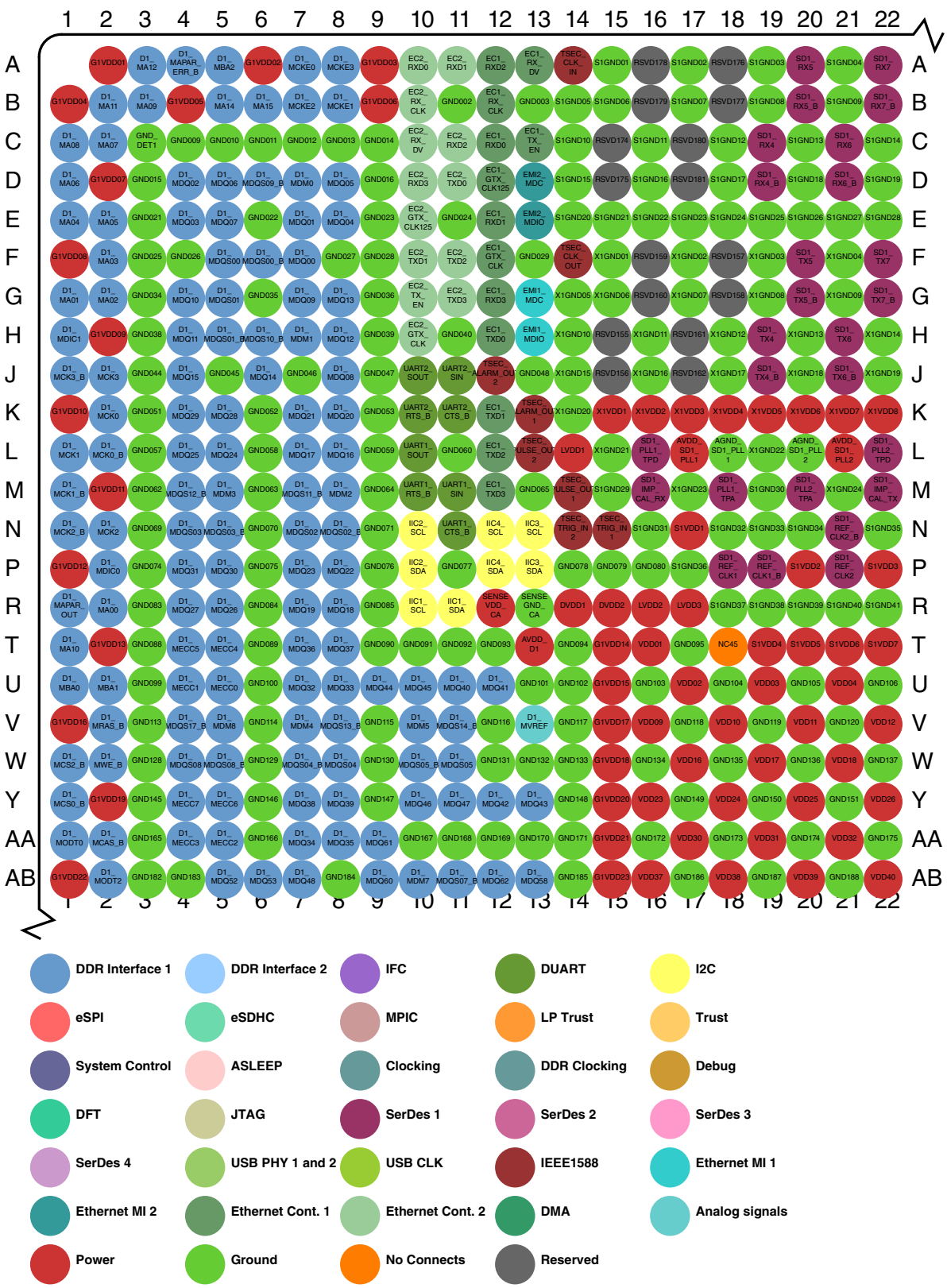

Figure 4. Detail A

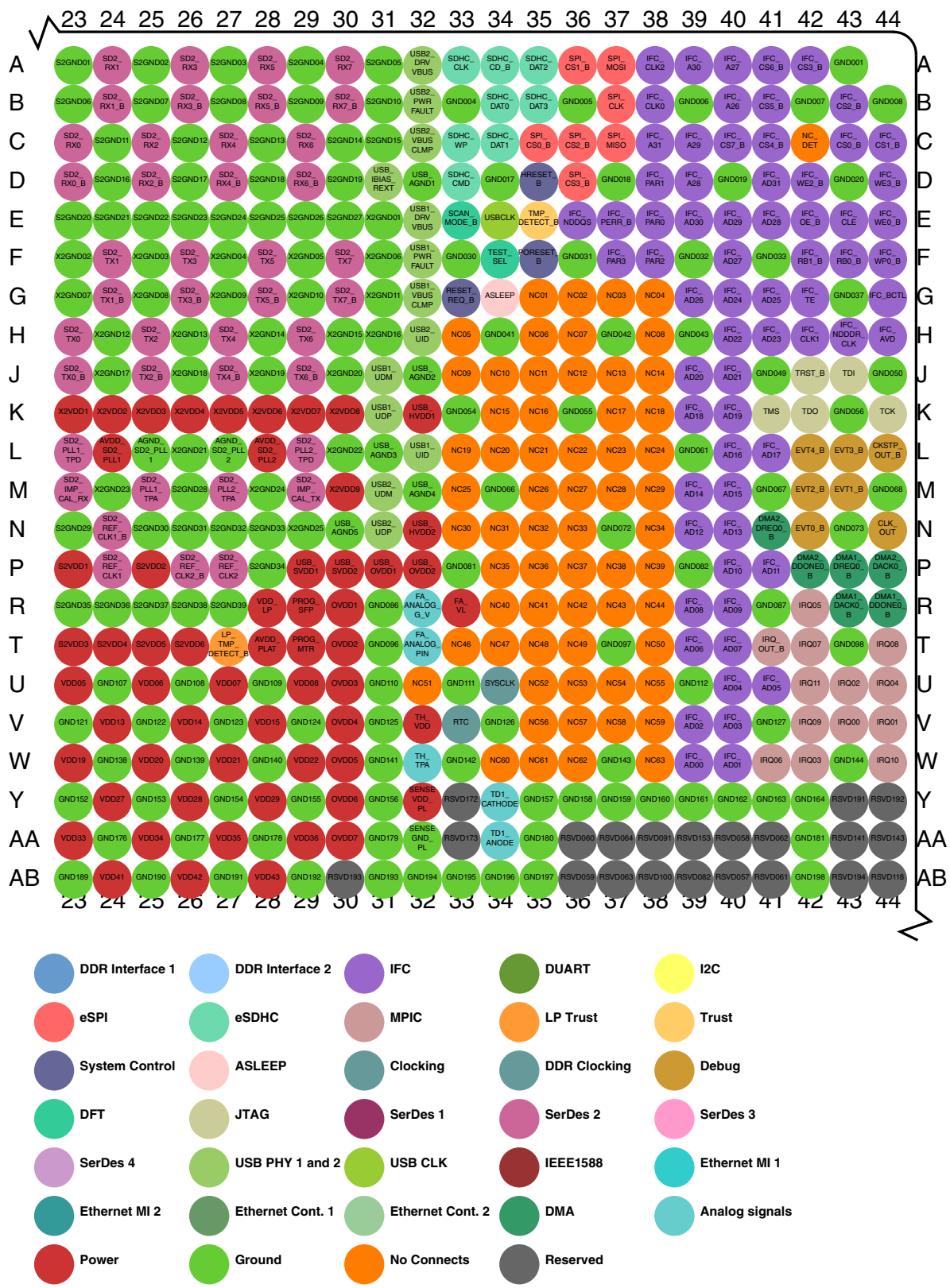

Figure 5. Detail B

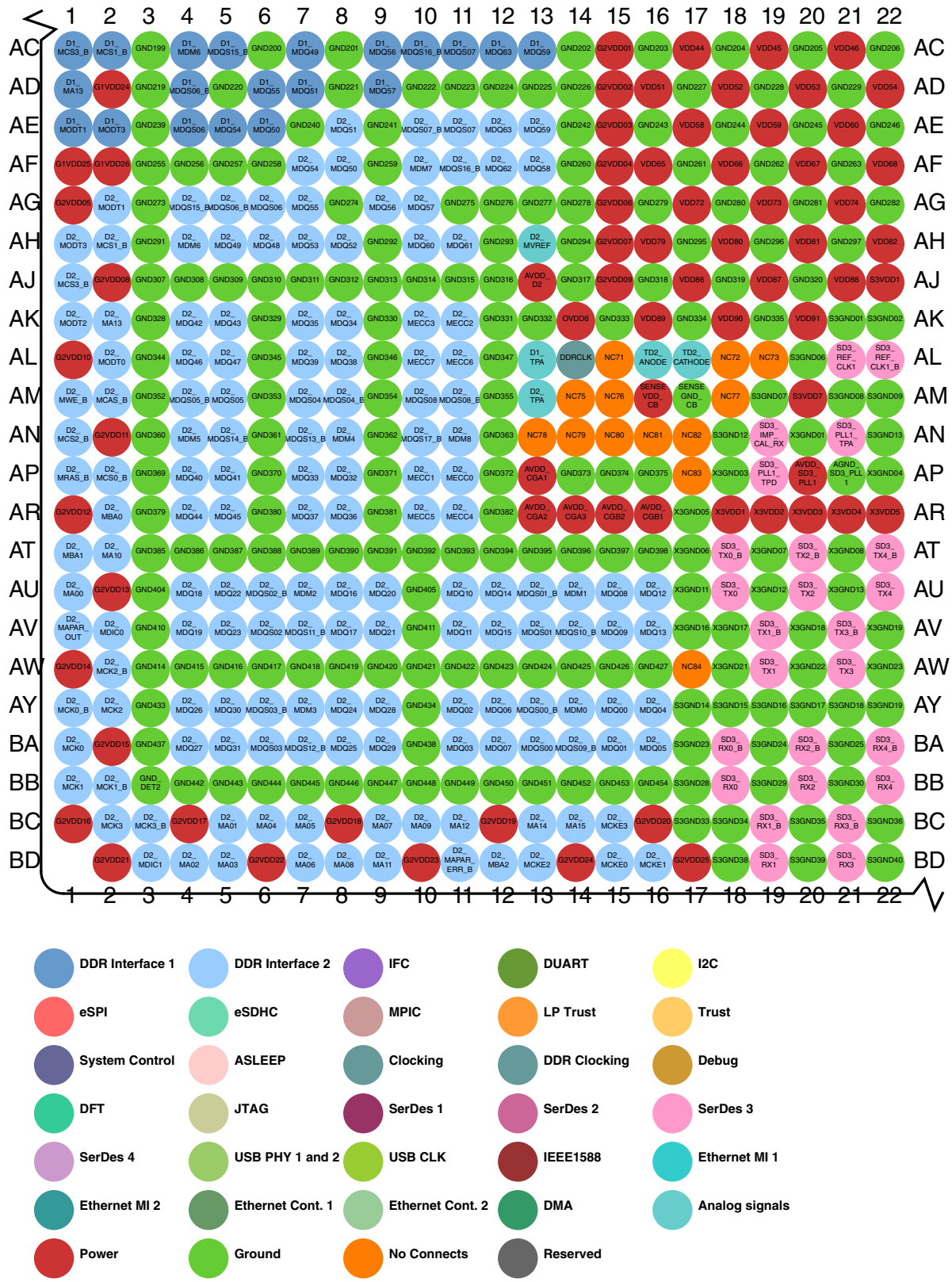

Figure 6. Detail C

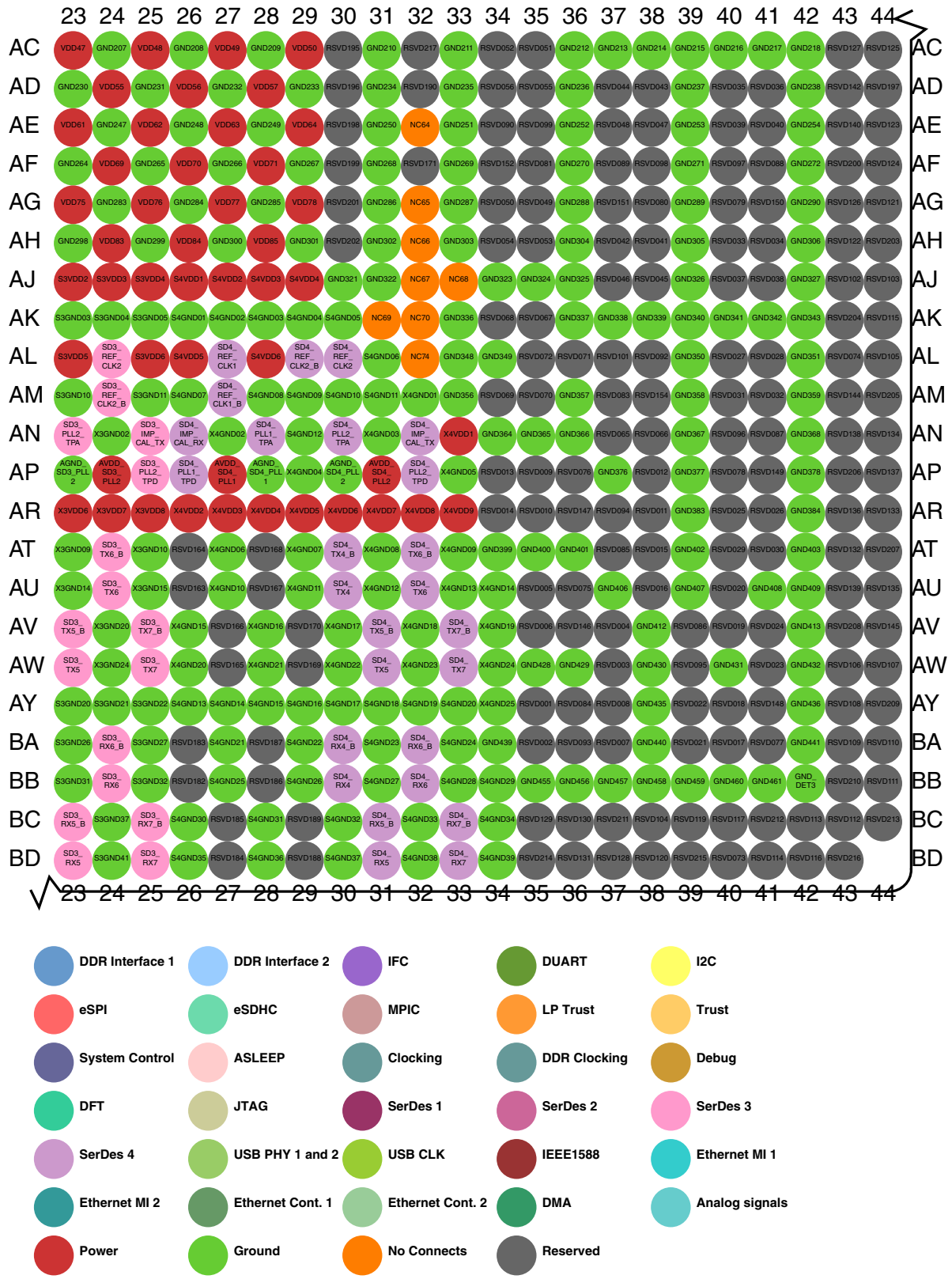

Figure 7. Detail D

2.2 Pinout list

This table provides the pinout listing for the T4160 by bus. Primary functions are **bolded** in the table.

Table 1. Pinout list by bus

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
DDR SDRAM Memory Interface 1					
D1_MA00	Address	R2	O	$G1V_{DD}$	---
D1_MA01	Address	G1	O	$G1V_{DD}$	---
D1_MA02	Address	G2	O	$G1V_{DD}$	---
D1_MA03	Address	F2	O	$G1V_{DD}$	---
D1_MA04	Address	E1	O	$G1V_{DD}$	---
D1_MA05	Address	E2	O	$G1V_{DD}$	---
D1_MA06	Address	D1	O	$G1V_{DD}$	---
D1_MA07	Address	C2	O	$G1V_{DD}$	---
D1_MA08	Address	C1	O	$G1V_{DD}$	---
D1_MA09	Address	B3	O	$G1V_{DD}$	---
D1_MA10	Address	T1	O	$G1V_{DD}$	---
D1_MA11	Address	B2	O	$G1V_{DD}$	---
D1_MA12	Address	A3	O	$G1V_{DD}$	---
D1_MA13	Address	AD1	O	$G1V_{DD}$	---
D1_MA14	Address	B5	O	$G1V_{DD}$	---
D1_MA15	Address	B6	O	$G1V_{DD}$	---
D1_MAPAR_ERR_B	Address Parity Error	A4	I	$G1V_{DD}$	1, 18
D1_MAPAR_OUT	Address Parity Out	R1	O	$G1V_{DD}$	---
D1_MBA0	Bank Select	U1	O	$G1V_{DD}$	---
D1_MBA1	Bank Select	U2	O	$G1V_{DD}$	---
D1_MBA2	Bank Select	A5	O	$G1V_{DD}$	---
D1_MCAS_B	Column Address Strobe	AA2	O	$G1V_{DD}$	---
D1_MCK0	Clock	K2	O	$G1V_{DD}$	---
D1_MCK0_B	Clock Complements	L2	O	$G1V_{DD}$	---
D1_MCK1	Clock	L1	O	$G1V_{DD}$	---
D1_MCK1_B	Clock Complements	M1	O	$G1V_{DD}$	---
D1_MCK2	Clock	N2	O	$G1V_{DD}$	---
D1_MCK2_B	Clock Complements	N1	O	$G1V_{DD}$	---
D1_MCK3	Clock	J2	O	$G1V_{DD}$	---
D1_MCK3_B	Clock Complements	J1	O	$G1V_{DD}$	---
D1_MCKE0	Clock Enable	A7	O	$G1V_{DD}$	2

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MCKE1	Clock Enable	B8	O	$G1V_{DD}$	2
D1_MCKE2	Clock Enable	B7	O	$G1V_{DD}$	2
D1_MCKE3	Clock Enable	A8	O	$G1V_{DD}$	2
D1_MCS0_B	Chip Select	Y1	O	$G1V_{DD}$	---
D1_MCS1_B	Chip Select	AC2	O	$G1V_{DD}$	---
D1_MCS2_B	Chip Select	W1	O	$G1V_{DD}$	---
D1_MCS3_B	Chip Select	AC1	O	$G1V_{DD}$	---
D1_MDIC0	Driver Impedence Calibration	P2	IO	$G1V_{DD}$	3
D1_MDIC1	Driver Impedence Calibration	H1	IO	$G1V_{DD}$	3
D1_MDM0/D1_MDQS09	Data Mask	D7	O	$G1V_{DD}$	1
D1_MDM1/D1_MDQS10	Data Mask	H7	O	$G1V_{DD}$	1
D1_MDM2/D1_MDQS11	Data Mask	M8	O	$G1V_{DD}$	1
D1_MDM3/D1_MDQS12	Data Mask	M5	O	$G1V_{DD}$	1
D1_MDM4/D1_MDQS13	Data Mask	V7	O	$G1V_{DD}$	1
D1_MDM5/D1_MDQS14	Data Mask	V10	O	$G1V_{DD}$	1
D1_MDM6/D1_MDQS15	Data Mask	AC4	O	$G1V_{DD}$	1
D1_MDM7/D1_MDQS16	Data Mask	AB10	O	$G1V_{DD}$	1
D1_MDM8/D1_MDQS17	Data Mask	V5	O	$G1V_{DD}$	1
D1_MDQ00	Data	F7	IO	$G1V_{DD}$	---
D1_MDQ01	Data	E7	IO	$G1V_{DD}$	---
D1_MDQ02	Data	D4	IO	$G1V_{DD}$	---
D1_MDQ03	Data	E4	IO	$G1V_{DD}$	---
D1_MDQ04	Data	E8	IO	$G1V_{DD}$	---
D1_MDQ05	Data	D8	IO	$G1V_{DD}$	---
D1_MDQ06	Data	D5	IO	$G1V_{DD}$	---
D1_MDQ07	Data	E5	IO	$G1V_{DD}$	---
D1_MDQ08	Data	J8	IO	$G1V_{DD}$	---
D1_MDQ09	Data	G7	IO	$G1V_{DD}$	---
D1_MDQ10	Data	G4	IO	$G1V_{DD}$	---
D1_MDQ11	Data	H4	IO	$G1V_{DD}$	---
D1_MDQ12	Data	H8	IO	$G1V_{DD}$	---
D1_MDQ13	Data	G8	IO	$G1V_{DD}$	---
D1_MDQ14	Data	J6	IO	$G1V_{DD}$	---
D1_MDQ15	Data	J4	IO	$G1V_{DD}$	---
D1_MDQ16	Data	L8	IO	$G1V_{DD}$	---
D1_MDQ17	Data	L7	IO	$G1V_{DD}$	---
D1_MDQ18	Data	R8	IO	$G1V_{DD}$	---
D1_MDQ19	Data	R7	IO	$G1V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MDQ20	Data	K8	IO	$G1V_{DD}$	---
D1_MDQ21	Data	K7	IO	$G1V_{DD}$	---
D1_MDQ22	Data	P8	IO	$G1V_{DD}$	---
D1_MDQ23	Data	P7	IO	$G1V_{DD}$	---
D1_MDQ24	Data	L5	IO	$G1V_{DD}$	---
D1_MDQ25	Data	L4	IO	$G1V_{DD}$	---
D1_MDQ26	Data	R5	IO	$G1V_{DD}$	---
D1_MDQ27	Data	R4	IO	$G1V_{DD}$	---
D1_MDQ28	Data	K5	IO	$G1V_{DD}$	---
D1_MDQ29	Data	K4	IO	$G1V_{DD}$	---
D1_MDQ30	Data	P5	IO	$G1V_{DD}$	---
D1_MDQ31	Data	P4	IO	$G1V_{DD}$	---
D1_MDQ32	Data	U7	IO	$G1V_{DD}$	---
D1_MDQ33	Data	U8	IO	$G1V_{DD}$	---
D1_MDQ34	Data	AA7	IO	$G1V_{DD}$	---
D1_MDQ35	Data	AA8	IO	$G1V_{DD}$	---
D1_MDQ36	Data	T7	IO	$G1V_{DD}$	---
D1_MDQ37	Data	T8	IO	$G1V_{DD}$	---
D1_MDQ38	Data	Y7	IO	$G1V_{DD}$	---
D1_MDQ39	Data	Y8	IO	$G1V_{DD}$	---
D1_MDQ40	Data	U11	IO	$G1V_{DD}$	---
D1_MDQ41	Data	U12	IO	$G1V_{DD}$	---
D1_MDQ42	Data	Y12	IO	$G1V_{DD}$	---
D1_MDQ43	Data	Y13	IO	$G1V_{DD}$	---
D1_MDQ44	Data	U9	IO	$G1V_{DD}$	---
D1_MDQ45	Data	U10	IO	$G1V_{DD}$	---
D1_MDQ46	Data	Y10	IO	$G1V_{DD}$	---
D1_MDQ47	Data	Y11	IO	$G1V_{DD}$	---
D1_MDQ48	Data	AB7	IO	$G1V_{DD}$	---
D1_MDQ49	Data	AC7	IO	$G1V_{DD}$	---
D1_MDQ50	Data	AE6	IO	$G1V_{DD}$	---
D1_MDQ51	Data	AD7	IO	$G1V_{DD}$	---
D1_MDQ52	Data	AB5	IO	$G1V_{DD}$	---
D1_MDQ53	Data	AB6	IO	$G1V_{DD}$	---
D1_MDQ54	Data	AE5	IO	$G1V_{DD}$	---
D1_MDQ55	Data	AD6	IO	$G1V_{DD}$	---
D1_MDQ56	Data	AC9	IO	$G1V_{DD}$	---
D1_MDQ57	Data	AD9	IO	$G1V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MDQ58	Data	AB13	IO	$G1V_{DD}$	---
D1_MDQ59	Data	AC13	IO	$G1V_{DD}$	---
D1_MDQ60	Data	AB9	IO	$G1V_{DD}$	---
D1_MDQ61	Data	AA9	IO	$G1V_{DD}$	---
D1_MDQ62	Data	AB12	IO	$G1V_{DD}$	---
D1_MDQ63	Data	AC12	IO	$G1V_{DD}$	---
D1_MDQS00	Data Strobe	F5	IO	$G1V_{DD}$	---
D1_MDQS00_B	Data Strobe	F6	IO	$G1V_{DD}$	---
D1_MDQS01	Data Strobe	G5	IO	$G1V_{DD}$	---
D1_MDQS01_B	Data Strobe	H5	IO	$G1V_{DD}$	---
D1_MDQS02	Data Strobe	N7	IO	$G1V_{DD}$	---
D1_MDQS02_B	Data Strobe	N8	IO	$G1V_{DD}$	---
D1_MDQS03	Data Strobe	N4	IO	$G1V_{DD}$	---
D1_MDQS03_B	Data Strobe	N5	IO	$G1V_{DD}$	---
D1_MDQS04	Data Strobe	W8	IO	$G1V_{DD}$	---
D1_MDQS04_B	Data Strobe	W7	IO	$G1V_{DD}$	---
D1_MDQS05	Data Strobe	W11	IO	$G1V_{DD}$	---
D1_MDQS05_B	Data Strobe	W10	IO	$G1V_{DD}$	---
D1_MDQS06	Data Strobe	AE4	IO	$G1V_{DD}$	---
D1_MDQS06_B	Data Strobe	AD4	IO	$G1V_{DD}$	---
D1_MDQS07	Data Strobe	AC11	IO	$G1V_{DD}$	---
D1_MDQS07_B	Data Strobe	AB11	IO	$G1V_{DD}$	---
D1_MDQS08	Data Strobe	W4	IO	$G1V_{DD}$	---
D1_MDQS08_B	Data Strobe	W5	IO	$G1V_{DD}$	---
D1_MDQS09/**D1_MDM0**	Data Strobe (x4 support)	D7	IO	$G1V_{DD}$	---
D1_MDQS09_B	Data Strobe (x4 support)	D6	IO	$G1V_{DD}$	28
D1_MDQS10/**D1_MDM1**	Data Strobe (x4 support)	H7	IO	$G1V_{DD}$	---
D1_MDQS10_B	Data Strobe (x4 support)	H6	IO	$G1V_{DD}$	28
D1_MDQS11/**D1_MDM2**	Data Strobe (x4 support)	M8	IO	$G1V_{DD}$	---
D1_MDQS11_B	Data Strobe (x4 support)	M7	IO	$G1V_{DD}$	28
D1_MDQS12/**D1_MDM3**	Data Strobe (x4 support)	M5	IO	$G1V_{DD}$	---
D1_MDQS12_B	Data Strobe (x4 support)	M4	IO	$G1V_{DD}$	28
D1_MDQS13/**D1_MDM4**	Data Strobe (x4 support)	V7	IO	$G1V_{DD}$	---
D1_MDQS13_B	Data Strobe (x4 support)	V8	IO	$G1V_{DD}$	28
D1_MDQS14/**D1_MDM5**	Data Strobe (x4 support)	V10	IO	$G1V_{DD}$	---
D1_MDQS14_B	Data Strobe (x4 support)	V11	IO	$G1V_{DD}$	28
D1_MDQS15/**D1_MDM6**	Data Strobe (x4 support)	AC4	IO	$G1V_{DD}$	---
D1_MDQS15_B	Data Strobe (x4 support)	AC5	IO	$G1V_{DD}$	28

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MDQS16/**D1_MDM7**	Data Strobe (x4 support)	AB10	IO	$G1V_{DD}$	---
D1_MDQS16_B	Data Strobe (x4 support)	AC10	IO	$G1V_{DD}$	28
D1_MDQS17/**D1_MDM8**	Data Strobe (x4 support)	V5	IO	$G1V_{DD}$	---
D1_MDQS17_B	Data Strobe (x4 support)	V4	IO	$G1V_{DD}$	28
D1_MECC0	Error Correcting Code	U5	IO	$G1V_{DD}$	---
D1_MECC1	Error Correcting Code	U4	IO	$G1V_{DD}$	---
D1_MECC2	Error Correcting Code	AA5	IO	$G1V_{DD}$	---
D1_MECC3	Error Correcting Code	AA4	IO	$G1V_{DD}$	---
D1_MECC4	Error Correcting Code	T5	IO	$G1V_{DD}$	---
D1_MECC5	Error Correcting Code	T4	IO	$G1V_{DD}$	---
D1_MECC6	Error Correcting Code	Y5	IO	$G1V_{DD}$	---
D1_MECC7	Error Correcting Code	Y4	IO	$G1V_{DD}$	---
D1_MODT0	On Die Termination	AA1	O	$G1V_{DD}$	2
D1_MODT1	On Die Termination	AE1	O	$G1V_{DD}$	2
D1_MODT2	On Die Termination	AB2	O	$G1V_{DD}$	2
D1_MODT3	On Die Termination	AE2	O	$G1V_{DD}$	2
D1_MRAS_B	Row Address Strobe	V2	O	$G1V_{DD}$	---
D1_MWE_B	Write Enable	W2	O	$G1V_{DD}$	---
DDR SDRAM Memory Interface 2					
D2_MA00	Address	AU1	O	$G2V_{DD}$	---
D2_MA01	Address	BC5	O	$G2V_{DD}$	---
D2_MA02	Address	BD4	O	$G2V_{DD}$	---
D2_MA03	Address	BD5	O	$G2V_{DD}$	---
D2_MA04	Address	BC6	O	$G2V_{DD}$	---
D2_MA05	Address	BC7	O	$G2V_{DD}$	---
D2_MA06	Address	BD7	O	$G2V_{DD}$	---
D2_MA07	Address	BC9	O	$G2V_{DD}$	---
D2_MA08	Address	BD8	O	$G2V_{DD}$	---
D2_MA09	Address	BC10	O	$G2V_{DD}$	---
D2_MA10	Address	AT2	O	$G2V_{DD}$	---
D2_MA11	Address	BD9	O	$G2V_{DD}$	---
D2_MA12	Address	BC11	O	$G2V_{DD}$	---
D2_MA13	Address	AK2	O	$G2V_{DD}$	---
D2_MA14	Address	BC13	O	$G2V_{DD}$	---
D2_MA15	Address	BC14	O	$G2V_{DD}$	---
D2_MAPAR_ERR_B	Address Parity Error	BD11	I	$G2V_{DD}$	1, 18
D2_MAPAR_OUT	Address Parity Out	AV1	O	$G2V_{DD}$	---
D2_MBA0	Bank Select	AR2	O	$G2V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D2_MBA1	Bank Select	AT1	O	$G2V_{DD}$	---
D2_MBA2	Bank Select	BD12	O	$G2V_{DD}$	---
D2_MCAS_B	Column Address Strobe	AM2	O	$G2V_{DD}$	---
D2_MCK0	Clock	BA1	O	$G2V_{DD}$	---
D2_MCK0_B	Clock Complements	AY1	O	$G2V_{DD}$	---
D2_MCK1	Clock	BB1	O	$G2V_{DD}$	---
D2_MCK1_B	Clock Complements	BB2	O	$G2V_{DD}$	---
D2_MCK2	Clock	AY2	O	$G2V_{DD}$	---
D2_MCK2_B	Clock Complements	AW2	O	$G2V_{DD}$	---
D2_MCK3	Clock	BC2	O	$G2V_{DD}$	---
D2_MCK3_B	Clock Complements	BC3	O	$G2V_{DD}$	---
D2_MCKE0	Clock Enable	BD15	O	$G2V_{DD}$	2
D2_MCKE1	Clock Enable	BD16	O	$G2V_{DD}$	2
D2_MCKE2	Clock Enable	BD13	O	$G2V_{DD}$	2
D2_MCKE3	Clock Enable	BC15	O	$G2V_{DD}$	2
D2_MCS0_B	Chip Select	AP2	O	$G2V_{DD}$	---
D2_MCS1_B	Chip Select	AH2	O	$G2V_{DD}$	---
D2_MCS2_B	Chip Select	AN1	O	$G2V_{DD}$	---
D2_MCS3_B	Chip Select	AJ1	O	$G2V_{DD}$	---
D2_MDIC0	Driver Impedence Calibration	AV2	IO	$G2V_{DD}$	3
D2_MDIC1	Driver Impedence Calibration	BD3	IO	$G2V_{DD}$	3
D2_MDM0/D2_MDQS09	Data Mask	AY14	O	$G2V_{DD}$	1
D2_MDM1/D2_MDQS10	Data Mask	AU14	O	$G2V_{DD}$	1
D2_MDM2/D2_MDQS11	Data Mask	AU7	O	$G2V_{DD}$	1
D2_MDM3/D2_MDQS12	Data Mask	AY7	O	$G2V_{DD}$	1
D2_MDM4/D2_MDQS13	Data Mask	AN8	O	$G2V_{DD}$	1
D2_MDM5/D2_MDQS14	Data Mask	AN4	O	$G2V_{DD}$	1
D2_MDM6/D2_MDQS15	Data Mask	AH4	O	$G2V_{DD}$	1
D2_MDM7/D2_MDQS16	Data Mask	AF10	O	$G2V_{DD}$	1
D2_MDM8/D2_MDQS17	Data Mask	AN11	O	$G2V_{DD}$	1
D2_MDQ00	Data	AY15	IO	$G2V_{DD}$	---
D2_MDQ01	Data	BA15	IO	$G2V_{DD}$	---
D2_MDQ02	Data	AY11	IO	$G2V_{DD}$	---
D2_MDQ03	Data	BA11	IO	$G2V_{DD}$	---
D2_MDQ04	Data	AY16	IO	$G2V_{DD}$	---
D2_MDQ05	Data	BA16	IO	$G2V_{DD}$	---
D2_MDQ06	Data	AY12	IO	$G2V_{DD}$	---
D2_MDQ07	Data	BA12	IO	$G2V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D2_MDQ08	Data	AU15	IO	$G2V_{DD}$	---
D2_MDQ09	Data	AV15	IO	$G2V_{DD}$	---
D2_MDQ10	Data	AU11	IO	$G2V_{DD}$	---
D2_MDQ11	Data	AV11	IO	$G2V_{DD}$	---
D2_MDQ12	Data	AU16	IO	$G2V_{DD}$	---
D2_MDQ13	Data	AV16	IO	$G2V_{DD}$	---
D2_MDQ14	Data	AU12	IO	$G2V_{DD}$	---
D2_MDQ15	Data	AV12	IO	$G2V_{DD}$	---
D2_MDQ16	Data	AU8	IO	$G2V_{DD}$	---
D2_MDQ17	Data	AV8	IO	$G2V_{DD}$	---
D2_MDQ18	Data	AU4	IO	$G2V_{DD}$	---
D2_MDQ19	Data	AV4	IO	$G2V_{DD}$	---
D2_MDQ20	Data	AU9	IO	$G2V_{DD}$	---
D2_MDQ21	Data	AV9	IO	$G2V_{DD}$	---
D2_MDQ22	Data	AU5	IO	$G2V_{DD}$	---
D2_MDQ23	Data	AV5	IO	$G2V_{DD}$	---
D2_MDQ24	Data	AY8	IO	$G2V_{DD}$	---
D2_MDQ25	Data	BA8	IO	$G2V_{DD}$	---
D2_MDQ26	Data	AY4	IO	$G2V_{DD}$	---
D2_MDQ27	Data	BA4	IO	$G2V_{DD}$	---
D2_MDQ28	Data	AY9	IO	$G2V_{DD}$	---
D2_MDQ29	Data	BA9	IO	$G2V_{DD}$	---
D2_MDQ30	Data	AY5	IO	$G2V_{DD}$	---
D2_MDQ31	Data	BA5	IO	$G2V_{DD}$	---
D2_MDQ32	Data	AP8	IO	$G2V_{DD}$	---
D2_MDQ33	Data	AP7	IO	$G2V_{DD}$	---
D2_MDQ34	Data	AK8	IO	$G2V_{DD}$	---
D2_MDQ35	Data	AK7	IO	$G2V_{DD}$	---
D2_MDQ36	Data	AR8	IO	$G2V_{DD}$	---
D2_MDQ37	Data	AR7	IO	$G2V_{DD}$	---
D2_MDQ38	Data	AL8	IO	$G2V_{DD}$	---
D2_MDQ39	Data	AL7	IO	$G2V_{DD}$	---
D2_MDQ40	Data	AP4	IO	$G2V_{DD}$	---
D2_MDQ41	Data	AP5	IO	$G2V_{DD}$	---
D2_MDQ42	Data	AK4	IO	$G2V_{DD}$	---
D2_MDQ43	Data	AK5	IO	$G2V_{DD}$	---
D2_MDQ44	Data	AR4	IO	$G2V_{DD}$	---
D2_MDQ45	Data	AR5	IO	$G2V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D2_MDQ46	Data	AL4	IO	$G2V_{DD}$	---
D2_MDQ47	Data	AL5	IO	$G2V_{DD}$	---
D2_MDQ48	Data	AH6	IO	$G2V_{DD}$	---
D2_MDQ49	Data	AH5	IO	$G2V_{DD}$	---
D2_MDQ50	Data	AF8	IO	$G2V_{DD}$	---
D2_MDQ51	Data	AE8	IO	$G2V_{DD}$	---
D2_MDQ52	Data	AH8	IO	$G2V_{DD}$	---
D2_MDQ53	Data	AH7	IO	$G2V_{DD}$	---
D2_MDQ54	Data	AF7	IO	$G2V_{DD}$	---
D2_MDQ55	Data	AG7	IO	$G2V_{DD}$	---
D2_MDQ56	Data	AG9	IO	$G2V_{DD}$	---
D2_MDQ57	Data	AG10	IO	$G2V_{DD}$	---
D2_MDQ58	Data	AF13	IO	$G2V_{DD}$	---
D2_MDQ59	Data	AE13	IO	$G2V_{DD}$	---
D2_MDQ60	Data	AH10	IO	$G2V_{DD}$	---
D2_MDQ61	Data	AH11	IO	$G2V_{DD}$	---
D2_MDQ62	Data	AF12	IO	$G2V_{DD}$	---
D2_MDQ63	Data	AE12	IO	$G2V_{DD}$	---
D2_MDQS00	Data Strobe	BA13	IO	$G2V_{DD}$	---
D2_MDQS00_B	Data Strobe	AY13	IO	$G2V_{DD}$	---
D2_MDQS01	Data Strobe	AV13	IO	$G2V_{DD}$	---
D2_MDQS01_B	Data Strobe	AU13	IO	$G2V_{DD}$	---
D2_MDQS02	Data Strobe	AV6	IO	$G2V_{DD}$	---
D2_MDQS02_B	Data Strobe	AU6	IO	$G2V_{DD}$	---
D2_MDQS03	Data Strobe	BA6	IO	$G2V_{DD}$	---
D2_MDQS03_B	Data Strobe	AY6	IO	$G2V_{DD}$	---
D2_MDQS04	Data Strobe	AM7	IO	$G2V_{DD}$	---
D2_MDQS04_B	Data Strobe	AM8	IO	$G2V_{DD}$	---
D2_MDQS05	Data Strobe	AM5	IO	$G2V_{DD}$	---
D2_MDQS05_B	Data Strobe	AM4	IO	$G2V_{DD}$	---
D2_MDQS06	Data Strobe	AG6	IO	$G2V_{DD}$	---
D2_MDQS06_B	Data Strobe	AG5	IO	$G2V_{DD}$	---
D2_MDQS07	Data Strobe	AE11	IO	$G2V_{DD}$	---
D2_MDQS07_B	Data Strobe	AE10	IO	$G2V_{DD}$	---
D2_MDQS08	Data Strobe	AM10	IO	$G2V_{DD}$	---
D2_MDQS08_B	Data Strobe	AM11	IO	$G2V_{DD}$	---
D2_MDQS09/**D2_MDM0**	Data Strobe (x4 support)	AY14	IO	$G2V_{DD}$	---
D2_MDQS09_B	Data Strobe (x4 support)	BA14	IO	$G2V_{DD}$	28

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D2_MDQS10/**D2_MDM1**	Data Strobe (x4 support)	AU14	IO	$G2V_{DD}$	---
D2_MDQS10_B	Data Strobe (x4 support)	AV14	IO	$G2V_{DD}$	28
D2_MDQS11/**D2_MDM2**	Data Strobe (x4 support)	AU7	IO	$G2V_{DD}$	---
D2_MDQS11_B	Data Strobe (x4 support)	AV7	IO	$G2V_{DD}$	28
D2_MDQS12/**D2_MDM3**	Data Strobe (x4 support)	AY7	IO	$G2V_{DD}$	---
D2_MDQS12_B	Data Strobe (x4 support)	BA7	IO	$G2V_{DD}$	28
D2_MDQS13/**D2_MDM4**	Data Strobe (x4 support)	AN8	IO	$G2V_{DD}$	---
D2_MDQS13_B	Data Strobe (x4 support)	AN7	IO	$G2V_{DD}$	28
D2_MDQS14/**D2_MDM5**	Data Strobe (x4 support)	AN4	IO	$G2V_{DD}$	---
D2_MDQS14_B	Data Strobe (x4 support)	AN5	IO	$G2V_{DD}$	28
D2_MDQS15/**D2_MDM6**	Data Strobe (x4 support)	AH4	IO	$G2V_{DD}$	---
D2_MDQS15_B	Data Strobe (x4 support)	AG4	IO	$G2V_{DD}$	28
D2_MDQS16/**D2_MDM7**	Data Strobe (x4 support)	AF10	IO	$G2V_{DD}$	---
D2_MDQS16_B	Data Strobe (x4 support)	AF11	IO	$G2V_{DD}$	28
D2_MDQS17/**D2_MDM8**	Data Strobe (x4 support)	AN11	IO	$G2V_{DD}$	---
D2_MDQS17_B	Data Strobe (x4 support)	AN10	IO	$G2V_{DD}$	28
D2_MECC0	Error Correcting Code	AP11	IO	$G2V_{DD}$	---
D2_MECC1	Error Correcting Code	AP10	IO	$G2V_{DD}$	---
D2_MECC2	Error Correcting Code	AK11	IO	$G2V_{DD}$	---
D2_MECC3	Error Correcting Code	AK10	IO	$G2V_{DD}$	---
D2_MECC4	Error Correcting Code	AR11	IO	$G2V_{DD}$	---
D2_MECC5	Error Correcting Code	AR10	IO	$G2V_{DD}$	---
D2_MECC6	Error Correcting Code	AL11	IO	$G2V_{DD}$	---
D2_MECC7	Error Correcting Code	AL10	IO	$G2V_{DD}$	---
D2_MODT0	On Die Termination	AL2	O	$G2V_{DD}$	2
D2_MODT1	On Die Termination	AG2	O	$G2V_{DD}$	2
D2_MODT2	On Die Termination	AK1	O	$G2V_{DD}$	2
D2_MODT3	On Die Termination	AH1	O	$G2V_{DD}$	2
D2_MRAS_B	Row Address Strobe	AP1	O	$G2V_{DD}$	---
D2_MWE_B	Write Enable	AM1	O	$G2V_{DD}$	---
Integrated Flash Controller					
IFC_A26/GPIO2_18	IFC Address	B40	O	OV_{DD}	1
IFC_A27/GPIO2_19	IFC Address	A40	O	OV_{DD}	1
IFC_A28/GPIO2_20	IFC Address	D39	O	OV_{DD}	1
IFC_A29/GPIO2_21	IFC Address	C39	O	OV_{DD}	1
IFC_A30/GPIO2_22	IFC Address	A39	O	OV_{DD}	1
IFC_A31/GPIO2_23	IFC Address	C38	O	OV_{DD}	1
IFC_AD00/cfg_gpinput0	IFC Address/Data	W39	IO	OV_{DD}	4, 21

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
IFC_AD01/cfg_gpinput1	IFC Address/Data	W40	IO	OV_{DD}	4, 21
IFC_AD02/cfg_gpinput2	IFC Address/Data	V39	IO	OV_{DD}	4, 21
IFC_AD03/cfg_gpinput3	IFC Address/Data	V40	IO	OV_{DD}	4, 21
IFC_AD04/cfg_gpinput4	IFC Address/Data	U40	IO	OV_{DD}	4, 21
IFC_AD05/cfg_gpinput5	IFC Address/Data	U41	IO	OV_{DD}	4, 21
IFC_AD06/cfg_gpinput6	IFC Address/Data	T39	IO	OV_{DD}	4, 21
IFC_AD07/cfg_gpinput7	IFC Address/Data	T40	IO	OV_{DD}	4, 21
IFC_AD08/cfg_rcw_src0	IFC Address/Data	R39	IO	OV_{DD}	4, 21
IFC_AD09/cfg_rcw_src1	IFC Address/Data	R40	IO	OV_{DD}	4, 21
IFC_AD10/cfg_rcw_src2	IFC Address/Data	P40	IO	OV_{DD}	4, 21
IFC_AD11/cfg_rcw_src3	IFC Address/Data	P41	IO	OV_{DD}	4, 21
IFC_AD12/cfg_rcw_src4	IFC Address/Data	N39	IO	OV_{DD}	4, 21
IFC_AD13/cfg_rcw_src5	IFC Address/Data	N40	IO	OV_{DD}	4, 21
IFC_AD14/cfg_rcw_src6	IFC Address/Data	M39	IO	OV_{DD}	4, 21
IFC_AD15/cfg_rcw_src7	IFC Address/Data	M40	IO	OV_{DD}	4, 21
IFC_AD16	IFC Address/Data	L40	IO	OV_{DD}	29
IFC_AD17	IFC Address/Data	L41	IO	OV_{DD}	5, 20
IFC_AD18	IFC Address/Data	K39	IO	OV_{DD}	5, 20
IFC_AD19	IFC Address/Data	K40	IO	OV_{DD}	5, 20
IFC_AD20	IFC Address/Data	J39	IO	OV_{DD}	5, 20
IFC_AD21/cfg_dram_type	IFC Address/Data	J40	IO	OV_{DD}	4, 21
IFC_AD22	IFC Address/Data	H40	IO	OV_{DD}	20
IFC_AD23	IFC Address/Data	H41	IO	OV_{DD}	20
IFC_AD24	IFC Address/Data	G40	IO	OV_{DD}	20
IFC_AD25/GPIO2_25/ IFC_WP1_B	IFC Address/Data	G41	IO	OV_{DD}	20
IFC_AD26/GPIO2_26/ IFC_WP2_B	IFC Address/Data	G39	IO	OV_{DD}	20
IFC_AD27/GPIO2_27/ IFC_WP3_B	IFC Address/Data	F40	IO	OV_{DD}	20
IFC_AD28/GPIO2_28	IFC Address/Data	E41	IO	OV_{DD}	20
IFC_AD29/GPIO2_29/ IFC_RB2_B	IFC Address/Data	E40	IO	OV_{DD}	20
IFC_AD30/GPIO2_30/ IFC_RB3_B	IFC Address/Data	E39	IO	OV_{DD}	20
IFC_AD31/GPIO2_31/ IFC_RB4_B	IFC Address/Data	D41	IO	OV_{DD}	20
IFC_AVD	IFC Address Valid	H44	O	OV_{DD}	1, 5
IFC_BCTL	IFC Buffer Control	G44	O	OV_{DD}	1
IFC_CLE/cfg_rcw_src8	IFC Command Latch Enable	E43	O	OV_{DD}	1, 4, 25

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
IFC_CLK0	IFC Clock	B38	O	OV_{DD}	1
IFC_CLK1	IFC Clock	H42	O	OV_{DD}	1
IFC_CLK2	IFC Clock	A38	O	OV_{DD}	1
IFC_CS0_B	IFC Chip Select	C43	O	OV_{DD}	1, 6
IFC_CS1_B/GPIO2_10	IFC Chip Select	C44	O	OV_{DD}	1, 6
IFC_CS2_B/GPIO2_11	IFC Chip Select	B43	O	OV_{DD}	1, 6
IFC_CS3_B/GPIO2_12	IFC Chip Select	A42	O	OV_{DD}	1, 6
IFC_CS4_B/GPIO1_09	IFC Chip Select	C41	O	OV_{DD}	1, 6
IFC_CS5_B/GPIO1_10	IFC Chip Select	B41	O	OV_{DD}	1, 6
IFC_CS6_B/GPIO1_11	IFC Chip Select	A41	O	OV_{DD}	1, 6
IFC_CS7_B/GPIO1_12	IFC Chip Select	C40	O	OV_{DD}	1, 6
IFC_NDDDR_CLK	IFC NAND DDR Clock	H43	O	OV_{DD}	1
IFC_NDDQS	IFC DQS Strobe	E36	IO	OV_{DD}	20
IFC_OE_B	IFC Output Enable	E42	O	OV_{DD}	1, 5
IFC_PAR0/GPIO2_13	IFC Address and Data Parity	E38	IO	OV_{DD}	20
IFC_PAR1/GPIO2_14	IFC Address and Data Parity	D38	IO	OV_{DD}	20
IFC_PAR2/GPIO2_16	IFC Address and Data Parity	F38	IO	OV_{DD}	20
IFC_PAR3/GPIO2_17	IFC Address and Data Parity	F37	IO	OV_{DD}	20
IFC_PERR_B/GPIO2_15	IFC Parity Error	E37	I	OV_{DD}	1, 18
IFC_RB0_B	IFC Ready / Busy CS0	F43	I	OV_{DD}	8
IFC_RB1_B	IFC Ready / Busy CS1	F42	I	OV_{DD}	8
IFC_RB2_B/**IFC_AD29**/ GPIO2_29	IFC Ready / Busy CS 2	E40	I	OV_{DD}	1
IFC_RB3_B/**IFC_AD30**/ GPIO2_30	IFC Ready / Busy CS 3	E39	I	OV_{DD}	1
IFC_RB4_B/**IFC_AD31**/ GPIO2_31	IFC Ready / Busy CS 4	D41	I	OV_{DD}	1
IFC_TE/cfg_ifc_te	IFC External Transceiver Enable	G42	O	OV_{DD}	1, 4
IFC_WE0_B	IFC Write Enable	E44	O	OV_{DD}	1, 5
IFC_WE2_B	IFC Write Enable	D42	O	OV_{DD}	1
IFC_WE3_B	IFC Write Enable	D44	O	OV_{DD}	1
IFC_WP0_B	IFC Write Protect	F44	O	OV_{DD}	1, 5
IFC_WP1_B/**IFC_AD25**/ GPIO2_25	IFC Write Protect	G41	O	OV_{DD}	1
IFC_WP2_B/**IFC_AD26**/ GPIO2_26	IFC Write Protect	G39	O	OV_{DD}	1
IFC_WP3_B/**IFC_AD27**/ GPIO2_27	IFC Write Protect	F40	O	OV_{DD}	1
DUART					

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
UART1_CTS_B/GPIO1_21/ UART3_SIN	Clear To Send	N11	I	DV_{DD}	1
UART1_RTS_B/GPIO1_19/ UART3_SOUT	Ready to Send	M10	O	DV_{DD}	1
UART1_SIN/GPIO1_17	Receive Data	M11	I	DV_{DD}	1
UART1_SOUT/GPIO1_15	Transmit Data	L10	O	DV_{DD}	1
UART2_CTS_B/GPIO1_22/ UART4_SIN	Clear To Send	K11	I	DV_{DD}	1
UART2_RTS_B/GPIO1_20/ UART4_SOUT	Ready to Send	K10	O	DV_{DD}	1
UART2_SIN/GPIO1_18	Receive Data	J11	I	DV_{DD}	1
UART2_SOUT/GPIO1_16	Transmit Data	J10	O	DV_{DD}	1
UART3_SIN/**UART1_CTS_B**/ GPIO1_21	Receive Data	N11	I	DV_{DD}	1
UART3_SOUT/ **UART1_RTS_B**/GPIO1_19	Transmit Data	M10	O	DV_{DD}	1
UART4_SIN/**UART2_CTS_B**/ GPIO1_22	Receive Data	K11	I	DV_{DD}	1
UART4_SOUT/ **UART2_RTS_B**/GPIO1_20	Transmit Data	K10	O	DV_{DD}	1
I2C					
IIC1_SCL	Serial Clock (supports PBL)	R10	IO	DV_{DD}	7, 8
IIC1_SDA	Serial Data (supports PBL)	R11	IO	DV_{DD}	7, 8
IIC2_SCL	Serial Clock	N10	IO	DV_{DD}	7, 8
IIC2_SDA	Serial Data	P10	IO	DV_{DD}	7, 8
IIC3_SCL/GPIO4_00	Serial Clock	N13	IO	DV_{DD}	7, 8
IIC3_SDA/GPIO4_01	Serial Data	P13	IO	DV_{DD}	7, 8
IIC4_SCL/GPIO4_02/EVT5_B	Serial Clock	N12	IO	DV_{DD}	7, 8
IIC4_SDA/GPIO4_03/EVT6_B	Serial Data	P12	IO	DV_{DD}	7, 8
eSPI Interface					
SPI_CLK	SPI Clock	B37	O	OV_{DD}	1
SPI_CS0_B/GPIO2_00/ SDHC_DAT4	SPI Chip Select	C35	O	OV_{DD}	1, 22
SPI_CS1_B/GPIO2_01/ SDHC_DAT5	SPI Chip Select	A36	O	OV_{DD}	1, 22
SPI_CS2_B/GPIO2_02/ SDHC_DAT6	SPI Chip Select	C36	O	OV_{DD}	1, 22
SPI_CS3_B/GPIO2_03/ SDHC_DAT7	SPI Chip Select	D36	O	OV_{DD}	1, 22
SPI_MISO	Master In Slave Out	C37	I	OV_{DD}	---
SPI_MOSI	Master Out Slave In	A37	IO	OV_{DD}	20

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Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
eSDHC					
SDHC_CD_B	Card Detection	A34	I	OV_{DD}	26
SDHC_CLK/GPIO2_09	Host to Card Clock	A33	O	OV_{DD}	1
SDHC_CMD/GPIO2_04	Command/Response	D33	IO	OV_{DD}	22
SDHC_DAT0/GPIO2_05	Data	B34	IO	OV_{DD}	22
SDHC_DAT1/GPIO2_06	Data	C34	IO	OV_{DD}	22
SDHC_DAT2/GPIO2_07	Data	A35	IO	OV_{DD}	22
SDHC_DAT3/GPIO2_08	Data	B35	IO	OV_{DD}	22
SDHC_DAT4/**SPI_CS0_B**/ GPIO2_00	Data	C35	IO	OV_{DD}	---
SDHC_DAT5/**SPI_CS1_B**/ GPIO2_01	Data	A36	IO	OV_{DD}	---
SDHC_DAT6/**SPI_CS2_B**/ GPIO2_02	Data	C36	IO	OV_{DD}	---
SDHC_DAT7/**SPI_CS3_B**/ GPIO2_03	Data	D36	IO	OV_{DD}	---
SDHC_WP	Card Write Protection	C33	I	OV_{DD}	26
Programmable Interrupt Controller					
IRQ00	External Interrupts	V43	I	OV_{DD}	1
IRQ01	External Interrupts	V44	I	OV_{DD}	1
IRQ02	External Interrupts	U43	I	OV_{DD}	1
IRQ03/GPIO1_23	External Interrupts	W42	I	OV_{DD}	1
IRQ04/GPIO1_24	External Interrupts	U44	I	OV_{DD}	1
IRQ05/GPIO1_25	External Interrupts	R42	I	OV_{DD}	1
IRQ06/GPIO1_26	External Interrupts	W41	I	OV_{DD}	1
IRQ07/GPIO1_27	External Interrupts	T42	I	OV_{DD}	1
IRQ08/GPIO1_28	External Interrupts	T44	I	OV_{DD}	1
IRQ09/GPIO1_29	External Interrupts	V42	I	OV_{DD}	1
IRQ10/GPIO1_30	External Interrupts	W44	I	OV_{DD}	1
IRQ11/GPIO1_31	External Interrupts	U42	I	OV_{DD}	1
IRQ_OUT_B/EVT9_B	Interrupt Output	T41	O	OV_{DD}	1, 6, 7
LP Trust					
LP_TMP_DETECT_B	Low Power Tamper Detect	T27	I	V_{DD}_LP	---
Trust					
TMP_DETECT_B	Tamper Detect	E35	I	OV_{DD}	1
System Control					
HRESET_B	Hard Reset	D35	IO	OV_{DD}	6, 7
PORESET_B	Power On Reset	F35	I	OV_{DD}	---
RESET_REQ_B	Reset Request (POR or Hard)	G33	O	OV_{DD}	1, 5

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
Power Management					
ASLEEP/GPIO1_13/ cfg_xvdd_sel	Asleep	G34	O	OV_{DD}	1, 4
Clocking					
RTC/GPIO1_14	Real Time Clock	V33	I	OV_{DD}	1
SYSCLK	System Clock	U34	I	OV_{DD}	---
DDR Clocking					
DDRCLK	DDR Controllers Clock	AL14	I	OV_{DD}	---
Debug					
CKSTP_OUT_B	Checkstop Out	L44	O	OV_{DD}	1, 6, 7
CLK_OUT	Clock Out	N44	O	OV_{DD}	2
EVT0_B	Event 0	N42	IO	OV_{DD}	9
EVT1_B	Event 1	M43	IO	OV_{DD}	---
EVT2_B	Event 2	M42	IO	OV_{DD}	---
EVT3_B	Event 3	L43	IO	OV_{DD}	---
EVT4_B	Event 4	L42	IO	OV_{DD}	---
EVT5_B/**IIC4_SCL**/GPIO4_02	Event 5	N12	IO	DV_{DD}	---
EVT6_B/**IIC4_SDA**/GPIO4_03	Event 6	P12	IO	DV_{DD}	---
EVT7_B/**DMA2_DACK0_B**/ GPIO4_08	Event 7	P44	IO	OV_{DD}	---
EVT8_B/**DMA2_DDONE0_B**/ GPIO4_09	Event 8	P42	IO	OV_{DD}	---
EVT9_B/**IRQ_OUT_B**	Event 9	T41	IO	OV_{DD}	---
DFT					
SCAN_MODE_B	Reserved for internal use only	E33	I	OV_{DD}	10
TEST_SEL	Reserved for internal use only	F34	I	OV_{DD}	15
JTAG					
TCK	Test Clock	K44	I	OV_{DD}	---
TDI	Test Data In	J43	I	OV_{DD}	9
TDO	Test Data Out	K42	O	OV_{DD}	2
TMS	Test Mode Select	K41	I	OV_{DD}	9
TRST_B	Test Reset	J42	I	OV_{DD}	9
SerDes 1					
SD1_IMP_CAL_RX	SerDes Receive Impedence Calibration	M16	I	$S1V_{DD}$	11
SD1_IMP_CAL_TX	SerDes Transmit Impedance Calibration	M22	I	$X1V_{DD}$	16
SD1_PLL1_TPA	Reserved for internal use only	M18	O	AVDD_SD1_PLL1	12
SD1_PLL1_TPD	Reserved for internal use only	L16	O	$X1V_{DD}$	12

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD1_PLL2_TPA	Reserved for internal use only	M20	O	AVDD_SD1_PLL2	12
SD1_PLL2_TPD	Reserved for internal use only	L22	O	$X1V_{DD}$	12
SD1_REF_CLK1	SerDes PLL 1 Reference Clock	P18	I	$S1V_{DD}$	---
SD1_REF_CLK1_B	SerDes PLL 1 Reference Clock Complement	P19	I	$S1V_{DD}$	---
SD1_REF_CLK2	SerDes PLL 2 Reference Clock	P21	I	$S1V_{DD}$	---
SD1_REF_CLK2_B	SerDes PLL 2 Reference Clock Complement	N21	I	$S1V_{DD}$	---
SD1_RX4	SerDes Receive Data (positive)	C19	I	$S1V_{DD}$	---
SD1_RX4_B	SerDes Receive Data (negative)	D19	I	$S1V_{DD}$	---
SD1_RX5	SerDes Receive Data (positive)	A20	I	$S1V_{DD}$	---
SD1_RX5_B	SerDes Receive Data (negative)	B20	I	$S1V_{DD}$	---
SD1_RX6	SerDes Receive Data (positive)	C21	I	$S1V_{DD}$	---
SD1_RX6_B	SerDes Receive Data (negative)	D21	I	$S1V_{DD}$	---
SD1_RX7	SerDes Receive Data (positive)	A22	I	$S1V_{DD}$	---
SD1_RX7_B	SerDes Receive Data (negative)	B22	I	$S1V_{DD}$	---
SD1_TX4	SerDes Transmit Data (positive)	H19	O	$X1V_{DD}$	---
SD1_TX4_B	SerDes Transmit Data (negative)	J19	O	$X1V_{DD}$	---
SD1_TX5	SerDes Transmit Data (positive)	F20	O	$X1V_{DD}$	---
SD1_TX5_B	SerDes Transmit Data (negative)	G20	O	$X1V_{DD}$	---
SD1_TX6	SerDes Transmit Data (positive)	H21	O	$X1V_{DD}$	---
SD1_TX6_B	SerDes Transmit Data (negative)	J21	O	$X1V_{DD}$	---
SD1_TX7	SerDes Transmit Data (positive)	F22	O	$X1V_{DD}$	---
SD1_TX7_B	SerDes Transmit Data (negative)	G22	O	$X1V_{DD}$	---
SerDes 2					
SD2_IMP_CAL_RX	SerDes Receive Impedence Calibration	M23	I	$S2V_{DD}$	11

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD2_IMP_CAL_TX	SerDes Transmit Impedance Calibration	M29	I	$X2V_{DD}$	16
SD2_PLL1_TPA	Reserved for internal use only	M25	O	AVDD_SD2_PLL1	12
SD2_PLL1_TPD	Reserved for internal use only	L23	O	$X2V_{DD}$	12
SD2_PLL2_TPA	Reserved for internal use only	M27	O	AVDD_SD2_PLL2	12
SD2_PLL2_TPD	Reserved for internal use only	L29	O	$X2V_{DD}$	12
SD2_REF_CLK1	SerDes PLL 1 Reference Clock	P24	I	$S2V_{DD}$	---
SD2_REF_CLK1_B	SerDes PLL 1 Reference Clock Complement	N24	I	$S2V_{DD}$	---
SD2_REF_CLK2	SerDes PLL 2 Reference Clock	P27	I	$S2V_{DD}$	---
SD2_REF_CLK2_B	SerDes PLL 2 Reference Clock Complement	P26	I	$S2V_{DD}$	---
SD2_RX0	SerDes Receive Data (positive)	C23	I	$S2V_{DD}$	---
SD2_RX0_B	SerDes Receive Data (negative)	D23	I	$S2V_{DD}$	---
SD2_RX1	SerDes Receive Data (positive)	A24	I	$S2V_{DD}$	---
SD2_RX1_B	SerDes Receive Data (negative)	B24	I	$S2V_{DD}$	---
SD2_RX2	SerDes Receive Data (positive)	C25	I	$S2V_{DD}$	---
SD2_RX2_B	SerDes Receive Data (negative)	D25	I	$S2V_{DD}$	---
SD2_RX3	SerDes Receive Data (positive)	A26	I	$S2V_{DD}$	---
SD2_RX3_B	SerDes Receive Data (negative)	B26	I	$S2V_{DD}$	---
SD2_RX4	SerDes Receive Data (positive)	C27	I	$S2V_{DD}$	---
SD2_RX4_B	SerDes Receive Data (negative)	D27	I	$S2V_{DD}$	---
SD2_RX5	SerDes Receive Data (positive)	A28	I	$S2V_{DD}$	---
SD2_RX5_B	SerDes Receive Data (negative)	B28	I	$S2V_{DD}$	---
SD2_RX6	SerDes Receive Data (positive)	C29	I	$S2V_{DD}$	---
SD2_RX6_B	SerDes Receive Data (negative)	D29	I	$S2V_{DD}$	---
SD2_RX7	SerDes Receive Data (positive)	A30	I	$S2V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD2_RX7_B	SerDes Receive Data (negative)	B30	I	S2V $_{DD}$	---
SD2_TX0	SerDes Transmit Data (positive)	H23	O	X2V $_{DD}$	---
SD2_TX0_B	SerDes Transmit Data (negative)	J23	O	X2V $_{DD}$	---
SD2_TX1	SerDes Transmit Data (positive)	F24	O	X2V $_{DD}$	---
SD2_TX1_B	SerDes Transmit Data (negative)	G24	O	X2V $_{DD}$	---
SD2_TX2	SerDes Transmit Data (positive)	H25	O	X2V $_{DD}$	---
SD2_TX2_B	SerDes Transmit Data (negative)	J25	O	X2V $_{DD}$	---
SD2_TX3	SerDes Transmit Data (positive)	F26	O	X2V $_{DD}$	---
SD2_TX3_B	SerDes Transmit Data (negative)	G26	O	X2V $_{DD}$	---
SD2_TX4	SerDes Transmit Data (positive)	H27	O	X2V $_{DD}$	---
SD2_TX4_B	SerDes Transmit Data (negative)	J27	O	X2V $_{DD}$	---
SD2_TX5	SerDes Transmit Data (positive)	F28	O	X2V $_{DD}$	---
SD2_TX5_B	SerDes Transmit Data (negative)	G28	O	X2V $_{DD}$	---
SD2_TX6	SerDes Transmit Data (positive)	H29	O	X2V $_{DD}$	---
SD2_TX6_B	SerDes Transmit Data (negative)	J29	O	X2V $_{DD}$	---
SD2_TX7	SerDes Transmit Data (positive)	F30	O	X2V $_{DD}$	---
SD2_TX7_B	SerDes Transmit Data (negative)	G30	O	X2V $_{DD}$	---
SerDes 3					
SD3_IMP_CAL_RX	SerDes Receive Impedence Calibration	AN19	I	S3V $_{DD}$	11
SD3_IMP_CAL_TX	SerDes Transmit Impedance Calibration	AN25	I	X3V $_{DD}$	16
SD3_PLL1_TPA	Reserved for internal use only	AN21	O	AVDD_SD3_PLL1	12
SD3_PLL1_TPD	Reserved for internal use only	AP19	O	X3V $_{DD}$	12
SD3_PLL2_TPA	Reserved for internal use only	AN23	O	AVDD_SD3_PLL2	12
SD3_PLL2_TPD	Reserved for internal use only	AP25	O	X3V $_{DD}$	12

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD3_REF_CLK1	SerDes PLL 1 Reference Clock	AL21	I	$S3V_{DD}$	---
SD3_REF_CLK1_B	SerDes PLL 1 Reference Clock Complement	AL22	I	$S3V_{DD}$	---
SD3_REF_CLK2	SerDes PLL 2 Reference Clock	AL24	I	$S3V_{DD}$	---
SD3_REF_CLK2_B	SerDes PLL 2 Reference Clock Complement	AM24	I	$S3V_{DD}$	---
SD3_RX0	SerDes Receive Data (positive)	BB18	I	$S3V_{DD}$	---
SD3_RX0_B	SerDes Receive Data (negative)	BA18	I	$S3V_{DD}$	---
SD3_RX1	SerDes Receive Data (positive)	BD19	I	$S3V_{DD}$	---
SD3_RX1_B	SerDes Receive Data (negative)	BC19	I	$S3V_{DD}$	---
SD3_RX2	SerDes Receive Data (positive)	BB20	I	$S3V_{DD}$	---
SD3_RX2_B	SerDes Receive Data (negative)	BA20	I	$S3V_{DD}$	---
SD3_RX3	SerDes Receive Data (positive)	BD21	I	$S3V_{DD}$	---
SD3_RX3_B	SerDes Receive Data (negative)	BC21	I	$S3V_{DD}$	---
SD3_RX4	SerDes Receive Data (positive)	BB22	I	$S3V_{DD}$	---
SD3_RX4_B	SerDes Receive Data (negative)	BA22	I	$S3V_{DD}$	---
SD3_RX5	SerDes Receive Data (positive)	BD23	I	$S3V_{DD}$	---
SD3_RX5_B	SerDes Receive Data (negative)	BC23	I	$S3V_{DD}$	---
SD3_RX6	SerDes Receive Data (positive)	BB24	I	$S3V_{DD}$	---
SD3_RX6_B	SerDes Receive Data (negative)	BA24	I	$S3V_{DD}$	---
SD3_RX7	SerDes Receive Data (positive)	BD25	I	$S3V_{DD}$	---
SD3_RX7_B	SerDes Receive Data (negative)	BC25	I	$S3V_{DD}$	---
SD3_TX0	SerDes Transmit Data (positive)	AU18	O	$X3V_{DD}$	---
SD3_TX0_B	SerDes Transmit Data (negative)	AT18	O	$X3V_{DD}$	---
SD3_TX1	SerDes Transmit Data (positive)	AW19	O	$X3V_{DD}$	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD3_TX1_B	SerDes Transmit Data (negative)	AV19	O	$X3V_{DD}$	---
SD3_TX2	SerDes Transmit Data (positive)	AU20	O	$X3V_{DD}$	---
SD3_TX2_B	SerDes Transmit Data (negative)	AT20	O	$X3V_{DD}$	---
SD3_TX3	SerDes Transmit Data (positive)	AW21	O	$X3V_{DD}$	---
SD3_TX3_B	SerDes Transmit Data (negative)	AV21	O	$X3V_{DD}$	---
SD3_TX4	SerDes Transmit Data (positive)	AU22	O	$X3V_{DD}$	---
SD3_TX4_B	SerDes Transmit Data (negative)	AT22	O	$X3V_{DD}$	---
SD3_TX5	SerDes Transmit Data (positive)	AW23	O	$X3V_{DD}$	---
SD3_TX5_B	SerDes Transmit Data (negative)	AV23	O	$X3V_{DD}$	---
SD3_TX6	SerDes Transmit Data (positive)	AU24	O	$X3V_{DD}$	---
SD3_TX6_B	SerDes Transmit Data (negative)	AT24	O	$X3V_{DD}$	---
SD3_TX7	SerDes Transmit Data (positive)	AW25	O	$X3V_{DD}$	---
SD3_TX7_B	SerDes Transmit Data (negative)	AV25	O	$X3V_{DD}$	---
SerDes 4					
SD4_IMP_CAL_RX	SerDes Receive Impedence Calibration	AN26	I	$S4V_{DD}$	11
SD4_IMP_CAL_TX	SerDes Transmit Impedance Calibration	AN32	I	$X4V_{DD}$	16
SD4_PLL1_TPA	Reserved for internal use only	AN28	O	AVDD_SD4_PLL1	12
SD4_PLL1_TPD	Reserved for internal use only	AP26	O	$X4V_{DD}$	12
SD4_PLL2_TPA	Reserved for internal use only	AN30	O	AVDD_SD4_PLL2	12
SD4_PLL2_TPD	Reserved for internal use only	AP32	O	$X4V_{DD}$	12
SD4_REF_CLK1	SerDes PLL 1 Reference Clock	AL27	I	$S4V_{DD}$	---
SD4_REF_CLK1_B	SerDes PLL 1 Reference Clock Complement	AM27	I	$S4V_{DD}$	---
SD4_REF_CLK2	SerDes PLL 2 Reference Clock	AL30	I	$S4V_{DD}$	---
SD4_REF_CLK2_B	SerDes PLL 2 Reference Clock Complement	AL29	I	$S4V_{DD}$	---
SD4_RX4	SerDes Receive Data (positive)	BB30	I	$S4V_{DD}$	---

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Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SD4_RX4_B	SerDes Receive Data (negative)	BA30	I	$S4V_{DD}$	---
SD4_RX5	SerDes Receive Data (positive)	BD31	I	$S4V_{DD}$	---
SD4_RX5_B	SerDes Receive Data (negative)	BC31	I	$S4V_{DD}$	---
SD4_RX6	SerDes Receive Data (positive)	BB32	I	$S4V_{DD}$	---
SD4_RX6_B	SerDes Receive Data (negative)	BA32	I	$S4V_{DD}$	---
SD4_RX7	SerDes Receive Data (positive)	BD33	I	$S4V_{DD}$	---
SD4_RX7_B	SerDes Receive Data (negative)	BC33	I	$S4V_{DD}$	---
SD4_TX4	SerDes Transmit Data (positive)	AU30	O	$X4V_{DD}$	---
SD4_TX4_B	SerDes Transmit Data (negative)	AT30	O	$X4V_{DD}$	---
SD4_TX5	SerDes Transmit Data (positive)	AW31	O	$X4V_{DD}$	---
SD4_TX5_B	SerDes Transmit Data (negative)	AV31	O	$X4V_{DD}$	---
SD4_TX6	SerDes Transmit Data (positive)	AU32	O	$X4V_{DD}$	---
SD4_TX6_B	SerDes Transmit Data (negative)	AT32	O	$X4V_{DD}$	---
SD4_TX7	SerDes Transmit Data (positive)	AW33	O	$X4V_{DD}$	---
SD4_TX7_B	SerDes Transmit Data (negative)	AV33	O	$X4V_{DD}$	---
USB PHY 1 & 2					
USB1_DRVVBUS	USB PHY Digital signal - Drive VBUS	E32	O	USB_HV_{DD}	---
USB1_PWRFAULT	USB PHY Digital signal - Power Fault	F32	I	USB_HV_{DD}	---
USB1_UDM	USB PHY Data Minus	J31	IO	USB_HV_{DD}	---
USB1_UDP	USB PHY Data Plus	K31	IO	USB_HV_{DD}	---
USB1_UID	USB PHY ID Detect	L32	I	USB_OV_{DD}	---
USB1_VBUSCLMP	USB PHY VBUS	G32	I	USB_HV_{DD}	---
USB2_DRVVBUS	USB PHY Digital signal - Drive VBUS	A32	O	USB_HV_{DD}	---
USB2_PWRFAULT	USB PHY Digital signal - Power Fault	B32	I	USB_HV_{DD}	---

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Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
USB2_UDM	USB PHY Data Minus	M31	IO	USB_HV_{DD}	---
USB2_UDP	USB PHY Data Plus	N31	IO	USB_HV_{DD}	---
USB2_UID	USB PHY ID Detect	H32	I	USB_OV_{DD}	---
USB2_VBUSCLMP	USB PHY VBUS	C32	I	USB_HV_{DD}	---
USB_IBIAS_REXT	USB PHY Impedance Calibration	D31	IO	-	23
USB CLK					
USBCLK	USB PHY Clock In	E34	I	OV_{DD}	---
IEEE1588					
TSEC_1588_ALARM_OUT1/ GPIO3_03	Alarm Out 1	K13	O	LV_{DD}	1
TSEC_1588_ALARM_OUT2/ GPIO3_04	Alarm Out 2	J12	O	LV_{DD}	1
TSEC_1588_CLK_IN/ GPIO3_00	Clock In	A14	I	LV_{DD}	1
TSEC_1588_CLK_OUT/ GPIO3_05	Clock Out	F14	O	LV_{DD}	1
TSEC_1588_PULSE_OUT1/ GPIO3_06	Pulse Out 1	M14	O	LV_{DD}	1
TSEC_1588_PULSE_OUT2/ GPIO3_07	Pulse Out 2	L13	O	LV_{DD}	1
TSEC_1588_TRIG_IN1/ GPIO3_01	Trigger In 1	N15	I	LV_{DD}	1
TSEC_1588_TRIG_IN2/ GPIO3_02	Trigger In 2	N14	I	LV_{DD}	1
Ethernet Management Interface 1					
EMI1_MDC	Management Data Clock	G13	O	LV_{DD}	---
EMI1_MDIO	Management Data In/Out	H13	IO	LV_{DD}	6
Ethernet Management Interface 2					
EMI2_MDC	Management Data Clock (1.2V open drain)	D13	O	OV_{DD}	7, 13
EMI2_MDIO	Management Data In/Out (1.2V open drain)	E13	IO	OV_{DD}	7, 13
Ethernet Controller 1					
EC1_GTX_CLK/GPIO3_13	Transmit Clock Out	F12	O	LV_{DD}	1
EC1_GTX_CLK125	Reference Clock	D12	I	LV_{DD}	---
EC1_RXD0/GPIO3_19	Receive Data	C12	I	LV_{DD}	1
EC1_RXD1/GPIO3_18	Receive Data	E12	I	LV_{DD}	1
EC1_RXD2/GPIO3_17	Receive Data	A12	I	LV_{DD}	1
EC1_RXD3/GPIO3_16	Receive Data	G12	I	LV_{DD}	1
EC1_RX_CLK/GPIO3_15	Receive Clock	B12	I	LV_{DD}	1

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
EC1_RX_DV/GPIO3_14	Receive Data Valid	A13	I	LV_{DD}	1
EC1_TXD0/GPIO3_11	Transmit Data	H12	O	LV_{DD}	1
EC1_TXD1/GPIO3_10	Transmit Data	K12	O	LV_{DD}	1
EC1_TXD2/GPIO3_09	Transmit Data	L12	O	LV_{DD}	1
EC1_TXD3/GPIO3_08	Transmit Data	M12	O	LV_{DD}	1
EC1_TX_EN/GPIO3_12	Transmit Enable	C13	O	LV_{DD}	1, 14
Ethernet Controller 2					
EC2_GTX_CLK/GPIO3_25	Transmit Clock Out	H10	O	LV_{DD}	1
EC2_GTX_CLK125	Reference Clock	E10	I	LV_{DD}	---
EC2_RXD0/GPIO3_31	Receive Data	A10	I	LV_{DD}	1
EC2_RXD1/GPIO3_30	Receive Data	A11	I	LV_{DD}	1
EC2_RXD2/GPIO3_29	Receive Data	C11	I	LV_{DD}	1
EC2_RXD3/GPIO3_28	Receive Data	D10	I	LV_{DD}	1
EC2_RX_CLK/GPIO3_27	Receive Clock	B10	I	LV_{DD}	1
EC2_RX_DV/GPIO3_26	Receive Data Valid	C10	I	LV_{DD}	1
EC2_TXD0/GPIO3_23	Transmit Data	D11	O	LV_{DD}	1
EC2_TXD1/GPIO3_22	Transmit Data	F10	O	LV_{DD}	1
EC2_TXD2/GPIO3_21	Transmit Data	F11	O	LV_{DD}	1
EC2_TXD3/GPIO3_20	Transmit Data	G11	O	LV_{DD}	1
EC2_TX_EN/GPIO3_24	Transmit Enable	G10	O	LV_{DD}	1, 14
DMA					
DMA1_DACK0_B/GPIO4_05	DMA1 channel 0 acknowledge	R43	O	OV_{DD}	1
DMA1_DDONE0_B/GPIO4_06	DMA1 channel 0 done	R44	O	OV_{DD}	1
DMA1_DREQ0_B/GPIO4_04	DMA1 channel 0 request	P43	I	OV_{DD}	1
DMA2_DACK0_B/GPIO4_08/ EVT7_B	DMA2 channel 0 acknowledge	P44	O	OV_{DD}	1
DMA2_DDONE0_B/ GPIO4_09/EVT8_B	DMA2 channel 0 done	P42	O	OV_{DD}	1
DMA2_DREQ0_B/GPIO4_07	DMA2 channel 0 request	N41	I	OV_{DD}	1
Analog signals					
D1_MVREF	SSTL1.35/1.5 Reference Voltage	V13	I	$G1V_{DD}/2$	---
D1_TPA	Reserved for internal use only	AL13	-	-	12
D2_MVREF	SSTL1.35/1.5 Reference Voltage	AH13	I	$G2V_{DD}/2$	---
D2_TPA	Reserved for internal use only	AM13	-	-	12
FA_ANALOG_G_V	Reserved for internal use only	R32	-	-	15
FA_ANALOG_PIN	Reserved for internal use only	T32	-	-	15
TD1_ANODE	Thermal diode anode pin	AA34	-	Internal Diode	19, 24

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Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
TD1_CATHODE	Thermal diode cathode pin	Y34	-	Internal Diode	19, 24
TD2_ANODE	Thermal diode anode pin	AL16	-	Internal Diode	19, 24
TD2_CATHODE	Thermal diode cathode pin	AL17	-	Internal Diode	19, 24
TH_TPA	Thermal Test Point Analog	W32	-	-	12
Power-On-Reset Configuration					
cfg_dram_type/**IFC_AD21**	Power-On-Reset Configuration Signal	J40	I	OV_{DD}	1, 4
cfg_gpinput0/**IFC_AD00**	Power-On-Reset Configuration Signal	W39	I	OV_{DD}	1, 4
cfg_gpinput1/**IFC_AD01**	Power-On-Reset Configuration Signal	W40	I	OV_{DD}	1, 4
cfg_gpinput2/**IFC_AD02**	Power-On-Reset Configuration Signal	V39	I	OV_{DD}	1, 4
cfg_gpinput3/**IFC_AD03**	Power-On-Reset Configuration Signal	V40	I	OV_{DD}	1, 4
cfg_gpinput4/**IFC_AD04**	Power-On-Reset Configuration Signal	U40	I	OV_{DD}	1, 4
cfg_gpinput5/**IFC_AD05**	Power-On-Reset Configuration Signal	U41	I	OV_{DD}	1, 4
cfg_gpinput6/**IFC_AD06**	Power-On-Reset Configuration Signal	T39	I	OV_{DD}	1, 4
cfg_gpinput7/**IFC_AD07**	Power-On-Reset Configuration Signal	T40	I	OV_{DD}	1, 4
cfg_ifc_te/**IFC_TE**	Power-On-Reset Configuration Signal	G42	I	OV_{DD}	1, 4
cfg_rcw_src0/**IFC_AD08**	Power-On-Reset Configuration Signal	R39	I	OV_{DD}	1, 4
cfg_rcw_src1/**IFC_AD09**	Power-On-Reset Configuration Signal	R40	I	OV_{DD}	1, 4
cfg_rcw_src2/**IFC_AD10**	Power-On-Reset Configuration Signal	P40	I	OV_{DD}	1, 4
cfg_rcw_src3/**IFC_AD11**	Power-On-Reset Configuration Signal	P41	I	OV_{DD}	1, 4
cfg_rcw_src4/**IFC_AD12**	Power-On-Reset Configuration Signal	N39	I	OV_{DD}	1, 4
cfg_rcw_src5/**IFC_AD13**	Power-On-Reset Configuration Signal	N40	I	OV_{DD}	1, 4
cfg_rcw_src6/**IFC_AD14**	Power-On-Reset Configuration Signal	M39	I	OV_{DD}	1, 4
cfg_rcw_src7/**IFC_AD15**	Power-On-Reset Configuration Signal	M40	I	OV_{DD}	1, 4
cfg_rcw_src8/**IFC_CLE**	Power-On-Reset Configuration Signal	E43	I	OV_{DD}	1, 4

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
cfg_xvdd_sel/**ASLEEP**/ GPIO1_13	Power-On-Reset Configuration Signal	G34	I	OV_{DD}	1, 4
General Purpose Input/Output					
GPIO1_09/**IFC_CS4_B**	General Purpose Input/Output	C41	IO	OV_{DD}	---
GPIO1_10/**IFC_CS5_B**	General Purpose Input/Output	B41	IO	OV_{DD}	---
GPIO1_11/**IFC_CS6_B**	General Purpose Input/Output	A41	IO	OV_{DD}	---
GPIO1_12/**IFC_CS7_B**	General Purpose Input/Output	C40	IO	OV_{DD}	---
GPIO1_13/**ASLEEP**/ cfg_xvdd_sel	General Purpose Input/Output	G34	O	OV_{DD}	1, 4
GPIO1_14/**RTC**	General Purpose Input/Output	V33	IO	OV_{DD}	---
GPIO1_15/**UART1_SOUT**	General Purpose Input/Output	L10	IO	DV_{DD}	---
GPIO1_16/**UART2_SOUT**	General Purpose Input/Output	J10	IO	DV_{DD}	---
GPIO1_17/**UART1_SIN**	General Purpose Input/Output	M11	IO	DV_{DD}	---
GPIO1_18/**UART2_SIN**	General Purpose Input/Output	J11	IO	DV_{DD}	---
GPIO1_19/**UART1_RTS_B**/ UART3_SOUT	General Purpose Input/Output	M10	IO	DV_{DD}	---
GPIO1_20/**UART2_RTS_B**/ UART4_SOUT	General Purpose Input/Output	K10	IO	DV_{DD}	---
GPIO1_21/**UART1_CTS_B**/ UART3_SIN	General Purpose Input/Output	N11	IO	DV_{DD}	---
GPIO1_22/**UART2_CTS_B**/ UART4_SIN	General Purpose Input/Output	K11	IO	DV_{DD}	---
GPIO1_23/**IRQ03**	General Purpose Input/Output	W42	IO	OV_{DD}	---
GPIO1_24/**IRQ04**	General Purpose Input/Output	U44	IO	OV_{DD}	---
GPIO1_25/**IRQ05**	General Purpose Input/Output	R42	IO	OV_{DD}	---
GPIO1_26/**IRQ06**	General Purpose Input/Output	W41	IO	OV_{DD}	---
GPIO1_27/**IRQ07**	General Purpose Input/Output	T42	IO	OV_{DD}	---
GPIO1_28/**IRQ08**	General Purpose Input/Output	T44	IO	OV_{DD}	---
GPIO1_29/**IRQ09**	General Purpose Input/Output	V42	IO	OV_{DD}	---
GPIO1_30/**IRQ10**	General Purpose Input/Output	W44	IO	OV_{DD}	---
GPIO1_31/**IRQ11**	General Purpose Input/Output	U42	IO	OV_{DD}	---
GPIO2_00/**SPI_CS0_B**/ SDHC_DAT4	General Purpose Input/Output	C35	IO	OV_{DD}	---
GPIO2_01/**SPI_CS1_B**/ SDHC_DAT5	General Purpose Input/Output	A36	IO	OV_{DD}	---
GPIO2_02/**SPI_CS2_B**/ SDHC_DAT6	General Purpose Input/Output	C36	IO	OV_{DD}	---
GPIO2_03/**SPI_CS3_B**/ SDHC_DAT7	General Purpose Input/Output	D36	IO	OV_{DD}	---
GPIO2_04/**SDHC_CMD**	General Purpose Input/Output	D33	IO	OV_{DD}	---
GPIO2_05/**SDHC_DAT0**	General Purpose Input/Output	B34	IO	OV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GPIO2_06/**SDHC_DAT1**	General Purpose Input/Output	C34	IO	OV_{DD}	---
GPIO2_07/**SDHC_DAT2**	General Purpose Input/Output	A35	IO	OV_{DD}	---
GPIO2_08/**SDHC_DAT3**	General Purpose Input/Output	B35	IO	OV_{DD}	---
GPIO2_09/**SDHC_CLK**	General Purpose Input/Output	A33	IO	OV_{DD}	---
GPIO2_10/**IFC_CS1_B**	General Purpose Input/Output	C44	IO	OV_{DD}	---
GPIO2_11/**IFC_CS2_B**	General Purpose Input/Output	B43	IO	OV_{DD}	---
GPIO2_12/**IFC_CS3_B**	General Purpose Input/Output	A42	IO	OV_{DD}	---
GPIO2_13/**IFC_PAR0**	General Purpose Input/Output	E38	IO	OV_{DD}	---
GPIO2_14/**IFC_PAR1**	General Purpose Input/Output	D38	IO	OV_{DD}	---
GPIO2_15/**IFC_PERR_B**	General Purpose Input/Output	E37	IO	OV_{DD}	---
GPIO2_16/**IFC_PAR2**	General Purpose Input/Output	F38	IO	OV_{DD}	---
GPIO2_17/**IFC_PAR3**	General Purpose Input/Output	F37	IO	OV_{DD}	---
GPIO2_18/**IFC_A26**	General Purpose Input/Output	B40	IO	OV_{DD}	---
GPIO2_19/**IFC_A27**	General Purpose Input/Output	A40	IO	OV_{DD}	---
GPIO2_20/**IFC_A28**	General Purpose Input/Output	D39	IO	OV_{DD}	---
GPIO2_21/**IFC_A29**	General Purpose Input/Output	C39	IO	OV_{DD}	---
GPIO2_22/**IFC_A30**	General Purpose Input/Output	A39	IO	OV_{DD}	---
GPIO2_23/**IFC_A31**	General Purpose Input/Output	C38	IO	OV_{DD}	---
GPIO2_25/**IFC_AD25**/ IFC_WP1_B	General Purpose Input/Output	G41	IO	OV_{DD}	---
GPIO2_26/**IFC_AD26**/ IFC_WP2_B	General Purpose Input/Output	G39	IO	OV_{DD}	---
GPIO2_27/**IFC_AD27**/ IFC_WP3_B	General Purpose Input/Output	F40	IO	OV_{DD}	---
GPIO2_28/**IFC_AD28**	General Purpose Input/Output	E41	IO	OV_{DD}	---
GPIO2_29/**IFC_AD29**/ IFC_RB2_B	General Purpose Input/Output	E40	IO	OV_{DD}	---
GPIO2_30/**IFC_AD30**/ IFC_RB3_B	General Purpose Input/Output	E39	IO	OV_{DD}	---
GPIO2_31/**IFC_AD31**/ IFC_RB4_B	General Purpose Input/Output	D41	IO	OV_{DD}	---
GPIO3_00/ **TSEC_1588_CLK_IN**	General Purpose Input/Output	A14	IO	LV_{DD}	---
GPIO3_01/ **TSEC_1588_TRIG_IN1**	General Purpose Input/Output	N15	IO	LV_{DD}	---
GPIO3_02/ **TSEC_1588_TRIG_IN2**	General Purpose Input/Output	N14	IO	LV_{DD}	---
GPIO3_03/ **TSEC_1588_ALARM_OUT1**	General Purpose Input/Output	K13	IO	LV_{DD}	---
GPIO3_04/ **TSEC_1588_ALARM_OUT2**	General Purpose Input/Output	J12	IO	LV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GPIO3_05/ **TSEC_1588_CLK_OUT**	General Purpose Input/Output	F14	IO	LV_{DD}	---
GPIO3_06/ **TSEC_1588_PULSE_OUT1**	General Purpose Input/Output	M14	IO	LV_{DD}	---
GPIO3_07/ **TSEC_1588_PULSE_OUT2**	General Purpose Input/Output	L13	IO	LV_{DD}	---
GPIO3_08/**EC1_TXD3**	General Purpose Input/Output	M12	IO	LV_{DD}	---
GPIO3_09/**EC1_TXD2**	General Purpose Input/Output	L12	IO	LV_{DD}	---
GPIO3_10/**EC1_TXD1**	General Purpose Input/Output	K12	IO	LV_{DD}	---
GPIO3_11/**EC1_TXD0**	General Purpose Input/Output	H12	IO	LV_{DD}	---
GPIO3_12/**EC1_TX_EN**	General Purpose Input/Output	C13	IO	LV_{DD}	---
GPIO3_13/**EC1_GTX_CLK**	General Purpose Input/Output	F12	IO	LV_{DD}	---
GPIO3_14/**EC1_RX_DV**	General Purpose Input/Output	A13	IO	LV_{DD}	---
GPIO3_15/**EC1_RX_CLK**	General Purpose Input/Output	B12	IO	LV_{DD}	---
GPIO3_16/**EC1_RXD3**	General Purpose Input/Output	G12	IO	LV_{DD}	---
GPIO3_17/**EC1_RXD2**	General Purpose Input/Output	A12	IO	LV_{DD}	---
GPIO3_18/**EC1_RXD1**	General Purpose Input/Output	E12	IO	LV_{DD}	---
GPIO3_19/**EC1_RXD0**	General Purpose Input/Output	C12	IO	LV_{DD}	---
GPIO3_20/**EC2_TXD3**	General Purpose Input/Output	G11	IO	LV_{DD}	---
GPIO3_21/**EC2_TXD2**	General Purpose Input/Output	F11	IO	LV_{DD}	---
GPIO3_22/**EC2_TXD1**	General Purpose Input/Output	F10	IO	LV_{DD}	---
GPIO3_23/**EC2_TXD0**	General Purpose Input/Output	D11	IO	LV_{DD}	---
GPIO3_24/**EC2_TX_EN**	General Purpose Input/Output	G10	IO	LV_{DD}	---
GPIO3_25/**EC2_GTX_CLK**	General Purpose Input/Output	H10	IO	LV_{DD}	---
GPIO3_26/**EC2_RX_DV**	General Purpose Input/Output	C10	IO	LV_{DD}	---
GPIO3_27/**EC2_RX_CLK**	General Purpose Input/Output	B10	IO	LV_{DD}	---
GPIO3_28/**EC2_RXD3**	General Purpose Input/Output	D10	IO	LV_{DD}	---
GPIO3_29/**EC2_RXD2**	General Purpose Input/Output	C11	IO	LV_{DD}	---
GPIO3_30/**EC2_RXD1**	General Purpose Input/Output	A11	IO	LV_{DD}	---
GPIO3_31/**EC2_RXD0**	General Purpose Input/Output	A10	IO	LV_{DD}	---
GPIO4_00/**IIC3_SCL**	General Purpose Input/Output	N13	IO	DV_{DD}	---
GPIO4_01/**IIC3_SDA**	General Purpose Input/Output	P13	IO	DV_{DD}	---
GPIO4_02/**IIC4_SCL**/EVT5_B	General Purpose Input/Output	N12	IO	DV_{DD}	---
GPIO4_03/**IIC4_SDA**/EVT6_B	General Purpose Input/Output	P12	IO	DV_{DD}	---
GPIO4_04/**DMA1_DREQ0_B**	General Purpose Input/Output	P43	IO	OV_{DD}	---
GPIO4_05/**DMA1_DACK0_B**	General Purpose Input/Output	R43	IO	OV_{DD}	---
GPIO4_06/**DMA1_DDONE0_B**	General Purpose Input/Output	R44	IO	OV_{DD}	---
GPIO4_07/**DMA2_DREQ0_B**	General Purpose Input/Output	N41	IO	OV_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GPIO4_08/**DMA2_DACK0_B**/ EVT7_B	General Purpose Input/Output	P44	IO	OV_{DD}	---
GPIO4_09/ **DMA2_DDONE0_B**/EVT8_B	General Purpose Input/Output	P42	IO	OV_{DD}	---
Power and Ground Signals					
GND001	GND	A43	---	---	---
GND002	GND	B11	---	---	---
GND003	GND	B13	---	---	---
GND004	GND	B33	---	---	---
GND005	GND	B36	---	---	---
GND006	GND	B39	---	---	---
GND007	GND	B42	---	---	---
GND008	GND	B44	---	---	---
GND009	GND	C4	---	---	---
GND010	GND	C5	---	---	---
GND011	GND	C6	---	---	---
GND012	GND	C7	---	---	---
GND013	GND	C8	---	---	---
GND014	GND	C9	---	---	---
GND015	GND	D3	---	---	---
GND016	GND	D9	---	---	---
GND017	GND	D34	---	---	---
GND018	GND	D37	---	---	---
GND019	GND	D40	---	---	---
GND020	GND	D43	---	---	---
GND021	GND	E3	---	---	---
GND022	GND	E6	---	---	---
GND023	GND	E9	---	---	---
GND024	GND	E11	---	---	---
GND025	GND	F3	---	---	---
GND026	GND	F4	---	---	---
GND027	GND	F8	---	---	---
GND028	GND	F9	---	---	---
GND029	GND	F13	---	---	---
GND030	GND	F33	---	---	---
GND031	GND	F36	---	---	---
GND032	GND	F39	---	---	---
GND033	GND	F41	---	---	---
GND034	GND	G3	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND035	GND	G6	---	---	---
GND036	GND	G9	---	---	---
GND037	GND	G43	---	---	---
GND038	GND	H3	---	---	---
GND039	GND	H9	---	---	---
GND040	GND	H11	---	---	---
GND041	GND	H34	---	---	---
GND042	GND	H37	---	---	---
GND043	GND	H39	---	---	---
GND044	GND	J3	---	---	---
GND045	GND	J5	---	---	---
GND046	GND	J7	---	---	---
GND047	GND	J9	---	---	---
GND048	GND	J13	---	---	---
GND049	GND	J41	---	---	---
GND050	GND	J44	---	---	---
GND051	GND	K3	---	---	---
GND052	GND	K6	---	---	---
GND053	GND	K9	---	---	---
GND054	GND	K33	---	---	---
GND055	GND	K36	---	---	---
GND056	GND	K43	---	---	---
GND057	GND	L3	---	---	---
GND058	GND	L6	---	---	---
GND059	GND	L9	---	---	---
GND060	GND	L11	---	---	---
GND061	GND	L39	---	---	---
GND062	GND	M3	---	---	---
GND063	GND	M6	---	---	---
GND064	GND	M9	---	---	---
GND065	GND	M13	---	---	---
GND066	GND	M34	---	---	---
GND067	GND	M41	---	---	---
GND068	GND	M44	---	---	---
GND069	GND	N3	---	---	---
GND070	GND	N6	---	---	---
GND071	GND	N9	---	---	---
GND072	GND	N37	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND073	GND	N43	---	---	---
GND074	GND	P3	---	---	---
GND075	GND	P6	---	---	---
GND076	GND	P9	---	---	---
GND077	GND	P11	---	---	---
GND078	GND	P14	---	---	---
GND079	GND	P15	---	---	---
GND080	GND	P16	---	---	---
GND081	GND	P33	---	---	---
GND082	GND	P39	---	---	---
GND083	GND	R3	---	---	---
GND084	GND	R6	---	---	---
GND085	GND	R9	---	---	---
GND086	GND	R31	---	---	---
GND087	GND	R41	---	---	---
GND088	GND	T3	---	---	---
GND089	GND	T6	---	---	---
GND090	GND	T9	---	---	---
GND091	GND	T10	---	---	---
GND092	GND	T11	---	---	---
GND093	GND	T12	---	---	---
GND094	GND	T14	---	---	---
GND095	GND	T17	---	---	---
GND096	GND	T31	---	---	---
GND097	GND	T37	---	---	---
GND098	GND	T43	---	---	---
GND099	GND	U3	---	---	---
GND100	GND	U6	---	---	---
GND101	GND	U13	---	---	---
GND102	GND	U14	---	---	---
GND103	GND	U16	---	---	---
GND104	GND	U18	---	---	---
GND105	GND	U20	---	---	---
GND106	GND	U22	---	---	---
GND107	GND	U24	---	---	---
GND108	GND	U26	---	---	---
GND109	GND	U28	---	---	---
GND110	GND	U31	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND111	GND	U33	---	---	---
GND112	GND	U39	---	---	---
GND113	GND	V3	---	---	---
GND114	GND	V6	---	---	---
GND115	GND	V9	---	---	---
GND116	GND	V12	---	---	---
GND117	GND	V14	---	---	---
GND118	GND	V17	---	---	---
GND119	GND	V19	---	---	---
GND120	GND	V21	---	---	---
GND121	GND	V23	---	---	---
GND122	GND	V25	---	---	---
GND123	GND	V27	---	---	---
GND124	GND	V29	---	---	---
GND125	GND	V31	---	---	---
GND126	GND	V34	---	---	---
GND127	GND	V41	---	---	---
GND128	GND	W3	---	---	---
GND129	GND	W6	---	---	---
GND130	GND	W9	---	---	---
GND131	GND	W12	---	---	---
GND132	GND	W13	---	---	---
GND133	GND	W14	---	---	---
GND134	GND	W16	---	---	---
GND135	GND	W18	---	---	---
GND136	GND	W20	---	---	---
GND137	GND	W22	---	---	---
GND138	GND	W24	---	---	---
GND139	GND	W26	---	---	---
GND140	GND	W28	---	---	---
GND141	GND	W31	---	---	---
GND142	GND	W33	---	---	---
GND143	GND	W37	---	---	---
GND144	GND	W43	---	---	---
GND145	GND	Y3	---	---	---
GND146	GND	Y6	---	---	---
GND147	GND	Y9	---	---	---
GND148	GND	Y14	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND149	GND	Y17	---	---	---
GND150	GND	Y19	---	---	---
GND151	GND	Y21	---	---	---
GND152	GND	Y23	---	---	---
GND153	GND	Y25	---	---	---
GND154	GND	Y27	---	---	---
GND155	GND	Y29	---	---	---
GND156	GND	Y31	---	---	---
GND157	GND	Y35	---	---	---
GND158	GND	Y36	---	---	---
GND159	GND	Y37	---	---	---
GND160	GND	Y38	---	---	---
GND161	GND	Y39	---	---	---
GND162	GND	Y40	---	---	---
GND163	GND	Y41	---	---	---
GND164	GND	Y42	---	---	---
GND165	GND	AA3	---	---	---
GND166	GND	AA6	---	---	---
GND167	GND	AA10	---	---	---
GND168	GND	AA11	---	---	---
GND169	GND	AA12	---	---	---
GND170	GND	AA13	---	---	---
GND171	GND	AA14	---	---	---
GND172	GND	AA16	---	---	---
GND173	GND	AA18	---	---	---
GND174	GND	AA20	---	---	---
GND175	GND	AA22	---	---	---
GND176	GND	AA24	---	---	---
GND177	GND	AA26	---	---	---
GND178	GND	AA28	---	---	---
GND179	GND	AA31	---	---	---
GND180	GND	AA35	---	---	---
GND181	GND	AA42	---	---	---
GND182	GND	AB3	---	---	---
GND183	GND	AB4	---	---	---
GND184	GND	AB8	---	---	---
GND185	GND	AB14	---	---	---
GND186	GND	AB17	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND187	GND	AB19	---	---	---
GND188	GND	AB21	---	---	---
GND189	GND	AB23	---	---	---
GND190	GND	AB25	---	---	---
GND191	GND	AB27	---	---	---
GND192	GND	AB29	---	---	---
GND193	GND	AB31	---	---	---
GND194	GND	AB32	---	---	---
GND195	GND	AB33	---	---	---
GND196	GND	AB34	---	---	---
GND197	GND	AB35	---	---	---
GND198	GND	AB42	---	---	---
GND199	GND	AC3	---	---	---
GND200	GND	AC6	---	---	---
GND201	GND	AC8	---	---	---
GND202	GND	AC14	---	---	---
GND203	GND	AC16	---	---	---
GND204	GND	AC18	---	---	---
GND205	GND	AC20	---	---	---
GND206	GND	AC22	---	---	---
GND207	GND	AC24	---	---	---
GND208	GND	AC26	---	---	---
GND209	GND	AC28	---	---	---
GND210	GND	AC31	---	---	---
GND211	GND	AC33	---	---	---
GND212	GND	AC36	---	---	---
GND213	GND	AC37	---	---	---
GND214	GND	AC38	---	---	---
GND215	GND	AC39	---	---	---
GND216	GND	AC40	---	---	---
GND217	GND	AC41	---	---	---
GND218	GND	AC42	---	---	---
GND219	GND	AD3	---	---	---
GND220	GND	AD5	---	---	---
GND221	GND	AD8	---	---	---
GND222	GND	AD10	---	---	---
GND223	GND	AD11	---	---	---
GND224	GND	AD12	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND225	GND	AD13	---	---	---
GND226	GND	AD14	---	---	---
GND227	GND	AD17	---	---	---
GND228	GND	AD19	---	---	---
GND229	GND	AD21	---	---	---
GND230	GND	AD23	---	---	---
GND231	GND	AD25	---	---	---
GND232	GND	AD27	---	---	---
GND233	GND	AD29	---	---	---
GND234	GND	AD31	---	---	---
GND235	GND	AD33	---	---	---
GND236	GND	AD36	---	---	---
GND237	GND	AD39	---	---	---
GND238	GND	AD42	---	---	---
GND239	GND	AE3	---	---	---
GND240	GND	AE7	---	---	---
GND241	GND	AE9	---	---	---
GND242	GND	AE14	---	---	---
GND243	GND	AE16	---	---	---
GND244	GND	AE18	---	---	---
GND245	GND	AE20	---	---	---
GND246	GND	AE22	---	---	---
GND247	GND	AE24	---	---	---
GND248	GND	AE26	---	---	---
GND249	GND	AE28	---	---	---
GND250	GND	AE31	---	---	---
GND251	GND	AE33	---	---	---
GND252	GND	AE36	---	---	---
GND253	GND	AE39	---	---	---
GND254	GND	AE42	---	---	---
GND255	GND	AF3	---	---	---
GND256	GND	AF4	---	---	---
GND257	GND	AF5	---	---	---
GND258	GND	AF6	---	---	---
GND259	GND	AF9	---	---	---
GND260	GND	AF14	---	---	---
GND261	GND	AF17	---	---	---
GND262	GND	AF19	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND263	GND	AF21	---	---	---
GND264	GND	AF23	---	---	---
GND265	GND	AF25	---	---	---
GND266	GND	AF27	---	---	---
GND267	GND	AF29	---	---	---
GND268	GND	AF31	---	---	---
GND269	GND	AF33	---	---	---
GND270	GND	AF36	---	---	---
GND271	GND	AF39	---	---	---
GND272	GND	AF42	---	---	---
GND273	GND	AG3	---	---	---
GND274	GND	AG8	---	---	---
GND275	GND	AG11	---	---	---
GND276	GND	AG12	---	---	---
GND277	GND	AG13	---	---	---
GND278	GND	AG14	---	---	---
GND279	GND	AG16	---	---	---
GND280	GND	AG18	---	---	---
GND281	GND	AG20	---	---	---
GND282	GND	AG22	---	---	---
GND283	GND	AG24	---	---	---
GND284	GND	AG26	---	---	---
GND285	GND	AG28	---	---	---
GND286	GND	AG31	---	---	---
GND287	GND	AG33	---	---	---
GND288	GND	AG36	---	---	---
GND289	GND	AG39	---	---	---
GND290	GND	AG42	---	---	---
GND291	GND	AH3	---	---	---
GND292	GND	AH9	---	---	---
GND293	GND	AH12	---	---	---
GND294	GND	AH14	---	---	---
GND295	GND	AH17	---	---	---
GND296	GND	AH19	---	---	---
GND297	GND	AH21	---	---	---
GND298	GND	AH23	---	---	---
GND299	GND	AH25	---	---	---
GND300	GND	AH27	---	---	---

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Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND301	GND	AH29	---	---	---
GND302	GND	AH31	---	---	---
GND303	GND	AH33	---	---	---
GND304	GND	AH36	---	---	---
GND305	GND	AH39	---	---	---
GND306	GND	AH42	---	---	---
GND307	GND	AJ3	---	---	---
GND308	GND	AJ4	---	---	---
GND309	GND	AJ5	---	---	---
GND310	GND	AJ6	---	---	---
GND311	GND	AJ7	---	---	---
GND312	GND	AJ8	---	---	---
GND313	GND	AJ9	---	---	---
GND314	GND	AJ10	---	---	---
GND315	GND	AJ11	---	---	---
GND316	GND	AJ12	---	---	---
GND317	GND	AJ14	---	---	---
GND318	GND	AJ16	---	---	---
GND319	GND	AJ18	---	---	---
GND320	GND	AJ20	---	---	---
GND321	GND	AJ30	---	---	---
GND322	GND	AJ31	---	---	---
GND323	GND	AJ34	---	---	---
GND324	GND	AJ35	---	---	---
GND325	GND	AJ36	---	---	---
GND326	GND	AJ39	---	---	---
GND327	GND	AJ42	---	---	---
GND328	GND	AK3	---	---	---
GND329	GND	AK6	---	---	---
GND330	GND	AK9	---	---	---
GND331	GND	AK12	---	---	---
GND332	GND	AK13	---	---	---
GND333	GND	AK15	---	---	---
GND334	GND	AK17	---	---	---
GND335	GND	AK19	---	---	---
GND336	GND	AK33	---	---	---
GND337	GND	AK36	---	---	---
GND338	GND	AK37	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND339	GND	AK38	---	---	---
GND340	GND	AK39	---	---	---
GND341	GND	AK40	---	---	---
GND342	GND	AK41	---	---	---
GND343	GND	AK42	---	---	---
GND344	GND	AL3	---	---	---
GND345	GND	AL6	---	---	---
GND346	GND	AL9	---	---	---
GND347	GND	AL12	---	---	---
GND348	GND	AL33	---	---	---
GND349	GND	AL34	---	---	---
GND350	GND	AL39	---	---	---
GND351	GND	AL42	---	---	---
GND352	GND	AM3	---	---	---
GND353	GND	AM6	---	---	---
GND354	GND	AM9	---	---	---
GND355	GND	AM12	---	---	---
GND356	GND	AM33	---	---	---
GND357	GND	AM36	---	---	---
GND358	GND	AM39	---	---	---
GND359	GND	AM42	---	---	---
GND360	GND	AN3	---	---	---
GND361	GND	AN6	---	---	---
GND362	GND	AN9	---	---	---
GND363	GND	AN12	---	---	---
GND364	GND	AN34	---	---	---
GND365	GND	AN35	---	---	---
GND366	GND	AN36	---	---	---
GND367	GND	AN39	---	---	---
GND368	GND	AN42	---	---	---
GND369	GND	AP3	---	---	---
GND370	GND	AP6	---	---	---
GND371	GND	AP9	---	---	---
GND372	GND	AP12	---	---	---
GND373	GND	AP14	---	---	---
GND374	GND	AP15	---	---	---
GND375	GND	AP16	---	---	---
GND376	GND	AP37	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND377	GND	AP39	---	---	---
GND378	GND	AP42	---	---	---
GND379	GND	AR3	---	---	---
GND380	GND	AR6	---	---	---
GND381	GND	AR9	---	---	---
GND382	GND	AR12	---	---	---
GND383	GND	AR39	---	---	---
GND384	GND	AR42	---	---	---
GND385	GND	AT3	---	---	---
GND386	GND	AT4	---	---	---
GND387	GND	AT5	---	---	---
GND388	GND	AT6	---	---	---
GND389	GND	AT7	---	---	---
GND390	GND	AT8	---	---	---
GND391	GND	AT9	---	---	---
GND392	GND	AT10	---	---	---
GND393	GND	AT11	---	---	---
GND394	GND	AT12	---	---	---
GND395	GND	AT13	---	---	---
GND396	GND	AT14	---	---	---
GND397	GND	AT15	---	---	---
GND398	GND	AT16	---	---	---
GND399	GND	AT34	---	---	---
GND400	GND	AT35	---	---	---
GND401	GND	AT36	---	---	---
GND402	GND	AT39	---	---	---
GND403	GND	AT42	---	---	---
GND404	GND	AU3	---	---	---
GND405	GND	AU10	---	---	---
GND406	GND	AU37	---	---	---
GND407	GND	AU39	---	---	---
GND408	GND	AU41	---	---	---
GND409	GND	AU42	---	---	---
GND410	GND	AV3	---	---	---
GND411	GND	AV10	---	---	---
GND412	GND	AV38	---	---	---
GND413	GND	AV42	---	---	---
GND414	GND	AW3	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND415	GND	AW4	---	---	---
GND416	GND	AW5	---	---	---
GND417	GND	AW6	---	---	---
GND418	GND	AW7	---	---	---
GND419	GND	AW8	---	---	---
GND420	GND	AW9	---	---	---
GND421	GND	AW10	---	---	---
GND422	GND	AW11	---	---	---
GND423	GND	AW12	---	---	---
GND424	GND	AW13	---	---	---
GND425	GND	AW14	---	---	---
GND426	GND	AW15	---	---	---
GND427	GND	AW16	---	---	---
GND428	GND	AW35	---	---	---
GND429	GND	AW36	---	---	---
GND430	GND	AW38	---	---	---
GND431	GND	AW40	---	---	---
GND432	GND	AW42	---	---	---
GND433	GND	AY3	---	---	---
GND434	GND	AY10	---	---	---
GND435	GND	AY38	---	---	---
GND436	GND	AY42	---	---	---
GND437	GND	BA3	---	---	---
GND438	GND	BA10	---	---	---
GND439	GND	BA34	---	---	---
GND440	GND	BA38	---	---	---
GND441	GND	BA42	---	---	---
GND442	GND	BB4	---	---	---
GND443	GND	BB5	---	---	---
GND444	GND	BB6	---	---	---
GND445	GND	BB7	---	---	---
GND446	GND	BB8	---	---	---
GND447	GND	BB9	---	---	---
GND448	GND	BB10	---	---	---
GND449	GND	BB11	---	---	---
GND450	GND	BB12	---	---	---
GND451	GND	BB13	---	---	---
GND452	GND	BB14	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND453	GND	BB15	---	---	---
GND454	GND	BB16	---	---	---
GND455	GND	BB35	---	---	---
GND456	GND	BB36	---	---	---
GND457	GND	BB37	---	---	---
GND458	GND	BB38	---	---	---
GND459	GND	BB39	---	---	---
GND460	GND	BB40	---	---	---
GND461	GND	BB41	---	---	---
GND_DET1	GND	C3	---	---	---
GND_DET2	GND	BB3	---	---	---
GND_DET3	GND	BB42	---	---	---
USB_AGND1	USB PHY 1 Transceiver GND	D32	---	---	---
USB_AGND2	USB PHY 1 Transceiver GND	J32	---	---	---
USB_AGND3	USB PHY 1 Transceiver GND	L31	---	---	---
USB_AGND4	USB PHY 1 Transceiver GND	M32	---	---	---
USB_AGND5	USB PHY 1 Transceiver GND	N30	---	---	---
X1GND01	Serdes 1 Transceiver GND	F15	---	---	---
X1GND02	Serdes 1 Transceiver GND	F17	---	---	---
X1GND03	Serdes 1 Transceiver GND	F19	---	---	---
X1GND04	Serdes 1 Transceiver GND	F21	---	---	---
X1GND05	Serdes 1 Transceiver GND	G14	---	---	---
X1GND06	Serdes 1 Transceiver GND	G15	---	---	---
X1GND07	Serdes 1 Transceiver GND	G17	---	---	---
X1GND08	Serdes 1 Transceiver GND	G19	---	---	---
X1GND09	Serdes 1 Transceiver GND	G21	---	---	---
X1GND10	Serdes 1 Transceiver GND	H14	---	---	---
X1GND11	Serdes 1 Transceiver GND	H16	---	---	---
X1GND12	Serdes 1 Transceiver GND	H18	---	---	---
X1GND13	Serdes 1 Transceiver GND	H20	---	---	---
X1GND14	Serdes 1 Transceiver GND	H22	---	---	---
X1GND15	Serdes 1 Transceiver GND	J14	---	---	---
X1GND16	Serdes 1 Transceiver GND	J16	---	---	---
X1GND17	Serdes 1 Transceiver GND	J18	---	---	---
X1GND18	Serdes 1 Transceiver GND	J20	---	---	---
X1GND19	Serdes 1 Transceiver GND	J22	---	---	---
X1GND20	Serdes 1 Transceiver GND	K14	---	---	---
X1GND21	Serdes 1 Transceiver GND	L15	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
X1GND22	Serdes 1 Transceiver GND	L19	---	---	---
X1GND23	Serdes 1 Transceiver GND	M17	---	---	---
X1GND24	Serdes 1 Transceiver GND	M21	---	---	---
X2GND01	Serdes 2 Transceiver GND	E31	---	---	---
X2GND02	Serdes 2 Transceiver GND	F23	---	---	---
X2GND03	Serdes 2 Transceiver GND	F25	---	---	---
X2GND04	Serdes 2 Transceiver GND	F27	---	---	---
X2GND05	Serdes 2 Transceiver GND	F29	---	---	---
X2GND06	Serdes 2 Transceiver GND	F31	---	---	---
X2GND07	Serdes 2 Transceiver GND	G23	---	---	---
X2GND08	Serdes 2 Transceiver GND	G25	---	---	---
X2GND09	Serdes 2 Transceiver GND	G27	---	---	---
X2GND10	Serdes 2 Transceiver GND	G29	---	---	---
X2GND11	Serdes 2 Transceiver GND	G31	---	---	---
X2GND12	Serdes 2 Transceiver GND	H24	---	---	---
X2GND13	Serdes 2 Transceiver GND	H26	---	---	---
X2GND14	Serdes 2 Transceiver GND	H28	---	---	---
X2GND15	Serdes 2 Transceiver GND	H30	---	---	---
X2GND16	Serdes 2 Transceiver GND	H31	---	---	---
X2GND17	Serdes 2 Transceiver GND	J24	---	---	---
X2GND18	Serdes 2 Transceiver GND	J26	---	---	---
X2GND19	Serdes 2 Transceiver GND	J28	---	---	---
X2GND20	Serdes 2 Transceiver GND	J30	---	---	---
X2GND21	Serdes 2 Transceiver GND	L26	---	---	---
X2GND22	Serdes 2 Transceiver GND	L30	---	---	---
X2GND23	Serdes 2 Transceiver GND	M24	---	---	---
X2GND24	Serdes 2 Transceiver GND	M28	---	---	---
X2GND25	Serdes 2 Transceiver GND	N29	---	---	---
X3GND01	Serdes 3 Transceiver GND	AN20	---	---	---
X3GND02	Serdes 3 Transceiver GND	AN24	---	---	---
X3GND03	Serdes 3 Transceiver GND	AP18	---	---	---
X3GND04	Serdes 3 Transceiver GND	AP22	---	---	---
X3GND05	Serdes 3 Transceiver GND	AR17	---	---	---
X3GND06	Serdes 3 Transceiver GND	AT17	---	---	---
X3GND07	Serdes 3 Transceiver GND	AT19	---	---	---
X3GND08	Serdes 3 Transceiver GND	AT21	---	---	---
X3GND09	Serdes 3 Transceiver GND	AT23	---	---	---
X3GND10	Serdes 3 Transceiver GND	AT25	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
X3GND11	Serdes 3 Transceiver GND	AU17	---	---	---
X3GND12	Serdes 3 Transceiver GND	AU19	---	---	---
X3GND13	Serdes 3 Transceiver GND	AU21	---	---	---
X3GND14	Serdes 3 Transceiver GND	AU23	---	---	---
X3GND15	Serdes 3 Transceiver GND	AU25	---	---	---
X3GND16	Serdes 3 Transceiver GND	AV17	---	---	---
X3GND17	Serdes 3 Transceiver GND	AV18	---	---	---
X3GND18	Serdes 3 Transceiver GND	AV20	---	---	---
X3GND19	Serdes 3 Transceiver GND	AV22	---	---	---
X3GND20	Serdes 3 Transceiver GND	AV24	---	---	---
X3GND21	Serdes 3 Transceiver GND	AW18	---	---	---
X3GND22	Serdes 3 Transceiver GND	AW20	---	---	---
X3GND23	Serdes 3 Transceiver GND	AW22	---	---	---
X3GND24	Serdes 3 Transceiver GND	AW24	---	---	---
X4GND01	Serdes 4 Transceiver GND	AM32	---	---	---
X4GND02	Serdes 4 Transceiver GND	AN27	---	---	---
X4GND03	Serdes 4 Transceiver GND	AN31	---	---	---
X4GND04	Serdes 4 Transceiver GND	AP29	---	---	---
X4GND05	Serdes 4 Transceiver GND	AP33	---	---	---
X4GND06	Serdes 4 Transceiver GND	AT27	---	---	---
X4GND07	Serdes 4 Transceiver GND	AT29	---	---	---
X4GND08	Serdes 4 Transceiver GND	AT31	---	---	---
X4GND09	Serdes 4 Transceiver GND	AT33	---	---	---
X4GND10	Serdes 4 Transceiver GND	AU27	---	---	---
X4GND11	Serdes 4 Transceiver GND	AU29	---	---	---
X4GND12	Serdes 4 Transceiver GND	AU31	---	---	---
X4GND13	Serdes 4 Transceiver GND	AU33	---	---	---
X4GND14	Serdes 4 Transceiver GND	AU34	---	---	---
X4GND15	Serdes 4 Transceiver GND	AV26	---	---	---
X4GND16	Serdes 4 Transceiver GND	AV28	---	---	---
X4GND17	Serdes 4 Transceiver GND	AV30	---	---	---
X4GND18	Serdes 4 Transceiver GND	AV32	---	---	---
X4GND19	Serdes 4 Transceiver GND	AV34	---	---	---
X4GND20	Serdes 4 Transceiver GND	AW26	---	---	---
X4GND21	Serdes 4 Transceiver GND	AW28	---	---	---
X4GND22	Serdes 4 Transceiver GND	AW30	---	---	---
X4GND23	Serdes 4 Transceiver GND	AW32	---	---	---
X4GND24	Serdes 4 Transceiver GND	AW34	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
X4GND25	Serdes 4 Transceiver GND	AY34	---	---	---
S1GND01	Serdes 1 core logic GND	A15	---	---	---
S1GND02	Serdes 1 core logic GND	A17	---	---	---
S1GND03	Serdes 1 core logic GND	A19	---	---	---
S1GND04	Serdes 1 core logic GND	A21	---	---	---
S1GND05	Serdes 1 core logic GND	B14	---	---	---
S1GND06	Serdes 1 core logic GND	B15	---	---	---
S1GND07	Serdes 1 core logic GND	B17	---	---	---
S1GND08	Serdes 1 core logic GND	B19	---	---	---
S1GND09	Serdes 1 core logic GND	B21	---	---	---
S1GND10	Serdes 1 core logic GND	C14	---	---	---
S1GND11	Serdes 1 core logic GND	C16	---	---	---
S1GND12	Serdes 1 core logic GND	C18	---	---	---
S1GND13	Serdes 1 core logic GND	C20	---	---	---
S1GND14	Serdes 1 core logic GND	C22	---	---	---
S1GND15	Serdes 1 core logic GND	D14	---	---	---
S1GND16	Serdes 1 core logic GND	D16	---	---	---
S1GND17	Serdes 1 core logic GND	D18	---	---	---
S1GND18	Serdes 1 core logic GND	D20	---	---	---
S1GND19	Serdes 1 core logic GND	D22	---	---	---
S1GND20	Serdes 1 core logic GND	E14	---	---	---
S1GND21	Serdes 1 core logic GND	E15	---	---	---
S1GND22	Serdes 1 core logic GND	E16	---	---	---
S1GND23	Serdes 1 core logic GND	E17	---	---	---
S1GND24	Serdes 1 core logic GND	E18	---	---	---
S1GND25	Serdes 1 core logic GND	E19	---	---	---
S1GND26	Serdes 1 core logic GND	E20	---	---	---
S1GND27	Serdes 1 core logic GND	E21	---	---	---
S1GND28	Serdes 1 core logic GND	E22	---	---	---
S1GND29	Serdes 1 core logic GND	M15	---	---	---
S1GND30	Serdes 1 core logic GND	M19	---	---	---
S1GND31	Serdes 1 core logic GND	N16	---	---	---
S1GND32	Serdes 1 core logic GND	N18	---	---	---
S1GND33	Serdes 1 core logic GND	N19	---	---	---
S1GND34	Serdes 1 core logic GND	N20	---	---	---
S1GND35	Serdes 1 core logic GND	N22	---	---	---
S1GND36	Serdes 1 core logic GND	P17	---	---	---
S1GND37	Serdes 1 core logic GND	R18	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
S1GND38	Serdes 1 core logic GND	R19	---	---	---
S1GND39	Serdes 1 core logic GND	R20	---	---	---
S1GND40	Serdes 1 core logic GND	R21	---	---	---
S1GND41	Serdes 1 core logic GND	R22	---	---	---
S2GND01	Serdes 2 core logic GND	A23	---	---	---
S2GND02	Serdes 2 core logic GND	A25	---	---	---
S2GND03	Serdes 2 core logic GND	A27	---	---	---
S2GND04	Serdes 2 core logic GND	A29	---	---	---
S2GND05	Serdes 2 core logic GND	A31	---	---	---
S2GND06	Serdes 2 core logic GND	B23	---	---	---
S2GND07	Serdes 2 core logic GND	B25	---	---	---
S2GND08	Serdes 2 core logic GND	B27	---	---	---
S2GND09	Serdes 2 core logic GND	B29	---	---	---
S2GND10	Serdes 2 core logic GND	B31	---	---	---
S2GND11	Serdes 2 core logic GND	C24	---	---	---
S2GND12	Serdes 2 core logic GND	C26	---	---	---
S2GND13	Serdes 2 core logic GND	C28	---	---	---
S2GND14	Serdes 2 core logic GND	C30	---	---	---
S2GND15	Serdes 2 core logic GND	C31	---	---	---
S2GND16	Serdes 2 core logic GND	D24	---	---	---
S2GND17	Serdes 2 core logic GND	D26	---	---	---
S2GND18	Serdes 2 core logic GND	D28	---	---	---
S2GND19	Serdes 2 core logic GND	D30	---	---	---
S2GND20	Serdes 2 core logic GND	E23	---	---	---
S2GND21	Serdes 2 core logic GND	E24	---	---	---
S2GND22	Serdes 2 core logic GND	E25	---	---	---
S2GND23	Serdes 2 core logic GND	E26	---	---	---
S2GND24	Serdes 2 core logic GND	E27	---	---	---
S2GND25	Serdes 2 core logic GND	E28	---	---	---
S2GND26	Serdes 2 core logic GND	E29	---	---	---
S2GND27	Serdes 2 core logic GND	E30	---	---	---
S2GND28	Serdes 2 core logic GND	M26	---	---	---
S2GND29	Serdes 2 core logic GND	N23	---	---	---
S2GND30	Serdes 2 core logic GND	N25	---	---	---
S2GND31	Serdes 2 core logic GND	N26	---	---	---
S2GND32	Serdes 2 core logic GND	N27	---	---	---
S2GND33	Serdes 2 core logic GND	N28	---	---	---
S2GND34	Serdes 2 core logic GND	P28	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
S2GND35	Serdes 2 core logic GND	R23	---	---	---
S2GND36	Serdes 2 core logic GND	R24	---	---	---
S2GND37	Serdes 2 core logic GND	R25	---	---	---
S2GND38	Serdes 2 core logic GND	R26	---	---	---
S2GND39	Serdes 2 core logic GND	R27	---	---	---
S3GND01	Serdes 3 core logic GND	AK21	---	---	---
S3GND02	Serdes 3 core logic GND	AK22	---	---	---
S3GND03	Serdes 3 core logic GND	AK23	---	---	---
S3GND04	Serdes 3 core logic GND	AK24	---	---	---
S3GND05	Serdes 3 core logic GND	AK25	---	---	---
S3GND06	Serdes 3 core logic GND	AL20	---	---	---
S3GND07	Serdes 3 core logic GND	AM19	---	---	---
S3GND08	Serdes 3 core logic GND	AM21	---	---	---
S3GND09	Serdes 3 core logic GND	AM22	---	---	---
S3GND10	Serdes 3 core logic GND	AM23	---	---	---
S3GND11	Serdes 3 core logic GND	AM25	---	---	---
S3GND12	Serdes 3 core logic GND	AN18	---	---	---
S3GND13	Serdes 3 core logic GND	AN22	---	---	---
S3GND14	Serdes 3 core logic GND	AY17	---	---	---
S3GND15	Serdes 3 core logic GND	AY18	---	---	---
S3GND16	Serdes 3 core logic GND	AY19	---	---	---
S3GND17	Serdes 3 core logic GND	AY20	---	---	---
S3GND18	Serdes 3 core logic GND	AY21	---	---	---
S3GND19	Serdes 3 core logic GND	AY22	---	---	---
S3GND20	Serdes 3 core logic GND	AY23	---	---	---
S3GND21	Serdes 3 core logic GND	AY24	---	---	---
S3GND22	Serdes 3 core logic GND	AY25	---	---	---
S3GND23	Serdes 3 core logic GND	BA17	---	---	---
S3GND24	Serdes 3 core logic GND	BA19	---	---	---
S3GND25	Serdes 3 core logic GND	BA21	---	---	---
S3GND26	Serdes 3 core logic GND	BA23	---	---	---
S3GND27	Serdes 3 core logic GND	BA25	---	---	---
S3GND28	Serdes 3 core logic GND	BB17	---	---	---
S3GND29	Serdes 3 core logic GND	BB19	---	---	---
S3GND30	Serdes 3 core logic GND	BB21	---	---	---
S3GND31	Serdes 3 core logic GND	BB23	---	---	---
S3GND32	Serdes 3 core logic GND	BB25	---	---	---
S3GND33	Serdes 3 core logic GND	BC17	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
S3GND34	Serdes 3 core logic GND	BC18	---	---	---
S3GND35	Serdes 3 core logic GND	BC20	---	---	---
S3GND36	Serdes 3 core logic GND	BC22	---	---	---
S3GND37	Serdes 3 core logic GND	BC24	---	---	---
S3GND38	Serdes 3 core logic GND	BD18	---	---	---
S3GND39	Serdes 3 core logic GND	BD20	---	---	---
S3GND40	Serdes 3 core logic GND	BD22	---	---	---
S3GND41	Serdes 3 core logic GND	BD24	---	---	---
S4GND01	Serdes 4 core logic GND	AK26	---	---	---
S4GND02	Serdes 4 core logic GND	AK27	---	---	---
S4GND03	Serdes 4 core logic GND	AK28	---	---	---
S4GND04	Serdes 4 core logic GND	AK29	---	---	---
S4GND05	Serdes 4 core logic GND	AK30	---	---	---
S4GND06	Serdes 4 core logic GND	AL31	---	---	---
S4GND07	Serdes 4 core logic GND	AM26	---	---	---
S4GND08	Serdes 4 core logic GND	AM28	---	---	---
S4GND09	Serdes 4 core logic GND	AM29	---	---	---
S4GND10	Serdes 4 core logic GND	AM30	---	---	---
S4GND11	Serdes 4 core logic GND	AM31	---	---	---
S4GND12	Serdes 4 core logic GND	AN29	---	---	---
S4GND13	Serdes 4 core logic GND	AY26	---	---	---
S4GND14	Serdes 4 core logic GND	AY27	---	---	---
S4GND15	Serdes 4 core logic GND	AY28	---	---	---
S4GND16	Serdes 4 core logic GND	AY29	---	---	---
S4GND17	Serdes 4 core logic GND	AY30	---	---	---
S4GND18	Serdes 4 core logic GND	AY31	---	---	---
S4GND19	Serdes 4 core logic GND	AY32	---	---	---
S4GND20	Serdes 4 core logic GND	AY33	---	---	---
S4GND21	Serdes 4 core logic GND	BA27	---	---	---
S4GND22	Serdes 4 core logic GND	BA29	---	---	---
S4GND23	Serdes 4 core logic GND	BA31	---	---	---
S4GND24	Serdes 4 core logic GND	BA33	---	---	---
S4GND25	Serdes 4 core logic GND	BB27	---	---	---
S4GND26	Serdes 4 core logic GND	BB29	---	---	---
S4GND27	Serdes 4 core logic GND	BB31	---	---	---
S4GND28	Serdes 4 core logic GND	BB33	---	---	---
S4GND29	Serdes 4 core logic GND	BB34	---	---	---
S4GND30	Serdes 4 core logic GND	BC26	---	---	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
S4GND31	Serdes 4 core logic GND	BC28	---	---	---
S4GND32	Serdes 4 core logic GND	BC30	---	---	---
S4GND33	Serdes 4 core logic GND	BC32	---	---	---
S4GND34	Serdes 4 core logic GND	BC34	---	---	---
S4GND35	Serdes 4 core logic GND	BD26	---	---	---
S4GND36	Serdes 4 core logic GND	BD28	---	---	---
S4GND37	Serdes 4 core logic GND	BD30	---	---	---
S4GND38	Serdes 4 core logic GND	BD32	---	---	---
S4GND39	Serdes 4 core logic GND	BD34	---	---	---
AGND_SD1_PLL1	Serdes1 PLL 1 GND	L18	---	---	---
AGND_SD1_PLL2	Serdes1 PLL 2 GND	L20	---	---	---
AGND_SD2_PLL1	Serdes2 PLL 1 GND	L25	---	---	---
AGND_SD2_PLL2	Serdes2 PLL 2 GND	L27	---	---	---
AGND_SD3_PLL1	Serdes3 PLL 1 GND	AP21	---	---	---
AGND_SD3_PLL2	Serdes3 PLL 2 GND	AP23	---	---	---
AGND_SD4_PLL1	Serdes4 PLL 1 GND	AP28	---	---	---
AGND_SD4_PLL2	Serdes4 PLL 2 GND	AP30	---	---	---
SENSEGND_CA	GND Sense pin	R13	---	---	---
SENSEGND_CB	GND Sense pin	AM17	---	---	---
SENSEGND_PL	GND Sense pin	AA32	---	---	---
OVDD1	General I/O supply	R30	---	OV_{DD}	---
OVDD2	General I/O supply	T30	---	OV_{DD}	---
OVDD3	General I/O supply	U30	---	OV_{DD}	---
OVDD4	General I/O supply	V30	---	OV_{DD}	---
OVDD5	General I/O supply	W30	---	OV_{DD}	---
OVDD6	General I/O supply	Y30	---	OV_{DD}	---
OVDD7	General I/O supply	AA30	---	OV_{DD}	---
OVDD8	General I/O supply	AK14	---	OV_{DD}	---
DVDD1	UART/I2C supply	R14	---	DV_{DD}	---
DVDD2	UART/I2C supply	R15	---	DV_{DD}	---
G1VDD01	DDR supply for port 1	A2	---	$G1V_{DD}$	---
G1VDD02	DDR supply for port 1	A6	---	$G1V_{DD}$	---
G1VDD03	DDR supply for port 1	A9	---	$G1V_{DD}$	---
G1VDD04	DDR supply for port 1	B1	---	$G1V_{DD}$	---
G1VDD05	DDR supply for port 1	B4	---	$G1V_{DD}$	---
G1VDD06	DDR supply for port 1	B9	---	$G1V_{DD}$	---
G1VDD07	DDR supply for port 1	D2	---	$G1V_{DD}$	---
G1VDD08	DDR supply for port 1	F1	---	$G1V_{DD}$	---

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Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
G1VDD09	DDR supply for port 1	H2	---	$G1V_{DD}$	---
G1VDD10	DDR supply for port 1	K1	---	$G1V_{DD}$	---
G1VDD11	DDR supply for port 1	M2	---	$G1V_{DD}$	---
G1VDD12	DDR supply for port 1	P1	---	$G1V_{DD}$	---
G1VDD13	DDR supply for port 1	T2	---	$G1V_{DD}$	---
G1VDD14	DDR supply for port 1	T15	---	$G1V_{DD}$	---
G1VDD15	DDR supply for port 1	U15	---	$G1V_{DD}$	---
G1VDD16	DDR supply for port 1	V1	---	$G1V_{DD}$	---
G1VDD17	DDR supply for port 1	V15	---	$G1V_{DD}$	---
G1VDD18	DDR supply for port 1	W15	---	$G1V_{DD}$	---
G1VDD19	DDR supply for port 1	Y2	---	$G1V_{DD}$	---
G1VDD20	DDR supply for port 1	Y15	---	$G1V_{DD}$	---
G1VDD21	DDR supply for port 1	AA15	---	$G1V_{DD}$	---
G1VDD22	DDR supply for port 1	AB1	---	$G1V_{DD}$	---
G1VDD23	DDR supply for port 1	AB15	---	$G1V_{DD}$	---
G1VDD24	DDR supply for port 1	AD2	---	$G1V_{DD}$	---
G1VDD25	DDR supply for port 1	AF1	---	$G1V_{DD}$	---
G1VDD26	DDR supply for port 1	AF2	---	$G1V_{DD}$	---
G2VDD01	DDR supply for port 2	AC15	---	$G2V_{DD}$	---
G2VDD02	DDR supply for port 2	AD15	---	$G2V_{DD}$	---
G2VDD03	DDR supply for port 2	AE15	---	$G2V_{DD}$	---
G2VDD04	DDR supply for port 2	AF15	---	$G2V_{DD}$	---
G2VDD05	DDR supply for port 2	AG1	---	$G2V_{DD}$	---
G2VDD06	DDR supply for port 2	AG15	---	$G2V_{DD}$	---
G2VDD07	DDR supply for port 2	AH15	---	$G2V_{DD}$	---
G2VDD08	DDR supply for port 2	AJ2	---	$G2V_{DD}$	---
G2VDD09	DDR supply for port 2	AJ15	---	$G2V_{DD}$	---
G2VDD10	DDR supply for port 2	AL1	---	$G2V_{DD}$	---
G2VDD11	DDR supply for port 2	AN2	---	$G2V_{DD}$	---
G2VDD12	DDR supply for port 2	AR1	---	$G2V_{DD}$	---
G2VDD13	DDR supply for port 2	AU2	---	$G2V_{DD}$	---
G2VDD14	DDR supply for port 2	AW1	---	$G2V_{DD}$	---
G2VDD15	DDR supply for port 2	BA2	---	$G2V_{DD}$	---
G2VDD16	DDR supply for port 2	BC1	---	$G2V_{DD}$	---
G2VDD17	DDR supply for port 2	BC4	---	$G2V_{DD}$	---
G2VDD18	DDR supply for port 2	BC8	---	$G2V_{DD}$	---
G2VDD19	DDR supply for port 2	BC12	---	$G2V_{DD}$	---
G2VDD20	DDR supply for port 2	BC16	---	$G2V_{DD}$	---

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Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
G2VDD21	DDR supply for port 2	BD2	---	$G2V_{DD}$	---
G2VDD22	DDR supply for port 2	BD6	---	$G2V_{DD}$	---
G2VDD23	DDR supply for port 2	BD10	---	$G2V_{DD}$	---
G2VDD24	DDR supply for port 2	BD14	---	$G2V_{DD}$	---
G2VDD25	DDR supply for port 2	BD17	---	$G2V_{DD}$	---
S1VDD1	SerDes1 core logic supply	N17	---	$S1V_{DD}$	---
S1VDD2	SerDes1 core logic supply	P20	---	$S1V_{DD}$	---
S1VDD3	SerDes1 core logic supply	P22	---	$S1V_{DD}$	---
S1VDD4	SerDes1 core logic supply	T19	---	$S1V_{DD}$	---
S1VDD5	SerDes1 core logic supply	T20	---	$S1V_{DD}$	---
S1VDD6	SerDes1 core logic supply	T21	---	$S1V_{DD}$	---
S1VDD7	SerDes1 core logic supply	T22	---	$S1V_{DD}$	---
S2VDD1	SerDes2 core logic supply	P23	---	$S2V_{DD}$	---
S2VDD2	SerDes2 core logic supply	P25	---	$S2V_{DD}$	---
S2VDD3	SerDes2 core logic supply	T23	---	$S2V_{DD}$	---
S2VDD4	SerDes2 core logic supply	T24	---	$S2V_{DD}$	---
S2VDD5	SerDes2 core logic supply	T25	---	$S2V_{DD}$	---
S2VDD6	SerDes2 core logic supply	T26	---	$S2V_{DD}$	---
S3VDD1	SerDes3 core logic supply	AJ22	---	$S3V_{DD}$	---
S3VDD2	SerDes3 core logic supply	AJ23	---	$S3V_{DD}$	---
S3VDD3	SerDes3 core logic supply	AJ24	---	$S3V_{DD}$	---
S3VDD4	SerDes3 core logic supply	AJ25	---	$S3V_{DD}$	---
S3VDD5	SerDes3 core logic supply	AL23	---	$S3V_{DD}$	---
S3VDD6	SerDes3 core logic supply	AL25	---	$S3V_{DD}$	---
S3VDD7	SerDes3 core logic supply	AM20	---	$S3V_{DD}$	---
S4VDD1	SerDes4 core logic supply	AJ26	---	$S4V_{DD}$	---
S4VDD2	SerDes4 core logic supply	AJ27	---	$S4V_{DD}$	---
S4VDD3	SerDes4 core logic supply	AJ28	---	$S4V_{DD}$	---
S4VDD4	SerDes4 core logic supply	AJ29	---	$S4V_{DD}$	---
S4VDD5	SerDes4 core logic supply	AL26	---	$S4V_{DD}$	---
S4VDD6	SerDes4 core logic supply	AL28	---	$S4V_{DD}$	---
X1VDD1	SerDes1 transceiver supply	K15	---	$X1V_{DD}$	---
X1VDD2	SerDes1 transceiver supply	K16	---	$X1V_{DD}$	---
X1VDD3	SerDes1 transceiver supply	K17	---	$X1V_{DD}$	---
X1VDD4	SerDes1 transceiver supply	K18	---	$X1V_{DD}$	---
X1VDD5	SerDes1 transceiver supply	K19	---	$X1V_{DD}$	---
X1VDD6	SerDes1 transceiver supply	K20	---	$X1V_{DD}$	---
X1VDD7	SerDes1 transceiver supply	K21	---	$X1V_{DD}$	---

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Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
X1VDD8	SerDes1 transceiver supply	K22	---	$X1V_{DD}$	---
X2VDD1	SerDes2 transceiver supply	K23	---	$X2V_{DD}$	---
X2VDD2	SerDes2 transceiver supply	K24	---	$X2V_{DD}$	---
X2VDD3	SerDes2 transceiver supply	K25	---	$X2V_{DD}$	---
X2VDD4	SerDes2 transceiver supply	K26	---	$X2V_{DD}$	---
X2VDD5	SerDes2 transceiver supply	K27	---	$X2V_{DD}$	---
X2VDD6	SerDes2 transceiver supply	K28	---	$X2V_{DD}$	---
X2VDD7	SerDes2 transceiver supply	K29	---	$X2V_{DD}$	---
X2VDD8	SerDes2 transceiver supply	K30	---	$X2V_{DD}$	---
X2VDD9	SerDes2 transceiver supply	M30	---	$X2V_{DD}$	---
X3VDD1	SerDes3 transceiver supply	AR18	---	$X3V_{DD}$	---
X3VDD2	SerDes3 transceiver supply	AR19	---	$X3V_{DD}$	---
X3VDD3	SerDes3 transceiver supply	AR20	---	$X3V_{DD}$	---
X3VDD4	SerDes3 transceiver supply	AR21	---	$X3V_{DD}$	---
X3VDD5	SerDes3 transceiver supply	AR22	---	$X3V_{DD}$	---
X3VDD6	SerDes3 transceiver supply	AR23	---	$X3V_{DD}$	---
X3VDD7	SerDes3 transceiver supply	AR24	---	$X3V_{DD}$	---
X3VDD8	SerDes3 transceiver supply	AR25	---	$X3V_{DD}$	---
X4VDD1	SerDes4 transceiver supply	AN33	---	$X4V_{DD}$	---
X4VDD2	SerDes4 transceiver supply	AR26	---	$X4V_{DD}$	---
X4VDD3	SerDes4 transceiver supply	AR27	---	$X4V_{DD}$	---
X4VDD4	SerDes4 transceiver supply	AR28	---	$X4V_{DD}$	---
X4VDD5	SerDes4 transceiver supply	AR29	---	$X4V_{DD}$	---
X4VDD6	SerDes4 transceiver supply	AR30	---	$X4V_{DD}$	---
X4VDD7	SerDes4 transceiver supply	AR31	---	$X4V_{DD}$	---
X4VDD8	SerDes4 transceiver supply	AR32	---	$X4V_{DD}$	---
X4VDD9	SerDes4 transceiver supply	AR33	---	$X4V_{DD}$	---
LVDD1	Ethernet controller and GPIO supply	L14	---	LV_{DD}	---
LVDD2	Ethernet controller and GPIO supply	R16	---	LV_{DD}	---
LVDD3	Ethernet controller and GPIO supply	R17	---	LV_{DD}	---
FA_VL	Reserved for internal use only	R33	---	FA_VL	15
PROG_MTR	Reserved for internal use only	T29	---	PROG_MTR	15
PROG_SFP	SFP Fuse Programming Override supply	R29	---	PROG_SFP	---
TH_VDD	Thermal Monitor Unit supply	V32	---	TH_V_{DD}	27
VDD01	Supply for cores and platform	T16	---	V_{DD}	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
VDD02	Supply for cores and platform	U17	---	V_{DD}	---
VDD03	Supply for cores and platform	U19	---	V_{DD}	---
VDD04	Supply for cores and platform	U21	---	V_{DD}	---
VDD05	Supply for cores and platform	U23	---	V_{DD}	---
VDD06	Supply for cores and platform	U25	---	V_{DD}	---
VDD07	Supply for cores and platform	U27	---	V_{DD}	---
VDD08	Supply for cores and platform	U29	---	V_{DD}	---
VDD09	Supply for cores and platform	V16	---	V_{DD}	---
VDD10	Supply for cores and platform	V18	---	V_{DD}	---
VDD11	Supply for cores and platform	V20	---	V_{DD}	---
VDD12	Supply for cores and platform	V22	---	V_{DD}	---
VDD13	Supply for cores and platform	V24	---	V_{DD}	---
VDD14	Supply for cores and platform	V26	---	V_{DD}	---
VDD15	Supply for cores and platform	V28	---	V_{DD}	---
VDD16	Supply for cores and platform	W17	---	V_{DD}	---
VDD17	Supply for cores and platform	W19	---	V_{DD}	---
VDD18	Supply for cores and platform	W21	---	V_{DD}	---
VDD19	Supply for cores and platform	W23	---	V_{DD}	---
VDD20	Supply for cores and platform	W25	---	V_{DD}	---
VDD21	Supply for cores and platform	W27	---	V_{DD}	---
VDD22	Supply for cores and platform	W29	---	V_{DD}	---
VDD23	Supply for cores and platform	Y16	---	V_{DD}	---
VDD24	Supply for cores and platform	Y18	---	V_{DD}	---
VDD25	Supply for cores and platform	Y20	---	V_{DD}	---
VDD26	Supply for cores and platform	Y22	---	V_{DD}	---
VDD27	Supply for cores and platform	Y24	---	V_{DD}	---
VDD28	Supply for cores and platform	Y26	---	V_{DD}	---
VDD29	Supply for cores and platform	Y28	---	V_{DD}	---
VDD30	Supply for cores and platform	AA17	---	V_{DD}	---
VDD31	Supply for cores and platform	AA19	---	V_{DD}	---
VDD32	Supply for cores and platform	AA21	---	V_{DD}	---
VDD33	Supply for cores and platform	AA23	---	V_{DD}	---
VDD34	Supply for cores and platform	AA25	---	V_{DD}	---
VDD35	Supply for cores and platform	AA27	---	V_{DD}	---
VDD36	Supply for cores and platform	AA29	---	V_{DD}	---
VDD37	Supply for cores and platform	AB16	---	V_{DD}	---
VDD38	Supply for cores and platform	AB18	---	V_{DD}	---
VDD39	Supply for cores and platform	AB20	---	V_{DD}	---

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Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
VDD40	Supply for cores and platform	AB22	---	V_{DD}	---
VDD41	Supply for cores and platform	AB24	---	V_{DD}	---
VDD42	Supply for cores and platform	AB26	---	V_{DD}	---
VDD43	Supply for cores and platform	AB28	---	V_{DD}	---
VDD44	Supply for cores and platform	AC17	---	V_{DD}	---
VDD45	Supply for cores and platform	AC19	---	V_{DD}	---
VDD46	Supply for cores and platform	AC21	---	V_{DD}	---
VDD47	Supply for cores and platform	AC23	---	V_{DD}	---
VDD48	Supply for cores and platform	AC25	---	V_{DD}	---
VDD49	Supply for cores and platform	AC27	---	V_{DD}	---
VDD50	Supply for cores and platform	AC29	---	V_{DD}	---
VDD51	Supply for cores and platform	AD16	---	V_{DD}	---
VDD52	Supply for cores and platform	AD18	---	V_{DD}	---
VDD53	Supply for cores and platform	AD20	---	V_{DD}	---
VDD54	Supply for cores and platform	AD22	---	V_{DD}	---
VDD55	Supply for cores and platform	AD24	---	V_{DD}	---
VDD56	Supply for cores and platform	AD26	---	V_{DD}	---
VDD57	Supply for cores and platform	AD28	---	V_{DD}	---
VDD58	Supply for cores and platform	AE17	---	V_{DD}	---
VDD59	Supply for cores and platform	AE19	---	V_{DD}	---
VDD60	Supply for cores and platform	AE21	---	V_{DD}	---
VDD61	Supply for cores and platform	AE23	---	V_{DD}	---
VDD62	Supply for cores and platform	AE25	---	V_{DD}	---
VDD63	Supply for cores and platform	AE27	---	V_{DD}	---
VDD64	Supply for cores and platform	AE29	---	V_{DD}	---
VDD65	Supply for cores and platform	AF16	---	V_{DD}	---
VDD66	Supply for cores and platform	AF18	---	V_{DD}	---
VDD67	Supply for cores and platform	AF20	---	V_{DD}	---
VDD68	Supply for cores and platform	AF22	---	V_{DD}	---
VDD69	Supply for cores and platform	AF24	---	V_{DD}	---
VDD70	Supply for cores and platform	AF26	---	V_{DD}	---
VDD71	Supply for cores and platform	AF28	---	V_{DD}	---
VDD72	Supply for cores and platform	AG17	---	V_{DD}	---
VDD73	Supply for cores and platform	AG19	---	V_{DD}	---
VDD74	Supply for cores and platform	AG21	---	V_{DD}	---
VDD75	Supply for cores and platform	AG23	---	V_{DD}	---
VDD76	Supply for cores and platform	AG25	---	V_{DD}	---
VDD77	Supply for cores and platform	AG27	---	V_{DD}	---

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Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
VDD78	Supply for cores and platform	AG29	---	V_{DD}	---
VDD79	Supply for cores and platform	AH16	---	V_{DD}	---
VDD80	Supply for cores and platform	AH18	---	V_{DD}	---
VDD81	Supply for cores and platform	AH20	---	V_{DD}	---
VDD82	Supply for cores and platform	AH22	---	V_{DD}	---
VDD83	Supply for cores and platform	AH24	---	V_{DD}	---
VDD84	Supply for cores and platform	AH26	---	V_{DD}	---
VDD85	Supply for cores and platform	AH28	---	V_{DD}	---
VDD86	Supply for cores and platform	AJ17	---	V_{DD}	---
VDD87	Supply for cores and platform	AJ19	---	V_{DD}	---
VDD88	Supply for cores and platform	AJ21	---	V_{DD}	---
VDD89	Supply for cores and platform	AK16	---	V_{DD}	---
VDD90	Supply for cores and platform	AK18	---	V_{DD}	---
VDD91	Supply for cores and platform	AK20	---	V_{DD}	---
VDD_LP	Low Power Security Monitor supply	R28	---	V_{DD}_LP	---
AVDD_CGA1	e6500 Cluster Group A PLL1 supply	AP13	---	AVDD_CGA1	---
AVDD_CGA2	e6500 Cluster Group A PLL2 supply	AR13	---	AVDD_CGA2	---
AVDD_CGA3	e6500 Cluster Group A PLL3 supply	AR14	---	AVDD_CGA3	---
AVDD_CGB1	e6500 Cluster Group B PLL1 supply	AR16	---	AVDD_CGB1	---
AVDD_CGB2	e6500 Cluster Group B PLL2 supply	AR15	---	AVDD_CGB2	---
AVDD_PLAT	Platform PLL supply	T28	---	AVDD_PLAT	---
AVDD_D1	DDR1 PLL supply	T13	---	AVDD_D1	---
AVDD_D2	DDR2 PLL supply	AJ13	---	AVDD_D2	---
AVDD_SD1_PLL1	SerDes1 PLL 1 supply	L17	---	AVDD_SD1_PLL1	---
AVDD_SD1_PLL2	SerDes1 PLL 2 supply	L21	---	AVDD_SD1_PLL2	---
AVDD_SD2_PLL1	SerDes2 PLL 1 supply	L24	---	AVDD_SD2_PLL1	---
AVDD_SD2_PLL2	SerDes2 PLL 2 supply	L28	---	AVDD_SD2_PLL2	---
AVDD_SD3_PLL1	SerDes3 PLL 1 supply	AP20	---	AVDD_SD3_PLL1	---
AVDD_SD3_PLL2	SerDes3 PLL 2 supply	AP24	---	AVDD_SD3_PLL2	---
AVDD_SD4_PLL1	SerDes4 PLL 1 supply	AP27	---	AVDD_SD4_PLL1	---
AVDD_SD4_PLL2	SerDes4 PLL 2 supply	AP31	---	AVDD_SD4_PLL2	---
SENSEVDD_CA	Vdd Sense pin for core cluster A	R12	---	SENSEVDD_CA	---

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SENSEVDD_CB	Vdd Sense pin for core cluster B	AM16	---	SENSEVDD_CB	---
SENSEVDD_PL	Vdd Sense pin for platform	Y32	---	SENSEVDD_PL	---
USB_HVDD1	USB PHY Transceiver 3.3V Supply	K32	---	USB_HV_{DD}	---
USB_HVDD2	USB PHY Transceiver 3.3V Supply	N32	---	USB_HV_{DD}	---
USB_OVDD1	USB PHY Transceiver 1.8V Supply	P31	---	USB_OV_{DD}	---
USB_OVDD2	USB PHY Transceiver 1.8V Supply	P32	---	USB_OV_{DD}	---
USB_SVDD1	USB PHY Analog 1.0V Supply	P29	---	USB_SV_{DD}	---
USB_SVDD2	USB PHY Analog 1.0V Supply	P30	---	USB_SV_{DD}	---
No Connection Pins					
NC01	No Connection	G35	---	---	12
NC02	No Connection	G36	---	---	12
NC03	No Connection	G37	---	---	12
NC04	No Connection	G38	---	---	12
NC05	No Connection	H33	---	---	12
NC06	No Connection	H35	---	---	12
NC07	No Connection	H36	---	---	12
NC08	No Connection	H38	---	---	12
NC09	No Connection	J33	---	---	12
NC10	No Connection	J34	---	---	12
NC11	No Connection	J35	---	---	12
NC12	No Connection	J36	---	---	12
NC13	No Connection	J37	---	---	12
NC14	No Connection	J38	---	---	12
NC15	No Connection	K34	---	---	12
NC16	No Connection	K35	---	---	12
NC17	No Connection	K37	---	---	12
NC18	No Connection	K38	---	---	12
NC19	No Connection	L33	---	---	12
NC20	No Connection	L34	---	---	12
NC21	No Connection	L35	---	---	12
NC22	No Connection	L36	---	---	12
NC23	No Connection	L37	---	---	12
NC24	No Connection	L38	---	---	12
NC25	No Connection	M33	---	---	12

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
NC26	No Connection	M35	---	---	12
NC27	No Connection	M36	---	---	12
NC28	No Connection	M37	---	---	12
NC29	No Connection	M38	---	---	12
NC30	No Connection	N33	---	---	12
NC31	No Connection	N34	---	---	12
NC32	No Connection	N35	---	---	12
NC33	No Connection	N36	---	---	12
NC34	No Connection	N38	---	---	12
NC35	No Connection	P34	---	---	12
NC36	No Connection	P35	---	---	12
NC37	No Connection	P36	---	---	12
NC38	No Connection	P37	---	---	12
NC39	No Connection	P38	---	---	12
NC40	No Connection	R34	---	---	12
NC41	No Connection	R35	---	---	12
NC42	No Connection	R36	---	---	12
NC43	No Connection	R37	---	---	12
NC44	No Connection	R38	---	---	12
NC45	No Connection	T18	---	---	12
NC46	No Connection	T33	---	---	12
NC47	No Connection	T34	---	---	12
NC48	No Connection	T35	---	---	12
NC49	No Connection	T36	---	---	12
NC50	No Connection	T38	---	---	12
NC51	No Connection	U32	---	---	12
NC52	No Connection	U35	---	---	12
NC53	No Connection	U36	---	---	12
NC54	No Connection	U37	---	---	12
NC55	No Connection	U38	---	---	12
NC56	No Connection	V35	---	---	12
NC57	No Connection	V36	---	---	12
NC58	No Connection	V37	---	---	12
NC59	No Connection	V38	---	---	12
NC60	No Connection	W34	---	---	12
NC61	No Connection	W35	---	---	12
NC62	No Connection	W36	---	---	12
NC63	No Connection	W38	---	---	12

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
NC64	No Connection	AE32	---	---	12
NC65	No Connection	AG32	---	---	12
NC66	No Connection	AH32	---	---	12
NC67	No Connection	AJ32	---	---	12
NC68	No Connection	AJ33	---	---	12
NC69	No Connection	AK31	---	---	12
NC70	No Connection	AK32	---	---	12
NC71	No Connection	AL15	---	---	12
NC72	No Connection	AL18	---	---	12
NC73	No Connection	AL19	---	---	12
NC74	No Connection	AL32	---	---	12
NC75	No Connection	AM14	---	---	12
NC76	No Connection	AM15	---	---	12
NC77	No Connection	AM18	---	---	12
NC78	No Connection	AN13	---	---	12
NC79	No Connection	AN14	---	---	12
NC80	No Connection	AN15	---	---	12
NC81	No Connection	AN16	---	---	12
NC82	No Connection	AN17	---	---	12
NC83	No Connection	AP17	---	---	12
NC84	No Connection	AW17	---	---	12
NC_DET	No Connection	C42	---	---	12
Reserved Pins					
RSVD001	---	AY35	---	---	12
RSVD002	---	BA35	---	---	12
RSVD003	---	AW37	---	---	12
RSVD004	---	AV37	---	---	12
RSVD005	---	AU35	---	---	12
RSVD006	---	AV35	---	---	12
RSVD007	---	BA37	---	---	12
RSVD008	---	AY37	---	---	12
RSVD009	---	AP35	---	---	12
RSVD010	---	AR35	---	---	12
RSVD011	---	AR38	---	---	12
RSVD012	---	AP38	---	---	12
RSVD013	---	AP34	---	---	12
RSVD014	---	AR34	---	---	12
RSVD015	---	AT38	---	---	12

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
RSVD016	---	AU38	---	---	12
RSVD017	---	BA40	---	---	12
RSVD018	---	AY40	---	---	12
RSVD019	---	AV40	---	---	12
RSVD020	---	AU40	---	---	12
RSVD021	---	BA39	---	---	12
RSVD022	---	AY39	---	---	12
RSVD023	---	AW41	---	---	12
RSVD024	---	AV41	---	---	12
RSVD025	---	AR40	---	---	12
RSVD026	---	AR41	---	---	12
RSVD027	---	AL40	---	---	12
RSVD028	---	AL41	---	---	12
RSVD029	---	AT40	---	---	12
RSVD030	---	AT41	---	---	12
RSVD031	---	AM40	---	---	12
RSVD032	---	AM41	---	---	12
RSVD033	---	AH40	---	---	12
RSVD034	---	AH41	---	---	12
RSVD035	---	AD40	---	---	12
RSVD036	---	AD41	---	---	12
RSVD037	---	AJ40	---	---	12
RSVD038	---	AJ41	---	---	12
RSVD039	---	AE40	---	---	12
RSVD040	---	AE41	---	---	12
RSVD041	---	AH38	---	---	12
RSVD042	---	AH37	---	---	12
RSVD043	---	AD38	---	---	12
RSVD044	---	AD37	---	---	12
RSVD045	---	AJ38	---	---	12
RSVD046	---	AJ37	---	---	12
RSVD047	---	AE38	---	---	12
RSVD048	---	AE37	---	---	12
RSVD049	---	AG35	---	---	12
RSVD050	---	AG34	---	---	12
RSVD051	---	AC35	---	---	12
RSVD052	---	AC34	---	---	12
RSVD053	---	AH35	---	---	12

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
RSVD054	---	AH34	---	---	12
RSVD055	---	AD35	---	---	12
RSVD056	---	AD34	---	---	12
RSVD057	---	AB40	---	---	12
RSVD058	---	AA40	---	---	12
RSVD059	---	AB36	---	---	12
RSVD060	---	AA36	---	---	12
RSVD061	---	AB41	---	---	12
RSVD062	---	AA41	---	---	12
RSVD063	---	AB37	---	---	12
RSVD064	---	AA37	---	---	12
RSVD065	---	AN37	---	---	12
RSVD066	---	AN38	---	---	12
RSVD067	---	AK35	---	---	12
RSVD068	---	AK34	---	---	12
RSVD069	---	AM34	---	---	12
RSVD070	---	AM35	---	---	12
RSVD071	---	AL36	---	---	12
RSVD072	---	AL35	---	---	12
RSVD073	---	BD40	---	---	12
RSVD074	---	AL43	---	---	12
RSVD075	---	AU36	---	---	12
RSVD076	---	AP36	---	---	12
RSVD077	---	BA41	---	---	12
RSVD078	---	AP40	---	---	12
RSVD079	---	AG40	---	---	12
RSVD080	---	AG38	---	---	12
RSVD081	---	AF35	---	---	12
RSVD082	---	AB39	---	---	12
RSVD083	---	AM37	---	---	12
RSVD084	---	AY36	---	---	12
RSVD085	---	AT37	---	---	12
RSVD086	---	AV39	---	---	12
RSVD087	---	AN41	---	---	12
RSVD088	---	AF41	---	---	12
RSVD089	---	AF37	---	---	12
RSVD090	---	AE34	---	---	12
RSVD091	---	AA38	---	---	12

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
RSVD092	---	AL38	---	---	12
RSVD093	---	BA36	---	---	12
RSVD094	---	AR37	---	---	12
RSVD095	---	AW39	---	---	12
RSVD096	---	AN40	---	---	12
RSVD097	---	AF40	---	---	12
RSVD098	---	AF38	---	---	12
RSVD099	---	AE35	---	---	12
RSVD100	---	AB38	---	---	12
RSVD101	---	AL37	---	---	12
RSVD102	---	AJ43	---	---	12
RSVD103	---	AJ44	---	---	12
RSVD104	---	BC38	---	---	12
RSVD105	---	AL44	---	---	12
RSVD106	---	AW43	---	---	12
RSVD107	---	AW44	---	---	12
RSVD108	---	AY43	---	---	12
RSVD109	---	BA43	---	---	12
RSVD110	---	BA44	---	---	12
RSVD111	---	BB44	---	---	12
RSVD112	---	BC43	---	---	12
RSVD113	---	BC42	---	---	12
RSVD114	---	BD41	---	---	12
RSVD115	---	AK44	---	---	12
RSVD116	---	BD42	---	---	12
RSVD117	---	BC40	---	---	12
RSVD118	---	AB44	---	---	12
RSVD119	---	BC39	---	---	12
RSVD120	---	BD38	---	---	12
RSVD121	---	AG44	---	---	12
RSVD122	---	AH43	---	---	12
RSVD123	---	AE44	---	---	12
RSVD124	---	AF44	---	---	12
RSVD125	---	AC44	---	---	12
RSVD126	---	AG43	---	---	12
RSVD127	---	AC43	---	---	12
RSVD128	---	BD37	---	---	12
RSVD129	---	BC35	---	---	12

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
RSVD130	---	BC36	---	---	12
RSVD131	---	BD36	---	---	12
RSVD132	---	AT43	---	---	12
RSVD133	---	AR44	---	---	12
RSVD134	---	AN44	---	---	12
RSVD135	---	AU44	---	---	12
RSVD136	---	AR43	---	---	12
RSVD137	---	AP44	---	---	12
RSVD138	---	AN43	---	---	12
RSVD139	---	AU43	---	---	12
RSVD140	---	AE43	---	---	12
RSVD141	---	AA43	---	---	12
RSVD142	---	AD43	---	---	12
RSVD143	---	AA44	---	---	12
RSVD144	---	AM43	---	---	12
RSVD145	---	AV44	---	---	12
RSVD146	---	AV36	---	---	12
RSVD147	---	AR36	---	---	12
RSVD148	---	AY41	---	---	12
RSVD149	---	AP41	---	---	12
RSVD150	---	AG41	---	---	12
RSVD151	---	AG37	---	---	12
RSVD152	---	AF34	---	---	12
RSVD153	---	AA39	---	---	12
RSVD154	---	AM38	---	---	12
RSVD155	---	H15	---	---	12
RSVD156	---	J15	---	---	12
RSVD157	---	F18	---	---	12
RSVD158	---	G18	---	---	12
RSVD159	---	F16	---	---	12
RSVD160	---	G16	---	---	12
RSVD161	---	H17	---	---	12
RSVD162	---	J17	---	---	12
RSVD163	---	AU26	---	---	12
RSVD164	---	AT26	---	---	12
RSVD165	---	AW27	---	---	12
RSVD166	---	AV27	---	---	12
RSVD167	---	AU28	---	---	12

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
RSVD168	---	AT28	---	---	12
RSVD169	---	AW29	---	---	12
RSVD170	---	AV29	---	---	12
RSVD171	---	AF32	---	---	12
RSVD172	---	Y33	---	---	12
RSVD173	---	AA33	---	---	12
RSVD174	---	C15	---	---	17
RSVD175	---	D15	---	---	17
RSVD176	---	A18	---	---	17
RSVD177	---	B18	---	---	17
RSVD178	---	A16	---	---	17
RSVD179	---	B16	---	---	17
RSVD180	---	C17	---	---	17
RSVD181	---	D17	---	---	17
RSVD182	---	BB26	---	---	17
RSVD183	---	BA26	---	---	17
RSVD184	---	BD27	---	---	17
RSVD185	---	BC27	---	---	17
RSVD186	---	BB28	---	---	17
RSVD187	---	BA28	---	---	17
RSVD188	---	BD29	---	---	17
RSVD189	---	BC29	---	---	17
RSVD190	---	AD32	---	---	15
RSVD191	---	Y43	---	---	15
RSVD192	---	Y44	---	---	15
RSVD193	---	AB30	---	---	15
RSVD194	---	AB43	---	---	15
RSVD195	---	AC30	---	---	15
RSVD196	---	AD30	---	---	15
RSVD197	---	AD44	---	---	15
RSVD198	---	AE30	---	---	15
RSVD199	---	AF30	---	---	15
RSVD200	---	AF43	---	---	15
RSVD201	---	AG30	---	---	15
RSVD202	---	AH30	---	---	15
RSVD203	---	AH44	---	---	15
RSVD204	---	AK43	---	---	15
RSVD205	---	AM44	---	---	15

Table continues on the next page...

Table 1. Pinout list by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
RSVD206	---	AP43	---	---	15
RSVD207	---	AT44	---	---	15
RSVD208	---	AV43	---	---	15
RSVD209	---	AY44	---	---	15
RSVD210	---	BB43	---	---	15
RSVD211	---	BC37	---	---	15
RSVD212	---	BC41	---	---	15
RSVD213	---	BC44	---	---	15
RSVD214	---	BD35	---	---	15
RSVD215	---	BD39	---	---	15
RSVD216	---	BD43	---	---	15
RSVD217	---	AC32	---	---	15

1. Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.

2. This output is actively driven during reset rather than being tri-stated during reset.

3. MDIC[0] is grounded through an 237 Ω (for Rev. 1) or 187 Ω (for Rev. 2) precision 1% resistor and MDIC[1] is connected to GV_{DD} through an 237 Ω (for Rev. 1) or 187 Ω (for Rev. 2) precision 1% resistor. For either full or half driver strength calibration of DDR I/Os, use the same MDIC resistor value of 237 Ω (for Rev. 1) or 187 Ω (for Rev. 2). Memory controller register setting can be used to determine automatic calibration is done to full or half drive strength. These pins are used for automatic calibration of the DDR3/DDR3L IOs. The MDIC[0:1] pins must be connected to 237 Ω (for Rev. 1) or 187 Ω (for Rev. 2) precision 1% resistors.

4. This pin is a reset configuration pin. It has a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the processor is in its reset state. This pull-up is designed such that it can be overpowered by an external 4.7 kΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed.

5. Pin must **NOT** be pulled down during power-on reset. This pin may be pulled up, driven high, or if there are any externally connected devices, left in tristate. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.

6. Recommend that a weak pull-up resistor (2 to 10 kΩ) be placed on this pin to the respective power supply, or appropriate pull up resistor value for signals like HRESET_B which might require 1 kΩ.

7. This pin is an open-drain signal.

8. Recommend a pull-up resistor be placed on this pin to the respective power supply. In the I2C interface, the value of the resistor should be calculated such that maximum rise time stays under 300 ns as well as VOL be under 0.4 V at IOL = 3 mA IOL and I2C load capacitance which should not exceed 400 pF.

9. This pin has a weak (~20 kΩ) internal pull-up P-FET that is always enabled.

10. These are test signals for factory use only and must be pulled up (100 Ω to 1 kΩ) to the respective power supply for normal operation.

11. This pin requires a 200 Ω pull-up to respective power supply.

12. Do not connect. These pins should be left floating.

13. These pins must be pulled up to 1.2 V through a 180 Ω ± 1% resistor for MDC and a 330 Ω ± 1% resistor for MDIO.

14. This pin requires an external 1 kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.

15. These pins must be pulled to ground (GND).

16. This pin requires a 698 Ω pull-up to respective power supply.

17. These pins must be pulled to SerDes core logic ground (SnGND).

18. Recommend that a weak pull-up resistor (4.7 kΩ) be placed on this pin to the respective power supply.

19. These pins should be tied to ground if the diode is not utilized for temperature monitoring.

20. This pin requires a pull-up of 10 to 50 kΩ to its corresponding I/O supply if it is not a GPIO or not used as one.

21. This pin always needs to be either pulled up by 10 to 50 kΩ or down by 4.7 kΩ to GND, depending on the intended RCW setting to be high or low, respectively.

22. If used as SDHC signal, pull-up 10 to 100 kΩ to the respective I/O supply.

23. New board designs should leave a place holder for a series resistor and capacitor filter, which is in parallel and very close proximity to a 1%, 10 kΩ resistor pulling USB_IBIAS_REXT low. This allows the flexibility of populating them if needed to

avoid board coupled noise to this pin. An SMD ceramic 100 nF low ESL in series with 100 Ω SMD resistor will do the filtration needed with slight variations that suit each board case.

24. The non-ideality factor over temperature range 85C° to 105C°, n = 1.006 ± 0.003, with approximate error +/- 1 C° and approximate error under +/- 3 C° for temperature range 0 C° to 85C°.

25. In GPCM mode, this pin also serves as IFC_WE1_B.

26. T4240/T4160/T4080 Rev. 2 silicon requires SDHC_CD_B and SDHC_WP signals even when eMMC/eSDHC is used.

27. TH_VDD is a quiet power domain used for the Thermal Unit. Despite being de-featured, it should be connected to a quiet recommended supply level.

28. When Dn_MDQS_B[9:17] pins are not used; terminate with 50 Ω to VTT or 100 Ω to GND. Place termination close to T4 pin when discrete x8 or x16 DRAM is used or close to the DIMM connector when signals are connected to DIMM connector to be used only by DIMMs with x8 or x16 DRAM.

29. For T4160, this pin may be left floating or pulled up. For T4080, this pin must be pulled to ground. Pull with a 4.7 k resistor.

Warning

See **"Connection Recommendations"** for additional details on properly connecting these pins for specific applications.

3 Electrical characteristics

This section provides the AC and DC electrical specifications for the chip. The chip is currently targeted to these specifications, some of which are independent of the I/O cell but are included for a more complete reference. These are not purely I/O buffer design specifications.

3.1 Overall DC electrical characteristics

This section describes the ratings, conditions, and other characteristics.

3.1.1 Absolute maximum ratings

This table provides the absolute maximum ratings.

Table 2. Absolute maximum ratings[1]

Absolute Maximum Ratings for Supply Voltage Levels					
Characteristic	**Symbol**	**Min**	**Max**	**Unit**	**Notes**
Core and platform supply voltage	V_{DD}	-0.3	1.08	V	9, 11
PLL supply voltage (core, platform, DDR)	AV_{DD}_CGAn AV_{DD}_CGBn AV_{DD}_PLAT AV_{DD}_Dn	-0.3	1.98	V	11
PLL supply voltage (SerDes, filtered from XnV_{DD})	AV_{DD}_SDn_PLLn	-0.3 -0.3	1.65 1.48	V	11
Fuse programming override supply	PROG_SFP	-0.3	1.98	V	11
Thermal monitor unit supply	TH_V_{DD}	-0.3	1.98	V	10, 11
eSHDC, eSPI, DMA, MPIC, GPIO, system control and power management, clocking, debug, IFC, DDRCLK supply, and JTAG I/O voltage	OV_{DD}	-0.3	1.98	V	11
DUART, I^2C I/O voltage	DV_{DD}	-0.3 -0.3	2.75 1.98	V	11
DDR3 DRAM I/O voltage	GnV_{DD}	-0.3	1.58	V	11
DDR3L DRAM I/O voltage	GnV_{DD}	-0.3	1.42	V	11
Main power supply for internal circuitry of SerDes and pad power supply for SerDes receivers	SnV_{DD}	-0.3	1.08	V	11
Pad power supply for SerDes transmitter	XnV_{DD}	-0.3 -0.3	1.65 1.45	V	8, 11
Ethernet, Ethernet management interface 1 (EMI1) 1588, GPIO I/O voltage	LV_{DD}	-0.3 -0.3	2.75 1.98	V	11
Ethernet management interface 2 (EMI2) I/O voltage	—	-0.3	1.32	V	7, 11
USB PHY Transceiver supply voltage	USB_HV_{DD}	-0.3	3.63	V	11
	USB_OV_{DD}	-0.3	1.98	V	11
USB PHY Analog supply voltage	USB_SV_{DD}	-0.3	1.08	V	11

Table continues on the next page...

Table 2. Absolute maximum ratings[1] (continued)

Low Power Security Monitor supply		V_{DD_LP}		-0.3		1.08	V	11
Absolute Maximum Ratings for Storage Temperature Conditions								
Characteristic		**Symbol**		**Min**		**Max**	**Unit**	**Notes**
Storage temperature range		T_{STG}		-55		155	°C	—
Absolute Maximum Ratings for Input Signal Voltage Levels								
Interface Input Signal		**Symbol**		**Min_DCV V_input**	**Max_DCV V_input**	**Min Undershoot Voltage**	**Max Overshoot Voltage**	**Unit**	**Notes**
DDR3 and DDR3L DRAM signals		MV_{IN}		GND	Nominal GV_{DD} x 1.05	-0.3	Nominal GV_{DD} x 1.1	V	2, 13
DDR3 and DDR3L DRAM reference		$D_n\_MV_{REF}$		GND	Nominal $GV_{DD}/2$ x 1.05	-0.3	Nominal $GV_{DD}/2$ x 1.1	V	5
Ethernet (except EMI2), 1588, GPIO signals		LV_{IN}		GND	Nominal LV_{DD} x 1.1	-0.3	Nominal LV_{DD} x 1.15	V	4, 5
eSHDC, eSPI, DMA, MPIC, GPIO, system control and power management, clocking, debug, IFC, DDRCLK supply, and JTAG signals		OV_{IN}		GND	Nominal OV_{DD} x 1.1	-0.3	Nominal OV_{DD} x 1.15	V	3, 5
DUART, I^2C signals		DV_{IN}		GND	Nominal DV_{DD} x 1.1	-0.3	Nominal DV_{DD} x 1.15	V	5, 6
SerDes signals	No internal termination selected	SV_{IN}	0.8 V maximum signal swing starting from 0.3 V	S_nGND	Nominal SnV_{DD} x 1.05	0.3	Nominal SnV_{DD} x 1.1	V	5
			0.8 V maximum signal swing starting from -0.4 V	S_nGND	Nominal SnV_{DD} x 1.05	-0.4	+0.4		
	50 Ω internal termination selected	SV_{IN}		S_nGND	+0.3	-0.4	+0.4		
USB PHY Transceiver signals		USB_HV_{IN}		USB_AGND	USB_HV_{DD} + 0.3	-0.3	USB_HV_{DD} + 0.3	V	5, 12
		USB_OV_{IN}		USB_AGND	USB_OV_{DD} x 1.1	-0.3	USB_OV_{DD} x 1.15	V	5, 12

Table continues on the next page...

Table 2. Absolute maximum ratings[1] (continued)

Ethernet management interface 2 signals	—	GND	1.2 x 1.1	-0.3	1.2 x 1.15	V	—
LP Trust signal LP_TMP_DETECT_B	V_{IN_LP}	GND	1.05 x V_{DD_LP}	-0.3	1.1 x V_{DD_LP}	V	—

Notes:

1. Functional operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

3. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

4. **Caution:**LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

5. (G,O,L,D,S, USB_H, USB_O)V_{IN} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 8. Note that the Dn_MV_{REF} maximum slew rate is restricted to 25 kv/s.

6. **Caution:** DV_{IN} must not exceed DV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

7. Ethernet MII management interface 2 pins function as open drain I/Os. The interface shall conform to 1.2 V nominal voltage levels.

8. The cfg_xvdd_sel (ASLEEP) reset configuration pin must select the correct XV_{DD} voltage.

9. Supply voltage specified at the voltage sense pin. Voltage input pins should be regulated to provide specified voltage at the sense pin. For additional information, see the "Ganged sense-line implementation example" section in the *T4240 QorIQ Integrated Processor Design Checklist* (AN4559). See also note 6 in Table 3.

10. Thermal monitoring unit is de featured on current silicon, but TH_V_{DD} should be biased always.

11. Exposing device to Absolute Maximum Ratings conditions for long periods of time may affect reliability or cause permanent damage.

12. USB Overshoot or Undershoot signal time should be under 10% of signal rise time or under 2 nSec.

13. Typical DDR interface uses ODT enabled mode. For test purposes with ODT off mode, simulation should be done first so as to make sure that the overshoot signal level at the input pin does not exceed GV_{DD} by more than 10%. The Overshoot/ Undershoot period should comply with JEDEC standards.

3.1.2 Recommended operating conditions

This table provides the recommended operating conditions for this chip.

NOTE

The values shown are the recommended operating conditions and proper device operation outside these conditions is not guaranteed.

Table 3. Recommended operating conditions

Characteristic		Symbol	Recommended Value	Unit	Notes
Core and platform supply voltage	At initial start-up	V_{DD}	(VID or 1.025 V) ± 30 mV	V	4, 5, 6, 7, 9
	During normal operation		VID ± 30 mV		
PLL supply voltage (core, platform, DDR)		AV_{DD}_CGAn AV_{DD}_CGBn AV_{DD}_PLAT AV_{DD}_Dn	1.8 V ± 90 mV	V	11
PLL supply voltage (SerDes, filtered from XnV_{DD})		AV_{DD}_SDn_PLLn	1.5 V ± 75 mV or 1.35 V ± 67 mV	V	-
Fuse programming override supply		PROG_SFP	1.8 V ± 90 mV	V	2
Thermal monitor unit supply		TH_V_{DD}	1.8 V ± 90 mV	V	8
eSHDC, eSPI, DMA, MPIC, GPIO, system control and power management, clocking, debug, IFC, DDRCLK supply, and JTAG I/O voltage		OV_{DD}	1.8 V ± 90 mV	V	-
DUART, I^2C I/O voltage		DV_{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	-
DDR DRAM I/O voltage	DDR3	GnV_{DD}	1.5 V ± 75 mV	V	-
	DDR3L		1.35 V ± 67 mV		
Main power supply for internal circuitry of SerDes and pad power supply for SerDes receivers		SnV_{DD}	1.0 V ± 50 mV	V	-
Pad power supply for SerDes transmitters		XnV_{DD}	1.5 V ± 75 mV 1.35 V ± 67 mV	V	-
Ethernet, Ethernet management interface 1 (EMI1), 1588, GPIO I/O voltage		LV_{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	1
Ethernet management interface 2 (EMI2) I/O voltage		-	1.2 V ± 60 mV	V	10
USB PHY Transceiver supply voltage		USB_HV_{DD}	3.3 V ± 165 mV	V	-
		USB_OV_{DD}	1.8 V ± 90 mV	V	-
USB PHY Analog supply voltage	At initial start-up	USB_SV_{DD}	(VID or 1.025 V) ± 30 mV	V	6,7,9
	During normal operation		VID ± 30 mV		
Low Power Security Monitor supply		V_{DD_LP}	1.0 V ± 50 mV	V	-
Input voltage	DDR3 and DDR3L DRAM signals	MV_{IN}	GND to GV_{DD}	V	-
	DDR3 and DDR3L DRAM reference	Dn_MV_{REF}	$GV_{DD}/2$ ± 1%	V	-
	Ethernet (except EMI2), 1588, GPIO signals	LV_{IN}	GND to LV_{DD}	V	-
	eSHDC, eSPI, DMA, MPIC, GPIO, system control and power management,	OV_{IN}	GND to OV_{DD}	V	-

Table continues on the next page...

Table 3. Recommended operating conditions (continued)

Characteristic		Symbol	Recommended Value	Unit	Notes
	clocking, debug, IFC, DDRCLK supply, and JTAG signals				
	DUART, I^2C signals	DV_{IN}	GND to DV_{DD}	V	-
	SerDes signals	SV_{IN}	GND to SV_{DD}	V	-
	USB PHY Transceiver signals	USB_HV_{IN}	GND to USB_HV_{DD}	V	-
		USB_OV_{IN}	GND to USB_OV_{DD}	V	-
	Ethernet management interface 2 (EMI2) signals	-	GND to 1.2V	V	3
	LP Trust signal LP_TMP_DETECT_B	V_{IN_LP}	GND to V_{DD_LP}	V	-
Operating temperature range	Normal operation	T_A, T_J	T_A = 0 (min) to T_J = 105(max)	°C	-
	Extended Temperature	T_A, T_J	T_A = -40 (min) to T_J = 105(max)	°C	-
	Secure boot fuse programming	T_A, T_J	T_A = 0 (min) to T_J = 70 (max)	°C	2

1. Selecting RGMII limits to LV_{DD} = 2.5 V.

2. PROG_SFP must be supplied 1.8 V and the chip must operate in the specified fuse programming temperature range only during secure boot fuse programming. For all other operating conditions, PROG_SFP must be tied to GND, subject to the power sequencing constraints shown in Power sequencing.

3. Ethernet MII management interface 2 pins function as open drain I/Os. The interface conforms to 1.2 V nominal voltage levels.

4. Refer to Voltage ID (VID) controllable supply and Core and platform supply voltage filtering for additional information.

5. Supply voltage specified at the voltage sense pin. Voltage input pins should be regulated to provide specified voltage at the sense pin. For additional information, see the "Ganged sense-line implementation example" section in the *T4240 QorIQ Integrated Processor Design Checklist* (AN4559).

6. Operation at 1.1V is allowable for up to 25ms at initial power on. Alternatively the initial start-up voltage can power up straight to the VID voltage if the system has previously programmed that specific part's VID value.

7. Voltage ID (VID) operating range is between 0.975V to 1.025V. Regulator selection should be based on Vout range wider than VIDmin to VIDmax with resolution of 12.5mV or better.

8. Keep this pin biased to the specified voltage, despite the thermal monitoring unit being de-featured.

9. If VID is known at initial start-up, set VDD=VID else if VID is not known at initial start-up, set VDD to 1.025V and change it immediately, to VDD=VID after reading VID at the beginning of booting.

10.This supply does not have a designated pin in this device because it is used only for EMI2 signals external pull-up resistor source.

11.Keep filter close to pin. Voltage and tolerance for AV_{DD} is defined at the input of the PLL supply filter and not the pin of AV_{DD}.

This figure shows the undershoot and overshoot voltages at the interfaces of the chip.

Notes:

The overshoot/undershoot period should be less than 10% of shortest possible toggling period " bit time", of the input signal or per input signal specific protocol requirement. For GPIO input signal overshoot/undershoot period, it should be less than 10% of the SYSCLK period.

Figure 8. Overshoot/Undershoot voltage for USB_OV_{IN}/USB_HV_{IN}/LV_{IN}/OV_{IN}/MV_{IN}/ SV_{IN}/DV_{IN}

See Table 3 for actual recommended core voltage. Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 3. The input voltage threshold scales with respect to the associated I/O supply voltage. DV_{DD}, OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses differential receivers referenced by the externally supplied D*n*_MV_{REF} signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL_1.35/SSTL_1.5 electrical signaling standard. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

3.1.3 Output driver characteristics

This chip provides information on the characteristics of the output driver strengths.

NOTE

These values are preliminary estimates.

Table 4. Output drive capability

Driver type	Output impedance (Ω)	Supply voltage	Notes
DDR3 signal	18(full-strength mode) 27(half-strength mode)	GV_{DD} = 1.5 V	1
DDR3L signal	18(full-strength mode) 27(half-strength mode)	GV_{DD} = 1.35 V	1
Ethernet signals	45	LV_{DD} = 2.5 V	2
eSPI, JTAG, system control, Integrated flash controller (IFC)	45	OV_{DD} = 1.8 V	2
DUART, I^2C	45	DV_{DD} = 2.5 V DV_{DD} = 1.8 V	2
1. The drive strength of the DDR3 or DDR3L interface in half-strength mode is at T_j = 105 °C and at GV_{DD} (min). 2. Impedance value varies by +/- 20%			

3.2 Power sequencing

For power up, the requirements are as follows:

1. Bring up V_{DD}, SnV_{DD}, USB_SV_{DD}, V_{DD}_LP, USB_HV_{DD}, LV_{DD}, DV_{DD}, USB_OV_{DD}, OV_{DD}, TH_V_{DD}, AV_{DD} (cores, platform, DDR), GnV_{DD}, XnV_{DD}, and AV_{DD}_SDn_PLLn. Drive PROG_SFP = GND.
   - PORESET_B input must be driven asserted and held during this step.

   Power supplies in this step have no ordering requirement with respect to one another except for the USB power supplies per the following note.

   NOTE

   a. USB_SV_{DD} supply must ramp before or after the USB_HV_{DD} and USB_OV_{DD} supplies have ramped. The supply set that ramp first must reach 90% of its final value before a supply from the other set can be ramped up.
   b. USB_HV_{DD} and USB_OV_{DD} supplies among themselves are sequence independent.
   c. USB_HV_{DD} rise time (10% to 90%) has a minimum of 100 us.

2. Negate PORESET_B input as long as the required assertion/hold time has been met per Table 25.
3. For secure boot fuse programming, use the following steps:
   a. After negation of PORESET_B, drive PROG_SFP = 1.8 V after a required minimum delay per Table 5.

b. After fuse programming is completed, it is required to return PROG_SFP = GND before the system is power cycled (PORESET_B assertion) or powered down (V_{DD} ramp down) per the required timing specified in Table 5. See Security fuse processor, for additional details.

Warning

No activity other than that required for secure boot fuse programming is permitted while PROG_SFP is driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while PROG_SFP = GND.

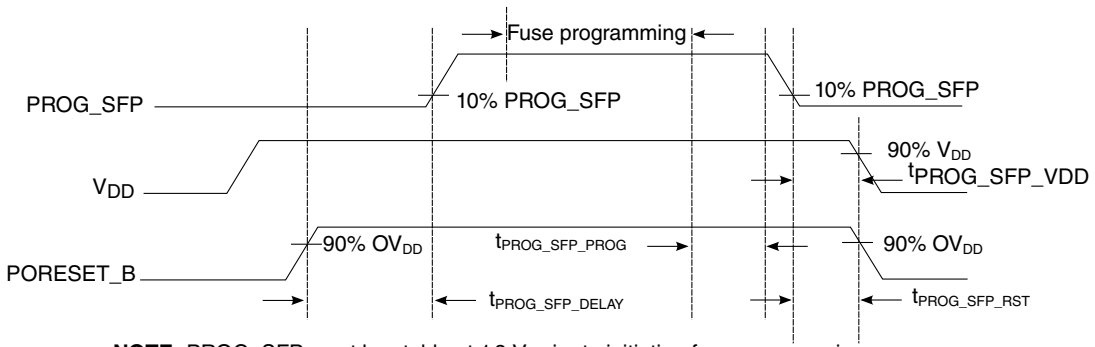
From a system standpoint, if any of the I/O power supplies ramp prior to the V_{DD} supply, there will be a brief period as the V_{DD} powers up that the I/Os associated with that I/O supply may go from being tri-stated to an indeterminate state (either driven to a logic one or zero), and extra current may be drawn by the device.

Only 300,000 POR cycles are permitted per lifetime of a device. Note that this value is based on design estimates and is preliminary.

All supplies must be at their stable values within 400 ms.

If using Trust Architecture Security Monitor battery backed features, then ensure that both, OVDD is ramped to recommended operational voltage, and SYSCLK is running, prior to VDD ramping up to the 0.5 Volt level. The running system clock should have a minimum frequency of 800HZ and a maximum frequency no greater than the supported maximum system clock frequency as in Table 18 table.

This figure provides the PROG_SFP timing diagram.



NOTE: PROG_SFP must be stable at 1.8 V prior to initiating fuse programming.

Figure 9. PROG_SFP timing diagram

This table provides information on the power-down and power-up sequence parameters for PROG_SFP.

Table 5. PROG_SFP timing [5]

Driver type	Min	Max	Unit	Notes
$t_{PROG\_SFP\_DELAY}$	100	-	SYSCLKs	1
$t_{PROG\_SFP\_PROG}$	0	-	µs	2
$t_{PROG\_SFP\_VDD}$	0	-	µs	3
$t_{PROG\_SFP\_RST}$	0	-	µs	4

1. Delay required from the deassertion of PORESET_B to driving PROG_SFP ramp up. Delay measured from PORESET_B deassertion at 90% OV_{DD} to 10% PROG_SFP ramp up.

2. Delay required from fuse programming finished to PROG_SFP ramp down start. Fuse programming must complete while PROG_SFP is stable at 1.8 V. No activity other than that required for secure boot fuse programming is permitted while PROG_SFP driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while PROG_SFP = GND. After fuse programming is completed, it is required to return PROG_SFP = GND.

3. Delay required from PROG_SFP ramp down complete to V_{DD} ramp down start. PROG_SFP must be grounded to minimum 10% PROG_SFP before V_{DD} is at 90% V_{DD}.

4. Delay required from PROG_SFP ramp down complete to PORESET_B assertion. PROG_SFP must be grounded to minimum 10% PROG_SFP before PORESET_B assertion reaches 90% OV_{DD}.

5. Only two secure boot fuse programming events are permitted per lifetime of a device.

Warning

PROG_SFP ramp up slew rate must not exceed 25kV/s. Ramp down does not have a slew rate constraint.

3.3 Power-down requirements

The power-down cycle must complete such that power supply values are below 0.4 V before a new power-up cycle can be started.

If performing secure boot fuse programming per Power sequencing, it is required that PROG_SFP = GND before the system is power cycled (PORESET_B assertion) or powered down (V_{DD} ramp down) per the required timing specified in Table 5.

NOTE

All input signals, including I/Os that are configured as inputs, driven into the chip need to monotonically increase/decrease through entire rise/fall durations.

3.4 Power characteristics

This table shows the power dissipations of the V_{DD} and S_nV_{DD} supply for various operating platform clock frequencies versus the core and DDR clock frequencies when Altivec power is gated off. See the e6500 core reference manual, section 8.6.1, "Altivec Power Down - Software Controlled Entry" for details on how to place Altivec in low power state.

Table 6. T4160 Power dissipation for rev 2 silicon with Altivec power-gated off[1]

Power mode	Core freq (MHz)	Plat freq (MHz)	DDR data rate (MT/s)	PME/FM freq (MHz)	V_{DD}[8] (V)	SnV_{DD} (V)	Junction temp. (°C)	VDD (Core + Platform) + SVDD Power (W)[1]	VDD (Core + Platform) Power	SnV_{DD} power (W)[9]	Notes
Typical	1500	667	1600	500/667	VID	1.0	65	25.9	24.2	1.7	2, 3
Thermal							105	35.1	33.4	1.7	4, 5
Maximum								41	39.3	1.7	5, 6, 7
Typical	1667	733	1866	550/733	VID	1.0	65	28.3	26.6	1.7	2, 3
Thermal							105	43.5	41.8	1.7	4, 5
Maximum								50.1	48.4	1.7	5, 6, 7
Typical	1800	733	1866	550/733	VID	1.0	65	31	29.3	1.7	2, 3
Thermal							105	45	43.3	1.7	4, 5
Maximum								52	50.3	1.7	5, 6, 7

Notes:

1. Combined power of V_{DD} and S_nV_{DD} with platform at power-on reset default state, all DDR controllers and all SerDes banks active. Does not include I/O power and Altivec is power-gated off.

2. Typical power assumes Dhrystone running with activity factor of 60% (on all cores) and is executing DMA on the platform with 100% activity factor.

3. Typical power based on nominal process distribution for this device.

4. Thermal power assumes Dhrystone running with activity factor of 60% (on all cores) and executing DMA on the platform at 100% activity factor.

5. Thermal and maximum power are based on worst-case process distribution for this device.

Table 6. T4160 Power dissipation for rev 2 silicon with Altivec power-gated off[1]

Power mode	Core freq (MHz)	Plat freq (MHz)	DDR data rate (MT/s)	PME/FM freq (MHz)	V_{DD}[8] (V)	SnV_{DD} (V)	Junction temp. (ºC)	VDD (Core + Platform) + SVDD Power (W)[1]	VDD (Core + Platform) Power	SnV_{DD} power (W)[9]	Notes

6. Maximum power assumes Dhrystone running with activity factor at 100% (on all cores) and is executing DMA on the platform at 115% activity factor.

7. Maximum power provided for power supply design sizing.

8. Voltage ID (VID) operating range is between 0.975 V to 1.025 V.

9. Total SnVDD Power Conditions (S1,S2,S3,S4). This represents the highest possible power at 105ºC based upon worst-case voltage tolerances and data patterns. Use the equations in Table 9 for average power at 105ºC.

a- SerDes1: 4 lanes @ 3.125 G.

b- SerDes2: 2 lanes @ 10.3125 G, 4 lanes @ 3.125 G.

c- SerDes3: 8 lanes @ 10.3125 G.

d- SerDes4: 4 lanes @ 5 G.

Table 7. T4080 Power dissipation for rev 2 silicon with Altivec power-gated off[1]

Power mode	Core freq (MHz)	Plat freq (MHz)	DDR data rate (MT/s)	PME/FM freq (MHz)	V_{DD}[8] (V)	SnV_{DD} (V)	Junction temp. (ºC)	VDD (Core + Platform) + SVDD Power (W)[1]	VDD (Core + Platform) Power	SnV_{DD} power (W)[9]	Notes
Typical	1500	667	1600	500/667	VID	1.0	65	20.2	18.5	1.7	2, 3
Thermal							105	28.6	26.9	1.7	4, 5
Maximum								32.3	30.6	1.7	5, 6, 7
Typical	1667	733	1866	550/733	VID	1.0	65	22.1	20.4	1.7	2, 3
Thermal							105	35.6	33.9	1.7	4, 5
Maximum								39.7	38.0	1.7	5, 6, 7

Notes:

1. Combined power of V_{DD} and S_nV_{DD} with platform at power-on reset default state, all DDR controllers and all SerDes banks active. Does not include I/O power and Altivec is power-gated off.

2. Typical power assumes Dhrystone running with activity factor of 60% (on all cores) and is executing DMA on the platform with 100% activity factor.

3. Typical power based on nominal process distribution for this device.

4. Thermal power assumes Dhrystone running with activity factor of 60% (on all cores) and executing DMA on the platform at 100% activity factor.

5. Thermal and maximum power are based on worst-case process distribution for this device.

6. Maximum power assumes Dhrystone running with activity factor at 100% (on all cores) and is executing DMA on the platform at 115% activity factor.

7. Maximum power provided for power supply design sizing.

8. Voltage ID (VID) operating range is between 0.975 V to 1.025 V.

Table 7. T4080 Power dissipation for rev 2 silicon with Altivec power-gated off[1]

Power mode	Core freq (MHz)	Plat freq (MHz)	DDR data rate (MT/s)	PME/FM freq (MHz)	V_{DD}[8] (V)	SnV_{DD} (V)	Junction temp. (ºC)	VDD (Core + Platform) + SVDD Power (W)[1]	VDD (Core + Platform) Power	SnV_{DD} power (W)[9]	Notes
9. Total SnVDD Power Conditions (S1,S2,S3,S4). This represents the highest possible power at 105ºC based upon worst-case voltage tolerances and data patterns. Use the equations in Table 9 for average power at 105ºC. a- SerDes1: 4-lanes @ 3.125 G. b- SerDes2: 2-lanes @ 10.3125 G, 4-lanes @ 3.125 G. c- SerDes3: 8-lanes @ 10.3125 G. d- SerDes4: 4-lanes @ 5 G.											

Table 8. T4161 Power dissipation for rev 2 silicon with Altivec power-gated off[1]

Power mode	Core freq (MHz)	Plat freq (MHz)	DDR data rate (MT/s)	PME/FM freq (MHz)	V_{DD}[8] (V)	SnV_{DD} (V)	Junction temp. (ºC)	VDD (Core + Platform) + SVDD Power (W)[1]	VDD (Core + Platform) Power	SnV_{DD} power (W)[9]	Notes
Typical	1500	667	1600	500/667	VID	1.0	65	22.5	20.8	1.7	2, 3
Thermal							105	30.3	28.6	1.7	4, 5
Maximum								35.4	33.7	1.7	5, 6, 7
Typical	1667	733	1866	550/733	VID	1.0	65	24.8	23.1	1.7	2, 3
Thermal							105	35.3	33.6	1.7	4, 5
Maximum								41.4	39.7	1.7	5, 6, 7
Typical	1800	733	1866	550/733	VID	1.0	65	26.1	24.4	1.7	2, 3
Thermal							105	36.2	34.5	1.7	4, 5
Maximum								42.8	41.1	1.7	5, 6, 7

Notes:

1. Combined power of V_{DD} and S_nV_{DD} with platform at power-on reset default state, all DDR controllers and all SerDes banks active. Does not include I/O power and Altivec is power-gated off.

2. Typical power assumes Dhrystone running with activity factor of 60% (on all cores) and is executing DMA on the platform with 100% activity factor.

3. Typical power based on nominal process distribution for this device.

4. Thermal power assumes Dhrystone running with activity factor of 60% (on all cores) and executing DMA on the platform at 100% activity factor.

5. Thermal and maximum power are based on worst-case process distribution for this device.

6. Maximum power assumes Dhrystone running with activity factor at 100% (on all cores) and is executing DMA on the platform at 115% activity factor.

7. Maximum power provided for power supply design sizing.

8. Voltage ID (VID) operating range is between 0.975 V to 1.025 V.

Table 8. T4161 Power dissipation for rev 2 silicon with Altivec power-gated off[1]

Power mode	Core freq (MHz)	Plat freq (MHz)	DDR data rate (MT/s)	PME/FM freq (MHz)	V_{DD}[8] (V)	SnV_{DD} (V)	Junction temp. (ºC)	VDD (Core + Platform) + SVDD Power (W)[1]	VDD (Core + Platform) Power	SnV_{DD} power (W)[9]	Notes
9. Total SnVDD Power Conditions (S1,S2,S3,S4). This represents the highest possible power at 105ºC based upon worst-case voltage tolerances and data patterns. Use the equations in Table 9 for average power at 105ºC. a- SerDes1: 4 lanes @ 3.125 G. b- SerDes2: 2 lanes @ 10.3125 G, 4 lanes @ 3.125 G. c- SerDes3: 8 lanes @ 10.3125 G. d- SerDes4: 4 lanes @ 5 G.											

Table 9. T4081 Power dissipation for rev 2 silicon with Altivec power-gated off[1]

Power mode	Core freq (MHz)	Plat freq (MHz)	DDR data rate (MT/s)	PME/FM freq (MHz)	V_{DD}[8] (V)	SnV_{DD} (V)	Junction temp. (ºC)	VDD (Core + Platform) + SVDD Power (W)[1]	VDD (Core + Platform) Power	SnV_{DD} power (W)[9]	Notes
Typical	1500	667	1600	500/667	VID	1.0	65	16.8	15.1	1.7	2, 3
Thermal							105	24	22.3	1.7	4, 5
Maximum								27.1	25.4	1.7	5, 6, 7
Typical	1667	733	1866	550/733	VID	1.0	65	18.6	16.9	1.7	2, 3
Thermal							105	28.1	26.4	1.7	4, 5
Maximum								31.6	29.9	1.7	5, 6, 7
Typical	1800	733	1866	550/733	VID	1.0	65	19.4	17.7	1.7	2, 3
Thermal							105	28.6	26.9	1.7	4, 5
Maximum								32.2	30.5	1.7	5, 6, 7

Notes:

1. Combined power of V_{DD} and S_nV_{DD} with platform at power-on reset default state, all DDR controllers and all SerDes banks active. Does not include I/O power and Altivec is power-gated off.

2. Typical power assumes Dhrystone running with activity factor of 60% (on all cores) and is executing DMA on the platform with 100% activity factor.

3. Typical power based on nominal process distribution for this device.

4. Thermal power assumes Dhrystone running with activity factor of 60% (on all cores) and executing DMA on the platform at 100% activity factor.

5. Thermal and maximum power are based on worst-case process distribution for this device.

6. Maximum power assumes Dhrystone running with activity factor at 100% (on all cores) and is executing DMA on the platform at 115% activity factor.

7. Maximum power provided for power supply design sizing.

8. Voltage ID (VID) operating range is between 0.975 V to 1.025 V.

Table 9. T4081 Power dissipation for rev 2 silicon with Altivec power-gated off[1]

Power mode	Core freq (MHz)	Plat freq (MHz)	DDR data rate (MT/s)	PME/FM freq (MHz)	V_{DD}[8] (V)	SnV_{DD} (V)	Junction temp. (ºC)	VDD (Core + Platform) + SVDD Power (W)[1]	VDD (Core + Platform) Power	SnV_{DD} power (W)[9]	Notes
9. Total SnVDD Power Conditions (S1,S2,S3,S4). This represents the highest possible power at 105ºC based upon worst-case voltage tolerances and data patterns. Use the equations in Table 9 for average power at 105ºC. a- SerDes1: 4-lanes @ 3.125 G. b- SerDes2: 2-lanes @ 10.3125 G, 4-lanes @ 3.125 G. c- SerDes3: 8-lanes @ 10.3125 G. d- SerDes4: 4-lanes @ 5 G.											

This table shows the power dissipations of the V_{DD} and S*n*V_{DD} supplies for various operating platform clock frequencies versus the core and DDR clock frequencies when Altivec power is on.

Table 10. T4160 Power dissipation for rev 2 silicon with Altivec enabled[1]

Power mode	Core freq (MHz)	Plat freq (MHz)	DDR data rate (MT/s)	PME /FM freq (MHz)	V_{DD}[8] (V)	SnV_{DD} (V)	Junction temp. (ºC)	VDD(Core + Platform) + SVDD (W)[1]	VDD (Core+ Platform) power	SnV_{DD} power (W)[9]	Notes
Typical	1500	667	1600	500/667	VID	1.0	65	27.9	26.2	1.7	2, 3
Thermal							105	37.1	35.4	1.7	4, 5
Maximum								43	41.3	1.7	5, 6, 7
Typical	1667	733	1867	550/733	VID	1.0	65	30.3	28.6	1.7	2, 3
Thermal							105	45.5	43.8	1.7	4, 5
Maximum								52.1	50.4	1.7	5, 6, 7
Typical	1800	800	1867	550/733	VID	1.0	65	33	31.3	1.7	2, 3
Thermal							105	47	45.3	1.7	4, 5
Maximum								54	52.3	1.7	5, 6, 7

Notes:

1. Combined power of V_{DD} and S_nV_{DD} with platform at power-on reset default state, all DDR controllers and all SerDes banks active. Does not include I/O power.

2. Typical power assumes Altivec benchmark running (on all cores) and is executing DMA on the platform with 100% activity factor.

3. Typical power based on nominal process distribution for this device.

4. Thermal power assumes Altivec benchmark running with work power activity factor of 100% (on all cores) and executing DMA on the platform at 100% activity factor.

5. Thermal and maximum power are based on worst-case process distribution for this device.

6. Maximum power assumes Altivec benchmark running with work power activity factor at 100% (on all cores) and is executing DMA on the platform at 115% activity factor.

Table 10. T4160 Power dissipation for rev 2 silicon with Altivec enabled[1]

Power mode	Core freq (MHz)	Plat freq (MHz)	DDR data rate (MT/s)	PME /FM freq (MHz)	V_{DD}[8] (V)	SnV_{DD} (V)	Junction temp. (ºC)	VDD(Core + Platform) + SVDD (W)[1]	VDD (Core+ Platform) power	SnV_{DD} power (W)[9]	Notes

7. Maximum power provided for power supply design sizing.

8. Voltage ID (VID) operating range is between 0.975 V to 1.025 V.

9. Total SnVDD Power Conditions (S1,S2,S3,S4). This represents the highest possible power at 105ºC based upon worst-case voltage tolerances and data patterns. Use the equations in Table 9 for average power at 105ºC.

a- SerDes1: 4-lanes @ 3.125 G.

b- SerDes2: 2-lanes @ 10.3125 G, 4-lanes @ 3.125 G.

c- SerDes3: 8-lanes @ 10.3125 G.

d- SerDes4: 4-lanes @ 5 G.

Table 11. T4080 Power dissipation for rev 2 silicon with Altivec enabled[1]

Power mode	Core freq (MHz)	Plat freq (MHz)	DDR data rate (MT/s)	PME /FM freq (MHz)	V_{DD}[8] (V)	SnV_{DD} (V)	Junction temp. (ºC)	VDD(Core + Platform) + SVDD (W)[1]	VDD (Core+ Platform) power	SnV_{DD} power (W)[9]	Notes
Typical	1500	667	1600	500/667	VID	1.0	65	21.2	19.5	1.7	2, 3
Thermal							105	29.6	27.9	1.7	4, 5
Maximum								33.3	31.6	1.7	5, 6, 7
Typical	1667	733	1867	550/733	VID	1.0	65	23.1	21.4	1.7	2, 3
Thermal							105	36.6	34.9	1.7	4, 5
Maximum								40.7	39.30	1.7	5, 6, 7

Notes:

1. Combined power of V_{DD} and S_nV_{DD} with platform at power-on reset default state, all DDR controllers and all SerDes banks active. Does not include I/O power.

2. Typical power assumes Altivec benchmark running (on all cores) and is executing DMA on the platform with 100% activity factor.

3. Typical power based on nominal process distribution for this device.

4. Thermal power assumes Altivec benchmark running with work power activity factor of 100% (on all cores) and executing DMA on the platform at 100% activity factor.

5. Thermal and maximum power are based on worst-case process distribution for this device.

6. Maximum power assumes Altivec benchmark running with work power activity factor at 100% (on all cores) and is executing DMA on the platform at 115% activity factor.

7. Maximum power provided for power supply design sizing.

8. Voltage ID (VID) operating range is between 0.975 V to 1.025 V.

9.Total SnVDD Power Conditions (S1,S2,S3,S4). This represents the highest possible power at 105ºC based upon worst-case voltage tolerances and data patterns. Use the equations in Table 9 for average power at 105ºC.

a- SerDes1: 4-lanes @ 3.125 G.

Table 11. T4080 Power dissipation for rev 2 silicon with Altivec enabled[1]

Power mode	Core freq (MHz)	Plat freq (MHz)	DDR data rate (MT/s)	PME /FM freq (MHz)	V_{DD}[8] (V)	SnV_{DD} (V)	Junction temp. (ºC)	VDD(Core + Platform) + SVDD (W)[1]	VDD (Core+ Platform) power	SnV_{DD} power (W)[9]	Notes
b- SerDes2: 2-lanes @ 10.3125 G, 4-lanes @ 3.125 G.											
c- SerDes3: 8-lanes @ 10.3125 G.											
d- SerDes4: 4-lanes @ 5 G.											

Table 12. T4161 Power dissipation for rev 2 silicon with Altivec enabled[1]

Power mode	Core freq (MHz)	Plat freq (MHz)	DDR data rate (MT/s)	PME /FM freq (MHz)	V_{DD}[8] (V)	SnV_{DD} (V)	Junction temp. (ºC)	VDD(Core + Platform) + SVDD (W)[1]	VDD (Core+ Platform) power	SnV_{DD} power (W)[9]	Notes
Typical	1500	667	1600	500/667	VID	1.0	65	24.2	22.5	1.7	2, 3
Thermal							105	32.5	30.8	1.7	4, 5
Maximum								37.6	35.9	1.7	5, 6, 7
Typical	1667	733	1867	550/733	VID	1.0	65	26.7	25	1.7	2, 3
Thermal							105	37.8	36.1	1.7	4, 5
Maximum								43.9	42.2	1.7	5, 6, 7
Typical	1800	800	1867	550/733	VID	1.0	65	28.2	26.5	1.7	2, 3
Thermal							105	38.8	37.1	1.7	4, 5
Maximum								45.5	43.8	1.7	5, 6, 7

Notes:

1. Combined power of V_{DD} and S_nV_{DD} with platform at power-on reset default state, all DDR controllers and all SerDes banks active. Does not include I/O power.

2. Typical power assumes Altivec benchmark running (on all cores) and is executing DMA on the platform with 100% activity factor.

3. Typical power based on nominal process distribution for this device.

4. Thermal power assumes Altivec benchmark running with work power activity factor of 100% (on all cores) and executing DMA on the platform at 100% activity factor.

5. Thermal and maximum power are based on worst-case process distribution for this device.

6. Maximum power assumes Altivec benchmark running with work power activity factor at 100% (on all cores) and is executing DMA on the platform at 115% activity factor.

7. Maximum power provided for power supply design sizing.

8. Voltage ID (VID) operating range is between 0.975 V to 1.025 V.

9. Total SnVDD Power Conditions (S1,S2,S3,S4). This represents the highest possible power at 105ºC based upon worst-case voltage tolerances and data patterns. Use the equations in Table 9 for average power at 105ºC.

a- SerDes1: 4-lanes @ 3.125 G.

b- SerDes2: 2-lanes @ 10.3125 G, 4-lanes @ 3.125 G.

c- SerDes3: 8-lanes @ 10.3125 G.

d- SerDes4: 4-lanes @ 5 G.

Table 13. T4081 Power dissipation for rev 2 silicon with Altivec enabled[1]

Power mode	Core freq (MHz)	Plat freq (MHz)	DDR data rate (MT/s)	PME /FM freq (MHz)	V_{DD}[8] (V)	SnV_{DD} (V)	Junction temp. (ºC)	VDD(Core + Platform) + SVDD (W)[1]	VDD (Core+ Platform) power	SnV_{DD} power (W)[9]	Notes
Typical	1500	667	1600	500/667	VID	1.0	65	17.8	16.1	1.7	2, 3
Thermal							105	25.4	23.7	1.7	4, 5
Maximum								28.5	26.8	1.7	5, 6, 7
Typical	1667	733	1867	550/733	VID	1.0	65	19.6	17.9	1.7	2, 3
Thermal							105	29.7	28	1.7	4, 5
Maximum								33.2	31.5	1.7	5, 6, 7
Typical	1800	733	1867	550/733	VID	1.0	65	20.5	18.8	1.7	2, 3
Thermal							105	30.3	28.6	1.7	4, 5
Maximum								33.9	32.2	1.7	5, 6, 7

Notes:

1. Combined power of V_{DD} and S_nV_{DD} with platform at power-on reset default state, all DDR controllers and all SerDes banks active. Does not include I/O power.

2. Typical power assumes Altivec benchmark running (on all cores) and is executing DMA on the platform with 100% activity factor.

3. Typical power based on nominal process distribution for this device.

4. Thermal power assumes Altivec benchmark running with work power activity factor of 100% (on all cores) and executing DMA on the platform at 100% activity factor.

5. Thermal and maximum power are based on worst-case process distribution for this device.

6. Maximum power assumes Altivec benchmark running with work power activity factor at 100% (on all cores) and is executing DMA on the platform at 115% activity factor.

7. Maximum power provided for power supply design sizing.

8. Voltage ID (VID) operating range is between 0.975 V to 1.025 V.

9.Total SnVDD Power Conditions (S1,S2,S3,S4). This represents the highest possible power at 105ºC based upon worst-case voltage tolerances and data patterns. Use the equations in Table 9 for average power at 105ºC.

a- SerDes1: 4-lanes @ 3.125 G.

b- SerDes2: 2-lanes @ 10.3125 G, 4-lanes @ 3.125 G.

c- SerDes3: 8-lanes @ 10.3125 G.

d- SerDes4: 4-lanes @ 5 G.

This table provides low power mode saving estimation.

Table 14. T4240/T4160/T4080 rev 2 single core, single cluster low power mode power savings, 1.0 V [1,2,3,7]

Mode	Temp	Core Frequency = 1.8 GHz	Core Frequency = 1.667 GHz	Core Frequency = 1.5 GHz	Units	Comment	Notes
PH10	65°C	0.95	0.88	0.79	Watts	Saving realized moving from PH00 to PH10 state, single core.	4
PH15	65°C	0.27	0.25	0.22	Watts	Saving realized moving from PH10 state to PH15 state, single core.	4,5
PH20	65°C	0.33	0.33	0.33	Watts	Saving realized moving from PH15 to PH20 state, single core.	4
PCL10	65°C	0.9	0.9	0.9	Watts	Saving realized moving from PH20 to PCL10 for single cluster.	6
LPM20 (T4080)	65°C	1.2	1.2	1.0	Watts	Saving realized moving from PCL10 to LPM20.	6
LPM20 (T4160)	65°C	1.2	1.2	1.0	Watts	Saving realized moving from PCL10 to LPM20.	6
LPM40	65°C	1.33	1.33	0.83	Watts	Saving realized moving from LPM20 to LPM40.	6

Notes:

1. Power for V_{DD} only.
2. Typical power assumes Dhrystone running (PH00 state) with activity factor of 60%.
3. Typical power based on nominal process distribution for this device.
4. PH10, PH15, PH20 power savings with one core. Maximum savings would be N times, where N is the number of used cores.
5. Require both threads of the core to enter the same low-power mode.
6. See the e6500 reference manual and the T4240 reference manual for additional low power mode details.
7. Also applicable for lower power T4161/T4081 devices.

This table provides all the estimated I/O power supply values based on preliminary measurements.

Table 15. T4160/T4080, T4161/T4081 I/O power dissipation

I/O Power Supply		Used in	Parameter	Typical (mW)	Maximum (mw)	Notes
LVCMOS	OV_{DD} 1.8 V	eSHDC, eSPI, DMA, MPIC, GPIO management, clocking, debug, IFC, DDRCLK supply, and JTAG	—	140	—	1, 3, 4, 5
LVCMOS	LV_{DD} 1.8 V	Ethernet, Ethernet management interface 1 (EMI1), 1588, GPIO	—	122	—	
LVCMOS	LV_{DD} 2.5 V	Ethernet, Ethernet management interface 1 (EMI1), 1588, GPIO	—	198	—	
LVCMOS	DV_{DD} 1.8 V	DUART, I 2 C	—	12	—	
LVCMOS	DV_{DD} 2.5 V	DUART, I 2 C	—	17	—	
LVCMOS	PROG_SFP 1.8V	Fuse programming	—	200	—	
LVCMOS	V_{DD}_LP 1 V	Low Power Security Monitor	—	8	—	
DDR I/O	GV_{DD} 1.5 V	All two DDR controllers	1866 MT/s	2700	3900	1, 2, 5
DDR I/O	GV_{DD} 1.5 V	All two DDR controllers	1600 MT/s	2600	3800	
DDR I/O	Dn_MV_REF	DDR3 and DDR3L DRAM reference	—	—	—	—
USB_PHY	USB_OV_{DD} 1.8 V	USB PHY Transceiver supply voltage	—	54	—	1, 5
USB_PHY	USB_HV_{DD} 3.3 V	USB PHY Transceiver supply voltage	—	59	—	
USB_PHY	USB_SV_{DD} 1 V	USB PHY Analog supply voltage	—	6	—	
PLL	AV_{DD} _CGAn 1.8 V AV_{DD} _CGBn 1.8 V AV_{DD} _PLAT 1.8 V	PLL of core and system	—	15 for each	—	1, 5
PLL_DDR	AV_{DD}_Dn 1.8 V	PLL of DDR	—	15	—	
PLL_SerDes	AV_{DD} _SDn_PLLn 1.5 V or 1.35 V	PLL of SerDes	—	60	—	
SerDes, 1.35 XV_{DD}, 1.0 V SV_{DD}	Pad power supply for single SerDes module's receivers	SV_{DD}	F_i = Lane data rate in Gbps	P_ SV_{DD} = 155.047 + 16.766 * N +	—	6

Table continues on the next page...

Table 15. T4160/T4080, T4161/T4081 I/O power dissipation (continued)

I/O Power Supply		Used in	Parameter	Typical (mW)	Maximum (mw)	Notes
			N = Total number of lanes used n_i = number of lanes running at F_i rate	3.287 * (Sum(n_i * F_i)) ± 15 mW		
SerDes, 1.35 XV_{DD}, 1.0 V SV_{DD}	Pad power supply for single SerDes module's transmitters	XV_{DD}	F_i = Lane data rate in Gbps N = Total number of lanes used n_i = number of lanes running at F_i rate	P_ XV_{DD} = 53.256 + 50.685 * N + 0.683 * (Sum(n_i * F_i)) ± 15 mW	—	6

Notes:

1. The maximum values are dependent on actual use case such as what application, external components used, environmental conditions such as temperature, voltage and frequency. This is not intended to be the maximum guaranteed power. Expect different results depending on the use case. The maximum values are estimated and they are based on simulations at 105 °C junction temperature.

2. Typical DDR power numbers are based on one 2-rank DIMM with 20% utilization, while maximum assumes 40% utilization of bus. These values are good for thermal design but for supply design it should be assumed 100% utilization of bus where DDR I/O power can be up to 7.5 Watts for the two controllers in the T4160/T4080. Writes at 60 Ω ODT & full.

3. Assuming 15 pF total capacitance load.

4. GPIOs are supported on 1.8 V and 2.5 V rails as specified in the hardware specification.

5. The typical values are estimates and based on measurements at nominal recommended voltage for the I/O power supply and assuming at 65° C junction temperature.

6. The total power numbers of XV_{DD} and SV_{DD} depend on the customer's application usecase. Power formulas assume 105° C junction temperature. If one PLL is used, then subtract 60 mW from the resulting P_ SV_{DD}. The following examples show how to use the formulas in estimating P_ SV_{DD} and P_ XV_{DD} for different SerDes usecases.

Example 1:

On a SerDes block running SGMII at 3.125 Gbps on one lane, the SerDes typical powers are expected to be:

P_ SV_{DD} = 155.047 + 16.766 * 1 + 3.287 *(1 * 3.125) ± 15 mW - (60 mW "because one PLL is used") = 122 mW ± 15 mW

P_ XV_{DD} = 53.256 + 50.685 * 1 + 0.683 * (1 * 3.125) ± 15 mW = 106 mW ± 15 mW

Example 2:

On a SerDes block running PCIe at 5 Gbps on eight lanes, the SerDes typical powers are expected to be:

P_ SV_{DD} = 155.047 + 16.766 * 8 + 3.287 * (8 * 5) ± 15 mW - (60 mW "because one PLL is used") = 361 ± 15 mW

P_ XV_{DD} = 53.256 + 50.685 * 8 + 0.683 *(8 * 5) ± 15 mW = 486 mW ± 15 mW

Example 3:

On a single SerDes block running XFI at 10.3125 Gbps on two lanes and SGMII at 3.75 G on four lanes, the single SerDes module typical powers are expected to be:

P_ SV_{DD} = 155.047 + 16.766 * 6 + 3.287 * (2 * 10.3125 + 4 * 3.75) ± 15 mW = 373 mW ± 15 mW

P_ XV_{DD} = 53.256 + 50.685 * 6 + 0.683 * (2 * 10.3125 + 4 * 3.75) ± 15 mW = 382 mW ± 15 mW

3.5 Power-on ramp rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum power-on ramp rate is required to avoid excess in-rush current.

This table provides the power supply ramp rate specifications.

Table 16. Power supply ramp rate

Parameter	Min	Max	Unit	Notes
Required ramp rate for all voltage supplies (including OV_{DD}/DV_{DD}/ GnV_{DD}/ SnV_{DD}/XnV_{DD}/LV_{DD}, all core and platform V_{DD} supplies, D*n*_MV_{REF} and all AV_{DD} supplies.)	-	25	V/ms	1, 2
Required ramp rate for PROG_SFP	-	25	V/ms	1, 2
Note: 1. Ramp rate is specified as a linear ramp from 10 to 90%. If non-linear (for example, exponential), the maximum rate of change from 200 to 500 mV is the most critical as this range might falsely trigger the ESD circuitry. 2. Over full recommended operating temperature range (see Table 3).				

3.6 Input clocks

3.6.1 System clock (SYSCLK) and real-time clock (RTC) timing specifications

This section provides the system clock and real-time clock DC and AC timing specifications.

3.6.1.1 SYSCLK and RTC DC timing specifications

This table provides the SYSCLK and RTC DC specifications.

Table 17. SYSCLK and RTC DC electrical characteristics[3]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	—	—	V	1
Input low voltage	V_{IL}	—	—	0.6	V	1
Input capacitance (SYSCLK)	C_{IN}	—	3.3	—	pF	—
Input capacitance (RTC)	C_{IN}	—	2.6	—	pF	—

Table continues on the next page...

Table 17. SYSCLK and RTC DC electrical characteristics[3] (continued)

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	-50	—	50	μA	2

Note:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN}, in this case, represents the OV_{IN} symbol referenced in Recommended operating conditions.
3. At recommended operating conditions with OV_{DD} = 1.8 V, see Table 3.

3.6.1.2 SYSCLK and RTC AC timing specifications

This table provides the SYSCLK AC timing specifications.

Table 18. SYSCLK AC timing specifications[5]

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	66.7	—	133.3	MHz	1, 2
SYSCLK cycle time	t_{SYSCLK}	7.5	—	15	ns	1, 2
SYSCLK duty cycle	t_{KHK} / t_{SYSCLK}	40	—	60	%	2
SYSCLK slew rate	—	1	—	4	V/ns	3
SYSCLK peak period jitter	—	—	—	± 150	ps	—
SYSCLK jitter phase noise at -56 dBc	—	—	—	500	KHz	4
AC Input Swing voltage	ΔV_{AC}	0.6 x OV_{DD}	—	1 x OV_{DD}	V	6

Notes:

1. **Caution:** The relevant clock ratio settings must be chosen such that the resulting SYSCLK frequency do not exceed their respective maximum or minimum operating frequencies.
2. Measured at the rising edge and/or the falling edge at OV_{DD}/2.
3. Slew rate as measured from 0.35 x OV_{DD} to 0.65 x OV_{DD}.
4. Phase noise is calculated as FFT of TIE jitter.
5. At recommended operating conditions with OV_{DD} = 1.8V, see Table 3.
6. AC swing measured relative to half OV_{DD} or VIH and VIL have equal absolute offset from OV_{DD} /2, So, Swing = (VIH-VIL)/ OVDD and ΔV_{AC} = Swing x OV_{DD}

This table provides the RTC AC timing specifications.

Table 19. RTC AC timing specifications[5]

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
RTC frequency	f_{RTC}		—	platform clock/16	MHz	1, 2
RTC cycle time	t_{RTC}	16/platform clock	—	—	ns	1, 2

Table continues on the next page...

Table 19. RTC AC timing specifications[5] (continued)

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
RTC duty cycle	t_{KHK} / t_{RTC}	40	—	60	%	2
RTC slew rate	—	1	—	4	V/ns	3
RTC peak period jitter	—	—	—	± 150	ps	—
RTC jitter phase noise at -56 dBc	—	—	—	500	KHz	4
AC Input Swing voltage	ΔV_{AC}	0.6 x OV_{DD}	—	1 x OV_{DD}	V	6

Notes:

1. **Caution:** The relevant clock ratio settings must be chosen such that it fits IEEE1588, or MPIC, or RCPM requirements.
2. Measured at the rising edge and/or the falling edge at OV_{DD}/2.
3. Slew rate as measured from 0.35 x OV_{DD} to 0.65 x OV_{DD}.
4. Phase noise is calculated as FFT of TIE jitter.
5. At recommended operating conditions with OV_{DD} = 1.8V, see Table 3.
6. AC swing measured relative to half OV_{DD} or VIH and VIL have equal absolute offset from OV_{DD} /2, So, Swing = (VIH-VIL)/ OVDD and ΔV_{AC} = Swing x OV_{DD}

3.6.2 Spread-spectrum sources

Spread-spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter to diffuse the EMI spectral content. The jitter specification given in this table considers short-term (cycle-to-cycle) jitter only. The clock generator's cycle-to-cycle output jitter should meet the chip's input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns; the chip is compatible with spread-spectrum sources if the recommendations listed in this table are observed.

Table 20. Spread-spectrum clock source recommendations[3]

Parameter	Min	Max	Unit	Notes
Frequency modulation	-	60	kHz	-
Frequency spread	-	1.0	%	1, 2

Notes:

1. SYSCLK frequencies that result from frequency spreading and the resulting core frequency must meet the minimum and maximum specifications given in Table 18.
2. Maximum spread-spectrum frequency may not result in exceeding any maximum operating frequency of the device.
3. At recommended operating conditions with OVDD = 1.8 V, see Table 3.

CAUTION

The processor's minimum and maximum SYSCLK and core/platform/DDR frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated core/platform/DDR frequency should avoid violating the stated limits by using down-spreading only.

3.6.3 Real-time clock (RTC) timing

The RTC timing input is sampled by the platform clock. The output of the sampling latch is then used as an input to the counters of the MPIC and the time base unit of the core; there is no need for jitter specification. The minimum period of the RTC signal should be greater than or equal to 16x the period of the platform clock. There is no minimum RTC frequency; RTC may be grounded if not needed.

3.6.4 Gigabit Ethernet reference clock timing

This table provides the Ethernet gigabit reference clock DC specifications.

Table 21. EC*n*_GTX_CLK125 DC electrical characteristics [1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	1.7	-	-	V	2
Input low voltage	V_{IL}	-	-	0.7	V	2
Input capacitance	C_{IN}	-	-	6	pF	-
Input current (LV_{IN} = 0 V or LV_{IN} = LV_{DD})	I_{IN}	-50	-	50	μA	3

1. At recommended operating conditions with LV_{DD} = 2.5 V

2. The min V_{IL} and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.

3. The symbol LV_{IN}, in this case, represents the LV_{IN} symbol referenced in Recommended operating conditions.

This table provides the Ethernet gigabit reference clocks AC timing specifications.

Table 22. EC*n*_GTX_CLK125 AC timing specifications [1]

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC*n*_GTX_CLK125 frequency	t_{G125}	125 - 100 ppm	125	125 + 100 ppm	MHz	-

Table continues on the next page...

Table 22. EC*n*_GTX_CLK125 AC timing specifications [1] (continued)

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
EC*n*_GTX_CLK125 cycle time	t_{G125}	-	8	-	ns	-
EC*n*_GTX_CLK125 rise and fall time LV_{DD} = 2.5 V	t_{G125R}/t_{G125F}	-	-	0.75	ns	2
EC*n*_GTX_CLK125 duty cycle 1000Base-T for RGMII	t_{G125H}/t_{G125}	47	-	53	%	3
EC*n*_GTX_CLK125 jitter	-	-	-	± 150	ps	3

1. At recommended operating conditions with LV_{DD} = 2.5 V ± 125 mV.

2. Rise and fall times for EC*n*_GTX_CLK125 are measured from 0.5 and 2.0 V for LV_{DD} = 2.5 V.

3. EC*n*_GTX_CLK125 is used to generate the GTX clock for the Ethernet transmitter with 2% degradation. The ECn_GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the GTX_CLK. See RGMII AC timing specifications for duty cycle for 10Base-T and 100Base-T reference clock.

3.6.5 DDR clock timing

This section provides the DDR clock DC and AC timing specifications.

3.6.5.1 DDR clock DC timing specifications

This table provides the DDR clock (DDRCLK) DC specifications.

Table 23. DDRCLK DC electrical characteristics[3]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	-	-	V	1
Input low voltage	V_{IL}	-	-	0.6	V	1
Input capacitance	C_{IN}	-	11		pF	-
Input current (OV_{IN}= 0 V or OV_{IN} = OV_{DD})	I_{IN}	-50	-	50	μA	2

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.

2. The symbol OV_{IN}, in this case, represents the OV_{IN} symbol referenced in Recommended operating conditions.

3. At recommended operating conditions with OV_{DD} = 1.8 V, see Table 3.

3.6.5.2 DDR clock AC timing specifications

This table provides the DDR clock (DDRCLK) AC timing specifications.

Table 24. DDRCLK AC timing specifications[5]

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
DDRCLK frequency	f_{DDRCLK}	66.7	-	133.3	MHz	1, 2
DDRCLK cycle time	t_{DDRCLK}	7.5	-	15	ns	1, 2
DDRCLK duty cycle	t_{KHK} / t_{DDRCLK}	40	-	60	%	2
DDRCLK slew rate	-	1	-	4	V/ns	3
DDRCLK peak period jitter	-	-	-	± 150	ps	-
DDRCLK jitter phase noise at -56 dBc	-	-	-	500	KHz	4
AC Input Swing voltage	ΔV_{AC}	0.6 x OV_{DD}	-	1 x OV_{DD}	V	6

Notes:

1. **Caution:** The relevant clock ratio settings must be chosen such that the resulting DDRCLK frequency do not exceed their respective maximum or minimum operating frequencies.

2. Measured at the rising edge and/or the falling edge at $OV_{DD}/2$.

3. Slew rate as measured from 0.35 x OV_{DD} to 0.65 x OV_{DD}.

4. Phase noise is calculated as FFT of TIE jitter.

5. At recommended operating conditions with OV_{DD} = 1.8V, see Table 3.

6. AC swing measured relative to half OV_{DD} or VIH and VIL have equal absolute offset from OV_{DD} /2, So, Swing = (VIH-VIL)/ OVDD and ΔV_{AC} = Swing x OV_{DD} .

3.6.6 Other input clocks

A description of the overall clocking of this device is available in the chip reference manual in the form of a clock subsystem block diagram. For information about the input clock requirements of functional modules sourced external of the chip, such as SerDes, Ethernet management, eSDHC, IFC, see the specific interface section.

3.7 RESET initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements. This table describes the AC electrical specifications for the RESET initialization timing.

Table 25. RESET Initialization timing specifications

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of PORESET_B	1	-	ms	1
Required input assertion time of HRESET_B	32	-	SYSCLKs	2, 3
Maximum rise/fall time of PORESET_B signal	-	1	SYSCLK	4
Maximum rise/fall time of HRESET_B signal	-	4	SYSCLK	4

Table continues on the next page...

Table 25. RESET Initialization timing specifications (continued)

Parameter/Condition	Min	Max	Unit	Notes
PLL input setup time with stable SYSCLK before HRESET_B negation	100	-	µs	-
Input setup time for POR configs with respect to negation of PORESET_B	4	-	SYSCLKs	2
Input hold time for all POR configs with respect to negation of PORESET_B	2	-	SYSCLKs	2
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of PORESET_B	-	5	SYSCLKs	2

1. PORESET_B must be driven asserted before the core and platform power supplies are powered up.

2. SYSCLK is the primary clock input for the chip.

3. The device asserts HRESET_B as an output when PORESET_B is asserted to initiate the power-on reset process. The device releases HRESET_B sometime after PORESET_B is deasserted. The exact sequencing of HRESET_B deassertion is documented in section "Power-On Reset Sequence" in the chip reference manual.

4. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing. For example On table 1, notes 6 and 7, recommends a week pull up resistor for HRESET signal pin in the range of 2K to 10K Ohms, But PCB designers have to reduce the pull up resistor (min of 280 Ohms) or in addition use bidirectional level shifter to comply with maximum rise/fall time requirement for HRESET if this pin is too loaded.

This table provides the PLL lock times.

Table 26. PLL lock times

Parameter/Condition	Min	Max	Unit	Notes
PLL lock times (Core, platform, DDR only)	-	100	µs	-

3.8 DDR3 and DDR3L SDRAM controller

This section describes the DC and AC electrical specifications for the DDR3 and DDR3L SDRAM controller interface. Note that the required GV_{DD}(typ) voltage is 1.5 V when interfacing to DDR3 SDRAM and the GV_{DD}(typ) voltage is 1.35 V when interfacing to DDR3L SDRAM.

NOTE

When operating at a DDR data rate of 1866 MT/s, only one dual-ranked module per memory controller is supported.

3.8.1 DDR3 and DDR3L SDRAM interface DC electrical characteristics

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3 SDRAM.

Table 27. DDR3 SDRAM interface DC electrical characteristics (GV_{DD} = 1.5 V)[1, 7]

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	D*n*_MV_{REF}	0.49 x GV_{DD}	0.51 x GV_{DD}	V	2, 3, 4
Input high voltage	V_{IH}	D*n*_MV_{REF} + 0.100	GV_{DD}	V	5
Input low voltage	V_{IL}	GND	D*n*_MV_{REF} - 0.100	V	5
I/O leakage current	I_{OZ}	-100	100	µA	6

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.

2. D*n*_MV_{REF} is expected to be equal to 0.5 x GV_{DD} and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on D*n*_MV_{REF} may not exceed the D*n*_MV_{REF} DC level by more than ±1% of GV_{DD}(i.e. ±15 mV).

3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to D*n*_MV_{REF} with a min value of D*n*_MV_{REF} - 0.04 and a max value of D*n*_MV_{REF} + 0.04. V_{TT} should track variations in the DC level of D*n*_MV_{REF}.

4. The voltage regulator for D*n*_MV_{REF} must meet the specifications stated in Table 29.

5. Input capacitance load for DQ, DQS, and DQS_B are available in the IBIS models.

6. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

7. For recommended operating conditions, see Table 3.

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3L SDRAM.

Table 28. DDR3L SDRAM interface DC electrical characteristics (GV_{DD} = 1.35 V)[1, 7]

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	D*n*_MV_{REF}	0.49 x GV_{DD}	0.51 x GV_{DD}	V	2, 3, 4
Input high voltage	V_{IH}	D*n*_MV_{REF} + 0.090	GV_{DD}	V	5
Input low voltage	V_{IL}	GND	D*n*_MV_{REF} - 0.090	V	5
I/O leakage current	I_{OZ}	-100	100	µA	6

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.

2. D*n*_MV_{REF} is expected to be equal to 0.5 x GV_{DD} and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on D*n*_MV_{REF} may not exceed the D*n*_MV_{REF} DC level by more than ±1% of GV_{DD} (i.e. ±13.5mV).

3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to D*n*_MV_{REF} with a min value of D*n*_MV_{REF} - 0.04 and a max value of D*n*_MV_{REF} + 0.04. V_{TT} should track variations in the DC level of D*n*_MV_{REF}.

Table 28. DDR3L SDRAM interface DC electrical characteristics (GV_{DD} = 1.35 V)[1, 7]

Parameter	Symbol	Min	Max	Unit	Note
4. The voltage regulator for D*n*_MV_{REF} must meet the specifications stated in Table 29.					
5. Input capacitance load for DQ, DQS, and DQS_B are available in the IBIS models.					
6. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.					
7. For recommended operating conditions, see Table 3.					

This table provides the current draw characteristics for D*n*_MV_{REF}.

Table 29. Current draw characteristics for D*n*_MV_{REF}[1]

Parameter	Symbol	Min	Max	Unit	Notes
Current draw for DDR3 SDRAM for D*n*_MV_{REF}	I_{Dn_MVREF}	-	500	µA	-
Current draw for DDR3L SDRAM for D*n*_MV_{REF}	I_{Dn_MVREF}	-	500	µA	-
Note:					
1. For recommended operating conditions, see Table 3.					

3.8.2 DDR3 and DDR3L SDRAM interface AC timing specifications

This section provides the AC timing specifications for the DDR SDRAM controller interface. The DDR controller supports DDR3 and DDR3L memories. Note that the required GV_{DD}(typ) voltage is 1.5 V when interfacing to DDR3 SDRAM and the required GV_{DD}(typ) voltage is 1.35 V when interfacing to DDR3L SDRAM.

3.8.2.1 DDR3 and DDR3L SDRAM interface input AC timing specifications

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3 SDRAM.

Table 30. DDR3 and DDR3L SDRAM interface input AC timing specifications[3]

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS-MDQ/MECC	t_{CISKEW}			ps	1
1866 MT/s data rate		-93	93		
1600 MT/s data rate		-112	112		
1333 MT/s data rate		-125	125		
1200 MT/s data rate		-142	142		
1066 MT/s data rate		-170	170		

Table continues on the next page...

Table 30. DDR3 and DDR3L SDRAM interface input AC timing specifications[3] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Tolerated Skew for MDQS-MDQ/MECC	t_{DISKEW}			ps	2
1866 MT/s data rate		-175	175		
1600 MT/s data rate		-200	200		
1333 MT/s data rate		-250	250		
1200 MT/s data rate		-275	275		
1066 MT/s data rate		-300	300		

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. This must be subtracted from the total timing budget.

2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}.This can be determined by the following equation: $t_{DISKEW} = \pm(T \div 4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.

3. For recommended operating conditions, see Table 3.

This figure shows the DDR3 and DDR3L SDRAM interface input timing diagram.

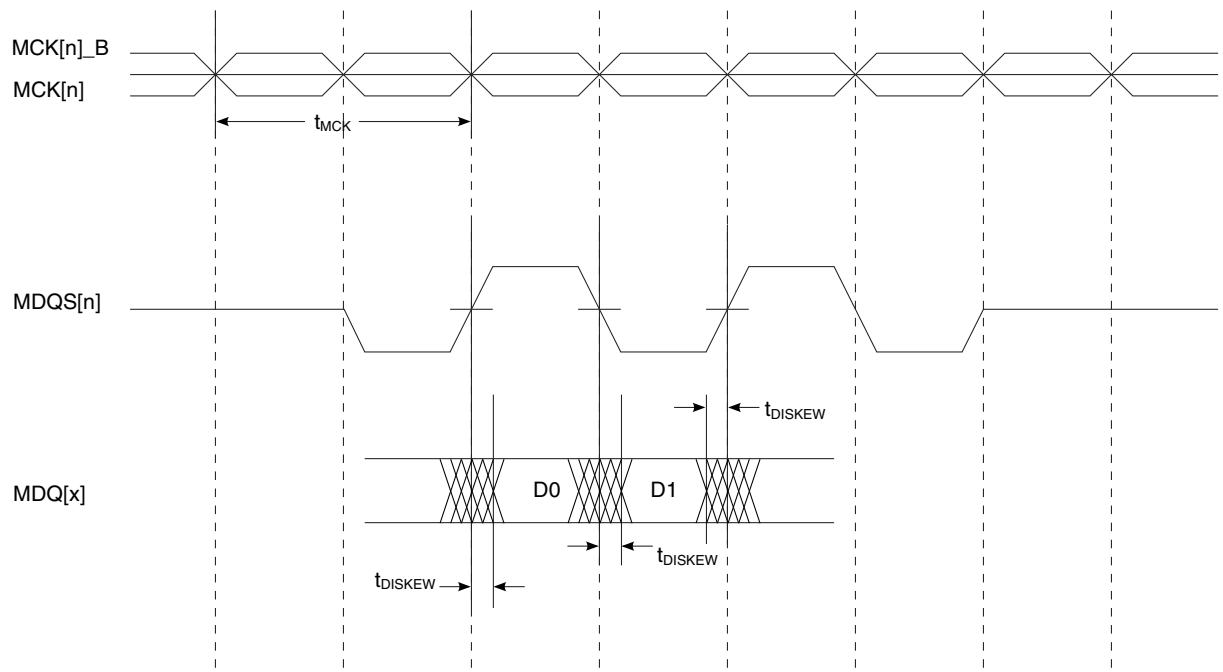


Figure 10. DDR3 and DDR3L SDRAM Interface Input Timing Diagram

3.8.2.2 DDR3 and DDR3L SDRAM interface output AC timing specifications

This table contains the output AC timing targets for the DDR3 SDRAM interface.

Table 31. DDR3 and DDR3L SDRAM interface output AC timing specifications[7]

Parameter	Symbol[1]	Min	Max	Unit	Notes
MCK[n] cycle time	t_{MCK}	0.938	2	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}			ns	3
1866 MT/s data rate		0.410	-		
1600 MT/s data rate		0.495	-		
1333 MT/s data rate		0.606	-		
1200 MT/s data rate		0.675	-		
1066 MT/s data rate		0.744	-		
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}			ns	3
1866MT/s data rate		0.390	-		
1600 MT/s data rate		0.495	-		
1333 MT/s data rate		0.606	-		
1200 MT/s data rate		0.675	-		
1066 MT/s data rate		0.744	-		
MCK to MDQS Skew	t_{DDKHMH}			ns	4
> 1600 MT/s data rate		-0.150	0.150		4, 6
> 1066 MT/s data rate, ≤ 1600 MT/s data rate		-0.245	0.245		4, 6
MDQ/MECC/MDM output Data eye	$t_{DDKXDEYE}$			ns	5
1866 MT/s data rate		0.350	-		
1600 MT/s data rate		0.400	-		
1333 MT/s data rate		0.500	-		
1200 MT/s data rate		0.550	-		
1066 MT/s data rate		0.600	-		
MDQS preamble	t_{DDKHMP}	0.9 x t_{MCK}	-	ns	-
MDQS postamble	t_{DDKHME}	0.4 x t_{MCK}	0.6 x t_{MCK}	ns	-

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time.

2. All MCK/MCK_B and MDQS/MDQS_B referenced measurements are made from the crossing of the two signals.

3. ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK_B, MCS_B, and MDQ/MECC/MDM/MDQS.

4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This is typically set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the chip reference manual for a description and explanation of the timing modifications enabled by the use of these bits.

5. Available eye for data (MDQ), ECC (MECC), and data mask (MDM) outputs at the pin of the processor. Memory controller will center the strobe (MDQS) in the available data eye at the DRAM (end point) during the initialization.

6. Note that for data rates of 1200 MT/s or higher, it is required to program the start value of the DQS adjust for write leveling.

7. For recommended operating conditions, see Table 3.

NOTE

For the ADDR/CMD setup and hold specifications in Table 31, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.

This figure shows the DDR3 and DDR3L SDRAM interface output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

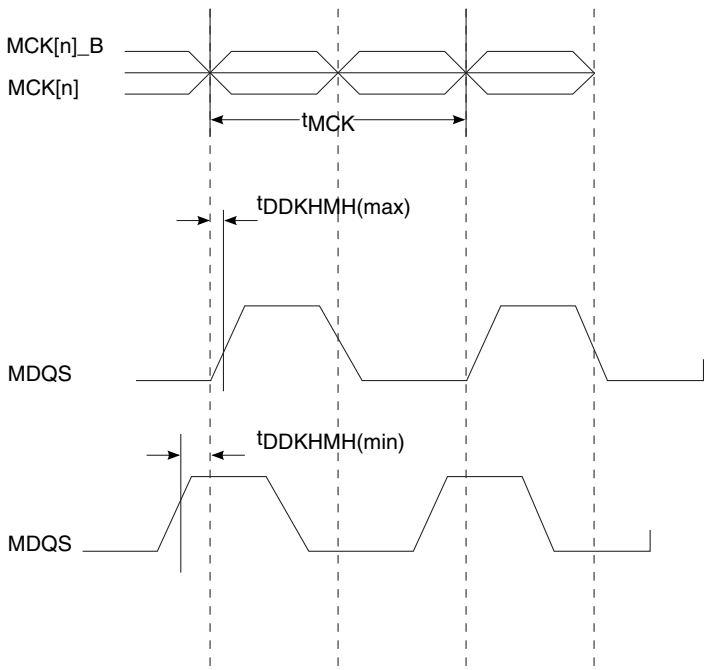


Figure 11. t_{DDKHMH} timing diagram

This figure shows the DDR3 and DDR3L SDRAM output timing diagram.

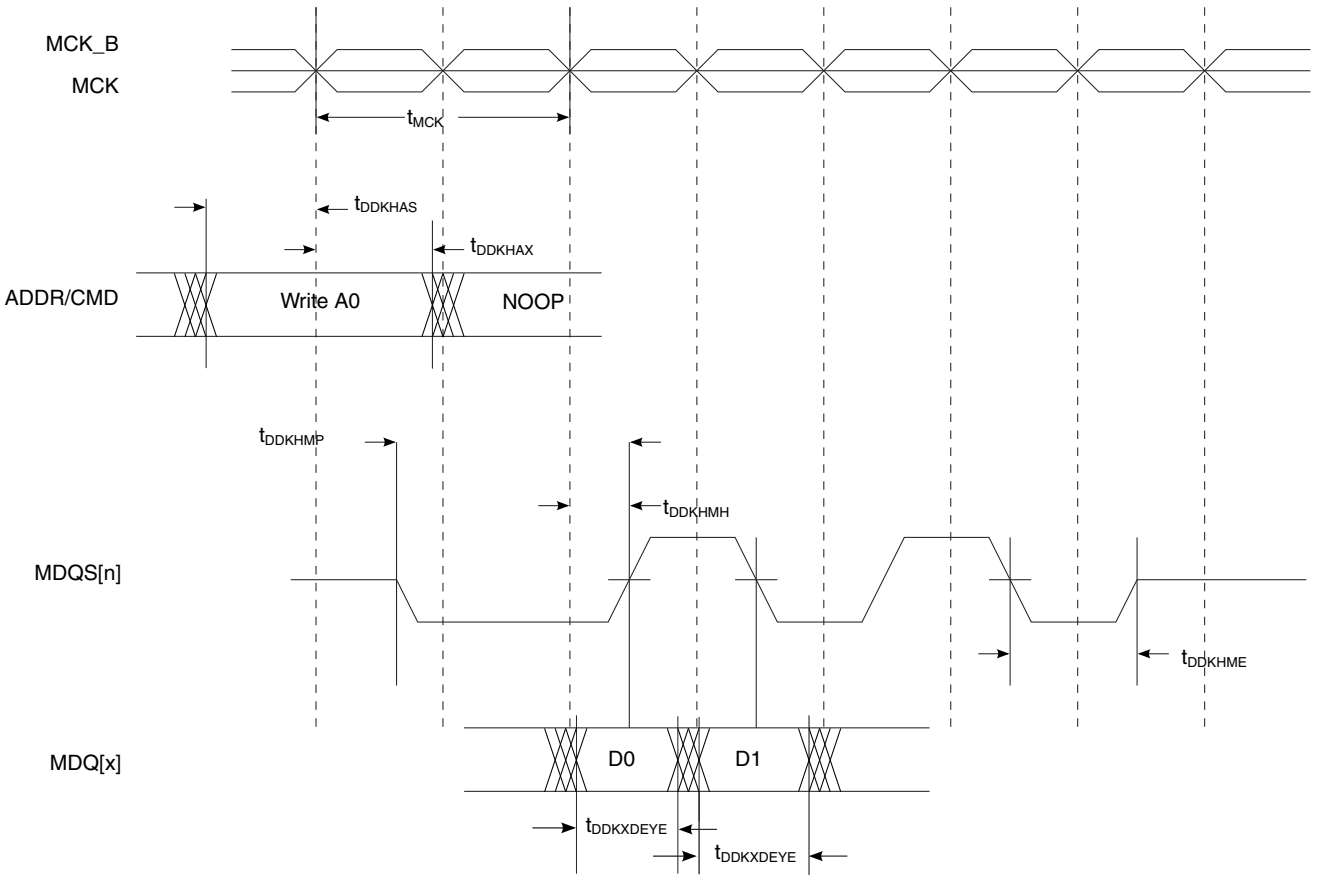


Figure 12. DDR3 and DDR3L output timing diagram

3.9 eSPI interface

This section describes the DC and AC electrical specifications for the eSPI interface.

3.9.1 eSPI DC electrical characteristics

This table provides the DC electrical characteristics for the eSPI interface operating at OV_{DD} = 1.8 V.

Table 32. eSPI DC electrical characteristics (1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	-	V	1
Input low voltage	V_{IL}	-	0.6	V	1
Input current (V_{IN} = 0 V or V_{IN} = OV_{DD})	I_{IN}	-50	50	μA	2
Output high voltage	V_{OH}	1.35	-	V	-

Table continues on the next page...

Table 32. eSPI DC electrical characteristics (1.8 V)[3] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
(OV_{DD} = min, I_{OH} = -0.5 mA)					
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

Notes:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 3.

3.9.2 eSPI AC timing specifications

This table provides the eSPI input and output AC timing specifications.

Table 33. eSPI AC timing specifications[3]

Parameter/Condition	Symbol [2]	Min	Max	Unit	Notes
SPI_MOSI output-Master data (internal clock) hold time	t_{NIKHOX}	n1 + ($t_{PLATFORM\_CLK}$ * SPMODE[HO_ADJ])	-	ns	1, 2, 4
SPI_MOSI output-Master data (internal clock) delay	t_{NIKHOV}	-	n2 + ($t_{PLATFORM\_CLK}$ * SPMODE[HO_ADJ])	ns	1, 2, 4
SPI_CS outputs-Master data (internal clock) hold time	$t_{NIKHOX2}$	0	-	ns	1
SPI_CS outputs-Master data (internal clock) delay	$t_{NIKHOV2}$	-	6.0	ns	1
SPI inputs-Master data (internal clock) input setup time	t_{NIIVKH}	3.0	-	ns	-
SPI inputs-Master data (internal clock) input hold time	t_{NIIXKH}	0	-	ns	-
Clock-high time	t_{NIKCKH}	4	-	ns	
Clock-low time	t_{NIKCKL}	4	-	ns	-

Notes:

1. See the chip reference manual for details about the SPMODE register.
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
3. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).
4. n1 and n2 values are -1.0 and 1.0 respectively.

This figure provides the AC test load for the eSPI.

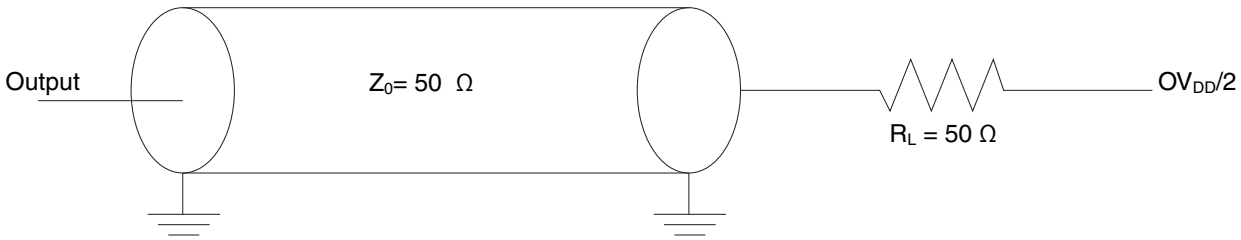


Figure 13. eSPI AC test load

This figure provides the eSPI clock output timing diagram.

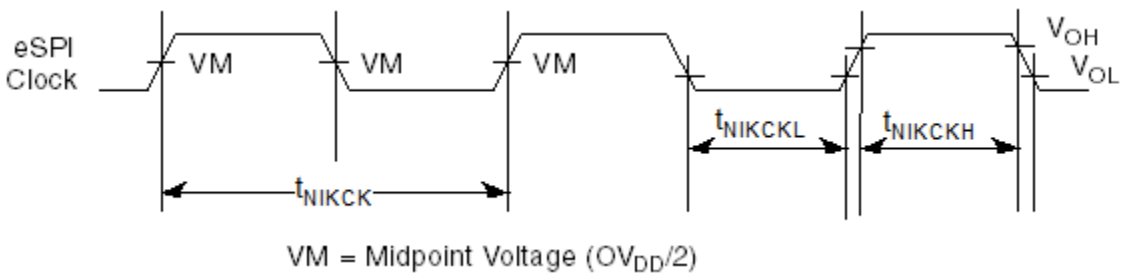


Figure 14. eSPI clock output timing diagram

This figure represents the AC timing from Table 33 in master mode (internal clock). Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge. Also, note that the clock edge is selectable on eSPI.

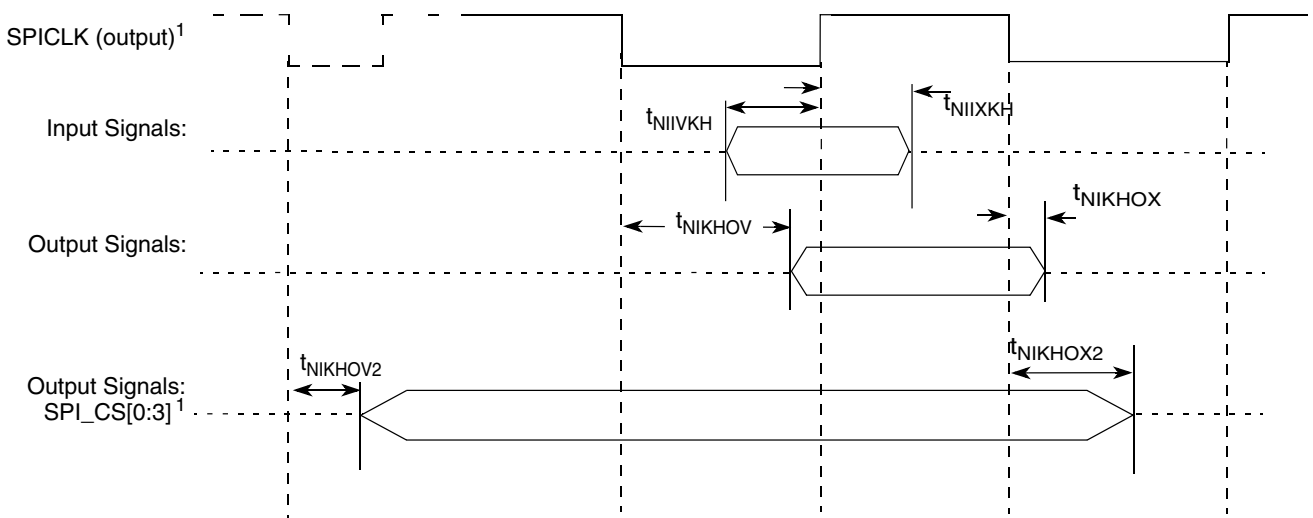


Figure 15. eSPI AC timing in master mode (internal clock) diagram

1. SPICLK appears on the interface only after CS assertion.

3.10 DUART interface

This section describes the DC and AC electrical specifications for the DUART interface.

3.10.1 DUART DC electrical characteristics

This table provides the DC electrical characteristics for the DUART interface at DV_{DD} = 2.5 V.

Table 34. DUART DC electrical characteristics(2.5 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.7	-	V	1
Input low voltage	V_{IL}	-	0.7	V	1
Input current (DV_{IN} = 0 V or DV_{IN} = DV_{DD})	I_{IN}	-50	50	μA	2
Output high voltage (DV_{DD} = min, I_{OH} = -1 mA)	V_{OH}	2.0	-	V	-
Output low voltage (DV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	-	0.4	V	-
Notes: 1. The min $V_{IL}$and max V_{IH} values are based on the min and max DV_{IN} respective values found in Table 3. 2. The symbol DV_{IN} represents the input voltage of the supply. It is referenced in Recommended operating conditions. 3. For recommended operating conditions, see Table 3.					

This table provides the DC electrical characteristics for the DUART interface at DV_{DD} = 1.8 V.

Table 35. DUART DC electrical characteristics(1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	-	V	1
Input low voltage	V_{IL}	-	0.6	V	1
Input current (DV_{IN} = 0 V or DV_{IN} = DV_{DD})	I_{IN}	-50	50	μA	2
Output high voltage (DV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (DV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-
Notes: 1. The min $V_{IL}$and max V_{IH} values are based on the min and max DV_{IN} respective values found in Table 3. 2. The symbol DV_{IN} represents the input voltage of the supply. It is referenced in Recommended operating conditions. 3. For recommended operating conditions, see Table 3.					

3.10.2 DUART AC electrical specifications

This table provides the AC timing parameters for the DUART interface.

Table 36. DUART AC timing specifications

Parameter/Condition	Value	Unit	Notes
Minimum baud rate	f_{PLAT}/(2 x 1,048,576)	baud	1, 3
Maximum baud rate	f_{PLAT}/(2 x 16)	baud	1, 2
Notes: 1. f_{PLAT} refers to the internal platform clock. 2. The actual attainable baud rate is limited by the latency of interrupt processing. 3. The middle of a start bit is detected as the eighth sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.			

3.11 Ethernet interface, Ethernet management interface 1 and 2, IEEE Std 1588™

This section provides the AC and DC electrical characteristics for the Ethernet controller and the Ethernet management interfaces.

3.11.1 SGMII electrical specifications

See SGMII interface.

3.11.2 RGMII electrical specifications

This section discusses the electrical characteristics for the RGMII interface.

3.11.2.1 RGMII DC electrical characteristics

This table shows the DC electrical characteristics for the RGMII interface.

Table 37. RGMII DC electrical characteristics(LV_{DD} = 2.5 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.70	-	V	1
Input low voltage	V_{IL}	-	0.70	V	1
Input current (LV_{IN}= 0 V or LV_{IN}= LV_{DD})	I_{IN}	-50	50	µA	2
Output high voltage (LV_{DD} = min, I_{OH} = -1.0 mA)	V_{OH}	2.00	LV_{DD} + 0.3	V	-

Table continues on the next page...

Table 37. RGMII DC electrical characteristics(LV_{DD} = 2.5 V)[3] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	GND - 0.3	0.40	V	-

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.

2. The symbol LV_{IN}, in this case, represents the LV_{IN} symbol referenced in Recommended operating conditions.

3. For recommended operating conditions, see Table 3.

3.11.2.2 RGMII AC timing specifications

This table presents the RGMII AC timing specifications.

Table 38. RGMII AC timing specifications (LV_{DD} = 2.5 V)[8]

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
Data to clock output skew (at transmitter)	t_{SKRGT_TX}	-750	0	1250	ps	7,9
Data to clock input skew (at receiver)	t_{SKRGT_RX}	1.0	-	2.6	ns	2,10
RGMII RX_CLK Clock period duration	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	3, 4
Duty cycle for Gigabit	t_{RGTH}/t_{RGT}	45	50	55	%	-
Rise time (20%-80%)	t_{RGTR}	-	-	0.75	ns	5, 6
Fall time (20%-80%)	t_{RGTF}	-	-	0.75	ns	5, 6

Notes:

1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII timing. Note that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).

2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns is added to the associated clock signal. Many PHY vendors already incorporate the necessary delay inside their device. If so, additional PCB delay is probably not needed.

3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.

4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.

5. Applies to inputs and outputs.

6. System/board must be designed to ensure this input requirement to the chip is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

7. The frequency of ECn_RX_CLK (input) should not exceed the frequency of ECn_GTX_CLK (output) by more than 300 ppm.

8. For recommended operating conditions, see Table 3.

9. IEEE spec mandates tSKRGT_TX = +- 0.5ns. Per erratum A-005177 we see tSKRGT_TX has a wider output skew range from -0.75ns to 1.25ns which is larger than the spec asks for. If can not cope with this wide skew then use RGMII at 100 Mbps or 10 Mbps (which allows larger maximum RX skews) or terminate 1000 Mbps RGMII links with PHYs that accommodate larger RX skews or terminate to a second Rev2 device.

10. This device has better input clock to data skew tSKRGT_RX tolerance (1ns to 3.5ns) than spec (1ns to 2.6ns) requires.

This figure shows the RGMII AC timing and multiplexing diagrams.

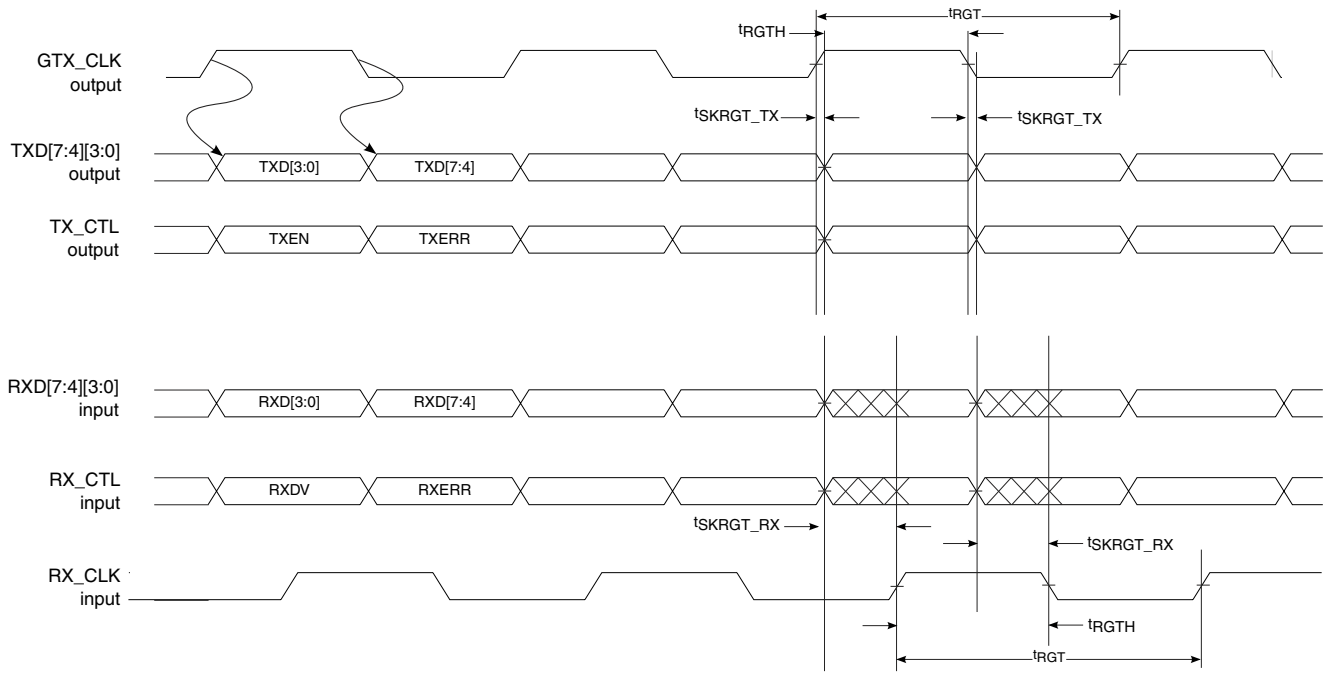


Figure 16. RGMII AC timing and multiplexing diagrams

Warning

NXP guarantees timings generated from the MAC. Board designers must ensure delays needed at the PHY or the MAC.

3.11.3 Ethernet management interface (EMI)

This section discusses the electrical characteristics for the EMI1 and EMI2 interfaces.

Frame Manager 2's external GE MDIO configures external GE PHYs connected to EMI1 pins. Frame Manager 2's external 10GE MDIO configures external XAUI, XFI and HiGig/HiGig2 PHYs connected to EMI2 pins.

The EMI1 interface timing is compatible with IEEE Std 802.3™ clause 22 and EMI2 interface timing is compatible with IEEE Std 802.3™ clause 45. The External MDIO interfaces on FM1 are not available for use.

3.11.3.1 Ethernet management interface 1 DC electrical characteristics

The DC electrical characteristics for EMI1_MDIO and EMI1_MDC are provided in this section.

Table 39. Ethernet management interface 1 DC electrical characteristics (LV_{DD} = 2.5 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.70	-	V	1
Input low voltage	V_{IL}	-	0.70	V	1
Input current (LV_{IN}=0V or LV_{IN}=LV_{DD})	I_{IN}	-50	50	µA	2
Output high voltage (LV_{DD} = min, I_{OH} = -1.0 mA)	V_{OH}	2.00	LV_{DD} + 0.3	V	-
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	GND - 0.3	0.40	V	-

Notes:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol VIN, in this case, represents the LV_{IN} symbol referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 3.

Table 40. DC electrical characteristics (1.8 V)

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	-	V	1
Input low voltage	V_{IL}	-	0.60	V	1
Input current (LV_{IN}= 0V or LV_{IN}=LV_{DD})	I_{IN}	-50	50	µA	2
Output high voltage (LV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (LV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.40	V	-

Notes:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN}/QV_{IN} values found in Table 3.
2. The symbol VIN, in this case, represents the OV_{IN} symbol referenced in Recommended operating conditions.

3.11.3.2 Ethernet management interface 2 DC electrical characteristics

Ethernet management interface 2 pins function as open drain I/Os. The interface conforms to 1.2 V nominal voltage levels. The DC electrical characteristics for EMI2_MDIO and EMI2_MDC are provided in this section.

Table 41. Ethernet management interface 2 DC electrical characteristics (1.2 V)[1]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.84	-	V	-
Input low voltage	V_{IL}	-	0.36	V	-
Output low voltage (I_{OL} = 5.5 mA)	V_{OL}	-	0.2	V	-
Input capacitance	C_{IN}	-	10	pF	-

Notes:

1. For recommended operating conditions, see Table 3.

3.11.3.3 Ethernet management interface 1 AC electrical specifications

This table provides the Ethernet management interface 1 AC timing specifications.

Table 42. Ethernet management interface 1 AC timing specifications[6]

Parameter/Condition		Symbol[1]	Min	Typ	Max	Unit	Notes
MDC frequency ($1/T_{MDC\_CIK}$)		f_{MDC}	—	—	2.5	MHz	2
MDC clock pulse width high		t_{MDCH}	160	—	—	ns	—
MDC to MDIO delay	Rev1 MDIO_CFG[EHOLD] = 0 MDIO_CFG[NEG] = 0	t_{MDKHDX}	(Y x t_{enet_clk}) - 3, Y = 2 x MDIO_CFG[MDIO_HOLD] + 1	—	(Y x t_{enet_clk}) + 3, Y = 2 x MDIO_CFG[MDIO_HOLD] + 1	ns	3, 4, 5
	Rev2 MDIO_CFG[NEG] = 0 MDIO_CFG[EHOLD] = 0	t_{MDKHDX}	(Y x t_{enet_clk}) - 3, Y = 2 x MDIO_CFG[MDIO_HOLD] + 1	—	(Y x t_{enet_clk}) + 3, Y = 2 x MDIO_CFG[MDIO_HOLD] + 1	ns	3, 4, 5
	Rev2 MDIO_CFG[NEG] = 0 MDIO_CFG[EHOLD] = 1	t_{MDKHDX}	(Y x t_{enet_clk}) - 3, Y = 8 x MDIO_CFG[MDIO_HOLD] +1	—	(Y x t_{enet_clk}) + 3, Y = 8 x MDIO_CFG[MDIO_HOLD] + 1	ns	3, 4, 5
	Rev2 MDIO_CFG[NEG] = 1	t_{MDKHDX}	(Y x T_{MDC_CIK}) - 3, Y = ½	—	(Y x T_{MDC_CIK}) + 3, Y = ½	ns	4
MDIO to MDC setup time		t_{MDDVKH}	9	—	—	ns	—
MDIO to MDC hold time		t_{MDDXKH}	0	—	—	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time.

2. This parameter is dependent on the Ethernet clock frequency. (MDIO_CFG [MDIO_CLK_DIV] field determines the clock frequency of the MgmtClk Clock MDIO_MDC).

3. This parameter is dependent on the Ethernet clock frequency. The delay is equal to Y x Ethernet clock periods ± 3 ns. For example, in default rev1 silicon, with an Ethernet clock of 400 MHz, the min/max delay is = (Y x t_{enet_clk}) ± 3 ns = ((2 x 2 + 1) x 1/400 M) ± 3 ns = 12.5 ns ± 3 ns.

Default values for Rev 1: silicon:
- MDIO_CFG[MDIO_HOLD]= 3'b010 which selects Y = 2 x 2 + 1 = 5 tenet_clk cycles.
- MDIO_CFG[NEG] = 0, in Rev 1, NEG bit field was not visible.
- MDIO_CFG[EHOLD] = 0, in Rev 1, NEG bit field was not visible.

Default values for Rev 2 silicon:
- MDIO_CFG[MDIO_HOLD]= 3'b010, since MDIO_CFG[NEG] = 1 then Y = ½.

Table 42. Ethernet management interface 1 AC timing specifications[6]

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes

• MDIO_CFG[NEG] = 1
• MDIO_CFG[EHOLD] = 0
 	
• For Rev 1 silicon: Y = 2 x MDIO_CFG[MDIO_HOLD] + 1
• For Rev 2 silicon:
  • If MDIO_CFG[EHOLD] = 0 and MDIO_CFG[NEG] = 0 then Y = 2 x MDIO_CFG[MDIO_HOLD] + 1
  • If MDIO_CFG[EHOLD] = 1 and MDIO_CFG[NEG] = 0 then Y = 8 x MDIO_CFG[MDIO_HOLD] + 1
  • If MDIO_CFG[NEG] = 1 then Y = ½ . Thus, Y is not affected by MDIO_CFG[HOLD] and MDIO_CFG[EHOLD] when MDIO_CFG[NEG] = 1. For example, in this case, if MDC clock = 2.5 MHz, then min/max of t_{MDKHDX} delay is = Y * T_{MDC_CIK} ± 3 ns = ½ x 1/2.5 M ± 3 ns = 200 ns ± 3 ns.
 	
4. t_{MDKHDX} transition:
• For Rev 1 silcon: t_{MDKHDX} is MDC positive edge to MDIO transition.
• For Rev 2 silicon:
  • If MDIO_CFG[NEG] = 0 then t_{MDKHDX} is MDC positive edge to MDIO transition.
  • If MDIO_CFG[NEG] = 1 then t_{MDKHDX} is MDC negative edge to MDIO transition.
  • The default value of MDIO_CFG [MDIO_CLK_DIV] is 0 which means no MDIO clock is available. Recommended to configure this field in PBL.
 	
5. t_{enet_clk} is the Ethernet clock period derived from Frame Manager clock, FM clock. t_{enet_clk}=1/FM_clock.
 	
6. For recommended operating conditions, see Table 3.						

3.11.3.4 Ethernet management interface 2 AC electrical characteristics

This table provides the Ethernet management interface 2 AC timing specifications.

Table 43. Ethernet management interface 2 AC timing specifications[6]

Parameter/Condition		Symbol[1]	Min	Typ	Max	Unit	Notes
MDC frequency (1/T_{MDC_CIK})		f_{MDC}	—	—	2.5	MHz	2
MDC clock pulse width high		t_{MDCH}	160	—	—	ns	—
MDC to MDIO delay	Rev1 MDIO_CFG[EHOLD] = 0 MDIO_CFG[NEG] = 0	t_{MDKHDX}	(Y x t_{enet_clk}) - 3, Y = 2 x MDIO_CFG[MDIO_HOLD] + 1	—	(Y x t_{enet_clk}) + 3, Y = 2 x MDIO_CFG[MDIO_HOLD] + 1	ns	3, 4, 5
	Rev2 MDIO_CFG[NEG] = 0 MDIO_CFG[EHOLD] = 0	t_{MDKHDX}	(Y x t_{enet_clk}) - 3, Y = 2 x MDIO_CFG[MDIO_HOLD] + 1	—	(Y x t_{enet_clk}) + 3, Y = 2 x MDIO_CFG[MDIO_HOLD] + 1	ns	3, 4, 5
	Rev2 MDIO_CFG[NEG] = 0	t_{MDKHDX}	(Y x t_{enet_clk}) - 3,	-	(Y x t_{enet_clk}) + 3,	ns	3, 4, 5

Table continues on the next page...

Table 43. Ethernet management interface 2 AC timing specifications[6] (continued)

Parameter/Condition		Symbol[1]	Min	Typ	Max	Unit	Notes
	MDIO_CFG[EHOLD] = 1		Y = 8 x MDIO_CFG[MDIO_HOLD] + 1		Y = 8 x MDIO_CFG[MDIO_HOLD] +1		
	Rev2 MDIO_CFG[NEG] = 1	t_{MDKHDX}	($Y \times T_{MDC\_CIK}$) - 3, Y = ½	—	($Y \times T_{MDC\_CIK}$) + 3, Y = ½	ns	4
MDIO to MDC setup time		t_{MDDVKH}	8	—	—	ns	7
MDIO to MDC hold time		t_{MDDXKH}	0	—	—	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time.

2. This parameter is dependent on the Ethernet clock frequency (MDIO_CFG [MDIO_CLK_DIV] field determines the clock frequency of the MgmtClk Clock MDIO_MDC).

3. This parameter is dependent on the Ethernet clock frequency. The delay is equal to Y x Ethernet clock periods ± 3 ns. For example, in default rev1 silicon, with an Ethernet clock of 400 MHz, the min/max delay is = ($Y \times t_{enet\_clk}$) = ((2 x 2 + 1) x 1/400M) ± 3 ns = 12.5 ns ± 3 ns.

Default values for Rev 1: silicon:
- MDIO_CFG[MDIO_HOLD] = 3'b010, which selects Y = 2 x 2 + 1 = 5 tenet_clk cycles.
- MDIO_CFG[NEG] = 0, in Rev 1, NEG bit field was not visible.
- MDIO_CFG[EHOLD] = 0, in Rev 1, NEG bit field was not visible.

Default values for Rev 2 silicon:
- MDIO_CFG[MDIO_HOLD] = 3'b010, since MDIO_CFG[NEG] = 1 then Y = ½.
- MDIO_CFG[NEG] = 1
- MDIO_CFG[EHOLD] = 0

- For Rev 1 silicon: Y = 2 x MDIO_CFG[MDIO_HOLD] + 1
- For Rev 2 silicon:
  - If MDIO_CFG[EHOLD] = 0 and MDIO_CFG[NEG] = 0 then Y = 2 x MDIO_CFG[MDIO_HOLD] + 1
  - If MDIO_CFG[EHOLD] = 1 and MDIO_CFG[NEG] = 0 then Y = 8 x MDIO_CFG[MDIO_HOLD] + 1
  - If MDIO_CFG[NEG] = 1 then Y = ½ . Thus Y is not affected by MDIO_CFG[HOLD] and MDIO_CFG[EHOLD] when MDIO_CFG[NEG]=1. For example in this case If MDC clock = 2.5 MHz, then min/max of t_{MDKHDX} delay is = $Y * T_{MDC\_CIK}$ ± 3 ns = ½ x 1/2.5 M ± 3ns = 200 ns ±3 ns.

4. t_{MDKHDX} transition:

- For Rev 1 silcon: t_{MDKHDX} is MDC positive edge to MDIO transition.
- For Rev 2 silicon:
  - If MDIO_CFG[NEG] = 0 then t_{MDKHDX} is MDC positive edge to MDIO transition.
  - If MDIO_CFG[NEG]= 1 then t_{MDKHDX} is MDC negative edge to MDIO transition.
  - The default value of MDIO_CFG [MDIO_CLK_DIV] is 0, which means no MDIO clock is available. Recommended to configure this field in PBL.

5. t_{enet_clk} is the Ethernet clock period derived from Frame Manager clock (FM clock). t_{enet_clk} = 1/FM_clock.

6. For recommended operating conditions, see Table 3.

Table 43. Ethernet management interface 2 AC timing specifications[6]

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
7. The actual setup time varies with the MDC slew rate. For a 180 Ω MDC pull-up and 470 pF load, the setup time is expected to be 68 ns measured at 50% points. To ensure setup time is met, the EMI2 clock frequency may need to be reduced from the default setting by selecting a larger clock divide via configuration of MDIO_CFG[MDIO_CLK_DIV] associated with EMI2.						

This figure shows the Ethernet management interface timing diagram.

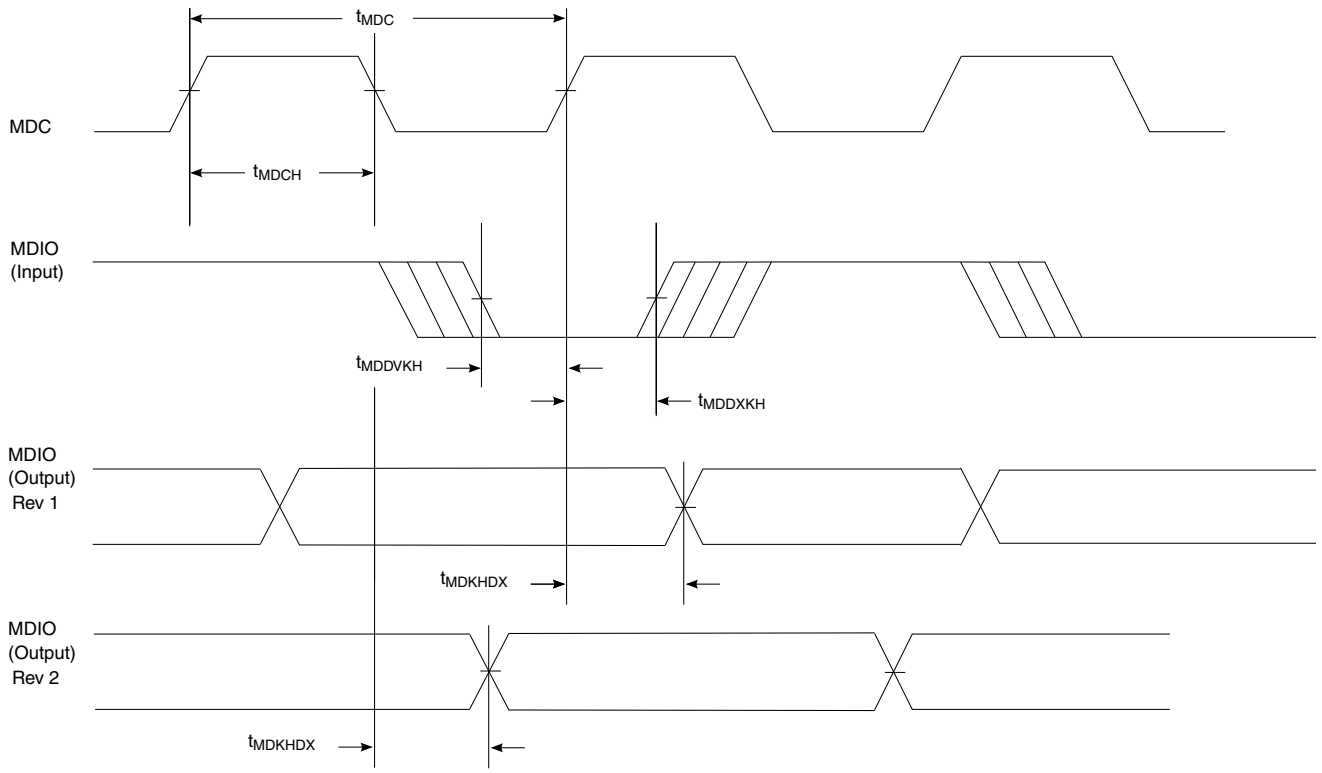


Figure 17. Ethernet management interface timing diagram

3.11.4 IEEE 1588 electrical specifications

3.11.4.1 IEEE 1588 DC electrical characteristics

This table shows IEEE 1588 DC electrical characteristics when operating at LV_{DD} = 2.5 V supply.

Table 44. IEEE 1588 DC electrical characteristics(LV_{DD} = 2.5 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.70	-	V	1

Table continues on the next page...

Table 44. IEEE 1588 DC electrical characteristics(LV_{DD} = 2.5 V)[3] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Input low voltage	V_{IL}	-	0.70	V	1
Input current (LV_{IN}= 0 V or LV_{IN}= LV_{DD})	I_{IN}	-50	50	µA	2
Output high voltage (LV_{DD} = min, I_{OH} = -1.0 mA)	V_{OH}	2.00	LV_{DD} + 0.3	V	-
Output low voltage (LV_{DD} = min, I_{OL} = 1.0 mA)	V_{OL}	GND - 0.3	0.40	V	-
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.					
2. The symbol LV_{IN}, in this case, represents the LV_{IN} symbol referenced in Recommended operating conditions.					
3. For recommended operating conditions, see Table 3.					

This table shows IEEE 1588 DC electrical characteristics when operating at LV_{DD} = 1.8 V supply.

Table 45. IEEE 1588 DC electrical characteristics(LV_{DD} = 1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	-	V	1
Input low voltage	V_{IL}	-	0.6	V	1
Input current (LV_{IN}= 0 V or LV_{IN}= LV_{DD})	I_{IN}	-50	50	µA	2
Output high voltage (LV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	LV_{DD} + 0.3	V	-
Output low voltage (LV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	GND - 0.3	0.40	V	-
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.					
2. The symbol LV_{IN}, in this case, represents the LV_{IN} symbol referenced in Recommended operating conditions.					
3. For recommended operating conditions, see Table 3.					

3.11.4.2 IEEE 1588 AC specifications

This table provides the IEEE 1588 AC timing specifications.

Table 46. IEEE 1588 AC timing specifications[3]

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
TSEC_1588_CLK_IN clock period	$t_{T1588CLK}$	6	-		ns	
TSEC_1588_CLK_IN duty cycle	$t_{T1588CLKH}$/ $t_{T1588CLK}$	40	50	60	%	
TSEC_1588_CLK_IN peak-to-peak jitter	$t_{T1588CLKINJ}$	-	-	250	ps	-
Rise time TSEC_1588_CLK_IN (20% -80%)	$t_{T1588CLKINR}$	1.0	-	2.0	ns	-
Fall time TSEC_1588_CLK_IN (80% -20%)	$t_{T1588CLKINF}$	1.0	-	2.0	ns	-
TSEC_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	2 x $t_{T1588CLK}$	-	-	ns	2

Table continues on the next page...

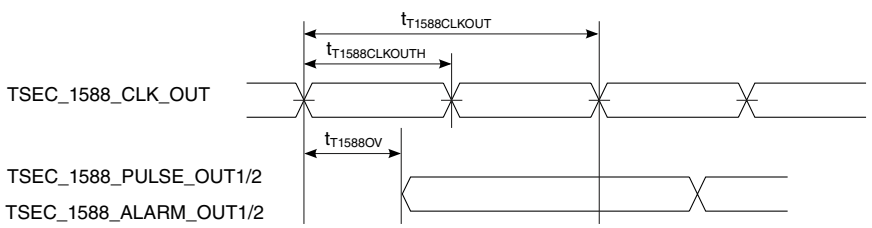
Table 46. IEEE 1588 AC timing specifications[3] (continued)

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
TSEC_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}$/ $t_{T1588CLKOUT}$	30	50	70	%	-
TSEC_1588_PULSE_OUT1/2, TSEC_1588_ALARM_OUT1/2 hold time	$t_{T1588OV}$	0.5	-	4.0	ns	-
TSEC_1588_TRIG_IN1/2 pulse width	$t_{T1588TRIGH}$	2 x $t_{T1588CLK}$	-	-	ns	1

Notes:

1. It needs to be at least two times the clock period of the clock selected by TMR_CTRL[CKSEL]. See the chip reference manual for a description of TMR_CTRL registers.
2. There are 3 input clock sources for 1588 i.e. TSEC_1588_CLK_IN, RTC, and MAC clock / 2 in rev1 silicon and MAC clock in rev2 silicon.
3. For recommended operating conditions, see Table 3.

This figure shows the data and command output AC timing diagram.



Note: The output delay is counted starting at the rising edge if $t_{T1588CLKOUT}$ is non-inverting. Otherwise, it is counted starting at the falling edge.

Figure 18. IEEE 1588 output AC timing

This figure shows the data and command input AC timing diagram.

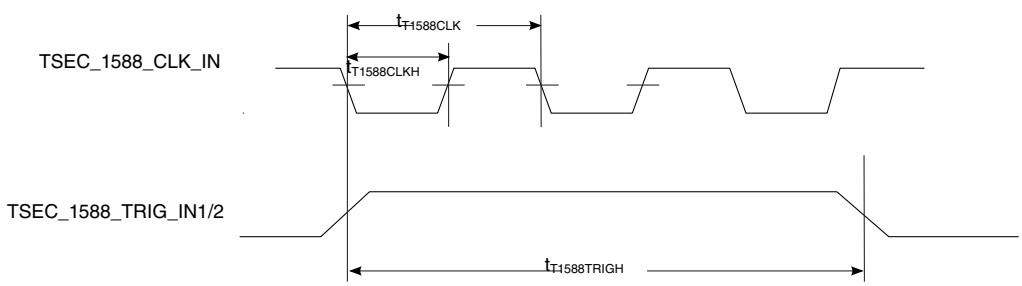


Figure 19. IEEE 1588 input AC timing

3.12 USB interface

This section provides the AC and DC electrical specifications for the USB interface.

3.12.1 USB DC electrical characteristics

This table provides the DC electrical characteristics for the USB interface at USB_HV_{DD} = 3.3 V.

Table 47. USB DC electrical characteristics (USB_HV_{DD} = 3.3 V) [3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	-	V	1, 4
Input low voltage	V_{IL}	-	0.8	V	1, 4
Input current (USB_HV_{IN} = 0 V or USB_HV_{IN}= USB_HV_{DD})	I_{IN}	-100	+100	µA	2, 4
Output high voltage (USB_HV_{DD} = min, I_{OH} = -2 mA)	V_{OH}	2.8	-	V	5
Output low voltage (USB_HV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	-	0.3	V	5

Notes:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max USB_HV_{IN} values found in Table 3.
2. The symbol USB_HV_{IN}, in this case, represents the USB_HV_{IN} symbol referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 3.
4. These specifications only apply to the following pins: USB1_PWRFAULT, USB2_PWRFAULT, USB1_UDM (full-speed mode), USB2_UDM (full-speed mode), USB1_UDP (full-speed mode), and USB2_UDP (full-speed mode).
5. This specification only applies to USB1_DRVVBUS and USB2_DRVVBUS pins.

This table provides the DC electrical characteristics for the USBCLK at OV_{DD} = 1.8 V.

Table 48. USBCLK DC electrical characteristics (1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	-	V	1
Input low voltage	V_{IL}	-	0.6	V	1
Input current (V_{IN} = 0 V or V_{IN} = OV_{DD})	I_{IN}	-50	50	µA	2

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 3.

3.12.2 USB AC timing specifications

This section describes the AC timing specifications for the on-chip USB PHY. See Chapter 7 in the *Universal Serial Bus Revision 2.0 Specification* for more information.

This table provides the USB clock input (USBCLK) AC timing specifications.

Table 49. USBCLK AC timing specifications[1]

Parameter/Condition	Symbol	Condition	Min	Typ	Max	Unit	Notes
USBCLK Frequency	$f_{USB\_CLK\_IN}$	-	-	24	-	MHz	-
USBCLK Rise/Fall time	t_{USRF}	Measured between 10% and 90%	-	-	6	ns	2
USBCLK frequency tolerance	t_{CLK_TOL}	-	-0.005	0	0.005	%	-
USBCLK duty cycle	t_{CLK_DUTY}	Measured at rising edge and/or failing edge at $OV_{DD}/2$	40	50	60	%	-
USBCLK total input jitter/time interval error	t_{CLK_PJ}	RMS value measured with a second-order, band-pass filter of 500 kHz to 4 MHz bandwidth at 10^{-12} BER	-	-	5	ps	-

Notes:

1. For recommended operating conditions, see Table 3

2. System/board must be designed to ensure the input requirement to the device is achieved. Proper device operation is guaranteed for inputs meeting this requirement by design, simulation, characterization, or functional testing.

3.13 Integrated flash controller

This section describes the DC and AC electrical specifications for the integrated flash controller.

3.13.1 Integrated flash controller DC electrical characteristics

This table provides the DC electrical characteristics for the integrated flash controller when operating at OV_{DD}= 1.8 V.

Table 50. Integrated flash controller DC electrical characteristics (1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.25	-	V	1
Input low voltage	V_{IL}	-	0.6	V	1
Input current (V_{IN} = 0 V or V_{IN} = OV_{DD})	I_{IN}	-50	50	µA	2
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.6	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.32	V	-

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.

2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Recommended operating conditions.

Table 50. Integrated flash controller DC electrical characteristics (1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Note
3. For recommended operating conditions, see Table 3.					

3.13.2 Integrated flash controller AC timing specification

This section describes the AC timing specifications for the integrated flash controller.

3.13.2.1 Test condition

This figure provides the AC test load for the integrated flash controller.

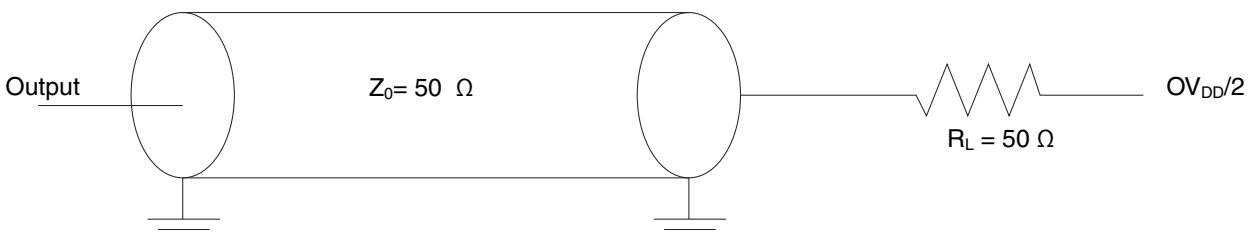


Figure 20. Integrated flash controller AC test load

3.13.2.2 Integrated flash controller AC timing specifications

All output signal timings are relative to the falling edge of any IFC_CLK. The external circuit must use the rising edge of the IFC_CLKs to latch the data.

All input timings are relative to the rising edge of IFC_CLKs.

This table describes the timing specifications of the integrated flash controller interface.

Table 51. Integrated flash controller timing specifications (OV_{DD} = 1.8 V)[5]

Parameter/Condition	Symbol[1]	Min	Max	Unit	Notes
IFC_CLK cycle time	t_{IBK}	10	-	ns	-
IFC_CLK duty cycle	t_{IBKH}/ t_{IBK}	45	55	%	-
IFC_CLK[n] skew to IFC_CLK[m]	$t_{IBKSKEW}$	0	±75	ps	2
Input setup	t_{IBIVKH}	4	-	ns	-
Input hold	t_{IBIXKH}	1	-	ns	-
Output delay	t_{IBKLOV}	-	1.5	ns	-
Output hold	t_{IBKLOX}	-2	-	ns	4

Table continues on the next page...

Table 51. Integrated flash controller timing specifications (OV_{DD} = 1.8 V)[5] (continued)

Parameter/Condition	Symbol[1]	Min	Max	Unit	Notes
IFC_CLK to output high impedance for AD	t_{IBKLOZ}	-	2	ns	3

1. All signals are measured from OV_{DD}/2 of rising/falling edge of IFC_CLK to OV_{DD}/2 of the signal in question.
2. Skew measured between different IFC_CLK signals at OV_{DD}/2.
3. For purposes of active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Here the negative sign means output transit happens earlier than the falling edge of IFC_CLK.
5. For recommended operating conditions, see Table 3.

This figure shows the AC timing diagram.

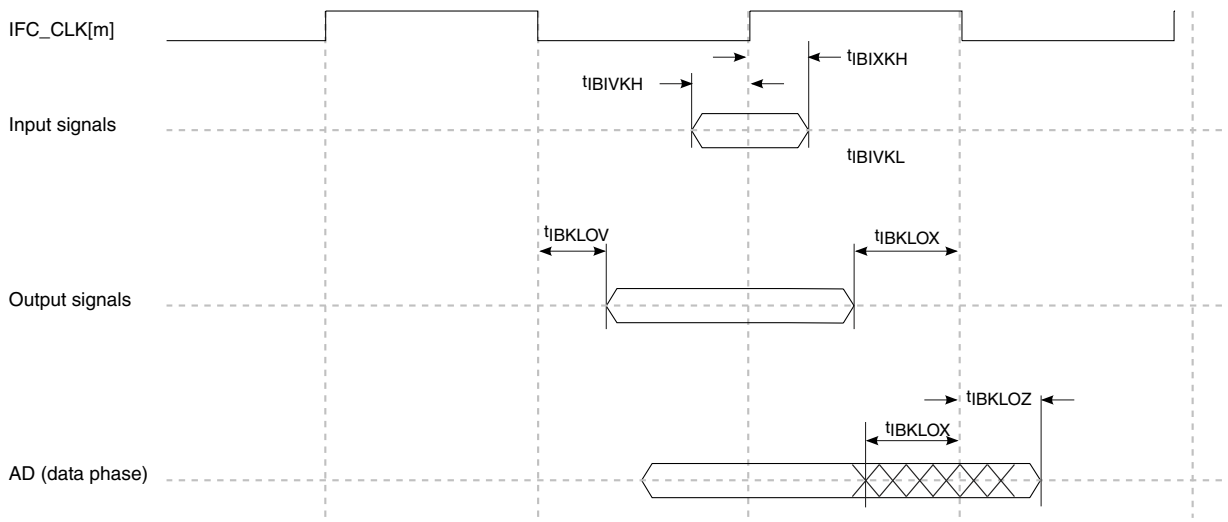


Figure 21. Integrated flash controller signals

The figure above applies to all the controllers that IFC supports.

- For input signals, the AC timing data is used directly for all controllers.
- For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay.

This figure shows how the AC timing diagram applies to GPCM. The same principle also applies to other controllers of IFC.

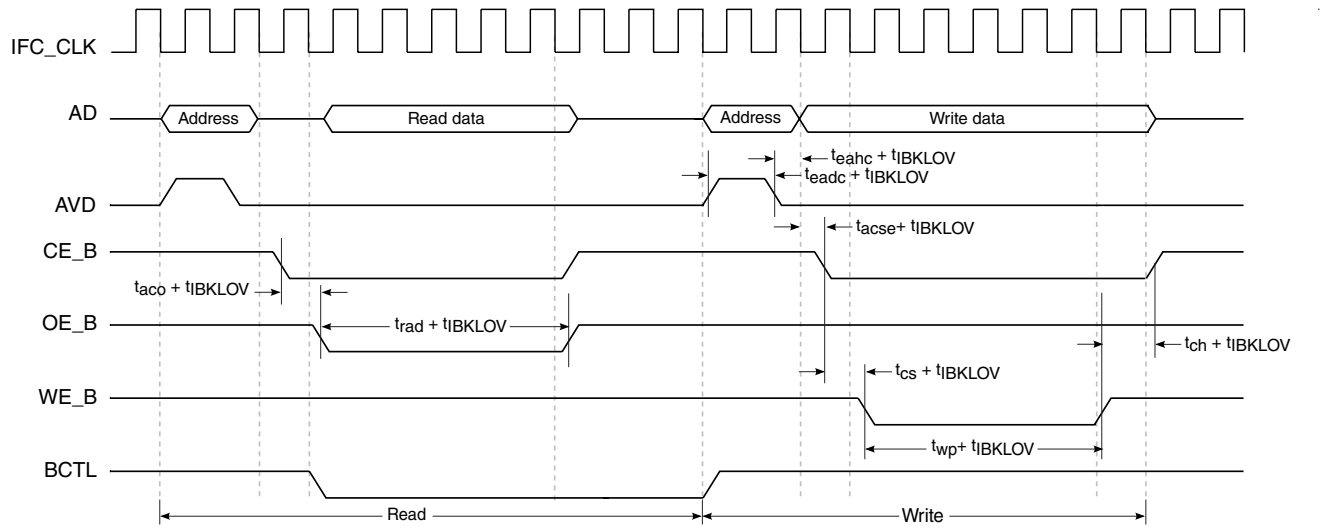


Figure 22. GPCM output timing diagram[1, 2]

Notes for figure:

1. t_{aco}, t_{rad},t_{eahc},t_{eadc}, t_{acse}, t_{cs}, t_{ch},t_{wp} are programmable. See the chip reference manual.

2. For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay.

3.14 Enhanced secure digital host controller (eSDHC)

This section describes the DC and AC electrical specifications for the eSDHC interface.

3.14.1 eSDHC DC electrical characteristics

This table provides the DC electrical characteristics for the eSDHC interface.

Table 52. eSDHC interface DC electrical characteristics (dual-voltage cards)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.7 x OV_{DD}	-	V	1
Input low voltage	V_{IL}	-	0.3 x OV_{DD}	V	1
I/O leakage current	I_{IN}/I_{OZ}	-50	50	µA	-
Output high voltage (I_{OH} = -100 µA at OV_{DD} min)	V_{OH}	OV_{DD} - 0.2 V	-	V	-
Output low voltage (I_{OL}= 100 µA at OV_{DD} min)	V_{OL}	-	0.2	V	-

Table continues on the next page...

Table 52. eSDHC interface DC electrical characteristics (dual-voltage cards)[3] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Output high voltage (I_{OH} = -100 µA)	V_{OH}	OV_{DD} - 0.2 V	-	V	2
Output low voltage (I_{OL} = 2 mA)	V_{OL}	-	0.3	V	2

1. The min V_{IL} and V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.

2. Open-drain mode is for MMC cards only.

3. For recommended operating conditions, see Table 3.

3.14.2 eSDHC AC timing specifications

This table provides the eSDHC AC timing specifications as defined in Figure 23.

Table 53. eSDHC AC timing specifications[6]

Parameter/Condition	Symbol[1]	Min	Max	Unit	Notes
SD_CLK clock frequency: SD/SDIO Full-speed/high-speed mode MMC Full-speed/high-speed mode	f_{SHSCK}	0	 25/50 20/52	MHz	2, 4
SD_CLK clock low time-Full-speed/High-speed mode	t_{SHSCKL}	10/7	-	ns	4
SD_CLK clock high time-Full-speed/High-speed mode	t_{SHSCKH}	10/7	-	ns	4
SD_CLK clock rise and fall times	t_{SHSCKR}/ t_{SHSCKF}	-	3	ns	4
Input setup times: SD_CMD, SD_DATx, SD_CD to SD_CLK	$t_{SHSIVKH}$	2.5	-	ns	3, 4, 5
Input hold times: SD_CMD, SD_DATx, SD_CD to SD_CLK	$t_{SHSIXKH}$	2.5	-	ns	4, 5
Output hold time: SD_CLK to SD_CMD, SD_DATx valid	$t_{SHSKHOX}$	-3	-	ns	4, 5
Output delay time: SD_CLK to SD_CMD, SD_DATx valid	$t_{SHSKHOV}$	-	3	ns	4, 5

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{FHSKHOV}$ symbolizes eSDHC high-speed mode device timing (SHS) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2. In full-speed mode, the clock frequency value can be 0-25 MHz for an SD/SDIO card and 0-20 MHz for an MMC card. In high-speed mode, the clock frequency value can be 0-50 MHz for an SD/SDIO card and 0-52 MHz for an MMC card.

3. To satisfy setup timing, one-way board-routing delay between Host and Card, on SD_CLK, SD_CMD, and SD_DATx should not exceed 1 ns for any high speed MMC card. For any high speed or default speed mode SD card, the one way board routing delay between Host and Card, on SD_CLK, SD_CMD, and SD_DATx should not exceed 1.5ns.

4. $C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 40$ pF.

5. The parameter values apply to both full-speed and high-speed modes.

6. For recommended operating conditions, see Table 3.

This figure provides the eSDHC clock input timing diagram.

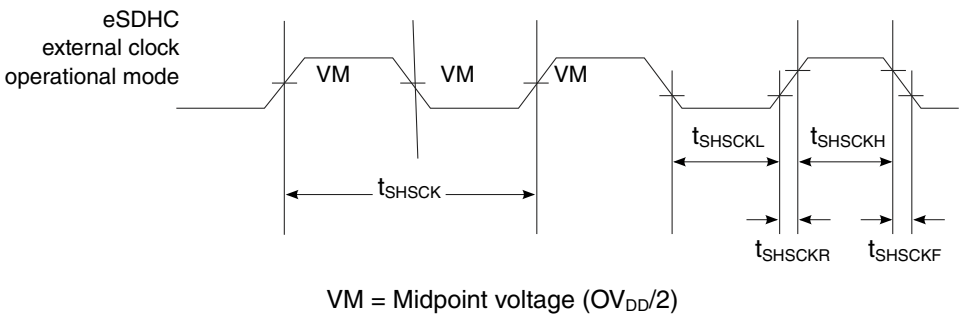


Figure 23. eSDHC clock input timing diagram

This figure provides the data and command input/output timing diagram.

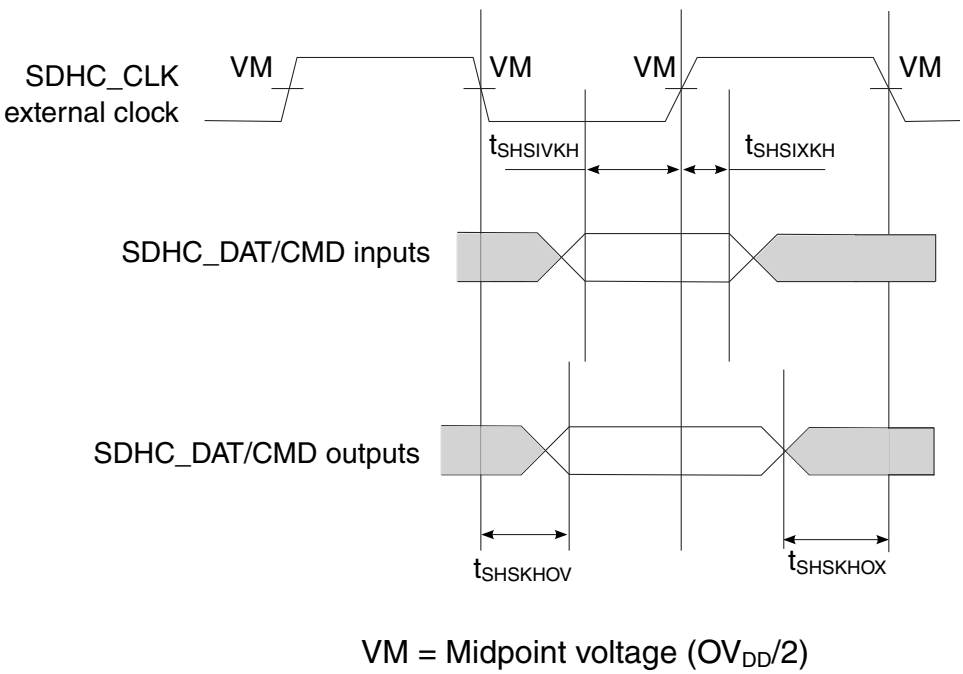


Figure 24. eSDHC data and command input/output timing diagram referenced to clock

3.15 Multicore programmable interrupt controller (MPIC)

This section describes the DC and AC electrical specifications for the multicore programmable interrupt controller.

3.15.1 MPIC DC specifications

This figure provides the DC electrical characteristics for the MPIC interface.

Table 54. MPIC DC electrical characteristics (OV_{DD} = 1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	-	V	1
Input low voltage	V_{IL}	-	0.6	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	-50	50	µA	2
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

Note:

1. The min $V_{IL}$and max V_{IH} values are based on the min and max OV_{IN} respective values found in Table 3.
2. The symbol OV_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.
3. For recommended operating conditions, see Table 3.

3.15.2 MPIC AC timing specifications

This table provides the MPIC input and output AC timing specifications.

Table 55. MPIC Input AC timing specifications[2]

Parameter/Condition	Symbol	Min	Max	Unit	Notes
MPIC inputs-minimum pulse width	t_{PIWID}	3	-	SYSCLKs	1

1. MPIC inputs and outputs are asynchronous to any visible clock. MPIC outputs must be synchronized before use by any external synchronous logic. MPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.
2. For recommended operating conditions, see Table 3.

3.16 JTAG controller

This section describes the DC and AC electrical specifications for the IEEE 1149.1 (JTAG) interface.

3.16.1 JTAG DC electrical characteristics

This table provides the JTAG DC electrical characteristics.

Table 56. JTAG DC electrical characteristics (OV_{DD} = 1.8V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	-	V	1
Input low voltage	V_{IL}	-	0.6	V	1

Table continues on the next page...

Table 56. JTAG DC electrical characteristics (OV_{DD} = 1.8V)[3] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	-100	50	µA	2, 4
Output high voltage (OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

Notes:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol found in Table 3.
3. For recommended operating conditions, see Table 3.
4. TMI, TMS, and TRST_B have internal pull-ups per the IEEE Std. 1149.1 specification.

3.16.2 JTAG AC timing specifications

This table provides the JTAG AC timing specifications as defined in Figure 25 through Figure 28.

Table 57. JTAG AC timing specifications[4]

Parameter/Condition		Symbol[1]	Min	Max	Unit	Notes
JTAG external clock frequency of operation		f_{JTG}	0	33.3	MHz	5
JTAG external clock cycle time		t_{JTG}	30	-	ns	6
JTAG external clock pulse width measured at 1.4 V		t_{JTKHKL}	15	-	ns	7
JTAG external clock rise and fall times		t_{JTGR}/t_{JTGF}	0	2	ns	8
TRST_B assert time		t_{TRST}	25	-	ns	2
Input setup times		t_{JTDVKH}	4.5	-	ns	9
Input hold times		t_{JTDXKH}	11	-	ns	10
Output valid times	Boundary-scan data	t_{JTKLDV}	-	15	ns	3, 11, 12
	TDO		-	10		
Output hold times		t_{JTKLDX}	0	-	ns	3

Notes:

1. The symbols used for timing specifications follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) reaching the invalid state (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

2.TRST_B is an asynchronous level sensitive signal. The setup time is for test purposes only.

3. All outputs are measured from the midpoint voltage of the falling edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load. Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

4. For recommended operating conditions, see Table 3.

Table 57. JTAG AC timing specifications[4]

Parameter/Condition	Symbol[1]	Min	Max	Unit	Notes
5. TCK frequency can be as high as 100MHz for internal debug modes.					
6. If TCK = 100 MHz then t_{JTG} = 10 nsec					
7. If TCK = 100 MHz then t_{JTKHKL} = 5 nsec					
8. If TCK = 100 MHz then t_{JTGR}/t_{JTGF}=<1 nsec					
9. If TCK = 100 MHz then t_{JTDVKH} = 1.33 nsec					
10. If TCK = 100 MHz then t_{JTDXKH} = 3.3 nsec					
11. Due to value of tJTKLDV, after Update-IR or Update-DR transitions for EXTEST* or CLAMP instructions, a transition through the optional Run-Test-Idle state is recommended to allow for board level propagation and setup times of observation points.					
12. DDR output pins when transitioning from a tristate to driving a logic 1 or 0 can require up to 24ns. Use of Run-Test Idle state is recommended after Update-IR or Update-DR TAP states.					

This figure provides the AC test load for TDO and the boundary-scan outputs of the device.

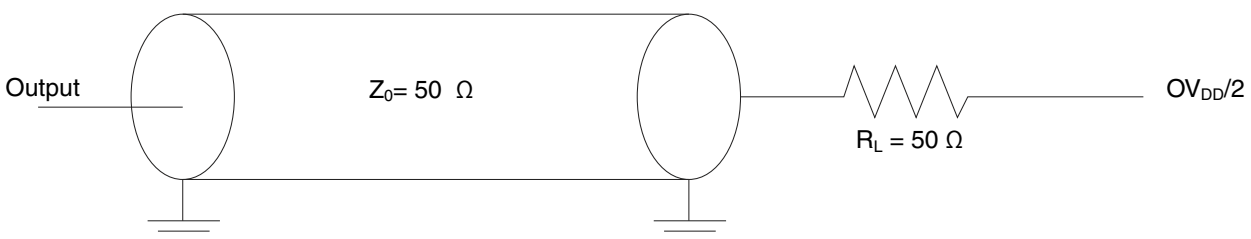


Figure 25. AC test load for the JTAG interface

This figure provides the JTAG clock input timing diagram.

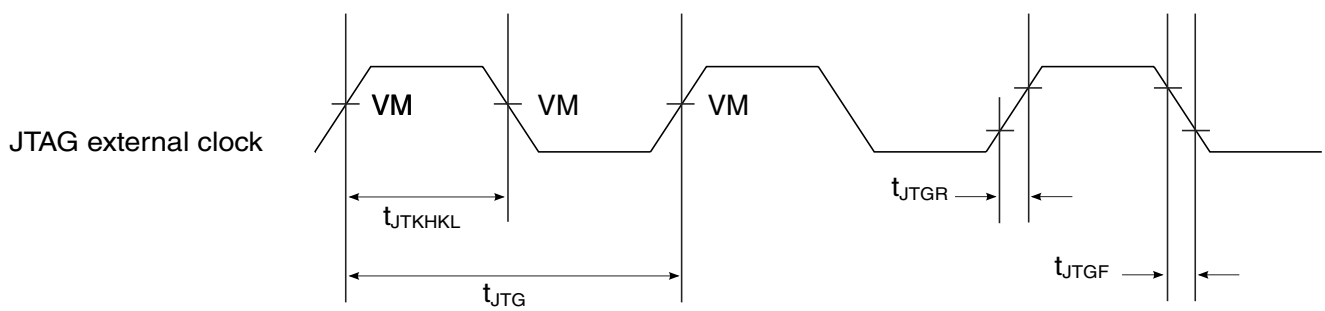


Figure 26. JTAG clock input timing diagram

This figure provides the TRST_B timing diagram.

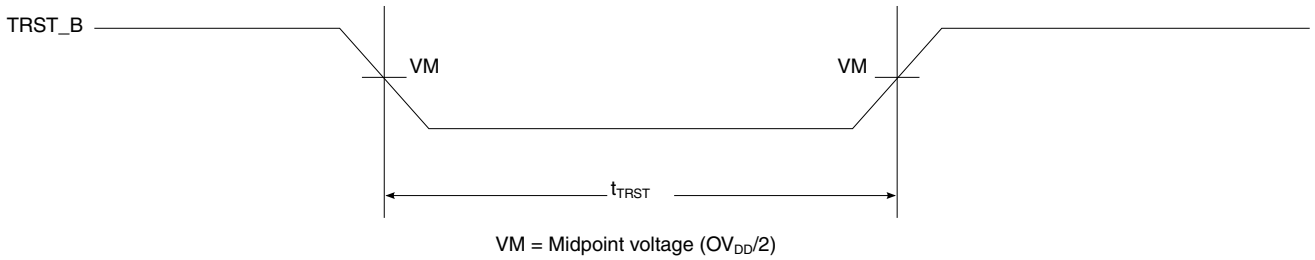


Figure 27. TRST_B timing diagram

This figure provides the boundary-scan timing diagram.

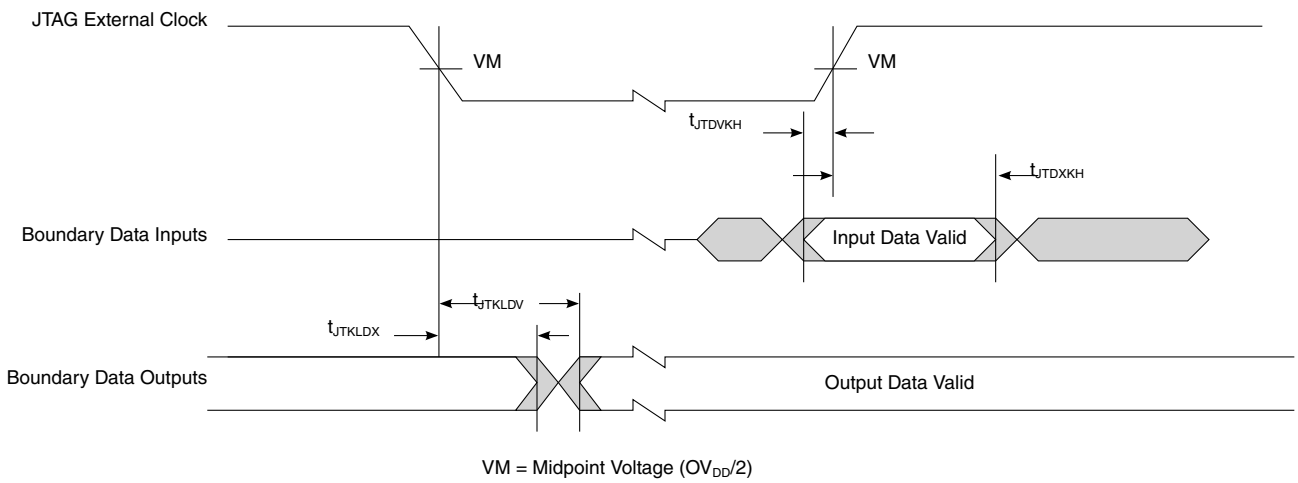


Figure 28. Boundary-scan timing diagram

3.17 I²C interface

This section describes the DC and AC electrical characteristics for the I²C interface.

3.17.1 I²C DC electrical characteristics

This table provides the DC electrical characteristics for the I²C interfaces operating at 2.5V.

Table 58. I²C DC electrical characteristics (DV_{DD} = 2.5V)[5]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.7	-	V	1

Table continues on the next page...

Table 58. I^2C DC electrical characteristics (DV_{DD} = 2.5V)[5] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Input low voltage	V_{IL}	-	0.7	V	1
Output low voltage (DV_{DD} = min, I_{OL} = 3 mA)	V_{OL}	0	0.4	V	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Leakage Input current at each I/O pin (input voltage is between 0.1 x DV_{DD} and 0.9 x DV_{DD}(max)	I_{OZ}	-50	50	µA	4
Capacitance for each I/O pin	C_I	-	10	pF	-

Notes:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 3.
2. See the chip reference manual for information about the digital filter used.
3. I/O pins obstruct the SDA and SCL lines if DV_{DD} is switched off.
4. For recommended operating conditions, see Table 3.

This table provides the DC electrical characteristics for the I^2C interfaces operating at 1.8V.

Table 59. I^2C DC electrical characteristics (DV_{DD} = 1.8V)[5]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	-	V	1
Input low voltage	V_{IL}	-	0.6	V	1
Output low voltage (DV_{DD} = min, I_{OL} = 3 mA)	V_{OL}	0	0.36	V	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Leakage Input current each I/O pin (input voltage is between 0.1 x DV_{DD} and 0.9 x DV_{DD}(max)	I_{OZ}	-50	50	µA	4
Capacitance for each I/O pin	C_I	-	10	pF	-

Notes:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max DV_{IN} values found in Table 3.
2. See the chip reference manual for information about the digital filter used.
3. I/O pins obstruct the SDA and SCL lines if DV_{DD} is switched off.
4. For recommended operating conditions, see Table 3.

3.17.2 I^2C AC timing specifications

This table provides the AC timing parameters for the I^2C interfaces.

Table 60. I²C AC timing specifications[5]

Parameter/Condition	Symbol[1]	Min	Max	Unit	Notes
SCL clock frequency	f_{I2C}	0	400	kHz	2
Low period of the SCL clock	t_{I2CL}	1.3	—	μs	—
High period of the SCL clock	t_{I2CH}	0.6	—	μs	—
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs	—
Data setup time	t_{I2DVKH}	100	—	ns	—
Data input hold time:	t_{I2DXKL}	—	—	μs	3
Data output delay time	t_{I2OVKL}	—	0.9	μs	4
Setup time for STOP condition	t_{I2PVKH}	0.6	—	μs	—
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs	—
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 x OV_{DD}	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 x OV_{DD}	—	V	—
Capacitive load for each bus line	Cb	—	400	pF	—

Notes:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time.

2. The requirements for I²C frequency calculation must be followed. See *Determining the I²C Frequency Divider Ratio for SCL* (AN2919).

3. As a transmitter, the chip provides a delay time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of a START or STOP condition. When the chip acts as the I²C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the chip does not generate an unintended START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If, under some rare condition, the 300 ns SDA output delay time is required for the chip as transmitter, see *Determining the I²C Frequency Divider Ratio for SCL* (AN2919).

4. The maximum t_{I2OVKL} has to be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.

5. For recommended operating conditions, see Table 3.

This figure provides the AC test load for the I²C.

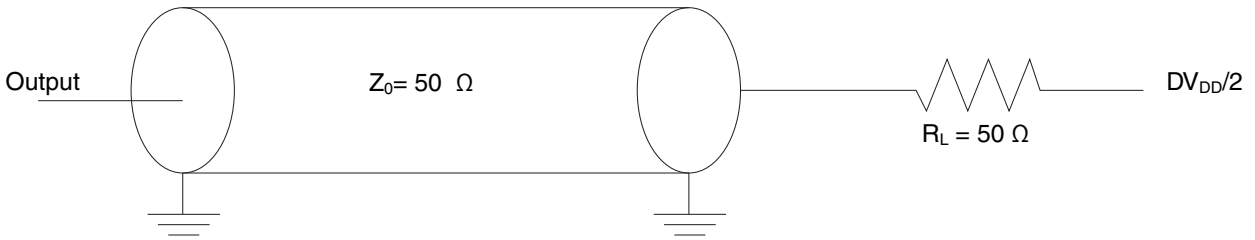


Figure 29. I²C AC test load

This figure shows the AC timing diagram for the I²C bus.

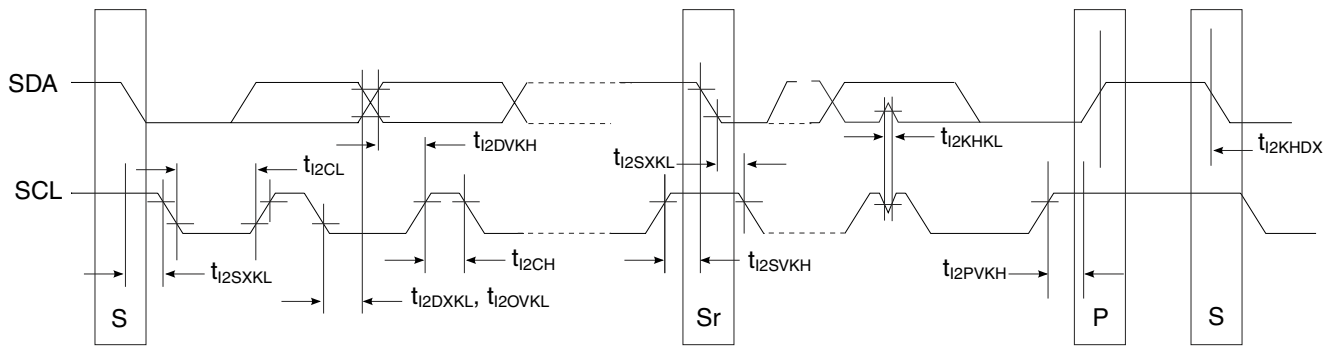


Figure 30. I²C Bus AC timing diagram

3.18 GPIO interface

This section describes the DC and AC electrical characteristics for the GPIO interface.

3.18.1 GPIO DC electrical characteristics

This table provides the DC electrical characteristics for GPIO pins operating at LV_{DD} = 2.5 V.

Table 61. GPIO DC electrical characteristics (2.5 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.7	-	V	1
Input low voltage	V_{IL}	-	0.7	V	1
Input current (V_{IN} = 0 V or V_{IN} = LV_{DD})	I_{IN}	-50	50	μA	2
Output high voltage (LV_{DD} = min, I_{OH} = -1 mA)	V_{OH}	2.0	-	V	-

Table continues on the next page...

Table 61. GPIO DC electrical characteristics (2.5 V)[3] (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Output low voltage (LV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	-	0.4	V	-

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3 .
2. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 3.

This table provides the DC electrical characteristics for GPIO pins operating at LV_{DD} or OV_{DD}= 1.8 V.

Table 62. GPIO DC electrical characteristics (1.8 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	-	V	1
Input low voltage	V_{IL}	-	0.6	V	1
Input current (V_{IN} = 0 V or V_{IN} = L/OV_{DD})	I_{IN}	-50	50	µA	2
Output high voltage (L/OV_{DD} = min, I_{OH} = -0.5 mA)	V_{OH}	1.35	-	V	-
Output low voltage (L/OV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	-	0.4	V	-

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max L/OV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the L/OV_{IN} symbol referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 3.

This table provides the DC electrical characteristics for the LP Trust pin, LP_TMP_DETECT_B, operating at V_{DD}LP = 1 V.

Table 63. LP_TMP_DETECT_B Pin DC electrical characteristics (1 V)[3]

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	0.8 x V_{DD_LP}	-	V	1
Input low voltage	V_{IL}	-	0.4 x V_{DD_LP}	V	1
Input current (V_{IN_LP} = 0 V or V_{IN_LP} = V_{DD_LP})	I_{IN}	-50	50	µA	2

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max V_{DD_LP} values found in Table 3.
2. The symbol V_{IN_LP}, in this case, represents the V_{IN_LP} symbol referenced in Recommended operating conditions.
3. For recommended operating conditions, see Table 3.

3.18.2 GPIO AC timing specifications

This table provides the GPIO input and output AC timing specifications.

Table 64. GPIO input AC timing specifications[2]

Parameter/Condition	Symbol	Min	Unit	Notes
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns	1

Notes:

1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} to ensure proper operation.
2. For recommended operating conditions, see Table 3.

This figure provides the AC test load for the GPIO.

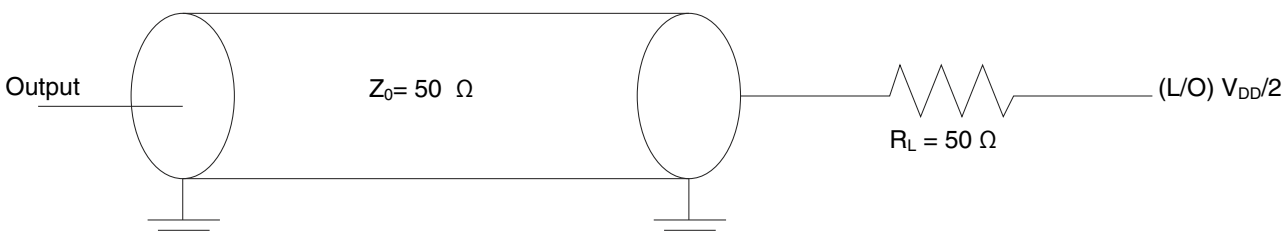


Figure 31. GPIO AC test load

3.19 High-speed serial interfaces (HSSI)

The chip features a serializer/deserializer (SerDes) interface to be used for high-speed serial interconnect applications. The SerDes interface can be used for PCI Express, SATA, Serial RapidIO, XAUI, XFI, 10GBase-KR, Aurora, Interlaken LA, HiGig/ HiGig2, SGMII, 2.5x SGMII and QSGMII data transfers.

This section describes the common portion of SerDes DC electrical specifications: the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter (Tx) and receiver (Rx) reference circuits are also shown.

3.19.1 Signal terms definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines the terms that are used in the description and specification of differential signals.

This figure shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. This figure shows the waveform for either a transmitter output (SD_TX*n* and SD_TX*n*_B) or a receiver input (SD_RX*n* and SD_RX*n*_B). Each signal swings between A volts and B volts where A > B.

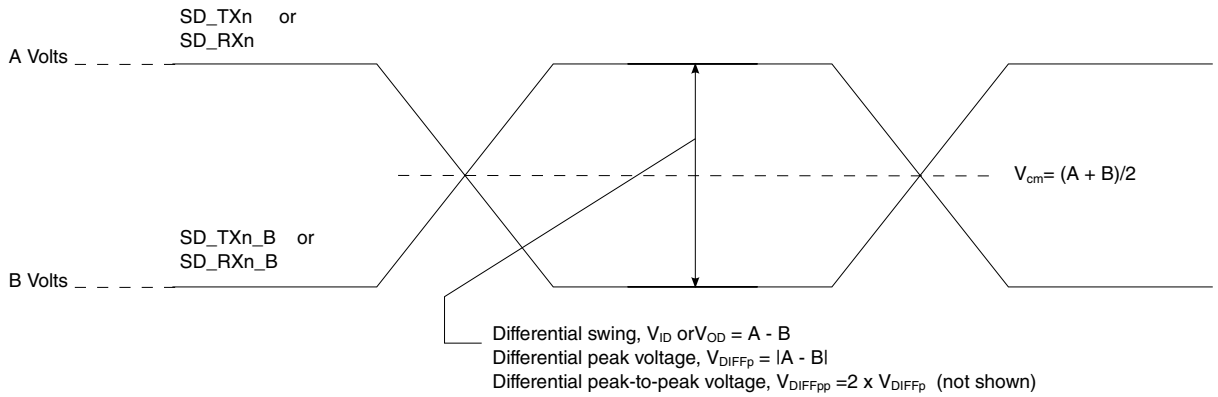


Figure 32. Differential voltage definitions for transmitter or receiver

Using this waveform, the definitions are as shown in the following list. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment:

Single-Ended Swing

The transmitter output signals and the receiver input signals SD_TX*n*, SD_TX*n*_B, SD_RX*n* and SD_RX*n*_B each have a peak-to-peak swing of A - B volts. This is also referred as each signal wire's single-ended swing.

Differential Output Voltage, V_{OD} (or Differential Output Swing)

The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complementary output voltages: V_{SD_TXn} - $V_{SD\_TXn\_B}$. The V_{OD} value can be either positive or negative.

Differential Input Voltage, V_{ID} (or Differential Input Swing)

The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complementary input voltages: V_{SD_RXn} - $V_{SD\_RXn\_B}$. The V_{ID} value can be either positive or negative.

Differential Peak Voltage, V_{DIFFp}

The peak value of the differential transmitter output signal or the differential receiver input signal is defined as the differential peak voltage, V_{DIFFp} = |A - B| volts.

Differential Peak-to-Peak, $V_{DIFFp-p}$

Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A - B to -(A - B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p}$ = 2 x V_{DIFFp} = 2 x |(A - B)| volts, which is twice the differential swing in amplitude, or twice of the differential peak. For

example, the output differential peak-to-peak voltage can also be calculated as $V_{TX\text{-}DIFFp\text{-}p} = 2 \times |V_{OD}|$.

Differential Waveform

The differential waveform is constructed by subtracting the inverting signal (SD_TX*n*_B, for example) from the non-inverting signal (SD_TX*n*, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. See Figure 37 as an example for differential waveform.

Common Mode Voltage, V_{cm}

The common mode voltage is equal to half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out} = (V_{SD\_TXn} + V_{SD\_TXn\_B}) \div 2 = (A + B) \div 2$, which is the arithmetic mean of the two complementary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. It may be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions.

To illustrate these definitions using real values, consider the example of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and outputs, TD and TD_B. If these outputs have a swing from 2.0 V to 2.5 V, the peak-to-peak voltage swing of each signal (TD or TD_B) is 500 mV p-p, which is referred to as the single-ended swing for each signal. Because the differential signaling environment is fully symmetrical in this example, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and -500 mV. In other words, V_{OD} is 500 mV in one phase and -500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp\text{-}p}$) is 1000 mV p-p.

3.19.2 SerDes reference clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD1_REF_CLK[1:2] and SD1_REF_CLK[1:2]_B for SerDes 1, SD2_REF_CLK[1:2] and SD2_REF_CLK[1:2]_B for SerDes 2, SD3_REF_CLK[1:2] and SD3_REF_CLK[1:2]_B for SerDes 3 and SD4_REF_CLK[1:2] and SD4_REF_CLK[1:2]_B for SerDes 4.

SerDes 1-4 may be used for various combinations of the following IP blocks based on the RCW Configuration field SRDS_PRTCLn:

- SerDes 1: SGMII (1.25 and 3.125 Gbaud), QSGMII (5 Gbps only), HiGig/HiGig2 (3.125 Gbps), HiGig/HiGig2 (3.75 Gbps) or XAUI (3.125 Gb/s)

- SerDes 2: SGMII (1.25 and 3.125 Gbaud), QSGMII (5 Gbps only), XAUI (3.125 Gb/s), HiGig/HiGig2 (3.125 Gbps), HiGig/HiGig2 (3.75 Gbps), XFI (10.3125 Gb/s only) or 10GBase-KR (10.3125 Gbaud only)
- SerDes 3: PEX1/2 (2.5, 5, and 8 GT/s), SRIO1(2.5, 3.125, and 5 Gbaud) or Interlaken-LA(6.25)
- SerDes 4: PEX4 (2.5, 5, and 8 GT/s),SRIO2(2.5, 3.125, and 5 Gbaud), Aurora (2.5, 3.125, and 5 Gbps) or SATA1/2 (1.5 and 3.0 Gbps)

The following sections describe the SerDes reference clock requirements and provide application information.

3.19.2.1 SerDes spread-spectrum clock source recommendations

SDn_REF_CLKn/SDn_REF_CLKn_B are designed to work with spread-spectrum clock for PCI Express protocol only with the spreading specification defined in Table 65. When using spread-spectrum clocking for PCI Express, both ends of the link partners should use the same reference clock. For best results, a source without significant unintended modulation must be used.

For SATA protocol, the SerDes transmitter does not support spread-spectrum clocking. The SerDes receiver does support spread-spectrum clocking on receive, which means the SerDes receiver can receive data correctly from a SATA serial link partner using spread-spectrum clocking

The spread-spectrum clocking cannot be used if the same SerDes reference clock is shared with other non-spread-spectrum supported protocols. For example, if the spread-spectrum clocking is desired on a SerDes reference clock for PCI Express and the same reference clock is used for any other protocol such as SATA/SGMII/QSGMII/SRIO/ XAUI due to the SerDes lane usage mapping option, spread-spectrum clocking cannot be used at all.

Table 65. SerDes spread-spectrum clock source recommendations [1]

Parameter	Min	Max	Unit	Notes
Frequency modulation	30	33	kHz	-
Frequency spread	+0	-0.5	%	2
1. At recommended operating conditions. See Table 3. 2. Only down-spreading is allowed.				

3.19.2.2 SerDes reference clock receiver characteristics

This figure shows a receiver reference diagram of the SerDes reference clocks.

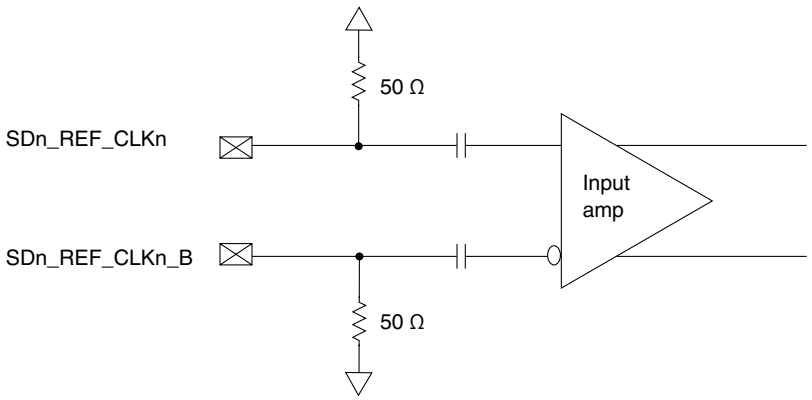


Figure 33. Receiver of SerDes reference clocks

The characteristics of the clock signals are as follows:

- The SerDes transceivers core power supply voltage requirements ($SV_{DD}n$) are as specified in Recommended operating conditions.
- The SerDes reference clock receiver reference circuit structure is as follows:
  - The SD*n*_REF_CLK*n* and SD*n*_REF_CLK*n*_B are internally AC-coupled differential inputs as shown in Figure 33. Each differential clock input (SD*n*_REF_CLK*n* or SD*n*_REF_CLK*n*_B) has on-chip 50 Ω termination to SGND*n* followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. See the differential mode and single-ended mode descriptions below for detailed requirements.
- The maximum average current requirement also determines the common mode voltage range.
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA because the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V ÷ 50 Ω = 8 mA) while the minimum common mode input level is 0.1 V above SGND*n*. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0-0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  - If the device driving the SD*n*_REF_CLK*n* and SD*n*_REF_CLK*n*_B inputs cannot drive 50 Ω to SGND*n* DC or the drive strength of the clock driver chip exceeds the maximum input current limitations, it must be AC-coupled off-chip.
- The input amplitude requirement is described in detail in the following sections.

3.19.2.3 DC-level requirement for SerDes reference clocks

The DC level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs, as described below:

- Differential Mode
  - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-to-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing of less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - For an external DC-coupled connection, as described in SerDes reference clock receiver characteristics, the maximum average current requirements sets the requirement for average voltage (common mode voltage) as between 100 mV and 400 mV. Figure 34 shows the SerDes reference clock input requirement for DC-coupled connection scheme.

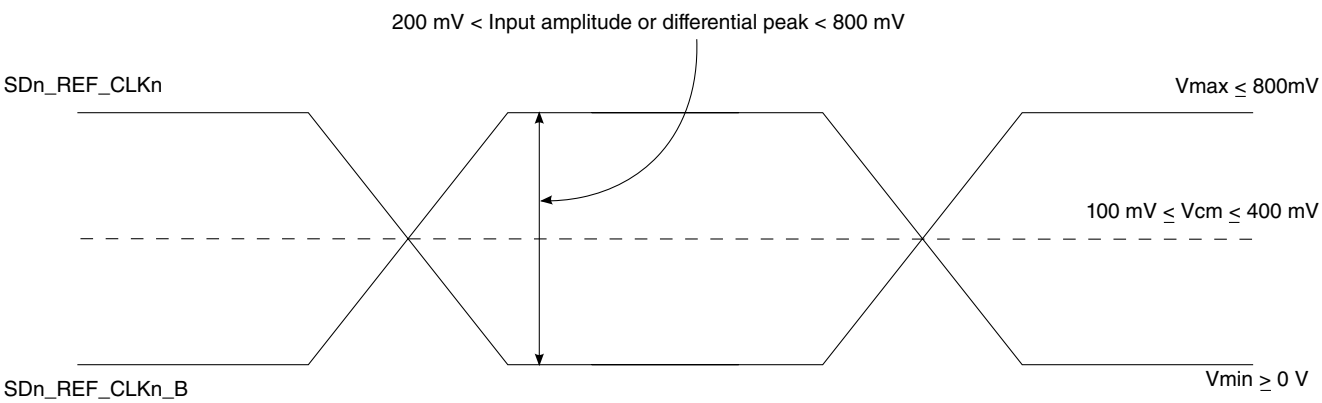


Figure 34. Differential reference clock input DC requirements (external DC-coupled)

  - For an external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different common mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND*n*. Each signal wire of the differential inputs is allowed to swing below and above the common mode voltage (SGND*n*). Figure 35 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

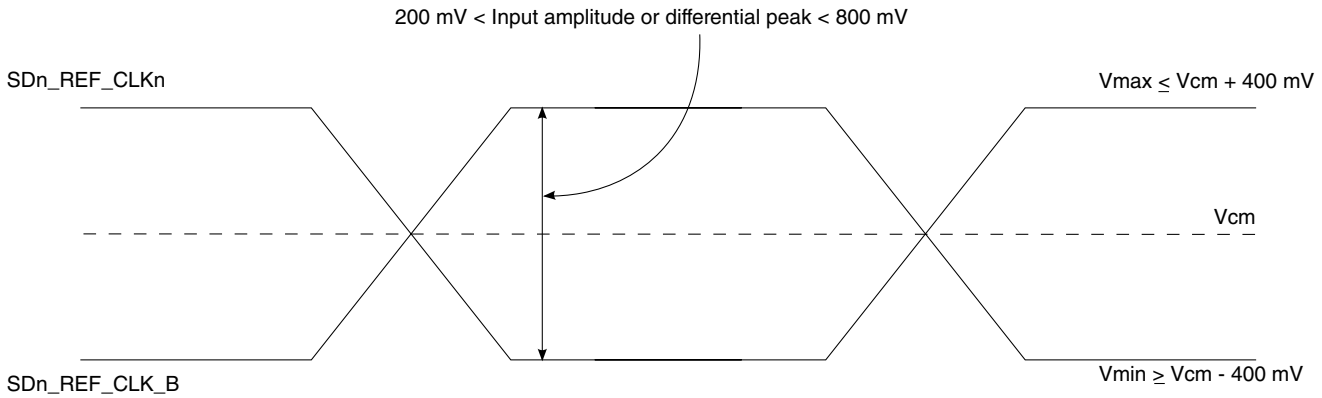


Figure 35. Differential reference clock input DC requirements (external AC-coupled)

- Single-Ended Mode
  - The reference clock can also be single-ended. The SD*n*_REF_CLK*n* input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-to-peak (from V_{MIN} to V_{MAX}) with SD*n*_REF_CLK*n*_B either left unconnected or tied to ground.
  - The SD*n*_REF_CLK*n* input average voltage must be between 200 and 400 mV. Figure 36 shows the SerDes reference clock input requirement for single-ended signaling mode.
  - To meet the input amplitude requirement, the reference clock inputs may need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase (SD*n*_REF_CLK*n*_B) through the same source impedance as the clock input (SD*n*_REF_CLK*n*) in use.

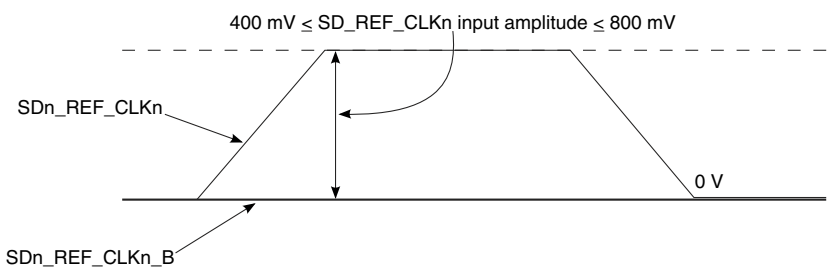


Figure 36. Single-ended reference clock input DC requirements

3.19.2.4 AC requirements for SerDes reference clocks

This table lists the AC requirements for SerDes reference clocks for protocols running at data rates up to 8 Gb/s.

This includes PCI Express (2.5, 5, 8 GT/s), SGMII (1.25 Gbaud), 2.5x SGMII (3.125 Gbaud), QSGMII (5 Gbps), Serial RapidIO (2.5, 3.125, 5 Gbaud), Aurora (2.5, 3.125, 5 Gbps), HiGig/HiGig2 (3.125 Gbps), HiGig/HiGig2 (3.75 Gbps), XAUI (3.125 Gb/s) and Interlaken-LA (6.25 Gbps) SerDes reference clocks to be guaranteed by the customer's application design.

Table 66. SD*n*_REF_CLK*n* and SD*n*_REF_CLK*n*_B input clock requirements (S*n*V_{DD} = 1.0 V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SDn_REF_CLKn/ SDn_REF_CLKn_B frequency range	t_{CLK_REF}	-	100/125/156.25	-	MHz	2
SDn_REF_CLKn/ SDn_REF_CLKn_B clock frequency tolerance	t_{CLK_TOL}	-300	-	300	ppm	3, 12
SDn_REF_CLKn/ SDn_REF_CLKn_B clock frequency tolerance	t_{CLK_TOL}	-100	-	100	ppm	4, 12
SDn_REF_CLKn/ SDn_REF_CLKn_B reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	5
SDn_REF_CLKn/ SDn_REF_CLKn_B max deterministic peak-to-peak jitter at 10^{-6} BER	t_{CLK_DJ}	-	-	42	ps	-
SDn_REF_CLKn/ SDn_REF_CLKn_B total reference clock jitter at 10^{-6} BER (peak-to-peak jitter at refClk input)	t_{CLK_TJ}	-	-	86	ps	6
SDn_REF_CLKn/ SDn_REF_CLKn_B 10 kHz to 1.5 MHz RMS jitter	$t_{REFCLK\text{-}LF\text{-}RMS}$	-	-	3	ps RMS	7
SDn_REF_CLKn/ SDn_REF_CLKn_B > 1.5 MHz to Nyquist RMS jitter	$t_{REFCLK\text{-}HF\text{-}RMS}$	-	-	3.1	ps RMS	7
SDn_REF_CLKn/ SDn_REF_CLKn_B RMS reference clock jitter	$t_{REFCLK\text{-}RMS\text{-}DC}$	-	-	1	ps RMS	8
SDn_REF_CLKn/ SDn_REF_CLKn_B rising/falling edge rate	t_{CLKRR}/t_{CLKFR}	1	-	4	V/ns	9
Differential input high voltage	-	V_{CM} +200 mV	-	-	mV	5
Differential input low voltage	-	-	-	V_{CM}-200 mV	mV	5
Rising edge rate (SDn_REF_CLKn) to falling edge rate (SDn_REF_CLKn) matching	Rise-Fall Matching	-	-	20	%	10, 11

1. For recommended operating conditions, see Table 3.
2. **Caution:** Only 100, 125 and 156.25 have been tested.In-between values do not work correctly with the rest of the system.
3. For PCI Express (2.5, 5, 8 GT/s)
4. For SGMII, 2.5x SGMII, QSGMII, sRIO, HiGig/HiGig2, XAUI, Interlaken-LA, Aurora
5. Measurement taken from differential waveform. VCM is the common mode voltage.
6. Limits from PCI Express CEM Rev 2.0
7. For PCI Express-5 GT/s, per PCI Express base specification rev 3.0
8. For PCI-Express-8 GT/s, per PCI-Express base specification rev 3.0

Table 66. SD*n*_REF_CLK*n* and SD*n*_REF_CLK*n*_B input clock requirements (SnV_{DD} = 1.0 V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
9. Measured from -200 mV to +200 mV on the differential waveform (derived from SD*n*_REF_CLK*n* minus SD*n*_REF_CLK*n*_B). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 37. 10. Measurement taken from single-ended waveform 11. Matching applies to rising edge for SD*n*_REF_CLK*n* and falling edge rate for SD*n*_REF_CLK*n*_B. It is measured using a 200 mV window centered on the median cross point where SD*n*_REF_CLK*n* rising meets SD*n*_REF_CLK*n*_B falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SD*n*_REF_CLK*n* must be compared to the fall edge rate of SD*n*_REF_CLK*n*_B, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 38. 12. When 2 or more protocols share the same PLL on a SerDes module, the tightest SDn_REF_CLKn/ SDn_REF_CLKn_B clock frequency tolerance must be followed.						

This table lists the AC requirements for SerDes reference clocks for protocols running at data rates greater than 8 Gb/s.

This includes XFI (10.3125 Gb/s) and 10GBase-KR (10.3125 GBd) SerDes reference clocks to be guaranteed by the customer's application design.

Table 67. SD*n*_REF_CLK*n* and SD*n*_REF_CLK*n*_B input clock requirements ($SV_{DD}n$ = 1.0 V) [1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SDn_REF_CLKn/ SDn_REF_CLKn_B frequency range	t_{CLK_REF}	-	156.25/ 161.1328135	-	MHz	2
SDn_REF_CLKn/ SDn_REF_CLKn_B clock frequency tolerance	t_{CLK_TOL}	-100	-	100	ppm	5
SDn_REF_CLKn/ SDn_REF_CLKn_B reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	3
SDn_REF_CLKn/ SDn_REF_CLKn_B single side band noise	@1 kHz	-	-	-85	dBC/Hz	4
SDn_REF_CLKn/ SDn_REF_CLKn_B single side band noise	@10 kHz	-	-	-108	dBC/Hz	4
SDn_REF_CLKn/ SDn_REF_CLKn_B single side band noise	@100 kHz	-	-	-128	dBC/Hz	4
SDn_REF_CLKn/ SDn_REF_CLKn_B single side band noise	@1 MHz	-	-	-138	dBC/Hz	4
SDn_REF_CLKn/ SDn_REF_CLKn_B single side band noise	@10 MHz	-	-	-138	dBC/Hz	4
SDn_REF_CLKn/ SDn_REF_CLKn_B random jitter (1.2 MHz to 15 MHz)	t_{CLK_RJ}	-	-	0.8	ps	-
SDn_REF_CLKn/ SDn_REF_CLKn_B total reference clock jitter at 10^{-12} BER (1.2 MHz to 15 MHz)	t_{CLK_TJ}	-	-	11	ps	-
SDn_REF_CLKn/ SDn_REF_CLKn_B spurious noise (1.2 MHz to 15 MHz)	-	-	-	-75	dBC	-

Table continues on the next page...

Table 67. SD*n*_REF_CLK*n* and SD*n*_REF_CLK*n*_B input clock requirements ($SV_{DD}n$ = 1.0 V) [1] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential input high voltage	-	V_{CM} +200 mV	-	-	mV	6
Differential input low voltage	-	-	-	V_{CM}-200 mV	mV	6
Rising edge rate (SDn_REF_CLKn) to falling edge rate (SDn_REF_CLKn) matching	Rise-Fall Matching	-	-	20	%	7, 8

1. For recommended operating conditions, see Table 3.

2. **Caution:** Only 156.25 and 161.1328135 have been tested. In-between values do not work correctly with the rest of the system.

3. Measurement taken from differential waveform.

4. Per XFP Spec. Rev 4.5, the Module Jitter Generation spec at XFI Optical Output is 10mUI (RMS) and 100 mUI (p-p). In the CDR mode the host is contributing 7 mUI (RMS) and 50 mUI (p-p) jitter.

5. When 2 or more protocols share the same PLL on a SerDes module, the tightest SDn_REF_CLKn/ SDn_REF_CLKn_B clock frequency tolerance must be followed.

6. Measurement taken from differential waveform. VCM is the common mode voltage.

7. Measurement taken from single-ended waveform .

8. Matching applies to rising edge for SD*n*_REF_CLK*n* and falling edge rate for SD*n*_REF_CLK*n*_B. It is measured using a 200 mV window centered on the median cross point where SD*n*_REF_CLK*n* rising meets SD*n*_REF_CLK*n*_B falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SD*n*_REF_CLK*n* must be compared to the fall edge rate of SD*n*_REF_CLK*n*_B, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 38.

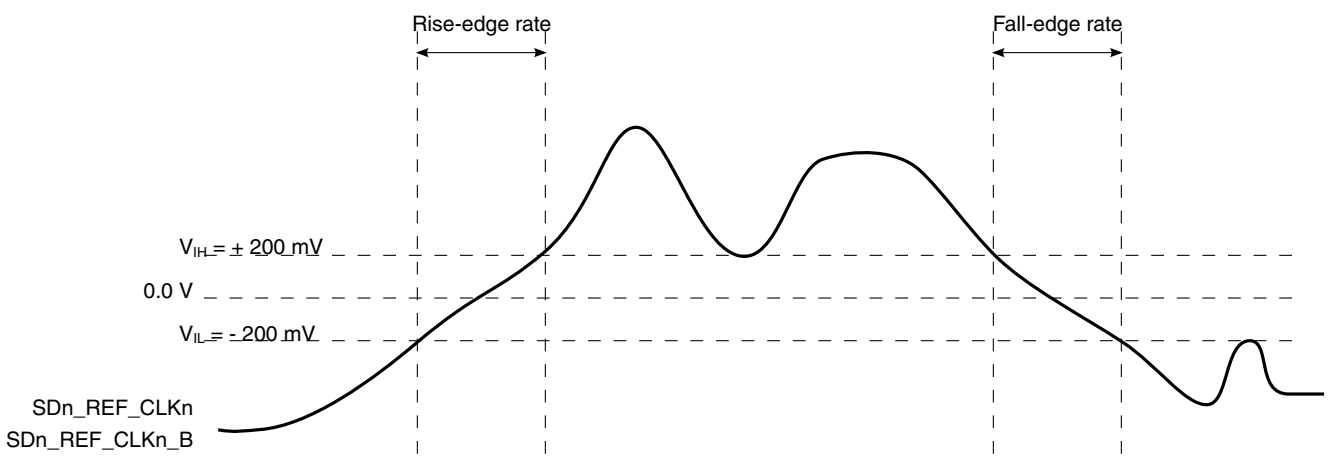


Figure 37. Differential measurement points for rise and fall time

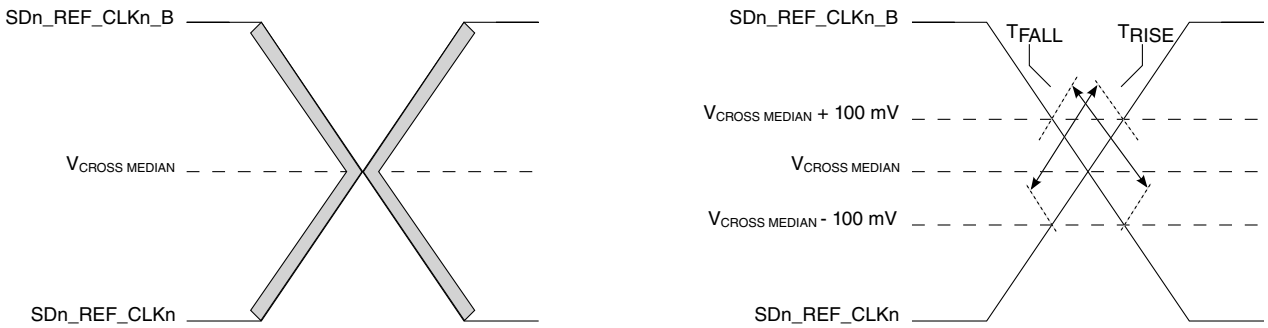


Figure 38. Single-ended measurement points for rise and fall time matching

3.19.3 SerDes transmitter and receiver reference circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

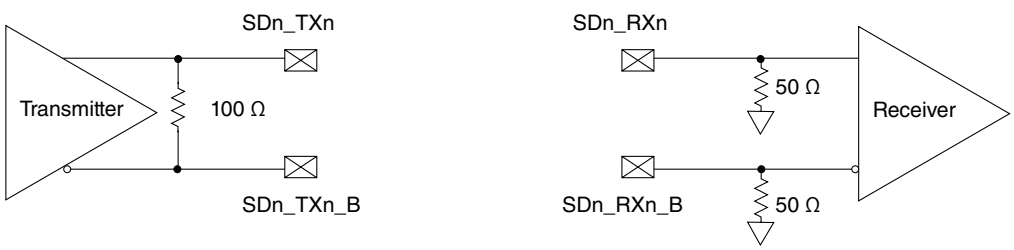


Figure 39. SerDes transmitter and receiver reference circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below based on the application usage:

- PCI Express
- Serial RapidIO (sRIO)
- XAUI interface
- Aurora interface
- Serial ATA (SATA) interface
- SGMII interface
- QSGMII interface
- HiGig/HiGig2 interface
- XFI interface
- Interlaken interface

Note that external AC-coupling capacitor is required for the above serial transmission protocols with the capacitor value defined in the specification of each protocol section.

3.19.4 PCI Express

This section describes the clocking dependencies, DC and AC electrical specifications for the PCI Express bus.

3.19.4.1 Clocking dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

3.19.4.2 PCI Express clocking requirements for SD*n*_REF_CLK*n* and SD*n*_REF_CLK*n*_B

SerDes 3-4 (SD[3:4]_REF_CLK[1:2] and SD[3:4]_REF_CLK[1:2]_B) may be used for various SerDes PCI Express configurations based on the RCW Configuration field SRDS_PRTCL. PCI Express is not supported on SerDes 1 and 2.

NOTE

PCI Express operating in x8 mode is only supported at 2.5 and 5.0 GT/s.

For more information on these specifications, see SerDes reference clocks.

3.19.4.3 PCI Express DC physical layer specifications

This section contains the DC specifications for the physical layer of PCI Express on this chip.

3.19.4.3.1 PCI Express DC physical layer transmitter specifications

This section discusses the PCI Express DC physical layer transmitter specifications for 2.5 GT/s, 5 GT/s and 8 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 68. PCI Express 2.0 (2.5 GT/s) differential transmitter output DC specifications (XV_{DD} = 1.35 V or 1.5 V)[1]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential peak-to-peak output voltage	$V_{TX\text{-}DIFFp\text{-}p}$	800	1000	1200	mV	$V_{TX\text{-}DIFFp\text{-}p}$ = 2 x $\lvert V_{TX\text{-}D+} - V_{TX\text{-}D-} \rvert$

Table continues on the next page...

Table 68. PCI Express 2.0 (2.5 GT/s) differential transmitter output DC specifications (XV_{DD} = 1.35 V or 1.5 V)[1] (continued)

Parameter	Symbol	Min	Typical	Max	Units	Notes
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.
DC differential transmitter impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Transmitter DC differential mode low Impedance
Transmitter DC impedance	Z_{TX-DC}	40	50	60	Ω	Required transmitter D+ as well as D- DC Impedance during all states

Notes:

1. For recommended operating conditions, see Table 3.

This table defines the PCI Express 2.0 (5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 69. PCI Express 2.0 (5 GT/s) differential transmitter output DC specifications (XV_{DD} = 1.35 V or 1.5 V)[1]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential peak-to-peak output voltage	$V_{TX-DIFFp-p}$	800	1000	1200	mV	$V_{TX-DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$
Low power differential peak-to-peak output voltage	$V_{TX-DIFFp-p\_low}$	400	500	1200	mV	$V_{TX-DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition.
DC differential transmitter impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Transmitter DC differential mode low impedance
Transmitter DC Impedance	Z_{TX-DC}	40	50	60	Ω	Required transmitter D+ as well as D- DC impedance during all states

Notes:

1. For recommended operating conditions, see Table 3.

This table defines the PCI Express 3.0 (8 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 70. PCI Express 3.0 (8 GT/s) differential transmitter output DC specifications (XV_{DD} = 1.35 V or 1.5 V)[3]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Full swing transmitter voltage with no TX Eq	$V_{TX-FS-NO-EQ}$	800	-	1300	mVp-p	See Note 1.
Reduced swing transmitter voltage with no TX Eq	$V_{TX-RS-NO-EQ}$	400	-	1300	mV	See Note 1.
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3.0	3.5	4.0	dB	-
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	-
Minimum swing during EIEOS for full swing	$V_{TX-EIEOS-FS}$	250	-	-	mVp-p	See Note 2
Minimum swing during EIEOS for reduced swing	$V_{TX-EIEOS-RS}$	232	-	-	mVp-p	See Note 2
DC differential transmitter impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Transmitter DC differential mode low impedance
Transmitter DC Impedance	Z_{TX-DC}	40	50	60	Ω	Required transmitter D+ as well as D- DC impedance during all states

Notes:

1. Voltage measurements for $V_{TX-FS-NO-EQ}$ and $V_{TX-RS-NO-EQ}$ are made using the 64-zeroes/64-ones pattern in the compliance pattern.

2. Voltage limits comprehend both full swing and reduced swing modes. The transmitter must reject any changes that would violate this specification. The maximum level is covered in the $V_{TX-FS-NO-EQ}$ measurement which represents the maximum peak voltage the transmitter can drive. The $V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ voltage limits are imposed to guarantee the EIEOS threshold of 175 mV_{P-P} at the receiver pin. This parameter is measured using the actual EIEOS pattern that is part of the compliance pattern and then removing the ISI contribution of the breakout channel.

3. For recommended operating conditions, see Table 3.

3.19.4.4 PCI Express DC physical layer receiver specifications

This section discusses the PCI Express DC physical layer receiver specifications for 2.5 GT/s, 5 GT/s and 8 GT/s.

This table defines the DC specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 71. PCI Express 2.0 (2.5 GT/s) differential receiver input DC specifications (SV_{DD} = 1.0 V)[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	120	1000	1200	mV	$V_{RX-DIFFp-p}$ = 2 x $\lvert V_{RX-D+} - V_{RX-D-} \rvert$ See Note 1.

Table continues on the next page...

Table 71. PCI Express 2.0 (2.5 GT/s) differential receiver input DC specifications (SV_{DD} = 1.0 V)[4] (continued)

Parameter	Symbol	Min	Typ	Max	Units	Notes
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	Receiver DC differential mode impedance. See Note 2
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required receiver D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	-	-	kΩ	Required receiver D+ as well as D- DC Impedance when the receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	-	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ Measured at the package pins of the receiver

Notes:

1. Measured at the package pins with a test load of 50Ω to GND on each pin.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground.
4. For recommended operating conditions, see Table 3.

This table defines the DC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 72. PCI Express 2.0 (5 GT/s) differential receiver input DC specifications (SV_{DD} = 1.0 V)[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	120	1000	1200	mV	$V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ See Note 1.
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	Receiver DC differential mode impedance. See Note 2
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required receiver D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	-	-	kΩ	Required receiver D+ as well as D- DC Impedance when the receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	-	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ Measured at the package pins of the receiver

Table continues on the next page...

Table 72. PCI Express 2.0 (5 GT/s) differential receiver input DC specifications (SV_{DD} = 1.0 V)[4] (continued)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Notes: 1. Measured at the package pins with a test load of 50 Ω to GND on each pin. 2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port. 3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground. 4. For recommended operating conditions, see Table 3.						

This table defines the DC specifications for the PCI Express 3.0 (8 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 73. PCI Express 3.0 (8 GT/s) differential receiver input DC specifications (SV_{DD} = 1.0 V)[6]

Parameter	Symbol	Min	Typ	Max	Units	Notes
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	Receiver DC differential mode impedance. See Note 2
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required receiver D+ as well as D- DC Impedance (50 ± 20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	-	-	kΩ	Required receiver D+ as well as D- DC Impedance when the receiver terminations do not have power. See Note 3.
Generator launch voltage	$V_{RX-LAUNCH-8G}$	-	800	-	mV	Measured at TP1 per PCI Express base spec. rev 3.0
Eye height (-20dB Channel)	$V_{RX-SV-8G}$	25	-	-	mV	Measured at TP2P per PCI Express base spec. rev 3.0. See Notes 4, 5
Eye height (-12dB Channel)	$V_{RX-SV-8G}$	50	-	-	mV	Measured at TP2P per PCI Express base spec. rev 3.0. See Notes 4, 5
Eye height (-3dB Channel)	$V_{RX-SV-8G}$	200	-	-	mV	Measured at TP2P per PCI Express base spec. rev 3.0. See Notes 4, 5
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	-	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ Measured at the package pins of the receiver
Notes: 1. Measured at the package pins with a test load of 50Ω to GND on each pin. 2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port. 3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground.						

Table 73. PCI Express 3.0 (8 GT/s) differential receiver input DC specifications (SV_{DD} = 1.0 V)[6]

Parameter	Symbol	Min	Typ	Max	Units	Notes
4. $V_{RX-SV-8G}$ is tested at three different voltages to ensure the receiver device under test is capable of equalizing over a range of channel loss profiles. The "SV" in the parameter names refers to stressed voltage.						
5. $V_{RX-SV-8G}$ is referenced to TP2P and is obtained after post processing data captured at TP2.						
6. For recommended operating conditions, see Table 3.						

3.19.4.5 PCI Express AC physical layer specifications

This section contains the AC specifications for the physical layer of PCI Express on this device.

3.19.4.5.1 PCI Express AC physical layer transmitter specifications

This section discusses the PCI Express AC physical layer transmitter specifications for 2.5 GT/s, 5 GT/s and 8 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 74. PCI Express 2.0 (2.5 GT/s) differential transmitter output AC specifications[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit interval	UI	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Minimum transmitter eye width	T_{TX-EYE}	0.75	-	-	UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER}$ = 1 - T_{TX-EYE} = 0.25 UI. Does not include spread-spectrum or RefCLK jitter. Includes device random jitter at 10^{-12}. See Notes 1 and 2.
Maximum time between the jitter median and maximum deviation from the median	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	-	-	0.125	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p}$ = 0 V) in relation to a recovered transmitter UI. A recovered transmitter UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the transmitter UI. See Notes 1 and 2.
AC coupling capacitor	C_{TX}	75	-	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 3.

Table continues on the next page...

Table 74. PCI Express 2.0 (2.5 GT/s) differential transmitter output AC specifications[4] (continued)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Notes: 1. Specified at the measurement point into a timing and voltage test load as shown in Figure 41 and measured over any 250 consecutive transmitter UIs. 2. A T_{TX-EYE} = 0.75 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.25 UI for the transmitter collected over any 250 consecutive transmitter UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total transmitter jitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. 3. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required. 4. For recommended operating conditions, see Table 3.						

This table defines the PCI Express 2.0 (5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 75. PCI Express 2.0 (5 GT/s) differential transmitter output AC specifications[3]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	199.94	200.00	200.06	ps	Each UI is 200 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Minimum transmitter eye width	T_{TX-EYE}	0.75	-	-	UI	The maximum transmitter jitter can be derived as: $T_{TX-MAX-JITTER}$ = 1 - T_{TX-EYE} = 0.25 UI. See Note 1.
Transmitter RMS deterministic jitter > 1.5 MHz	$T_{TX-HF-DJ-DD}$	-	-	0.15	ps	-
AC coupling capacitor	C_{TX}	75	-	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 2.
Notes: 1. Specified at the measurement point into a timing and voltage test load as shown in Figure 41 and measured over any 250 consecutive transmitter UIs. 2. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required. 3. For recommended operating conditions, see Table 3.						

This table defines the PCI Express 3.0 (8 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 76. PCI Express 3.0 (8 GT/s) differential transmitter output AC specifications[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	124.9625	125.00	125.0375	ps	Each UI is 125 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Transmitter uncorrelated total jitter	T_{TX-UTJ}	-	-	31.25	ps p-p	-
Transmitter uncorrelated deterministic jitter	$T_{TX-UDJ-DD}$	-	-	12	ps p-p	-
Total uncorrelated pulse width jitter (PWJ)	$T_{TX-UPW-TJ}$	-	-	24	ps p-p	See Note 1, 2
Deterministic data dependent jitter (DjDD) uncorrelated pulse width jitter (PWJ)	$T_{TX-UPW-DJDD}$	-	-	10	ps p-p	See Note 1, 2
Data dependent jitter	T_{TX-DDJ}	-	-	18	ps p-p	See Note 2
AC coupling capacitor	C_{TX}	176	-	265	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 3.

Notes:

1. PWJ parameters shall be measured after data dependent jitter (DDJ) separation.
2. Measured with optimized preset value after de-embedding to transmitter pin.
3. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.
4. For recommended operating conditions, see Table 3.

3.19.4.5.2 PCI Express AC physical layer receiver specifications

This section discusses the PCI Express AC physical layer receiver specifications for 2.5 GT/s, 5 GT/s and 8 GT/s.

This table defines the AC specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 77. PCI Express 2.0 (2.5 GT/s) differential receiver input AC specifications[4]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	399.88	400.00	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
Minimum receiver eye width	T_{RX-EYE}	0.4	-	-	UI	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER}$ = 1 - T_{RX-EYE}= 0.6 UI. See Notes 1 and 2.

Table continues on the next page...

Table 77. PCI Express 2.0 (2.5 GT/s) differential receiver input AC specifications[4] (continued)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Maximum time between the jitter median and maximum deviation from the median.	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	-	-	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered transmitter UI. A recovered transmitter UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the transmitter UI. See this table notes.

Notes:

1. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 41 must be used as the receiver device when taking measurements. If the clocks to the receiver and transmitter are not derived from the same reference clock, the transmitter UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
2. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive transmitter UIs. It must be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the receiver and transmitter are not derived from the same reference clock, the transmitter UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
3. It is recommended that the recovered transmitter UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.
4. For recommended operating conditions, see Table 3.
5. The TRX-EYE-MEDIAN-to-MAX-JITTER for common and separated reference clock architecture.
6. If spread spectrum clocking is desired, common clock receiver architecture must be used.
7. The AC specifications do not include Refclk jitter.

This table defines the AC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 78. PCI Express 2.0 (5 GT/s) differential receiver input AC specifications[1]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	199.40	200.00	200.06	ps	1, 2
Max receiver inherent timing error	$T_{RX-TJ-CC}$	-	-	0.4	UI	3, 5, 6
Max receiver inherent deterministic timing error	$T_{RX-DJ-DD-CC}$	-	-	0.30	UI	4, 5, 6

Note:

1. Each UI is 200 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations.
2. For recommended operating conditions, see Table 3.
3. The maximum inherent total timing error for common and separated RefClk receiver architecture.

Table 78. PCI Express 2.0 (5 GT/s) differential receiver input AC specifications[1]

Parameter	Symbol	Min	Typ	Max	Units	Notes
4. The maximum inherent deterministic timing error for common and separated RefClk receiver architecture.						
5. If spread spectrum clocking is desired, common clock must be used.						
6. The AC specifications do not include Refclk jitter.						

This table defines the AC specifications for the PCI Express 3.0 (8 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 79. PCI Express 3.0 (8 GT/s) differential receiver input AC specifications[5]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	124.9625	125.00	125.0375	ps	Each UI is 125 ps ± 300 ppm. UI does not account for spread-spectrum clock dictated variations. See Note 1.
Eye Width at TP2P	$T_{RX-SV-8G}$	0.3	-	0.35	UI	See Note 1
Differential mode interference	$V_{RX-SV-DIFF-8G}$	14	-	-	mV	Frequency = 2.1GHz. See Note 2.
Sinusoidal Jitter at 100 MHz	$T_{RX-SV-SJ-8G}$	-	-	0.1	UI p-p	Fixed at 100 MHz. See Note 3.
Random Jitter	$T_{RX-SV-RJ-8G}$	-	-	2.0	ps RMS	Random jitter spectrally flat before filtering. See Note 4.

Note:

1. $T_{RX-SV-8G}$ is referenced to TP2P and obtained after post processing data captured at TP2. $T_{RX-SV-8G}$ includes the effects of applying the behavioral receiver model and receiver behavioral equalization.

2. $V_{RX-SV-DIFF-8G}$ voltage may need to be adjusted over a wide range for the different loss calibration channels.

3. The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency as shown in Figure 40.

4. Random jitter (Rj) is applied over the following range: The low frequency limit may be between 1.5 and 10 MHz, and the upper limit is 1.0 GHz. See Figure 40 for details. Rj may be adjusted to meet the 0.3 UI value for $T_{RX-SV-8G}$.

5. For recommended operating conditions, see Table 3.

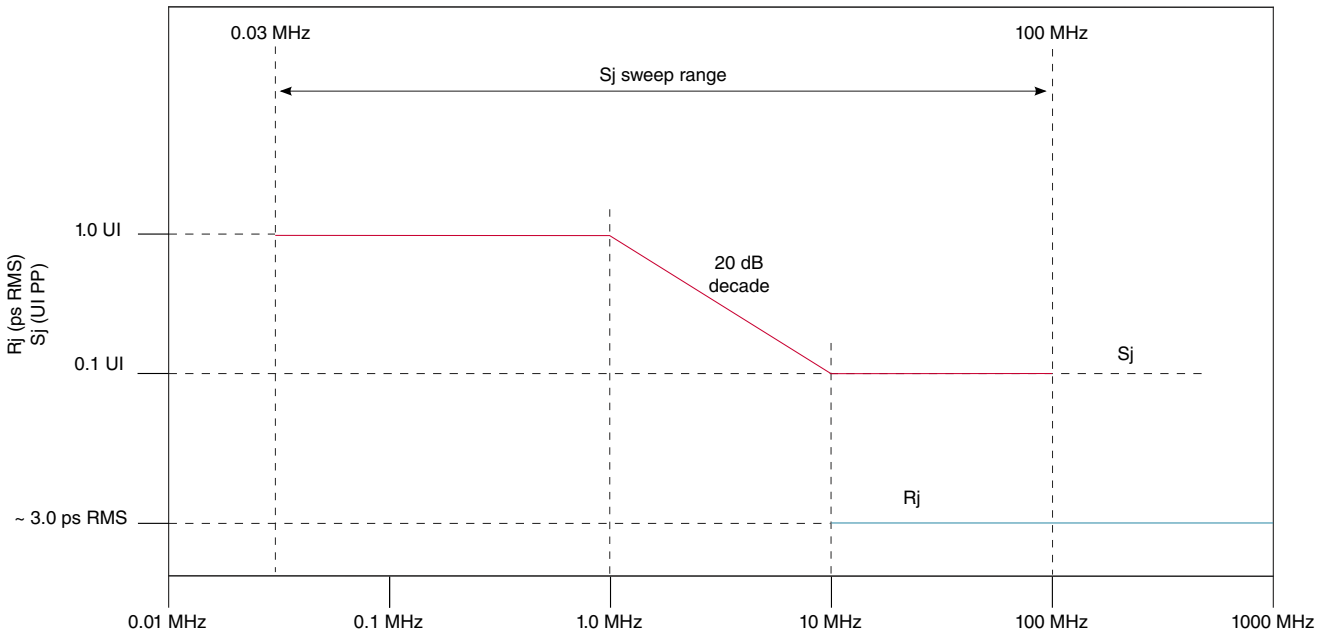


Figure 40. Swept sinusoidal jitter mask

3.19.4.6 Test and measurement load

The AC timing and voltage parameters must be verified at the measurement point. The package pins of the device must be connected to the test/measurement load within 0.2 inches of that load, as shown in the following figure.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D- not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D- package pins.

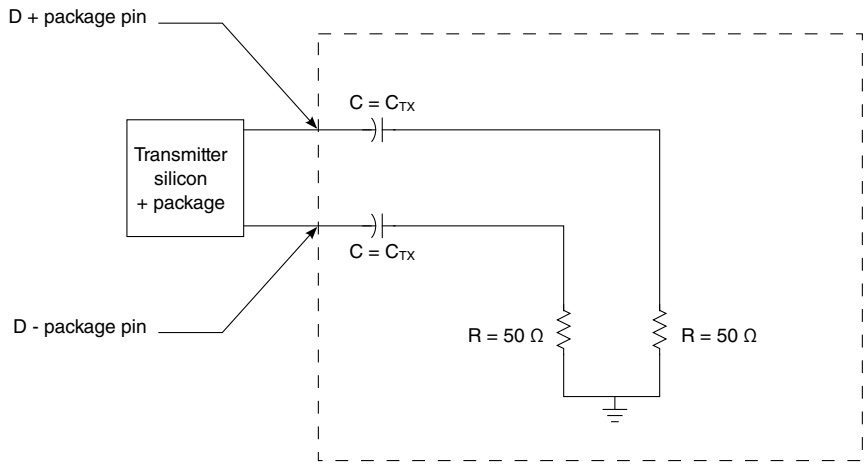


Figure 41. Test/measurement load

3.19.5 Serial RapidIO (sRIO)

This section describes the DC and AC electrical specifications for the serial RapidIO interface of the LP-Serial physical layer. The electrical specifications cover both single and multiple-lane links. Two transmitters (short run and long run) and a single receiver are specified for each of three baud rates: 2.50, 3.125 and 5 GBaud.

Two transmitter specifications allow for solutions ranging from simple board-to-board interconnect to driving two connectors across a backplane. A single receiver specification is given that accepts signals from both the short run and long run transmitter specifications.

The short run transmitter must be used mainly for chip-to-chip connections on either the same printed circuit board or across a single connector. This covers the case where connections are made to a mezzanine (daughter) card. The minimum swings of the short run specification reduce the overall power used by the transceivers.

The long run transmitter specifications use larger voltage swings that are capable of driving signals across backplanes. This allows a user to drive signals across two connectors and a backplane.

All unit intervals are specified with a tolerance of ± 100 ppm. The worst case frequency difference between any transmit and receive clock is 200 ppm.

To ensure interoperability between drivers and receivers of different vendors and technologies, AC coupling at the receiver input must be used.

3.19.5.1 Signal definitions

This section defines the terms used in the description and specification of the differential signals used by the LP-Serial links. The following figure shows how the signals are defined. The figures show waveforms for either a transmitter output (TD and TD_B) or a receiver input (RD and RD_B). Each signal swings between A volts and B volts where A > B. Using these waveforms, the definitions are as follows:

- The transmitter output signals and the receiver input signals-TD, TD_B, RD, and RD_B-each have a peak-to-peak swing of A - B volts.
- The differential output signal of the transmitter, V_{OD}, is defined as V_{TD} - V_{TD_B}
- The differential input signal of the receiver, V_{ID}, is defined as V_{RD} - V_{RD_B}
- The differential output signal of the transmitter and the differential input signal of the receiver each range from A - B to -(A - B) volts
- The peak value of the differential transmitter output signal and the differential receiver input signal is A - B volts.
- The peak-to-peak value of the differential transmitter output signal and the differential receiver input signal is 2 x (A - B) volts.

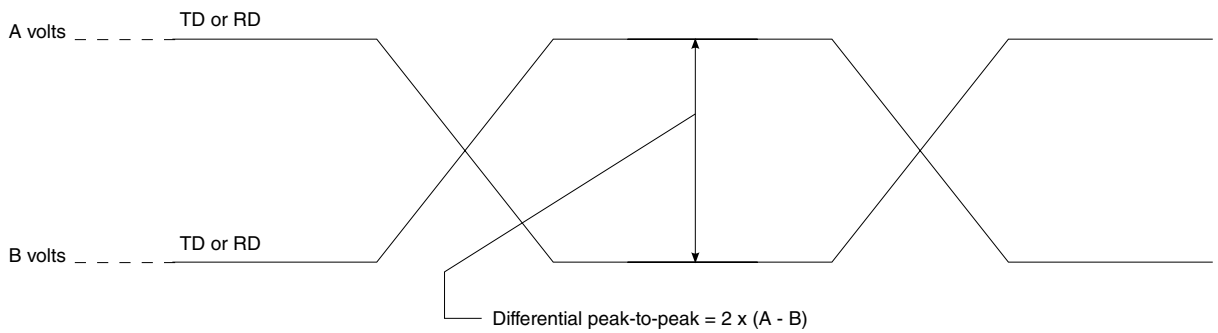


Figure 42. Differential peak-to-peak voltage of transmitter or receiver

To illustrate these definitions using real values, consider the case of a CML (current mode logic) transmitter that has a common mode voltage of 2.25 V, and each of its outputs TD and TD_B, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of the signals TD and TD_B is 500 mV p-p. The differential output signal ranges between 500 mV and -500 mV. The peak differential voltage is 500 mV. The peak-to-peak differential voltage is 1000 mV p-p.

3.19.5.2 Equalization

With the use of high-speed serial links, the interconnect media causes degradation of the signal at the receiver and produces effects such as inter-symbol interference (ISI) or data-dependent jitter. This loss can be large enough to degrade the eye opening at the receiver

beyond what is allowed in the specification. To negate a portion of these effects, equalization can be used. The most common equalization techniques that can be used are as follows:

- Pre-emphasis on the transmitter
- A passive high-pass filter network placed at the receiver, often referred to as passive equalization.
- The use of active circuits in the receiver, often referred to as adaptive equalization.

3.19.5.3 Serial RapidIO clocking requirements for SD*n*_REF_CLK*n* and SD*n*_REF_CLK*n*_B

SerDes 3 and SerDes 4 (SD[3:4]_REF_CLK[1:2] and SD[3:4]_REF_CLK[1:2]_B) may be used for various SerDes serial RapidIO configurations based on the RCW Configuration field SRDS_PRTCL. Serial RapidIO is not supported on SerDes 1 and 2. The ref clock frequency tolerance spec is ±100ppm.

For more information on these specifications, see SerDes reference clocks.

3.19.5.4 DC requirements for serial RapidIO

This section explains the DC requirements for the serial RapidIO interface.

3.19.5.4.1 DC serial RapidIO transmitter specifications

This table defines the transmitter DC specifications for serial RapidIO operating at 2.5 and 3.125 GBaud.

Table 80. Serial RapidIO transmitter DC specifications-2.5 GBaud, 3.125 GBaud[2]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Long-run differential output voltage	V_{DIFFPP}	800	-	1600	mV p-p	-
Short-run differential output voltage	V_{DIFFPP}	500	-	1000	mV p-p	-
DC Differential transmitter impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Transmitter DC differential impedance

Notes:

1. Voltage relative to COMMON of either signal comprising a differential pair
2. For recommended operating conditions, see Table 3.

This table defines the transmitter DC specifications for serial RapidIO operating at 5 GBaud.

Table 81. Serial RapidIO transmitter DC specifications-5 GBaud[1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Long-run differential output voltage	V_{DIFF}	800	-	1200	mV	-
Short-run differential output voltage	V_{DIFF}	400	-	750	mV	-
Long-run de-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3	3.5	4	dB	-
Long-run de-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	-
Differential resistance	T_{RD}	80	100	120	Ω	-

Notes:

1. For recommended operating conditions, see Table 3.

3.19.5.4.2 DC serial RapidIO receiver specifications

LP-Serial receiver electrical and timing specifications are stated in the text and tables of this section.

Receiver input impedance results in a differential return loss better than 10 dB and a common mode return loss better than 6 dB from 100 MHz to (0.8) x (Baud Frequency). This includes contributions from on-chip circuitry, the chip package, and any off-chip components related to the receiver. AC coupling components are included in this requirement. The reference impedance for return loss measurements is 100-Ω resistive for differential return loss and 25-Ω resistive for common mode.

This table defines the receiver DC specifications for serial RapidIO operating at 2.5 and 3.125 GBaud.

Table 82. Serial RapidIO receiver DC specifications-2.5 GBaud, 3.125 GBaud[2]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Differential input voltage	V_{IN}	200	-	1600	mV p-p	1
DC differential receiver input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	Receiver DC differential impedance

Notes:

1. Measured at the receiver
2. For recommended operating conditions, see Table 3.

This table defines the receiver DC specifications for serial RapidIO operating at 5 GBaud.

Table 83. Serial RapidIO receiver DC specifications-5 GBaud[2]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Long-run differential input voltage	V_{DIFF}	-	-	1200	mV	1
Short-run differential input voltage	V_{DIFF}	125	-	1200	mV	1
Differential resistance	R_{RD}	80	-	120	Ω	-

Notes:

1. Measured at the receiver.
2. For recommended operating conditions, see Table 3.

3.19.5.5 AC requirements for serial RapidIO

This section explains the AC requirements for the serial RapidIO interface.

3.19.5.5.1 AC requirements for serial RapidIO transmitter

This table defines the transmitter AC specifications for the serial RapidIO operating at 2.5 and 3.125 GBaud. The AC timing specifications do not include RefClk jitter.

Table 84. Serial RapidIO transmitter, 2.5 GBaud and 3.125 GBaud, AC timing specifications[1]

Parameter	Symbol	Min	Typical	Max	Unit
Deterministic jitter	J_D	-	-	0.17	UI p-p
Total jitter	J_T	-	-	0.35	UI p-p
Unit Interval: 2.5 GBaud	UI	400 - 100ppm	400	400 + 100ppm	ps
Unit Interval: 3.125 GBaud	UI	320 - 100ppm	320	320 + 100ppm	ps

Notes:

1. For recommended operating conditions, see Table 3.

This table defines the transmitter AC specifications for the serial RapidIO operating at 5 GBaud, short range. The AC timing specifications do not include RefClk jitter.

Table 85. Serial RapidIO transmitter, 5 GBaud, AC timing specifications[1]

Parameter	Symbol	Min	Typical	Max	Unit
Baud rate	T_{BAUD}	5.000 - 100ppm	5.000	5.000 + 100ppm	GBaud
Uncorrelated high probability jitter	T_{UHPJ}	-	-	0.155	UI p-p
Total jitter	T_J	-	-	0.30	UI p-p

Notes:

1. For recommended operating conditions, see Table 3.

This table defines the receiver AC specifications for serial RapidIO operating at 2.5 and 3.125 GBaud. The AC timing specifications do not include RefClk jitter.

Table 86. Serial RapidIO receiver, 2.5 GBaud and 3.125 GBaud, AC timing specifications[3]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Deterministic jitter tolerance	J_D	-	-	0.37	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	-	-	0.55	UI p-p	1
Total jitter tolerance[2]	J_T	-	-	0.65	UI p-p	1
Bit error rate	BER	-	-	10^{-12}	-	-
Unit Interval: 2.5 GBaud	UI	400 - 100ppm	400	400 + 100ppm	ps	-
Unit Interval: 3.125 GBaud	UI	320 - 100ppm	320	320 + 100ppm	ps	-

Notes:

1. Measured at receiver

2. Total jitter is composed of three components: deterministic jitter, random jitter and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 43. The sinusoidal jitter component is included to ensure margin for low-frequency jitter, wander, noise, crosstalk, and other variable system effects.

3. For recommended operating conditions, see Table 3.

This figure shows the single-frequency sinusoidal jitter limits for 2.5 GBaud and 3.125 GBaud rates.

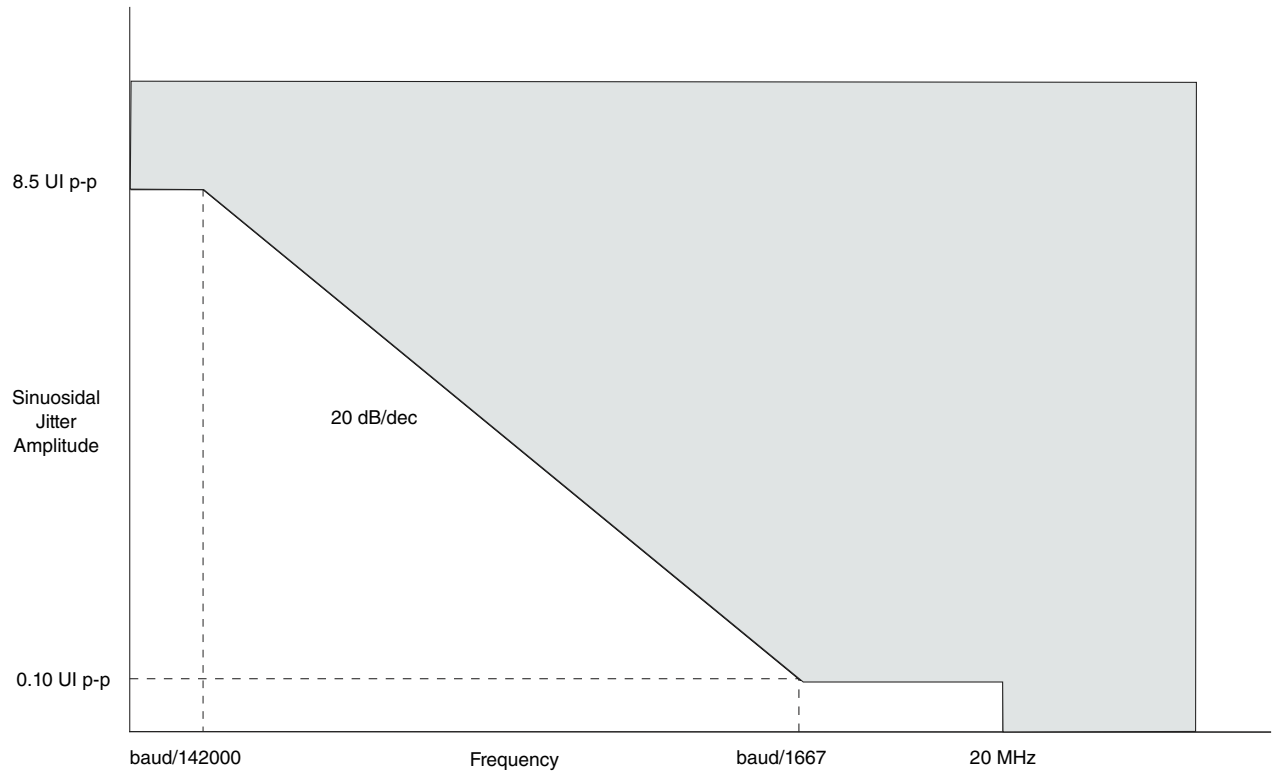


Figure 43. Single-frequency sinusoidal jitter limits, substitute the baud parameter in this figure by either 2.5G or 3.125G.

This table defines the receiver AC specifications for serial RapidIO operating at 5 GBaud. The AC timing specifications do not include RefClk jitter.

Table 87. Serial RapidIO receiver, 5G Baud, AC timing specifications[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Receiver baud rate	R_{BAUD}	5.000 - 100ppm	5.000	5.000 + 100ppm	Gbaud	-
Long-run Gaussian jitter	R_{GJ}	-	-	0.2	UI p-p	2
Long-Run Uncorrelated bounded high probability jitter	R_{UHPJ}	-	-	0.12	UI p-p	2, 3
Long-run correlated bounded high probability jitter	R_{CBHPJ}	-	-	0.63	UI p-p	2, 4
Short-run correlated bounded high probability jitter	R_{CBHPJ}	-	-	0.30	UI p-p	2, 4
Long-run bounded high probability jitter	R_{BHPJ}	-	-	0.75	UI p-p	3, 4
Short-run bounded high probability jitter	R_{BHPJ}	-	-	0.45	UI p-p	3, 4
Sinusoidal jitter, maximum	R_{SJ-max}	-	-	5.00	UI p-p	-
Sinusoidal jitter, high frequency	R_{SJ-hf}	-	-	0.05	UI p-p	-
Long-run total jitter (does not include sinusoidal jitter)	R_{Tj}	-	-	0.95	UI p-p	3, 4
Short-run total jitter (does not include sinusoidal jitter)	R_{Tj}	-	-	0.60	UI p-p	3, 4

Table continues on the next page...

Table 87. Serial RapidIO receiver, 5G Baud, AC timing specifications[1] (continued)

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Notes:						
1. For recommended operating conditions, see Table 3.						
2. The AC specifications do not include Refclk jitter.						
3. The jitter (R_{UHPJ}) is Bounded High Probability Jitter and is commonly caused by crosstalk coupling and can have periodic and bounded PRBS jitter subcomponents.						
4. The jitter (R_{CBHPJ}) and amplitude have to be correlated, for example by a PCB trace.						

This figure shows the single-frequency sinusoidal jitter limits for 5 GBaud rate.

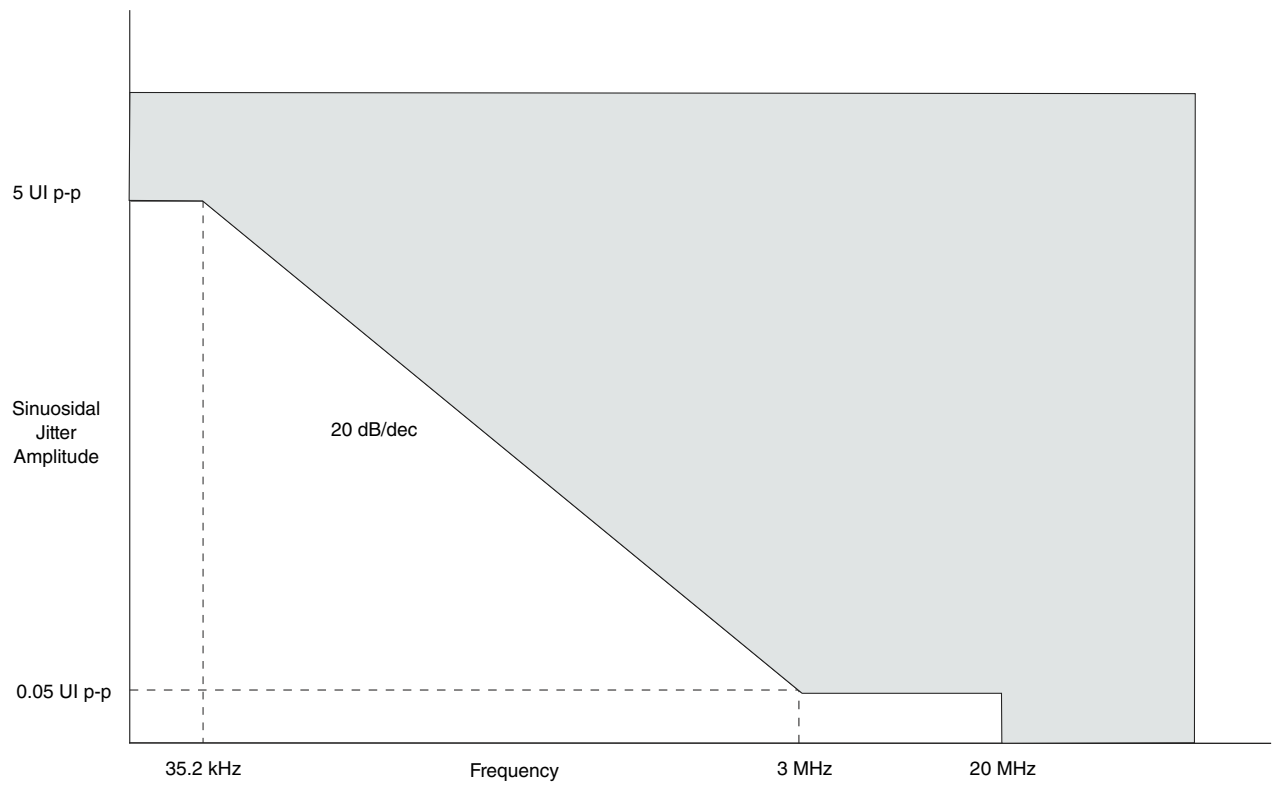


Figure 44. Single-frequency sinusoidal jitter limits

3.19.6 XAUI interface

This section describes the DC and AC electrical specifications for the XAUI bus.

3.19.6.1 XAUI DC electrical characteristics

This section discusses the XAUI DC electrical characteristics for the clocking signals, transmitter, and receiver.

3.19.6.1.1 DC requirements for XAUI SD*n*_REF_CLK*n* and SD*n*_REF_CLK*n*_B

Only SerDes 1-2 (SD[1:2]_REF_CLK[1:2] and SD[1:2]_REF_CLK[1:2]_B) may be used for various SerDes XAUI configurations based on the RCW Configuration field SRDS_PRTCL. The ref clock frequency tolerance spec is ±100ppm.

For more information on these specifications, see SerDes reference clocks.

3.19.6.1.2 XAUI transmitter DC electrical characteristics

This table defines the XAUI transmitter DC electrical characteristics.

Table 88. XAUI transmitter DC electrical characteristics (XV_{DD} = 1.35V or 1.5V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Differential output voltage	V_{DIFFPP}	800	1000	1600	mV p-p	-
DC Differential transmitter impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	3
1. For recommended operating conditions, see Table 3.						
2. Absolute output voltage limit						
3. Transmitter DC differential impedance						

3.19.6.1.3 XAUI receiver DC electrical characteristics

This table defines the XAUI receiver DC electrical characteristics.

Table 89. XAUI receiver DC timing specifications (SV_{DD} = 1.0 V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Differential input voltage	V_{IN}	200	-	1600	mV p-p	2
DC Differential receiver input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	3
1. For recommended operating conditions, see Table 3.						
2. Measured at the receiver.						
3. Receiver DC differential impedance						

3.19.6.2 XAUI AC timing specifications

This section explains the AC requirements for the XAUI interface.

3.19.6.2.1 XAUI transmitter AC timing specifications

This table defines the XAUI transmitter AC timing specifications. RefClk jitter is not included.

Table 90. XAUI transmitter AC timing specifications [1]

Parameter	Symbol	Min	Typical	Max	Unit
Deterministic jitter	J_D	-	-	0.17	UI p-p
Total jitter	J_T	-	-	0.35	UI p-p
Unit Interval: 3.125 Gb/s	UI	320 - 100 ppm	320	320 + 100 ppm	ps
1. For recommended operating conditions, see Table 3.					

3.19.6.2.2 XAUI receiver AC timing specifications

This table defines the receiver AC specifications for XAUI. RefClk jitter is not included.

Table 91. XAUI receiver AC timing specifications[3]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Deterministic jitter tolerance	J_D	-	-	0.37	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	-	-	0.55	UI p-p	1
Total jitter tolerance	J_T	-	-	0.65	UI p-p	1, 2
Bit error rate	BER	-	-	10^{-12}	-	-
Unit Interval: 3.125 Gb/s	UI	320 - 100 ppm	320	320 + 100 ppm	ps	-

Notes:

1. Measured at receiver.

2. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 44. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk, and other variable system effects.

3. For recommended operating conditions, see Table 3.

3.19.7 Aurora interface

This section describes the Aurora clocking requirements and its DC and AC electrical characteristics.

3.19.7.1 Aurora clocking requirements for SD*n*_REF_CLK*n* and SDn_REF_CLKn_B

Only SerDes 4 (SD4_REF_CLK[1:2] and SD4_REF_CLK[1:2]_B) may be used for SerDes Aurora configurations based on the RCW Configuration field SRDS_PRTCL. The ref clock frequency tolerance spec is ±100ppm. Aurora is not supported on SerDes 1-3.

For more information on these specifications, see SerDes reference clocks.

3.19.7.2 Aurora DC electrical characteristics

This section describes the DC electrical characteristics for the Aurora interface.

3.19.7.2.1 Aurora transmitter DC electrical characteristics

This table defines the Aurora transmitter DC electrical characteristics.

Table 92. Aurora transmitter DC electrical characteristics (XV_{DD} = 1.35 V or 1.5 V) [1]

Parameter	Symbol	Min	Typical	Max	Unit
Differential output voltage	V_{DIFFPP}	800	1000	1600	mV p-p
DC Differential transmitter impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω
1. For recommended operating conditions, see Table 3.					

3.19.7.2.2 Aurora receiver DC electrical characteristics

This table defines the Aurora receiver DC electrical characteristics for the Aurora interface.

Table 93. Aurora receiver DC electrical characteristics (SV_{DD} = 1.0V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Differential input voltage	V_{IN}	200	-	1600	mV p-p	2
DC Differential receiver impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	3
Notes: 1. For recommended operating conditions, see Table 3. 2. Measured at receiver 3. DC Differential receiver impedance						

3.19.7.3 Aurora AC timing specifications

This section describes the AC timing specifications for Aurora.

3.19.7.3.1 Aurora transmitter AC timing specifications

This table defines the Aurora transmitter AC timing specifications. RefClk jitter is not included.

Table 94. Aurora transmitter AC timing specifications[1]

Parameter	Symbol	Min	Typical	Max	Unit
Deterministic jitter	J_D	-	-	0.17	UI p-p
Total jitter	J_T	-	-	0.35	UI p-p
Unit interval: 2.5 Gbps	UI	400 - 100 ppm	400	400 + 100 ppm	ps
Unit interval: 3.125 Gbps	UI	320 - 100 ppm	320	320 + 100 ppm	ps
Unit interval: 5.0 Gbps	UI	200 - 100 ppm	200	200 + 100 ppm	ps

Notes:

1. For recommended operating conditions, see Table 3.

3.19.7.3.2 Aurora receiver AC timing specifications

This table defines the Aurora receiver AC timing specifications. RefClk jitter is not included.

Table 95. Aurora receiver AC timing specifications[3]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Deterministic jitter tolerance	J_D	-	-	0.37	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	-	-	0.55	UI p-p	1
Total jitter tolerance	J_T	-	-	0.65	UI p-p	1, 2
Bit error rate	BER	-	-	10^{-12}	-	-
Unit Interval: 2.5 Gbps	UI	400 - 100 ppm	400	400 + 100 ppm	ps	-
Unit Interval: 3.125 Gbps	UI	320 - 100 ppm	320	320 + 100 ppm	ps	-
Unit Interval: 5.0 Gbps	UI	200 - 100 ppm	200	200 + 100 ppm	ps	-

Notes:

1. Measured at receiver

2. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 43. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

3. For recommended operating conditions, see Table 3.

3.19.8 Serial ATA (SATA) interface

This section describes the DC and AC electrical specifications for the serial ATA (SATA) interface.

3.19.8.1 SATA DC electrical characteristics

This section describes the DC electrical characteristics for SATA.

3.19.8.1.1 SATA DC transmitter output characteristics

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen1i/1m or 1.5 Gbps transmission.

Table 96. Gen1i/1m 1.5G transmitter DC specifications (XV_{DD} = 1.35 V or 1.5 V)[3]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Tx differential output voltage	V_{SATA_TXDIFF}	400	500	600	mV p-p	1
Tx differential pair impedance	$Z_{SATA\_TXDIFFIM}$	85	100	115	Ω	2
Notes: 1. Terminated by 50 Ω load 2. DC impedance 3. For recommended operating conditions, see Table 3.						

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen2i/2m or 3.0 Gbps transmission.

Table 97. Gen 2i/2m 3G transmitter DC specifications (XV_{DD} = 1.35 V or 1.5 V)[2]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Transmitter differential output voltage	V_{SATA_TXDIFF}	400	-	700	mV p-p	1
Transmitter differential pair impedance	$Z_{SATA\_TXDIFFIM}$	85	100	115	Ω	-
Notes: 1. Terminated by 50 Ω load. 2. For recommended operating conditions, see Table 3.						

3.19.8.1.2 SATA DC receiver input characteristics

This table provides the Gen1i/1m or 1.5 Gbps differential receiver input DC characteristics for the SATA interface.

Table 98. Gen1i/1m 1.5 G receiver input DC specifications (SV_{DD} = 1.0 V)[3]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{SATA_RXDIFF}	240	500	600	mV p-p	1
Differential receiver input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	2
OOB signal detection threshold	V_{SATA_OOB}	50	120	240	mV p-p	-

Notes:

1. Voltage relative to common of either signal comprising a differential pair
2. DC impedance
3. For recommended operating conditions, see Table 3.

This table provides the Gen2i/2m or 3 Gbps differential receiver input DC characteristics for the SATA interface.

Table 99. Gen2i/2m 3 G receiver input DC specifications (SV_{DD} = 1.0 V)[3]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{SATA_RXDIFF}	240	-	750	mV p-p	1
Differential receiver input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	2
OOB signal detection threshold	V_{SATA_OOB}	75	120	240	mV p-p	2

Notes:

1. Voltage relative to common of either signal comprising a differential pair
2. DC impedance
3. For recommended operating conditions, see Table 3.

3.19.8.2 SATA AC timing specifications

This section discusses the SATA AC timing specifications.

3.19.8.2.1 AC requirements for SATA REF_CLK

The AC requirements for the SATA reference clock listed in this table are to be guaranteed by the customer's application design. SATA does not support TX Spread Spectrum Clock as it is an optional requirement in protocol. However T4 SATA supports RX spread spectrum data as it is required in the SATA standard that all SATA Receivers handle spread spectrum. SerDes can receive spread spectrum without affecting other protocols since this doesn’t affect SerDes PLL.

Table 100. SATA reference clock input requirements[6]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SDn_REF_CLKn/SDn_REF_CLKn_B frequency range	t_{CLK_REF}	-	100/125	-	MHz	1
SDn_REF_CLKn/SDn_REF_CLKn_B clock frequency tolerance	t_{CLK_TOL}	-350	-	+350	ppm	-
SDn_REF_CLKn/SDn_REF_CLKn_B reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	5
SDn_REF_CLKn/SDn_REF_CLKn_B cycle-to-cycle clock jitter (period jitter)	t_{CLK_CJ}	-	-	100	ps	2
SDn_REF_CLKn/SDn_REF_CLKn_B total reference clock jitter, phase jitter (peak-to-peak)	t_{CLK_PJ}	-50	-	+50	ps	2, 3, 4

Notes:

1. **Caution:** Only 100 and 125MHz have been tested. In-between values do not work correctly with the rest of the system.
2. At RefClk input
3. In a frequency band from 150 kHz to 15 MHz at BER of 10^{-12}
4. Total peak-to-peak deterministic jitter must be less than or equal to 50 ps.
5. Measurement taken from differential waveform
6. For recommended operating conditions, see Table 3.

3.19.8.3 AC transmitter output characteristics

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen1i/1m or 1.5 Gbps transmission. The AC timing specifications do not include RefClk jitter.

Table 101. Gen1i/1m 1.5 G transmitter AC specifications[2]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Channel speed	t_{CH_SPEED}	-	1.5	-	Gbps	-
Unit Interval	T_{UI}	666.4333	666.6667	670.2333	ps	-
Total jitter data-data 5 UI	$U_{SATA\_TXTJ5UI}$	-	-	0.355	UI p-p	1
Total jitter, data-data 250 UI	$U_{SATA\_TXTJ250UI}$	-	-	0.47	UI p-p	1
Deterministic jitter, data-data 5 UI	$U_{SATA\_TXDJ5UI}$	-	-	0.175	UI p-p	1
Deterministic jitter, data-data 250 UI	$U_{SATA\_TXDJ250UI}$	-	-	0.22	UI p-p	1

Notes:

1. Measured at transmitter output pins peak to peak phase variation, random data pattern
2. For recommended operating conditions, see Table 3.

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen2i/2m or 3.0 Gbps transmission. The AC timing specifications do not include RefClk jitter.

Table 102. Gen 2i/2m 3 G transmitter AC specifications[2]

Parameter	Symbol	Min	Typ	Max	Units	Notes
Channel speed	t_{CH_SPEED}	-	3.0	-	Gbps	-
Unit Interval	T_{UI}	333.2167	333.3333	335.1167	ps	-
Total jitter $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_TXTJfB/500}$	-	-	0.37	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_TXTJfB/1667}$	-	-	0.55	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_TXDJfB/500}$	-	-	0.19	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_TXDJfB/1667}$	-	-	0.35	UI p-p	1

Notes:

1. Measured at transmitter output pins peak-to-peak phase variation, random data pattern
2. For recommended operating conditions, see Table 3.

3.19.8.4 AC differential receiver input characteristics

This table provides the Gen1i/1m or 1.5 Gbps differential receiver input AC characteristics for the SATA interface. The AC timing specifications do not include RefClk jitter.

Table 103. Gen 1i/1m 1.5G receiver AC specifications[2]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Unit Interval	T_{UI}	666.4333	666.6667	670.2333	ps	-
Total jitter data-data 5 UI	$U_{SATA\_RXTJ5UI}$	-	-	0.43	UI p-p	1
Total jitter, data-data 250 UI	$U_{SATA\_RXTJ250UI}$	-	-	0.60	UI p-p	1
Deterministic jitter, data-data 5 UI	$U_{SATA\_RXDJ5UI}$	-	-	0.25	UI p-p	1
Deterministic jitter, data-data 250 UI	$U_{SATA\_RXDJ250UI}$	-	-	0.35	UI p-p	1

Notes:

1. Measured at receiver.
2. For recommended operating conditions, see Table 3.

This table provides the differential receiver input AC characteristics for the SATA interface at Gen2i/2m or 3.0 Gbps transmission. The AC timing specifications do not include RefClk jitter.

Table 104. Gen 2i/2m 3G receiver AC specifications[2]

Parameter	Symbol	Min	Typical	Max	Units	Notes
Unit Interval	T_{UI}	333.2167	333.3333	335.1167	ps	-
Total jitter $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_RXTJfB/500}$	-	-	0.60	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_RXTJfB/1667}$	-	-	0.65	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_RXDJfB/500}$	-	-	0.42	UI p-p	1

Table continues on the next page...

Table 104. Gen 2i/2m 3G receiver AC specifications[2] (continued)

Parameter	Symbol	Min	Typical	Max	Units	Notes
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_RXDJfB/1667}$	-	-	0.35	UI p-p	1

Notes:

1. Measured at receiver
2. For recommended operating conditions, see Table 3.

3.19.9 SGMII interface

Each SGMII port features a 4-wire AC-coupled serial link from the SerDes interface of the chip, as shown in Figure 45, where C_{TX} is the external (on board) AC-coupled capacitor. Each SerDes transmitter differential pair features 100-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to XGND*n*. The reference circuit of the SerDes transmitter and receiver is shown in Figure 39.

3.19.9.1 SGMII clocking requirements for SD*n*_REF_CLK*n* and SD*n*_REF_CLK*n*_B

When operating in SGMII mode, the EC*n*_GTX_CLK125 clock is not required for this port. Instead, a SerDes reference clock is required on SD[1:2]_REF_CLK[1:2] and SD[1:2]_REF_CLK[1:2]_Bpins. SerDes 1-2 may be used for SerDes SGMII configurations based on the RCW Configuration field SRDS_PRTCL.

For more information on these specifications, see SerDes reference clocks.

3.19.9.2 SGMII DC electrical characteristics

This section discusses the electrical characteristics for the SGMII interface.

3.19.9.2.1 SGMII and SGMII 2.5x transmit DC specifications

This table describes the SGMII SerDes transmitter AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD*n*_TX*n* and SD*n*_TX*n*_B)as shown in Figure 46.

Table 105. SGMII DC transmitter electrical characteristics (XV_{DD} = 1.35 V or 1.5 V)[4]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output high voltage	V_{OH}	-	-	1.5 x $\lvert V_{OD} \rvert_{-max}$	mV	1

Table continues on the next page...

Table 105. SGMII DC transmitter electrical characteristics (XV_{DD} = 1.35 V or 1.5 V)[4] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output low voltage	V_{OL}	$\|V_{OD}\|_{-min}/2$	-	-	mV	1
Output differential voltage[2, 3] (XV_{DD-Typ} at 1.35 V and 1.5 V)	$\|V_{OD}\|$	320	500	725	mV	SRDSxLNmTECR0 [AMP_RED] = 6b000000
		293.8	459.0	665.6		SRDSxLNmTECR0 [AMP_RED] = 6b000001
		266.9	417.0	604.7		SRDSxLNmTECR0 [AMP_RED] = 6b000011
		240.6	376.0	545.2		SRDSxLNmTECR0 [AMP_RED] = 6b000010
		213.1	333.0	482.9		SRDSxLNmTECR0 [AMP_RED] = 6b000110 (Default)
		186.9	292.0	423.4		SRDSxLNmTECR0 [AMP_RED] = 6b000111
		160.0	250.0	362.5		SRDSxLNmTECR0 [AMP_RED] = 6b010000
Output impedance (single ended)	R_O	40	50	60	Ω	-

Notes:

1. This does not align to DC-coupled SGMII.
2. $|V_{OD}| = |V_{SD\_TXn} - V_{SD\_TXn\_B}|$. $|V_{OD}|$ is also referred to as output differential peak voltage. $V_{TX-DIFFp-p} = 2 \times |V_{OD}|$.
3. The $|V_{OD}|$ value shown in the Typ column is based on the condition of XVDD_SRDSn-Typ = 1.35 V or 1.5 V, no common mode offset variation. SerDes transmitter is terminated with 100-Ω differential load between SDn _TXn and SDn_TXn_B.
4. For recommended operating conditions, see Table 3.

This figure shows an example of a 4-wire AC-coupled SGMII serial link connection.

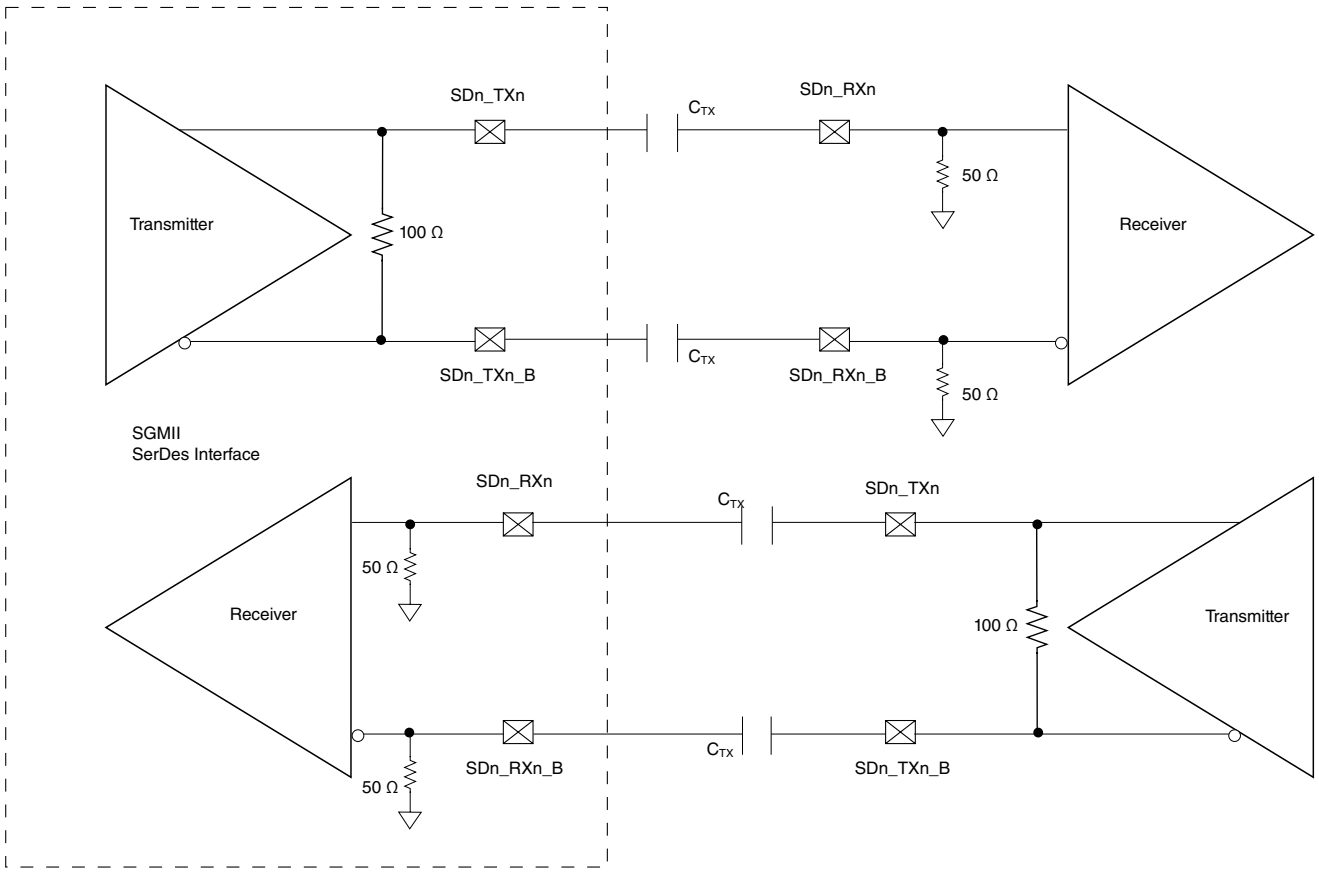


Figure 45. 4-wire AC-coupled SGMII serial link connection example

This figure shows the SGMII transmitter DC measurement circuit.

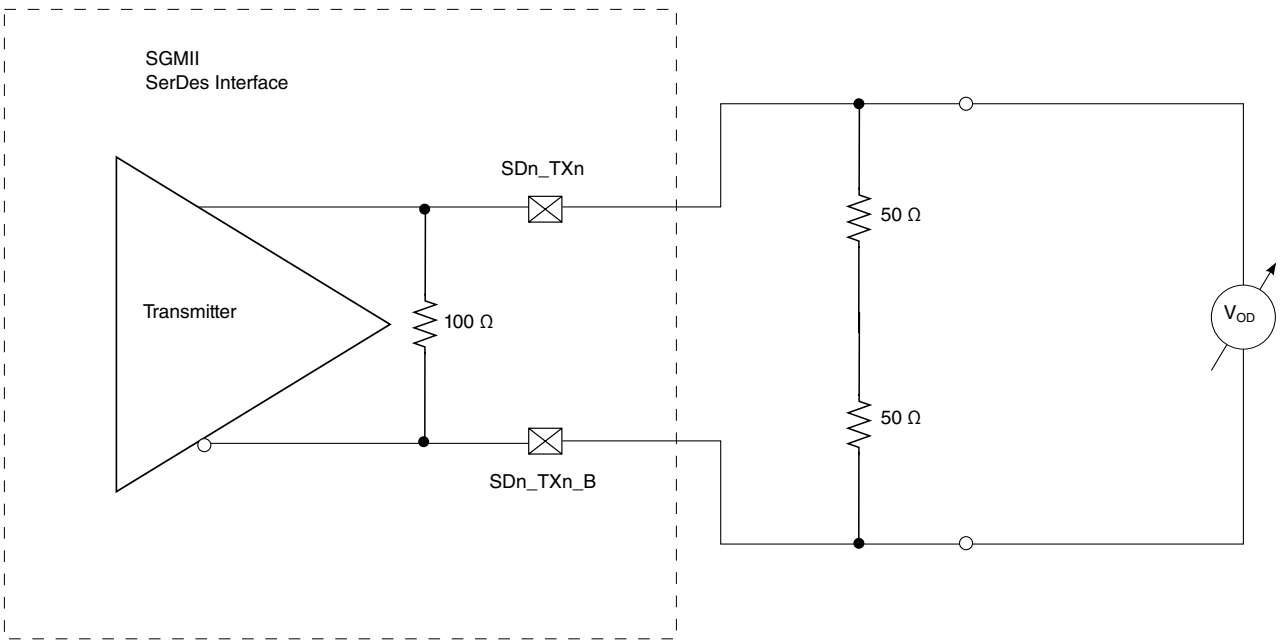


Figure 46. SGMII transmitter DC measurement circuit

This table defines the SGMII 2.5x transmitter DC electrical characteristics for 3.125 GBaud.

Table 106. SGMII 2.5x transmitter DC electrical characteristics (XV_{DD} = 1.35 V or 1.5 V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Output differential voltage	$\lvert V_{OD} \rvert$	400	-	600	mV	SRDSxLNmTECR0 [AMP_RED] = 6b000000
Output impedance (differential)	R_O	80	100	120	Ω	-
Notes: 1. For recommended operating conditions, see Table 3.						

3.19.9.2.2 SGMII and SGMII 2.5x DC receiver electrical characteristics

This table lists the SGMII DC receiver electrical characteristics. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 107. SGMII DC receiver electrical characteristics (SV_{DD} = 1.0V)[4]

Parameter		Symbol	Min	Typ	Max	Unit	Notes
DC input voltage range		-	N/A			-	1
Input differential voltage	SRDSxLNmGCR1 [REIDL_TH] = 001	$V_{RX\_DIFFp-p}$	100	-	1200	mV	2

Table continues on the next page...

Table 107. SGMII DC receiver electrical characteristics (SV_{DD} = 1.0V)[4] (continued)

Parameter		Symbol	Min	Typ	Max	Unit	Notes
	SRDSxLNmGCR1 [REIDL_TH] = 100		175	-			
Loss of signal threshold	SRDSxLNmGCR1 [REIDL_TH] = 001	V_{LOS}	30	-	100	mV	3
	SRDSxLNmGCR1 [REIDL_TH] = 100		65	-	175		
Receiver differential input impedance		Z_{RX_DIFF}	80	-	120	Ω	-

Notes:

1. Input must be externally AC coupled.
2. $V_{RX\_DIFFp\text{-}p}$ is also referred to as peak-to-peak input differential voltage.
3. The concept of this parameter is equivalent to the electrical idle detect threshold parameter in PCI Express. See PCI Express DC physical layer receiver specifications, and PCI Express AC physical layer receiver specifications, for further explanation.
4. For recommended operating conditions, see Table 3.

This table defines the SGMII 2.5x receiver DC electrical characteristics for 3.125 GBaud.

Table 108. SGMII 2.5x receiver DC timing specifications (SV_{DD} = 1.0V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage	$V_{RX\_DIFFp\text{-}p}$	200	-	1200	mV	-
Loss of signal threshold	V_{LOS}	75	-	200	mV	-
Receiver differential input impedance	Z_{RX_DIFF}	80	-	120	Ω	-

Notes:

1. For recommended operating conditions, see Table 3.

3.19.9.3 SGMII AC timing specifications

This section discusses the AC timing specifications for the SGMII interface.

3.19.9.3.1 SGMII and SGMII 2.5x transmit AC timing specifications

This table provides the SGMII and SGMII 2.5x transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include RefClk jitter.

Table 109. SGMII transmit AC timing specifications[4]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval: 1.25 GBaud (SGMII)	UI	800 - 100 ppm	800	800 + 100 ppm	ps	1
Unit Interval: 3.125 GBaud (2.5x SGMII])	UI	320 - 100 ppm	320	320 + 100 ppm	ps	1

Table continues on the next page...

Table 109. SGMII transmit AC timing specifications[4] (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter	JD	-	-	0.17	UI p-p	-
Total jitter	JT	-	-	0.35	UI p-p	2
AC coupling capacitor	C_{TX}	10	-	200	nF	3

Notes:

1. Each UI is 800 ps ± 100 ppm or 320 ps ± 100 ppm.
2. See Figure 43 for single frequency sinusoidal jitter measurements.
3. The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter outputs.
4. For recommended operating conditions, see Table 3.

3.19.9.3.2 SGMII AC measurement details

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD*n*_TX*n* and SD*n*_TX*n*_B) or at the receiver inputs (SD*n*_RX*n* and SD*n*_RX*n*_B) respectively, as depicted in this figure.

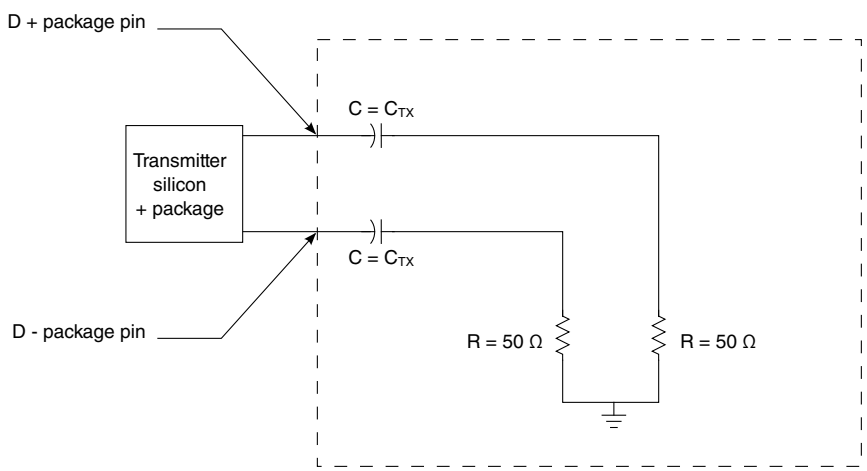


Figure 47. SGMII AC test/measurement load

3.19.9.3.3 SGMII and SGMII 2.5x receiver AC timing Specification

This table provides the SGMII and SGMII 2.5x receiver AC timing specifications. The AC timing specifications do not include RefClk jitter. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 110. SGMII Receive AC timing specifications[3]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter tolerance	J_D	-	-	0.37	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	-	-	0.55	UI p-p	1
Total jitter tolerance	J_T	-	-	0.65	UI p-p	1, 2
Bit error ratio	BER	-	-	10^{-12}	-	-
Unit Interval: 1.25 GBaud (SGMII)	UI	800 - 100 ppm	800	800 + 100 ppm	ps	1
Unit Interval: 3.125 GBaud (2.5x SGMII])	UI	320 - 100 ppm	320	320 + 100 ppm	ps	1

Notes:

1. Measured at receiver

2. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 43. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

3. For recommended operating conditions, see Table 3.

The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of Figure 44.

3.19.10 QSGMII interface

This section describes the QSGMII clocking and its DC and AC electrical characteristics.

3.19.10.1 QSGMII clocking requirements for SD*n*_REF_CLK*n* and SD*n*_REF_CLK*n*_B

The ref clock frequency tolerance spec is ±100ppm. For more information on these specifications, see SerDes reference clocks.

3.19.10.2 QSGMII DC electrical characteristics

This section discusses the electrical characteristics for the SGMII interface.

3.19.10.2.1 QSGMII transmitter DC specifications

This table describes the QSGMII SerDes transmitter AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD*n*_TX*n* and SD*n*_TX*n*_B).

Table 111. QSGMII DC transmitter electrical characteristics (XV_{DD} = 1.35V or 1.5V)[1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output differential voltage	V_{DIFF}	400	-	900	mV	-
Differential resistance	T_{RD}	80	100	120	Ω	-
Notes: 1. For recommended operating conditions, see Table 3.						

3.19.10.2.2 QSGMII DC receiver electrical characteristics

This table defines the QSGMII receiver DC electrical characteristics.

Table 112. QSGMII receiver DC timing specifications (SV_{DD} = 1.0V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage	V_{DIFF}	100	-	900	mV	-
Differential resistance	R_{RDIN}	80	100	120	Ω	-
Notes: 1. For recommended operating conditions, see Table 3.						

3.19.10.3 QSGMII AC timing specifications

This section discusses the AC timing specifications for the QSGMII interface.

3.19.10.3.1 QSGMII transmit AC timing specifications

This table provides the QSGMII transmitter AC timing specifications.

Table 113. QSGMII transmit AC timing specifications[1]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Transmitter baud rate	T_{BAUD}	5.000 - 100 ppm	5.000	5.000 + 100 ppm	Gbps	-
Uncorrelated high probability jitter	T_{UHPJ}	-	-	0.15	UI p-p	-
Total jitter tolerance	J_T	-	-	0.30	UI p-p	-
Notes: 1. For recommended operating conditions, see Table 3.						

3.19.10.3.2 QSGMII receiver AC timing Specification

This table provides the QSGMII receiver AC timing specifications.

Table 114. QSGMII receive AC timing specifications[2]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Receiver baud rate	R_{BAUD}	5.000 - 100 ppm	5.000	5.000 + 100 ppm	Gbps	-
Uncorrelated bounded high probability jitter	R_{DJ}	-	-	0.15	UI p-p	-
Correlated bounded high probability jitter	R_{CBHPJ}	-	-	0.30	UI p-p	1
Bounded high probability jitter	R_{BHPJ}	-	-	0.45	UI p-p	-
Sinusoidal jitter, maximum	R_{SJ-max}	-	-	5.00	UI p-p	-
Sinusoidal jitter, high frequency	R_{SJ-hf}	-	-	0.05	UI p-p	-
Total jitter (does not include sinusoidal jitter)	R_{Tj}	-	-	0.60	UI p-p	-

Notes:

1. The jitter (R_{CBHPJ}) and amplitude have to be correlated, for example, by a PCB trace.
2. For recommended operating conditions, see Table 3.

The sinusoidal jitter may have any amplitude and frequency in the unshaded region of this figure.

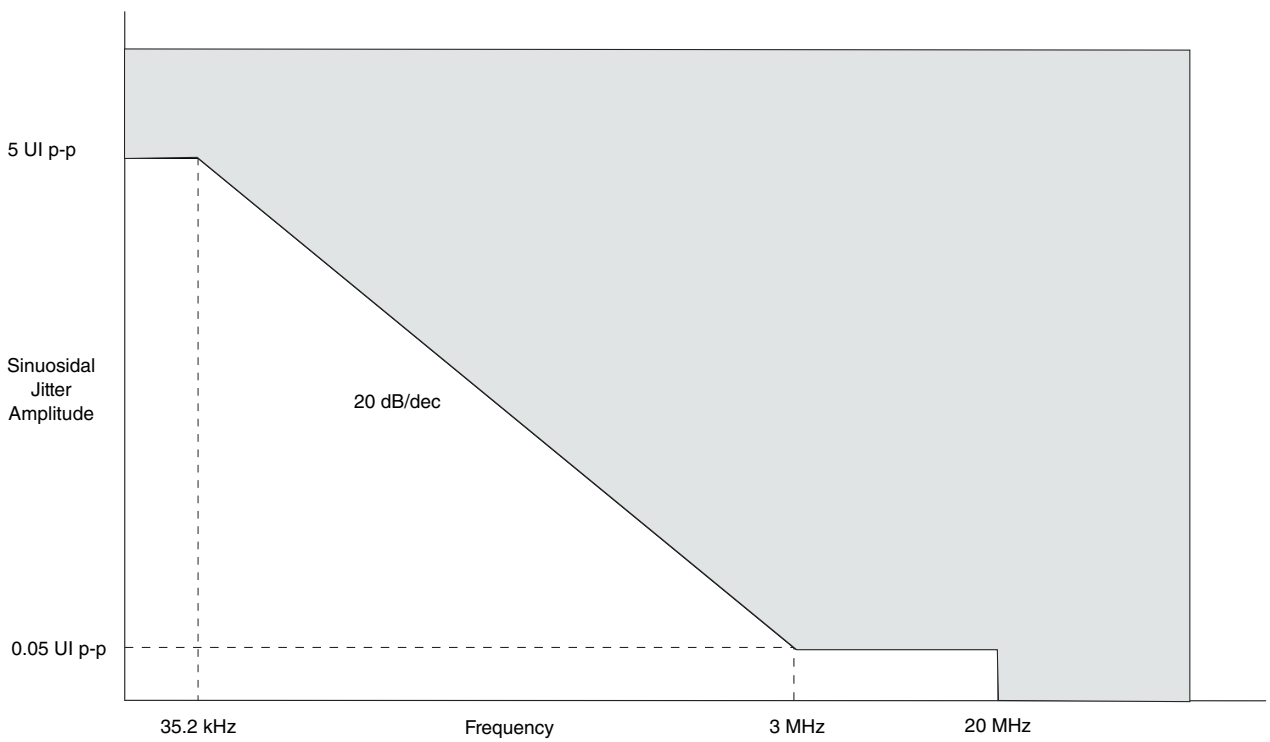


Figure 48. QSGMII single-frequency sinusoidal jitter limits

3.19.11 HiGig/HiGig2 interface

This section describes the HiGig/HiGig2 clocking requirements and its DC and AC electrical characteristics.

3.19.11.1 HiGig/HiGig2 clocking requirements for SD*n*_REF_CLK*n* and SD*n*_REF_CLK*n*_B

Only SerDes 1 and 2 (SD[1:2]_REF_CLK[1:2] and SD[1:2]_REF_CLK[1:2]_B) may be used for SerDes HiGig/HiGig2 configurations based on the RCW Configuration field SRDS_PRTCL. The ref clock frequency tolerance spec is ±100ppm.

For more information on these specifications, see SerDes reference clocks.

3.19.11.2 HiGig/HiGig2 DC electrical characteristics

This section describes the DC electrical characteristics for HiGig/HiGig2.

3.19.11.2.1 HiGig/HiGig2 transmitter DC electrical characteristics

This table defines the HiGig/HiGig2 transmitter DC electrical characteristics.

Table 115. HiGig/HiGig2 transmitter DC electrical characteristics (XV_{DD} = 1.35V or 1.5V)[2]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Differential output voltage	V_{DIFFPP}	800	1000	1600	mV p-p	-
DC Differential transmitter impedance	$Z_{TX-DIFF-DC}$	80	100	120	Ω	Transmitter DC differential impedance
Notes: 1. Absolute output voltage limit 2. For recommended operating conditions, see Table 3.						

3.19.11.2.2 HiGig/HiGig2 receiver DC electrical characteristics

This table defines the HiGig/HiGig2 receiver DC electrical characteristics.

Table 116. HiGig/HiGig2 receiver DC electrical characteristics (SV_{DD} = 1.0V)[2]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Differential input voltage	V_{IN}	200	-	1600	mV p-p	1
DC Differential receiver impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	DC Differential receiver impedance
1. Measured at receiver 2. For recommended operating conditions, see Table 3.						

3.19.11.3 HiGig/HiGig2 AC timing specifications

This section describes the AC timing specifications for HiGig/HiGig2.

3.19.11.3.1 HiGig/HiGig2 transmitter AC timing specifications

This table defines the HiGig/HiGig2 transmitter AC timing specifications. RefClk jitter is not included.

Table 117. HiGig/HiGig2 transmitter AC timing specifications[1]

Parameter	Symbol	Min	Typical	Max	Unit
Deterministic jitter	J_D	-	-	0.17	UI p-p
Total jitter	J_T	-	-	0.35	UI p-p
Unit Interval: 3.125 Gbps (HiGig/HiGig2)	UI	320 - 100 ppm	320	320 + 100 ppm	ps
Unit Interval: 3.75 Gbps (HiGig/HiGig2)	UI	266.66 - 100 ppm	266.66	266.66 + 100 ppm	ps

Notes:

1. For recommended operating conditions, see Table 3.

3.19.11.3.2 HiGig/HiGig2 receiver AC timing specifications

This table defines the HiGig/HiGig2 receiver AC timing specifications. RefClk jitter is not included.

Table 118. HiGig/HiGig2 receiver AC timing specifications[3]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Deterministic jitter tolerance	J_D	-	-	0.37	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	-	-	0.55	UI p-p	1
Total jitter tolerance	J_T	-	-	0.65	UI p-p	1, 2
Unit Interval: 3.125 Gbps (HiGig/ HiGig2)	UI	320 - 100ppm	320	320 + 100ppm	ps	-
Unit Interval: 3.75 Gbps (HiGig/HiGig2)	UI	266.66 - 100ppm	266.66	266.66 + 100ppm	ps	-

1. Measured at receiver

2. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 44. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

3. For recommended operating conditions, see Table 3.

3.19.12 XFI interface

This section describes the XFI clocking requirements and its DC and AC electrical characteristics.

3.19.12.1 XFI clocking requirements for SD*n*_REF_CLK*n* and SD*n*_REF_CLK*n*_B

Only SerDes 2 (SD2_REF_CLK[1:2] and SD2_REF_CLK[1:2]_B) may be used for SerDes XFI configurations based on the RCW Configuration field SRDS_PRTCL.

The ref clock frequency tolerance spec is ±100ppm. For more information on these specifications, see SerDes reference clocks.

3.19.12.2 XFI DC electrical characteristics

This section describes the DC electrical characteristics for XFI.

3.19.12.2.1 XFI transmitter DC electrical characteristics

This table defines the XFI transmitter DC electrical characteristics.

Table 119. XFI transmitter DC electrical characteristics (XV_{DD} = 1.35V or 1.5V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Output differential voltage	$V_{TX-DIFF}$	360	-	770	mV	-
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-1.14dB}$	0.6	1.1	1.6	dB	-
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3	3.5	4	dB	-
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-4.66dB}$	4.1	4.6	5.1	dB	-
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	-
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-9.5dB}$	9	9.5	10	dB	-
Differential resistance	T_{RD}	80	100	120	Ω	-

Notes:
1. For recommended operating conditions, see Table 3.

3.19.12.2.2 XFI receiver DC electrical characteristics

This table defines the XFI receiver DC electrical characteristics.

Table 120. XFI receiver DC electrical characteristics (SV_{DD} = 1.0V)[2]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage	$V_{RX-DIFF}$	110	-	1050	mV	1
Differential resistance	R_{RD}	80	100	120	Ω	-
1. Measured at receiver 2. For recommended operating conditions, see Table 3.						

3.19.12.3 XFI AC timing specifications

This section describes the AC timing specifications for XFI.

3.19.12.3.1 XFI transmitter AC timing specifications

This table defines the XFI transmitter AC timing specifications. RefClk jitter is not included.

Table 121. XFI transmitter AC timing specifications[1]

Parameter	Symbol	Min	Typical	Max	Unit
Transmitter baud rate	T_{BAUD}	10.3125 - 100ppm	10.3125	10.3125 + 100ppm	Gb/s
Unit Interval	UI	-	96.96	-	ps
Deterministic jitter	D_J	-	-	0.155	UI p-p
Total jitter	T_J	-	-	0.30	UI p-p
Notes: 1. For recommended operating conditions, see Table 3.					

3.19.12.3.2 XFI receiver AC timing specifications

This table defines the XFI receiver AC timing specifications. RefClk jitter is not included.

Table 122. XFI receiver AC timing specifications[3]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Receiver baud rate	R_{BAUD}	10.3125 - 100ppm	10.3125	10.3125 + 100ppm	Gb/s	-
Unit Interval	UI	-	96.96	-	ps	-
Total non-EQJ jitter	$T_{NON-EQJ}$	-	-	0.45	UI p-p	1
Total jitter tolerance	T_J	-	-	0.65	UI p-p	1, 2

Table continues on the next page...

Table 122. XFI receiver AC timing specifications[3] (continued)

Parameter	Symbol	Min	Typical	Max	Unit	Notes
1. The total jitter (T_J) consists of Random Jitter (R_J), Duty Cycle Distortion (DCD), Periodic Jitter (P_J), and Inter symbol Interference (ISI). Non-EQJ jitter can include duty cycle distortion (DCD), random jitter (R_J), and periodic jitter (P_J). Non-EQJ jitter is uncorrelated to the primary data stream with exception of the DCD and so cannot be equalized by the receiver under test. It can exhibit a wide spectrum. Non - EQJ = T_J - ISI = R_J + DCD + P_J						
2. The XFI channel has a loss budget of 9.6 dB @5.5GHz. The channel loss including connector @ 5.5GHz is 6dB. The channel crosstalk and reflection margin is 3.6dB. Manual tuning of TX Equalization and amplitude will be required for performance optimization.						
3. For recommended operating conditions, see Table 3.						

This figure shows the sinusoidal jitter tolerance of XFI receiver.

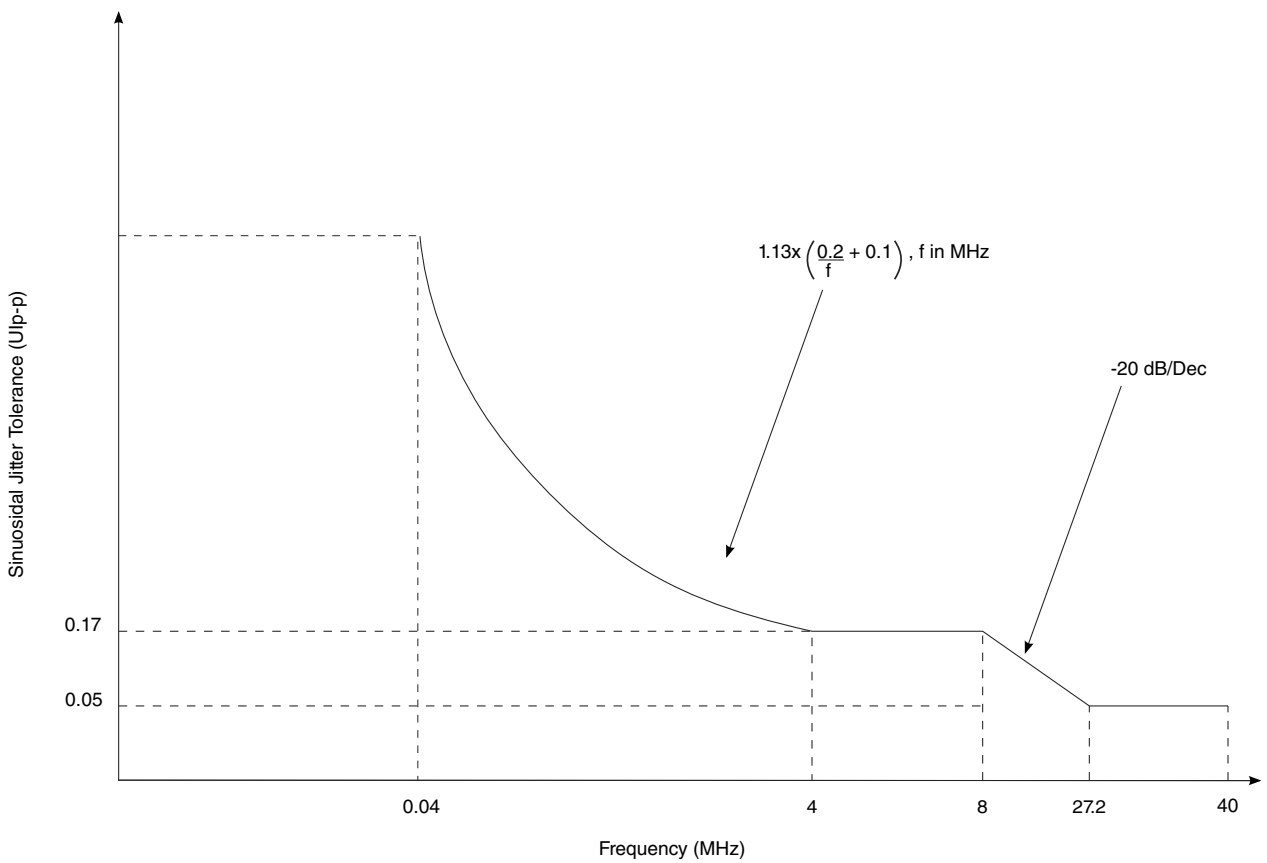


Figure 49. XFI host receiver input sinusoidal jitter tolerance

3.19.13 10GBase-KR interface

This section describes the 10GBase-KR clocking requirements and its DC and AC electrical characteristics.

3.19.13.1 10GBase-KR clocking requirements for SD*n*_REF_CLK*n* and SD*n*_REF_CLK*n*_B

Only SerDes 2 (SD2_REF_CLK[1:2] and SD2_REF_CLK[1:2]_B) may be used for SerDes 10GBase-KR configurations based on the RCW Configuration field SRDS_PRTCL. . The ref clock frequency tolerance spec is ±100ppm.

For more information on these specifications, see SerDes reference clocks .

3.19.13.2 10GBase-KR DC electrical characteristics

This section describes the DC electrical characteristics for 10GBase-KR.

3.19.13.2.1 10GBase-KR transmitter DC electrical characteristics

This table defines the 10GBase-KR transmitter DC electrical characteristics.

Table 123. 10GBaseKR transmitter DC electrical characteristics (XV_{DD} = 1.35V or 1.5V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Output differential voltage	$V_{TX-DIFF}$	800	-	1200	mV	-
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-1.14dB}$	0.6	1.1	1.6	dB	-
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-3.5dB}$	3	3.5	4	dB	-
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-4.66dB}$	4.1	4.6	5.1	dB	-
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-6.0dB}$	5.5	6.0	6.5	dB	-
De-emphasized differential output voltage (ratio)	$V_{TX-DE-RATIO-9.5dB}$	9	9.5	10	dB	-
Differential resistance	T_{RD}	80	100	120	Ω	-
1. For recommended operating conditions, see Table 3.						

3.19.13.2.2 10GBase-KR receiver DC electrical characteristics

This table defines the 10GBase-KR receiver DC electrical characteristics.

Table 124. 10GBase-KR receiver DC electrical characteristics (XV_{DD} = 1.35V or 1.5V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage	$V_{RX-DIFF}$	-	-	1200	mV	-
Differential resistance	R_{RD}	80	-	120	Ω	-
1. For recommended operating conditions, see Table 3.						

3.19.13.3 10GBase-KR AC timing specifications

This section describes the AC timing specifications for 10GBase-KR.

3.19.13.3.1 10GBase-KR transmitter AC timing specifications

This table defines the 10GBase-KR transmitter AC timing specifications. RefClk jitter is not included.

Table 125. 10GBase-KR transmitter AC timing specifications[1]

Parameter	Symbol	Min	Typical	Max	Unit
Transmitter baud rate	T_{BAUD}	10.3125 - 100 ppm	10.3125	10.3125 + 100 ppm	GBd
Deterministic jitter	D_J	-	-	0.155	UI p-p
Total jitter	T_J	-	-	0.30	UI p-p
1. For recommended operating conditions, see Table 3.					

3.19.13.3.2 10GBase-KR receiver AC timing specifications

This table defines the 10GBase-KR receiver AC timing specifications. RefClk jitter is not included.

Table 126. 10GBase-KR receiver AC timing specifications[4,3]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Receiver baud rate	R_{BAUD}	10.3125 - 100 ppm	10.3125	10.3125 + 100 ppm	GBd	-
Random jitter	R_J	-	-	0.130	UI p-p	1
Sinusodial jitter, maximum	S_{J-max}	-	-	0.115	UI p-p	1
Duty cycle distortion	D_{CD}	-	-	0.035	UI p-p	1
Total jitter	T_J	-	-	1.0	UI p-p	1,2
1. The AC specifications do not include Refclk jitter.						
2. The Total applied Jitter Tj = ISI + Rj + DCD + Sj-max where ISI is jitter due to frequency dependent loss.						
3. TX Equalization and amplitude tuning is through software for performance optimization, as in Freescale provided SDKs.						
4. For recommended operating conditions, see Table 3.						

3.19.14 Interlaken interface

This section describes the Interlaken clocking requirements and its DC and AC electrical characteristics.

3.19.14.1 Interlaken clocking requirements for SD*n*_REF_CLK*n* and SD*n*_REF_CLK*n*_B

Only SerDes 3 (SD3_REF_CLK[1:2] and SD3_REF_CLK[1:2]_B) may be used for SerDes Interlaken-LA configurations based on the RCW Configuration field SRDS_PRTCL. The ref clock frequency tolerance spec is ±100ppm.

For more information on these specifications, see SerDes reference clocks.

3.19.14.2 Interlaken-short reach DC electrical characteristics

This section describes the DC electrical characteristics for Interlaken-short reach.

3.19.14.2.1 Interlaken-short reach transmitter DC electrical characteristics

This table defines the Interlaken-short reach transmitter DC electrical characteristics.

Table 127. Interlaken-short reach transmitter DC electrical characteristics (XV_{DD} = 1.35V or 1.5V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Output differential voltage	V_{DIFF}	400	-	750	mV	-
Differential resistance	T_{RD}	80	100	120	Ω	-
Notes: 1. For recommended operating conditions, see Table 3.						

3.19.14.2.2 Interlaken-short reach receiver DC electrical characteristics

This table defines the Interlaken-short reach receiver DC electrical characteristics.

Table 128. Interlaken-short reach receiver DC electrical characteristics (SV_{DD} = 1.0V)[1]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input differential voltage	V_{DIFF}	125	-	1200	mV	-
Differential resistance	R_{RDIN}	80	100	120	Ω	-
Notes: 1. For recommended operating conditions, see Table 3.						

3.19.14.3 Interlaken-short reach AC timing specifications

This section describes the AC timing specifications for Interlaken-short reach.

3.19.14.3.1 Interlaken-short reach transmitter AC timing specifications

This table defines the Interlaken-short reach transmitter AC timing specifications. RefClk jitter is not included.

Table 129. Interlaken-short reach transmitter AC timing specifications[1]

Parameter	Symbol	Min	Typical	Max	Unit
Transmitter baud rate	T_{BAUD}	3.125 - 100ppm	3.125	3.125 + 100ppm	Gbps
Transmitter baud rate	T_{BAUD}	6.25 - 100 ppm	6.25	6.25 + 100 ppm	Gbps
Uncorrelated high probability jitter	T_{UHPJ}	-	-	0.155	UI p-p
Total jitter tolerance	T_J	-	-	0.30	UI p-p
Notes: 1. For recommended operating conditions, see Table 3.					

3.19.14.3.2 Interlaken-short reach receiver AC timing specifications

This table defines the Interlaken-short reach receiver AC timing specifications. RefClk jitter is not included.

Table 130. Interlaken-short reach receiver AC timing specifications[2]

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Receiver baud rate	R_{BAUD}	3.125 - 100 ppm	3.125	3.125 + 100 ppm	Gbps	-
Receiver baud rate	R_{BAUD}	6.25 - 100 ppm	6.25	6.25 + 100 ppm	Gbps	-
Uncorrelated bounded high probability jitter	R_{UBHPJ}	-	-	0.15	UI p-p	-
Correlated bounded high probability jitter	R_{CBHPJ}	-	-	0.30	UI p-p	1
Bounded high probability jitter	R_{BHPJ}	-	-	0.45	UI p-p	-
Sinusoidal jitter, maximum	R_{SJ-max}	-	-	5.00	UI p-p	-
Sinusoidal jitter, high frequency	R_{SJ-hf}	-	-	0.05	UI p-p	-
Total jitter (does not include sinusoidal jitter)	R_{Tj}	-	-	0.60	UI p-p	-
1. The jitter (R_{CBHPJ}) and amplitude have to be correlated, for example, by a PCB trace. 2. For recommended operating conditions, see Table 3.						

The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of this figure.

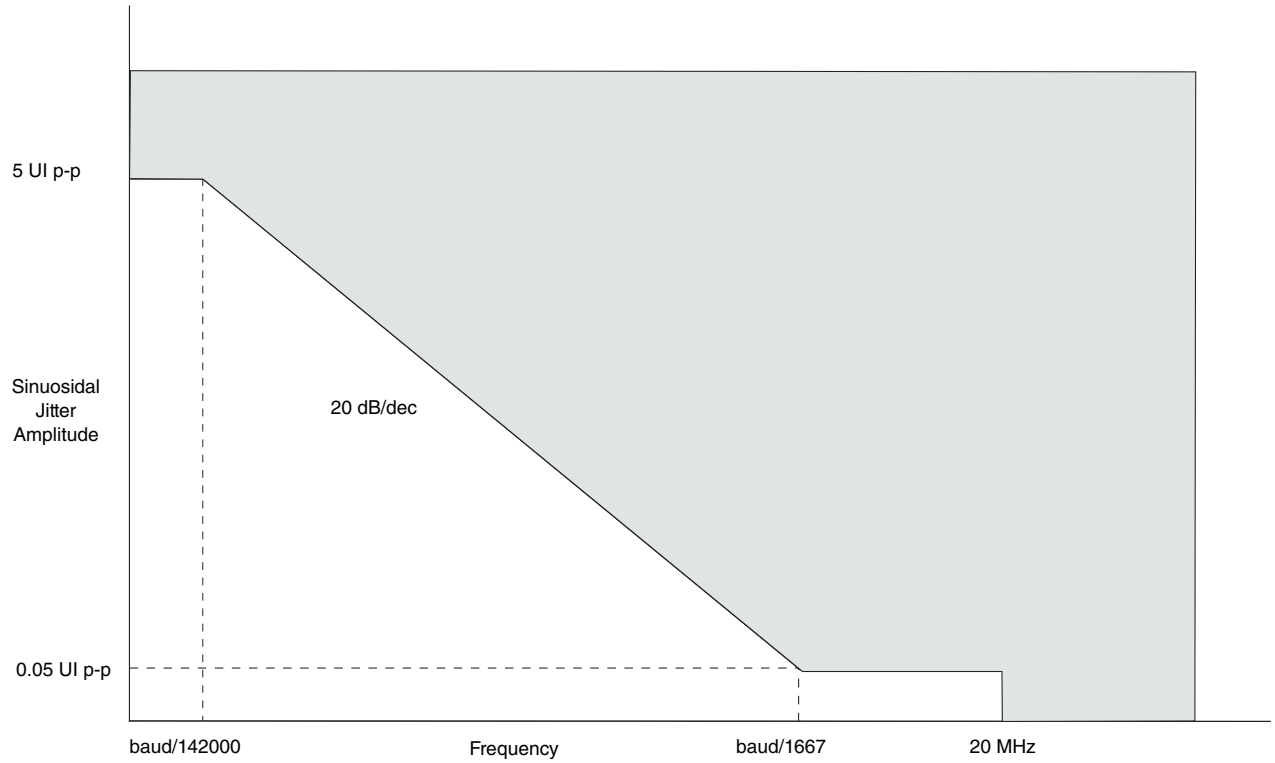


Figure 50. Single-frequency sinusoidal jitter limits

4 Hardware design considerations

4.1 System clocking

This section describes the PLL configuration of the chip.

4.1.1 PLL characteristics

Characteristics of the chip's PLLs include the following:

- There are three selectable core cluster PLLs which generate a clock for each core cluster from the externally supplied SYSCLK input.
  - Core cluster 1 (cores 0-3) can select from cluster group A PLL 1, 2 or 3 (CGA1, 2, 3 PLL)
  - Core cluster 2 (cores 4-7) can select from cluster group A PLL 1, 2 or 3 (CGA1, 2, 3 PLL), not applicable to T4080 parts
  - The frequency ratio between each of the core cluster PLLs and SYSCLK is selected using the configuration bits as described in Core cluster to SYSCLK

PLL ratio. The frequency for each core cluster 1-2 is selected using the configuration bits as described in Table 135 .

- The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Platform to SYSCLK PLL ratio.
- Cluster group A generates an asynchronous clock for PME from cluster group A PLL 1 or cluster group A PLL 2. Described in Frame Manager (FM*n*) clock select.
- Cluster group B generates an asynchronous clock for FMan 1 and FMan 2 from the platform PLL, cluster group B PLL 1, or cluster group B PLL 2. Described in Frame Manager (FM*n*) clock select.
- The DDR block PLL generates an asynchronous DDR clock from the externally supplied DDRCLK input. The frequency ratio is selected using the Memory Controller Complex PLL multiplier/ratio configuration bits as described in DDR controller PLL ratios.
- Each of the four SerDes blocks has 2 PLLs which generate a core clock from their respective externally supplied SD*n*_REF_CLK*n*/SD*n*_REF_CLK*n*_B inputs. The frequency ratio is selected using the SerDes PLL RCW configuration bits as described in SerDes PLL ratio.

4.1.2 Clock ranges

This table provides the clocking specifications for the processor core, platform, memory, and integrated flash controller.

Table 131. Processor, platform, and memory clocking specifications

Characteristic	Maximum processor core frequency						Unit	Notes
	1500 MHz		1667 MHz		1800 MHz			
	Min	Max	Min	Max	Min	Max		
Core cluster group PLL frequency	1000	1500	1000	1667	1000	1800	MHz	1, 2
Core cluster frequency	See note 2	1500	See note 2	1667	See note 2	1800	MHz	2
Platform clock frequency	400	667	400	733	400	733	MHz	1, 7
Memory bus clock frequency	533	800	533	933.333	533	933.333	MHz	1, 3, 4
IFC clock frequency	—	100	—	100	—	100	MHz	5
PME	See note 6	500	See note 6	550	See note 6	550	MHz	6
FM*n*	450/667	667	450/667	733	450/667	733	MHz	8

1. **Caution:**The platform clock to SYSCLK ratio and core to SYSCLK ratio settings must be chosen such that the resulting SYSCLK frequency, core frequency, and platform clock frequency do not exceed their respective maximum or minimum operating frequencies.

Table 131. Processor, platform, and memory clocking specifications

Characteristic	Maximum processor core frequency						Unit	Notes
	1500 MHz		1667 MHz		1800 MHz			
	Min	Max	Min	Max	Min	Max		
2. The core cluster can run at cluster group PLL/1, PLL/2, or PLL/4. For the PLL/1 case, the minimum frequency is 1000 MHz. With a minimum cluster group PLL frequency of 1000 MHz, this results in a minimum allowable core cluster frequency of 500 MHz for PLL/2. For the PLL/4 case, the minimum allowable core cluster frequency is platform clock frequency / 2. For the case of the minimum platform frequency = 400 MHz, the minimum core cluster frequency is 200 MHz. 3. The memory bus clock speed is half the DDR3/DDR3L data rate. DDR3/3L memory bus clock frequency is limited to min = 533 MHz. 4. The memory bus clock speed is dictated by its own PLL. 5. The integrated flash controller (IFC) clock speed on IFC_CLK[0:2] is determined by the IFC module input clock (platform clock / 2) divided by the IFC ratio programmed in CCR[CLKDIV]. See the chip reference manual for more information. 6. The PME minimum frequency is Platform Frequency / 2. For the case of the minimum platform frequency = 400 MHz, the minimum PME frequency is 200 MHz. 7. The minimum platform frequency should meet the requirements in Minimum platform frequency requirements for high-speed interfaces. For SRIO proper operations the FMAN minimum frequency has to be equal to 528 MHz. 8. If all MACs operate using RGMII or SGMII at 1.25 G, then the minimum required FMAN frequency is 450 MHz. Also, If any MAC operates at a higher rate then the minimum FMAN is 667 MHZ.								

4.1.2.1 DDR clock ranges

The DDR memory controller can run only in asynchronous mode, where the memory bus is clocked with the clock provided on the DDRCLK input pin, which has its own dedicated PLL.

This table provides the clocking specifications for the memory bus.

Table 132. Memory bus clocking specifications

Characteristic	Min	Max	Unit	Notes
Memory bus clock frequency	533	933.3333	MHz	1, 2, 3
Notes: 1. **Caution:** The platform clock to SYSCLK ratio and core to platform clock ratio settings must be chosen such that the resulting SYSCLK frequency, core frequency, and platform frequency do not exceed their respective maximum or minimum operating frequencies. See Platform to SYSCLK PLL ratio, and Core cluster to SYSCLK PLL ratio, and DDR controller PLL ratios, for ratio settings. 2. The memory bus clock refers to the chip's memory controllers' Dn_MCK[0:3] and Dn_MCK[0:3]_B output clocks, running at half of the DDR data rate. 3. The memory bus clock speed is dictated by its own PLL. See DDR controller PLL ratios.				

4.1.3 Platform to SYSCLK PLL ratio

This table lists the allowed platform clock to SYSCLK ratios.

Because the DDR operates asynchronously, the memory-bus clock-frequency is decoupled from the platform bus frequency.

For all valid platform frequencies supported on this chip, set the RCW Configuration field SYS_PLL_CFG = 0b00.

Table 133. Platform to SYSCLK PLL ratios

Binary Value of SYS_PLL_RAT	Platform:SYSCLK Ratio
0_0011	3:1
0_0100	4:1
0_0101	5:1
0_0110	6:1
0_0111	7:1
0_1000	8:1
0_1001	9:1
0_1010	10:1
0_1011	11:1
0_1100	12:1
0_1101	13:1
0_1110	14:1
0_1111	15:1
1_0000	16:1
All Others	Reserved

4.1.4 Core cluster to SYSCLK PLL ratio

The clock ratio between SYSCLK and each of the core cluster PLLs is determined by the binary value of the RCW Configuration field CG*m*_PLL*n*_RAT. This table describes the supported ratios. For all valid core cluster frequencies supported on this chip, set the RCW Configuration field CG*n*_PLL_CFG = 0b00.

This table lists the supported asynchronous core cluster to SYSCLK ratios.

Table 134. Core cluster PLL to SYSCLK ratios

Binary value of CG*m*_PLL*n*_RAT	Core cluster:SYSCLK Ratio
00_1000	8:1
00_1001	9:1

Table continues on the next page...

Table 134. Core cluster PLL to SYSCLK ratios (continued)

Binary value of CG*m*_PLL*n*_RAT	Core cluster:SYSCLK Ratio
00_1010	10:1
00_1011	11:1
00_1100	12:1
00_1101	13:1
00_1110	14:1
00_1111	15:1
01_0000	16:1
01_0010	18:1
01_0100	20:1
01_0110	22:1
01_1001	25:1
01_1010	26:1
01_1011	27:1
All others	Reserved

4.1.5 Core complex PLL select

The clock frequency of each core cluster is determined by the binary value of the RCW Configuration field C*n*_PLL_SEL. These tables describe the selections available to each core cluster, where each individual core cluster can select a frequency from their respective tables.

NOTE

There is a restriction that requires that the frequency provided to the e6500 core cluster after any dividers must always be greater than half of the platform frequency. Special care must be used when selecting the /2 or /4 outputs of a cluster PLL in which this restriction is observed.

Table 135. Core cluster [1-2] PLL select

Binary Value of C*n*_PLL_SEL for *n* = 1-2	Core cluster ratio
0000	CGA PLL1/1
0001	CGA PLL1/2
0010	CGA PLL1/4
0100	CGA PLL2/1
0101	CGA PLL2/2
0110	CGA PLL2/4

Table continues on the next page...

Table 135. Core cluster [1-2] PLL select (continued)

Binary Value of C*n*_PLL_SEL for *n* = 1-2	Core cluster ratio
1000	CGA PLL3/1
1001	CGA PLL3/2
1010	CGA PLL3/4
All Others	Reserved

4.1.6 DDR controller PLL ratios

The two DDR memory controller complexes operate asynchronous to the platform. All DDR controllers operate at the same frequency configuration.

In asynchronous DDR mode, the DDR data rate to DDRCLK ratios supported are listed in the following table. This ratio is determined by the binary value of the RCW Configuration field MEM_PLL_RAT (bits 10-15).

The RCW Configuration field MEM_PLL_CFG (bits 8-9) must be set to MEM_PLL_CFG = 0b00 for all valid DDR PLL reference clock frequencies supported on this chip.

Table 136. DDR data Rate to DDRCLK ratios[1]

Binary value of MEM_PLL_RAT		Decimal values of MEM_PLL_RAT		DDR data rate to DDRCLK Ratio value	Resulting DDR data-rate (MT/s)			
Rev 1 silicon	Rev 2 silicon	Rev 1 silicon	Rev 2 silicon		Examples of DDRCLK frequency values that give typical DDR data rata values at Ratio value			
					66.6667 MHz	100 MHz	125 MHz	133.333 MHz
00_1010	00_0101	10	5	10				1333.333
00_1100	00_0110	12	6	12			1500	1600
00_1110	00_0111	14	7	14			1750	1866.667
01_0000	00_1000	16	8	16	1066.667	1600		
01_0010	00_1001	18	9	18		1800		
01_0100	00_1010	20	10	20	1333.333			
All Others	All Others	Reserved	Reserved	Reserved				

Notes:

1. This table shows examples of standard DDR data rate resulted from multiplying the MEM_PLL_RAT by some common DDRCLK frequencies like 66.66MHZ, 100MHz, or 133MHZ. Customers can supply of course different DDRCLK frequency from the common ones presented in this table and thus they have to pick up the correct MEM_PLL_RAT value that will give them a common DDR data rate and always use a value for Rev2 silicon that is half of what is supposed to be given in Rev1 or simply in rev2 MEM_PLL_RAT = 0.5 * DDR data rate/ DDRCLK.

4.1.7 SerDes PLL ratio

The clock ratio between each of the three SerDes PLLs and their respective externally supplied SD*n*_REF_CLK*n*/SD*n*_REF_CLK*n*_B inputs is determined by a set of RCW Configuration fields-SRDS_PRTCL_S*n*, SRDS_PLL_REF_CLK_SEL_S*n*, and SRDS_DIV_*_S*n*-as shown in this table.

Table 137. Valid SerDes RCW encodings and reference clocks

SerDes protocol (given lane)	Valid reference clock frequency	Legal setting for SRDS_PRTCL_S*n*	Legal setting for SRDS_PLL_REF_CLK_SEL_S*n*	Legal setting for SRDS_DIV_*_S*n*	Notes
High-speed serial and debug interfaces					
PCI Express 2.5 GT/s	100 MHz	Any PCIe	0b0: 100 MHz	2b10: 2.5 G	1
(doesn't negotiate upwards)	125 MHz		0b1: 125 MHz		1
PCI Express 5 GT/s	100 MHz	Any PCIe	0b0: 100 MHz	2b01: 5.0 G	1
(can negotiate up to 5 GT/s)	125 MHz		0b1: 125 MHz		1
PCI Express 8 GT/s	100 MHz	Any PCIe	0b0: 100 MHz	2b00: 8.0 G	1
(can negotiate up to 8 GT/s)	125 MHz		0b1: 125 MHz		1
Serial RapidIO 2.5 Gbaud	100 MHz	SRIO @ 2.5/5 Gbaud	0b0: 100 MHz	0b1: 2.5 G	-
	125 MHz		0b1: 125 MHz		-
Serial RapidIO 3.125 Gbaud	125 MHz	SRIO @ 3.125 Gbaud	0b0: 125 MHz	Don't care	-
	156.25 MHz		0b1: 156.25 MHz		-
Serial RapidIO 5 Gbaud	100 MHz	SRIO @ 2.5/5 Gbaud	0b0: 100 MHz	0b0: 5.0 G	-
	125 MHz		0b1: 125 MHz		-
Interlaken Lookaside (6.25 Gbps)	125 MHz	Interlaken LA @ 6.25 Gbps	0b0: 125 MHz	Don't care	-
	156.25 MHz		0b1: 156.25 MHz		-
Interlaken Lookaside (10.3125 Gbps)	156.25 MHz	Interlaken LA @ 10.3125 Gbps	0b0: 156.25 MHz	Don't care	-
	161.1328125 MHz		0b1: 161.1328125 MHz		-
SATA (1.5 or 3 Gbps)	100 MHz	Any SATA	0b0: 100 MHz	Don't care	2
	125 MHz		0b1: 125 MHz		
Debug (2.5 Gbps)	100 MHz	Aurora @ 2.5/5 Gbps	0b0: 100 MHz	0b1: 2.5 G	-
	125 MHz		0b1: 125 MHz		-
Debug (3.125 Gbps)	125 MHz	Aurora @ 3.125 Gbps	0b0: 125 MHz	Don't Care	-
	156.25 MHz		0b1: 156.25 MHz		-
Debug (5 Gbps)	100 MHz	Aurora @ 2.5/5 Gbps	0b0: 100 MHz	0b0: 5.0 G	-
	125 MHz		0b1: 125 MHz		-
Networking interfaces					
SGMII (1.25 Gbaud)	100 MHz	SGMII @ 1.25 Gbaud	0b0: 100 MHz	Don't care	-
	125 MHz		0b1: 125 MHz		-

Table continues on the next page...

Table 137. Valid SerDes RCW encodings and reference clocks (continued)

SerDes protocol (given lane)	Valid reference clock frequency	Legal setting for SRDS_PRTCL_S*n*	Legal setting for SRDS_PLL_REF_CLK_SEL_S*n*	Legal setting for SRDS_DIV_*_S*n*	Notes
2.5x SGMII (3.125 Gbaud)	125 MHz	SGMII @ 3.125 Gbaud	0b0: 125 MHz	Don't care	-
	156.25 MHz		0b1: 156.25 MHz		-
QSGMII (5.0 Gbps)	100 MHz	Any QSGMII	0b0: 100 MHz	0b0: 5.0 G	-
	125 MHz		0b1: 125 MHz		-
XAUI (3.125 Gb/s)	125 MHz	XAUI @ 3.125 Gb/s	0b0: 125 MHz	Don't care	-
	156.25 MHz		0b1: 156.25 MHz		-
HiGig or HiGig2 (3.125 Gbps)	125 MHz	HiGig @ 3.125 Gbps	0b0: 125 MHz	Don't care	-
	156.25 MHz		0b1: 156.25 MHz		-
HiGig or HiGig2 (3.75 Gbps)	125 MHz	HiGig @ 3.75 Gbps	0b0: 125 MHz	Don't care	-
	156.25 MHz		0b1: 156.25 MHz		-
XFI (10.3125 Gbps)	156.25 MHz	XFI @ 10.3125 Gbps	0b0: 156.25 MHz	Don't care	-
10GBase-KR (10.3125 GBd)	156.25 MHz	10GBase-KR @ 10.3125 GBd	0b0: 156.25 MHz	Don't care	-

1. A spread-spectrum reference clock is permitted for PCI Express. However, if any other high-speed interfaces such as sRIO, Interlaken, SATA, SGMII, SGMII 2.5x, QSGMII, XAUI, XFI, 10GBase-KR, HiGig/HiGig2 or Aurora are used concurrently on the same SerDes bank, spread-spectrum clocking is not permitted.

2. SerDes lanes configured as SATA initially operate at 3.0 Gbps. 1.5 Gbps operation may later be enabled through the SATA IP itself. It is possible for software to set each SATA at different rates.

4.1.8 Frame Manager (FM*n*) clock select

The following tables describe the clocking options that may be applied to each FM. The clock selection is determined by the binary value of the RCW Clocking Configuration fields HWA_CGB_M1_CLK_SEL and HWA_CGB_M2_CLK_SEL.

Table 138. Frame Manager (FMn) clock select

Binary value of HWA_CGB_Mn_CLK_SEL	Frame Manager (FM1) clock select[1]	Frame Manager (FM2) clock select[1]
000b, 001b	Reserved	Reserved
010b	Cluster group B PLL 1/2	Cluster group B PLL 2/2
011b	Cluster group B PLL 1/3	Cluster group B PLL 2/3
100b	Cluster group B PLL 1/4	Cluster group B PLL 2/4
101b	Platform clock frequency/1	Platform clock frequency/1
110b	Cluster group B PLL 2/2	Cluster group B PLL 1/2
111b	Reserved	Cluster group B PLL 1/3
1. For max frequency, see Table 131 .		

4.1.9 Pattern Matching Engine (PME) clock select

The PME can be synchronous with or asynchronous to the platform, depending on configuration.

This table describes the clocking options that may be applied to the PME. The clock selection is determined by the binary value of the RCW Clocking Configuration field HWA_CGA_M1_CLK_SEL.

Table 139. Pattern Matching Engine clock select

Binary Value of HWA_CGA_M1_CLK_SEL	PME Frequency [1]
000b	Platform clock frequency/2 (synchronous mode)
001b	Reserved
010b	Cluster group A PLL 1/2 (Asynchronous mode)
011b	Cluster group A PLL 1/3 (Asynchronous mode)
100b	Cluster group A PLL 1/4 (Asynchronous mode)
101b	Reserved
110b	Cluster group A PLL 2/2 (Asynchronous mode)
111b	Cluster group A PLL 2/3 (Asynchronous mode)
Note: 1. For asynchronous mode, max frequency, see Table 131.	

4.1.10 Frequency options

This section discusses interface frequency options.

4.1.10.1 SYSCLK and core cluster frequency options

This table shows the expected frequency options for SYSCLK and core cluster frequencies.

Table 140. SYSCLK and core cluster frequency options

Core cluster: SYSCLK Ratio[2]	SYSCLK (MHz) [2]		
	66.67	100.00	133.33
	Core cluster Frequency (MHz)[1]		
8:1			1067
9:1			1200
10:1		1000	1333

Table continues on the next page...

Table 140. SYSCLK and core cluster frequency options (continued)

Core cluster: SYSCLK Ratio[2]	SYSCLK (MHz) [2]		
	66.67	100.00	133.33
	Core cluster Frequency (MHz)[1]		
11:1		1100	1467
12:1		1200	1600
13:1			
14:1		1400	
15:1	1000	1500	
16:1	1067	1600	
18:1	1200	1800	
20:1	1333		
22:1	1467		
25:1	1667		
26:1			
27:1	1800		

Notes:

1. Core cluster frequency values are shown rounded up to the nearest whole number (decimal place accuracy removed)
2. Example values.

4.1.10.2 SYSCLK and platform frequency options

This table shows the expected frequency options for SYSCLK and platform frequencies.

Table 141. SYSCLK and platform frequency options

Platform: SYSCLK Ratio[3]	SYSCLK (MHz)[3]		
	66.67	100.00	133.33
	Platform Frequency (MHz)[1]		
4:1		400	533
5:1			667
6:1	400[2]	600	
7:1		700	
8:1	533		
9:1	600		
10:1	667		
11:1	733		
12:1			

Notes:

1. Platform frequency values are shown rounded up to the nearest whole number (decimal place accuracy removed)

Table 141. SYSCLK and platform frequency options

Platform: SYSCLK Ratio[3]	SYSCLK (MHz)[3]		
	66.67	100.00	133.33
	Platform Frequency (MHz)[1]		
2. A minimum platform clock frequency requirement is 528MHz if x4 SRIO is used.			
3.Example values.			

4.1.10.3 DDRCLK and DDR data rate frequency options

This table shows the expected frequency options for DDRCLK and DDR data rate frequencies.

Table 142. DDRCLK and DDR data rate frequency options

DDR data rate: DDRCLK Ratio[2]	DDRCLK (MHz)[2]			
	66.67	100.00	125.00	133.33
	DDR Data Rate (MT/s)[1]			
10:1				1333
12:1			1500	1600
14:1			1750	1866
16:1	1067	1600		
18:1		1800		
20:1	1333			
Notes:				
1. DDR data rate values are shown rounded up to the nearest whole number (decimal place accuracy removed).				
2. Example values.				

4.1.10.4 SYSCLK and FMan frequency options

These table shows the expected frequency options for SYSCLK and FMan frequencies.

Table 143. SYSCLK and FMan frequency options (clocked by CGB PLLn / 2)

Core cluster: SYSCLK Ratio[3]	SYSCLK (MHz)[3]		
	66.67	100.00	133.33
	FMan Frequency (MHz)[1, 2]		
8:1			533
9:1			600
10:1		500	667
11:1		550	733
12:1		600	

Table continues on the next page...

Table 143. SYSCLK and FMan frequency options (clocked by CGB PLLn / 2) (continued)

Core cluster: SYSCLK Ratio[3]	SYSCLK (MHz)[3]		
	66.67	100.00	133.33
	FMan Frequency (MHz)[1, 2]		
13:1			
14:1		700	
15:1	500	750	
16:1	533		
18:1	600		
20:1	667		
22:1	733		
25:1			
26:1			
27:1			

Notes:

1. FMan frequency values are shown rounded up to the nearest whole number (decimal place accuracy removed).
2. For min frequency, see Table 131.
3. Example values.

Table 144. SYSCLK and FMan frequency options (clocked by CGB PLLn / 3)

Core cluster: SYSCLK Ratio[3]	SYSCLK (MHz)[3]		
	66.67	100.00	133.33
	FMan Frequency (MHz)[1, 2]		
8:1			
9:1			
10:1			
11:1			489
12:1			533
13:1			578
14:1		467	
15:1		500	
16:1		533	
18:1		600	
20:1			
22:1	489		
25:1	556		
26:1	578		
27:1	600		

Notes:

Table 144. SYSCLK and FMan frequency options (clocked by CGB PLLn / 3)

Core cluster: SYSCLK Ratio[3]	SYSCLK (MHz)[3]		
	66.67	100.00	133.33
	FMan Frequency (MHz)[1, 2]		

1. FMan frequency values are shown rounded up to the nearest whole number (decimal place accuracy removed)
2. For min frequency, see Table 131
3. Example values.

Table 145. SYSCLK and FMan frequency options (clocked by CGB PLL1 / 4)

Core cluster: SYSCLK Ratio[3]	SYSCLK (MHz)[3]		
	66.67	100.00	133.33
	FMan Frequency (MHz)[1, 2]		
8:1			
9:1			
10:1			
11:1			
12:1			
13:1			
14:1			
15:1			
16:1			
18:1		450	
20:1			
22:1			
25:1			
26:1			
27:1	450		

Notes:

1. FMan frequency values are shown rounded up to the nearest whole number (decimal place accuracy removed).
2. For min frequency, see Table 131.
3. Example values.

Table 146. SYSCLK and FMan frequency options (clocked by platform frequency/1)

Platform: SYSCLK Ratio[3]	SYSCLK (MHz)[3]		
	66.67	100.00	133.33
	FMan Frequency (MHz)[1, 2]		
4:1			533
5:1			667
6:1		600	

Table continues on the next page...

Table 146. SYSCLK and FMan frequency options (clocked by platform frequency/1) (continued)

Platform: SYSCLK Ratio[3]	SYSCLK (MHz)[3]		
	66.67	100.00	133.33
	FMan Frequency (MHz)[1, 2]		
7:1		700	
8:1	533		
9:1	600		
10:1	667		
11:1	733		
12:1			

Notes:

1. FMan frequency values are shown rounded up to the nearest whole number (decimal place accuracy removed).
2. For min frequency, see Table 131.
3. Example values.

4.1.10.5 SYSCLK and PME frequency options

These table shows the expected frequency options for SYSCLK and PME frequencies.

Table 147. SYSCLK and PME frequency options (clocked by CGA PLLn / 2)

Core cluster: SYSCLK Ratio[2]	SYSCLK (MHz)[2]		
	66.67	100.00	133.33
	PME Frequency (MHz)[1]		
8:1			533
9:1			600
10:1		500	
11:1		550	
12:1		600	
13:1			
14:1			
15:1	500		
16:1	533		
18:1	600		
20:1			
22:1			
25:1			
26:1			
27:1			

Notes:

Table 147. SYSCLK and PME frequency options (clocked by CGA PLLn / 2)

Core cluster: SYSCLK Ratio[2]	SYSCLK (MHz)[2]		
	66.67	100.00	133.33
	PME Frequency (MHz)[1]		

1. PME frequency values are shown rounded up to the nearest whole number (decimal place accuracy removed).
2. Example values.

Table 148. SYSCLK and PME frequency options (clocked by CGA PLLn / 3)

Core cluster: SYSCLK Ratio[2]	SYSCLK (MHz)[2]		
	66.67	100.00	133.33
	PME Frequency (MHz)[1]		
8:1			
9:1			400
10:1			444
11:1			489
12:1		400	533
13:1			578
14:1		467	
15:1		500	
16:1		533	
18:1	400	600	
20:1	444		
22:1	489		
25:1	556		
26:1	578		
27:1	600		

Notes:
1. PME frequency values are shown rounded up to the nearest whole number (decimal place accuracy removed).
2. Example values.

Table 149. SYSCLK and PME frequency options (clocked by platform frequency/2)

Platform: SYSCLK Ratio[2]	SYSCLK (MHz)[2]		
	66.67	100.00	133.33
	PME Frequency (MHz)[1]		
4:1		200	267
5:1			334
6:1	200	300	400
7:1		350	
8:1	267	400	

Table continues on the next page...

Table 149. SYSCLK and PME frequency options (clocked by platform frequency/2) (continued)

Platform: SYSCLK Ratio[2]	SYSCLK (MHz)[2]		
	66.67	100.00	133.33
	PME Frequency (MHz)[1]		
9:1	300		
10:1	334		
11:1	367		
12:1	400		

Notes:

1. PME frequency values are shown rounded up to the nearest whole number (decimal place accuracy removed).
2. Example values.

4.1.10.6 Minimum platform frequency requirements for high-speed interfaces

The platform clock frequency must be considered for proper operation of high-speed interfaces as described below.

For proper PCI Express operation, the platform clock frequency must be greater than or equal to:

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{16}$$

Figure 51. Gen 1 PEX minimum platform frequency

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{8}$$

Figure 52. Gen 2 PEX minimum platform frequency

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{4}$$

Figure 53. Gen 3 PEX minimum platform frequency

See section "Link Width," in the chip reference manual for PCI Express interface width details. Note that "PCI Express link width" in the above equation refers to the negotiated link width as the result of PCI Express link training, which may or may not be the same as the link width POR selection. It refers to the widest port in use, not the combined

width of the number ports in use. For instance, if two x4 PCIe Gen3 ports are in use, 527MHz platform frequency is needed to support by using Gen 3 equation (527 x 4 / 4, not 527 x 4 x 2 / 4).

4.2 Power supply design

4.2.1 Voltage ID (VID) controllable supply

To guarantee performance and power specifications, a specific method of selecting the optimum voltage-level must be implemented when the chip is used. As part of the chip's boot process, software must read the VID efuse values stored in the Fuse Status register (FUSESR) and then configure the external voltage regulator based on this information. This method requires a point of load voltage regulator for each chip.

NOTE

During the power-on reset process, the fuse values are read and stored in the FUSESR. It is expected that the chip's boot code reads the FUSESR value very early in the boot sequence and updates the regulator accordingly.

The default voltage regulator setting that is safe for the system to boot is the recommended operating V_{DD} at initial start-up of 1.025 V. It is highly recommended to select a regulator with a Vout range of at least 0.9 V to 1.1 V, with a resolution of 12.5 mV or better, when implementing a VID solution. If the VID for a specific part is already known at initial start-up, it is acceptable to program the voltage regulator to the VID value. The device does not require an initial voltage of 1.025V at start-up.

The table below lists the valid VID efuse values that will be programmed at the factory for this chip.

Table 150. Fuse Status Register (DCFG_CCSR_FUSESR)

Binary value of DA_V / DA_ALT_V	V_{DD} voltage
00001	0.9875 V
00010	0.9750 V
10000	1.0000 V
10001	1.0125 V
10010	1.0250 V
All other values	See the complete list in the Fuse Status Register (DCFG_CCSR_FUSESR) section of the chip reference manual.

If DA_ALT_V is not all zeros, then software should read DA_ALT_V for the VID value and not the DA_V. For additional information on VID, please see the chip reference manual.

4.2.1.1 Options for system design

There are several widely-accepted options available to the system designer for obtaining the benefits of a VID solution. The most common option is to use the VID solution to drive a system's controllable voltage-regulators through a sideband interface such as a simple parallel bus or PMBus interface. PMbus is similar to I^2C but with extensions to improve robustness and address shortcomings of I^2C; the PMBus specification can be found at www.pmbus.org. The simple parallel bus is supported by the chip through GPIO pins and the PMBus interface is supported by an I^2C interface. Other VID solutions may be to access an FPGA/ASIC or separate power management chip through the IFC, SPI, or other chip-specific interface, where the other device then manages the voltage regulator. The method chosen for implementing the chip-specific voltage in the system is decided by the user.

4.2.1.1.1 Example 1: Regulators supporting parallel bus configuration

In this example, a user builds a VID solution using controllable regulators with a parallel bus. In this implementation, the user chooses to utilize any subset of the available GPIO pins on the chip except those noted below.

NOTE

GPIO pins that are muxed on an interface used by the application for loading RCW information are not available for VID use.

It is recommended that all GPIO pins used for VID are located in the same 32-bit GPIO IP block so that all bits can be accessed with a single read or write.

The general procedure for setting the core voltage regulator to the desired operating voltage is as follows:

1. The GPIO pins are released to high-impedance at POR. Because GPIO pins default to being inputs, they do not begin automatically driving after POR, and only work as outputs under software control.
2. The board is responsible for a default voltage regulator setting that is "safe" for the system to boot. To achieve this, the user puts pull-up and/or pull-down resistors on the GPIO pins as needed for that specific system. For the case where the regulator's interface operates at a different voltage than OV_{DD}, the chip's GPIO module can be operated in an open drain configuration.

3. There is no direct connection between the Fuse Status Register (FUSESR) and the chip's pins. As part of the chip's boot process, software must read the efuse values stored in the FUSESR and then configure the voltage regulator based on this information. The software determines the proper value for the parallel interface and writes it to the GPIO block data (GPDAT) register. It then changes the GPIO direction (GPDIR) register from input to output to drive the new value on the device pins, thus overriding the board configuration default value. Note that some regulators may require a series of writes so that the voltage is slowly stepped from its old to its new value.
4. When the voltage has stabilized, software adjusts the operating frequencies as desired.

Upon completion of configuration, some regulators may have a write-protect pin to prevent undesired data changes after configuration is complete. A single GPIO pin on the chip could be allocated for this task if desired.

4.2.1.1.2 Example 2: Regulators supporting PMBus configuration

In this example, a user builds a VID solution using controllable regulators with a PMBus interface. For the case where the regulator's interface operates at a different voltage than DV_{DD}, the chip's I^2C module can be operated in an open-drain configuration.

In this implementation, the user chooses to utilize any I^2C interface available on the chip. These regulators have a means for setting a safe, default, operating value either through strapping pins or through a default, non-volatile store.

NOTE

If I^2C1 controller is selected, it is important that its calling address is different than the 7-bit value of 0x50h used by the pre-boot loader (PBL) for RCW and pre-boot initialization.

The general procedure for setting the core voltage regulator to the desired operating voltage is as follows:

1. The board is responsible for configuring a safe default value for the controllable regulator either through dedicated pins or its non-volatile store.
2. As part of the chip's boot process, software must read the efuse values stored in the FUSESR register and then configure the voltage regulator based on this information. The software decides on a new configuration and sends this value across the I^2C interface connected to the regulator's PMBus interface. Note that some regulators may require a series of writes so that the voltage is slowly stepped from its old to its new value.
3. When the voltage has stabilized, software adjusts the operating frequencies as desired.

Upon completion of configuration, some regulators may have a write-protect pin to prevent undesired data changes after configuration is complete. A single GPIO pin on the chip could be allocated for this task, if desired.

4.2.1.1.3 Example 3: Regulators supporting FPGA/ASIC or separate power management device configuration

In this example, a user builds a VID solution using controllable regulators that are managed by a FPGA/ASIC or a separate power-management device. In this implementation, the user chooses to utilize the IFC, eSPI or any other available chip interface to connect to the power-management device.

The general procedure for setting the core voltage regulator to the desired operating voltage is as follows:

1. The board is responsible for configuring a safe default value for the controllable regulator either through dedicated pins or its non-volatile store.
2. As part of the chip's boot process, software must read the efuse values stored in the FUSESR and then configure the voltage regulator based on this information. The software decides on a new configuration and sends this value across the IFC, eSPI, or any other interface that is used to connect to the FPGA/ASIC or separate power-management device that manages the regulator. Note that some regulators may require a series of writes so that the voltage is slowly stepped from its old to its new value.
3. When the voltage has stabilized, software adjusts the operating frequencies as desired.

Upon completion of configuration, some regulators may have a write-protect pin to prevent undesired data changes after configuration is complete. A single GPIO pin on the chip could be allocated for this task, if desired.

4.2.2 Core and platform supply voltage filtering

The V_{DD} supply is normally derived from a high current capacity linear or switching power supply which can regulate its output voltage very accurately despite changes in current demand from the chip within the regulator's relatively low bandwidth. Several bulk decoupling capacitors must be distributed around the PCB to supply transient current demand above the bandwidth of the voltage regulator.

These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. However, customers should work directly with their power regulator vendor for best values and types of bulk capacitors.

As a guideline for customers and their power regulator vendors, NXP recommends that these bulk capacitors be chosen to maintain the positive transient power surges to less than VID+50 mV (except that a positive transient of up to +100 mV can be tolerated for less than 1 us, negative transient undershoot should comply with specification of VID-30mV) for current steps of up to 20A for 12 cores, 15A for 8 cores and 10A for 4 cores with a slew rate of 12 A/us.

These bulk decoupling capacitors will ideally supply a stable voltage for current transients into the megahertz range. Above that, see Decoupling recommendations for further decoupling recommendations.

4.2.3 PLL power supply filtering

Each of the PLLs described in System clocking is provided with power through independent power supply pins (AV_{DD}_PLAT, A_{VDD}_CGAn, A_{VDD}_CGBn and AV_{DD}_Dn and AV_{DD}_SDn_PLLn). AV_{DD}_PLAT, A_{VDD}_CGAn, A_{VDD}_CGBn and AV_{DD}_Dn voltages must be derived directly from a 1.8 V voltage source through a low frequency filter scheme. AV_{DD}_SDn_PLLn voltages must be derived directly from the XnV_{DD} source through a low frequency filter scheme. The recommended solution for PLL filtering is to provide independent filter circuits per PLL power supply, as illustrated in Figure 54, one for each of the AV_{DD} pins. By providing independent filters to each PLL, the opportunity to cause noise injection from one PLL to the other is reduced. This circuit is intended to filter noise in the PLL's resonant frequency range from a 500 kHz to 10 MHz range.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the footprint, without the inductance of vias.

This figure shows the PLL power supply filter circuit.

Where:

- R = 5 Ω ± 5%
- C1 = 10 µF ± 10%, 0603, X5R, with ESL ≤ 0.5 nH
- C2 = 1.0 µF ± 10%, 0402, X5R, with ESL ≤ 0.5 nH

NOTE

A higher capacitance value for C2 may be used to improve the filter as long as the other C2 parameters do not change (0402 body, X5R, ESL ≤ 0.5 nH).

NOTE

Keep filter close to pin. Voltage and tolerance for AV_{DD} is defined at the input of the PLL supply filter and not the pin of AV_{DD}.

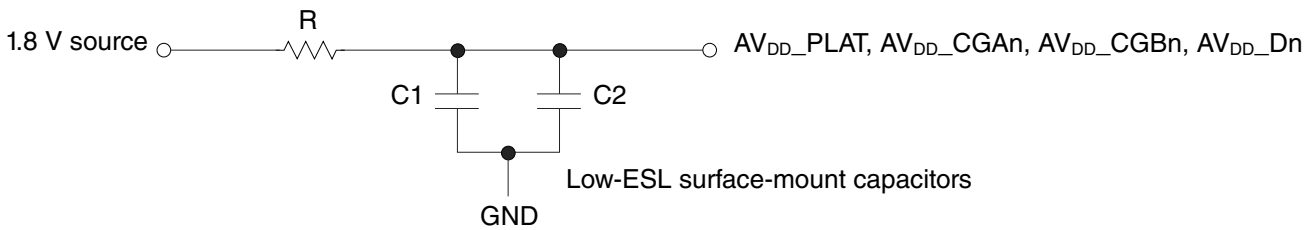


Figure 54. PLL power supply filter circuit

The AV_{DD}_SDn_PLLn signals provide power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following Figure 55. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD}_SDn_PLLn balls to ensure it filters out as much noise as possible. The ground connection should be near the AV_{DD}_SDn_PLLn balls. The 0.003-µF capacitors closest to the balls, followed by a 4.7-µF and 47-µF capacitor, and finally the 0.33 Ω resistor to the board supply plane. The capacitors are connected from AV_{DD}_SD*n*_PLL*n* to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide, and direct.

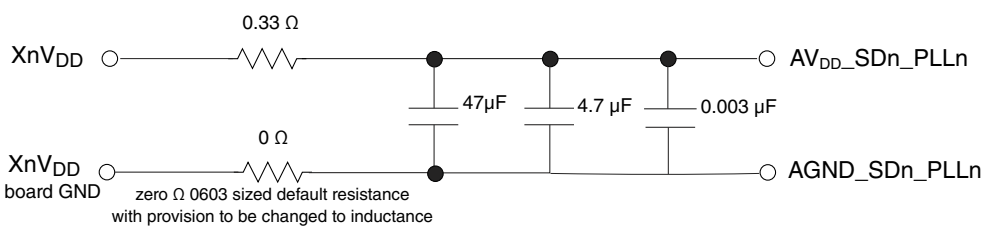


Figure 55. SerDes PLL power supply filter circuit

Note the following:

- AV_{DD}_SD*n*_PLL*n* should be a filtered version of X*n*V_{DD}.
- Signals on the SerDes interface are fed from the X*n*V_{DD} power plane.
- Voltage for AV_{DD}_SDn_PLLn is defined at the PLL supply filter and not the pin of AV_{DD}_SD*n*_PLL*n*.

- A 47-µF 0805 XR5 or XR7, 4.7-µF 0603, and 0.003-µF 0402 capacitor are recommended. The size and material type are important. A 0.33-Ω ± 1% resistor is recommended.
- There needs to be dedicated analog ground, AGND_SD*n*_PLL*n* for each AV_{DD}_SD*n*_PLL*n* pin up to the physical local of the filters themselves.

4.2.4 S*n*V_{DD} power supply filtering

S*n*V_{DD} must be supplied by a decicated linear regulator.

An example solution for S*n*V_{DD} filtering, where S*n*V_{DD} is sourced from a linear regulator, is illustrated in Figure 56. The component values in this example filter are system dependent and are still under characterization, component values may need adjustment based on the system or environment noise.

Where:

- C1 = 0.003 µF ± 10%, X5R, with ESL ≤ 0.5 nH
- C2 and C3 = 2.2 µF ± 10%, X5R, with ESL ≤ 0.5 nH
- F1 and F2 are 0603 sized Ferrite SMD, like the Murata part BLM18PG121SH1. Its maximum DC resistance is 0.05Ω, or 0.025Ω for the parallel resultant, and each has about a 120 Ω +/- 25% of AC impedance at 100 MHz, which is half valued for the parallel resultant, with individual maximum DC current carrying capacity of 2Amps.
- Bulk and decoupling capacitors are added, as needed, per power supply design.

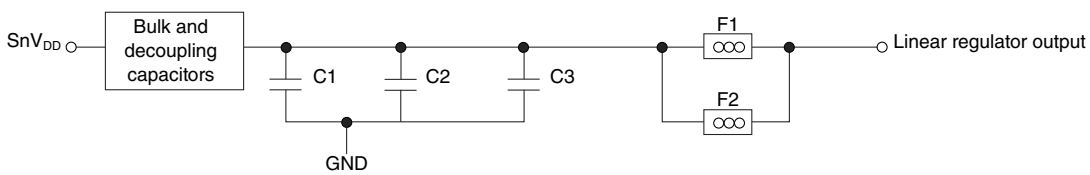


Figure 56. SV_{DD} power supply filter circuit

Note the following:

- Please refer to Power-on ramp rate, for maximum S*n*V_{DD} power-up ramp rate.
- There needs to be enough output capacitance or a soft start feature to assure ramp rate requirement is met.
- The ferrite beads should be placed in parallel to reduce voltage droop.
- Besides a linear regulator, a low noise dedicated switching regulator can also be used. 10 mVp-p, 50kHz - 500MHz is the noise goal.

4.2.5 X*n*V_{DD} power supply filtering

X*n*V_{DD} may be supplied by a linear regulator or sourced by a filtered G*n*V_{DD}. Systems may design in both options to allow flexibility to address system noise dependencies. However, for initial system bring-up, the linear regulator option is highly recommended.

An example solution for X*n*V_{DD} filtering, where X*n*V_{DD} is sourced from a linear regulator, is illustrated in Figure 57. The component values in this example filter are system dependent and are still under characterization, component values may need adjustment based on the system or environment noise.

Where:

- C1 = 0.003 µF ± 10%, X5R, with ESL ≤ 0.5 nH
- C2 and C3 = 2.2 µF ± 10%, X5R, with ESL ≤ 0.5 nH
- F1 and F2 are 0603 sized Ferrite SMD, like the Murata part BLM18PG121SH1. Its maximum DC resistance is 0.05Ω, or 0.025Ω for the parallel resultant, and each has about a 120+-25% Ω of AC impedance at 100 MHz, which is half valued for the parallel resultant, with individual maximum DC current carrying capacity of 2Amps.
- Bulk and decoupling capacitors are added, as needed, per power supply design.

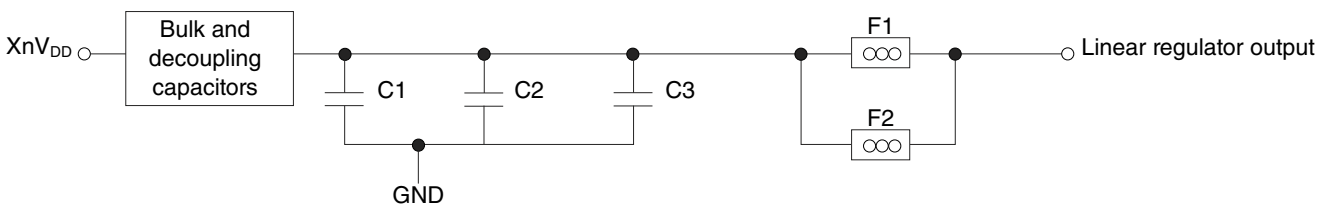


Figure 57. X*n*V_{DD} power supply filter circuit

Note the following:

- See Power-on ramp rate for maximum X*n*V_{DD} power-up ramp rate.
- There needs to be enough output capacitance or a soft-start feature to assure ramp rate requirement is met.
- The ferrite beads should be placed in parallel to reduce voltage droop.
- Besides a linear regulator, a low-noise, dedicated switching regulator can be used. 10 mVp-p, 50 kHz - 500 MHz is the noise goal.

4.2.6 USB_HV_{DD} and USB_OV_{DD} power supply filtering

USB_HV_{DD} and USB_OV_{DD} must be sourced by a filtered 3.3 V and 1.8 V voltage source using a star connection. An example solution for USB_HV_{DD} and USB_OV_{DD} filtering, where USB_HV_{DD} and USB_OV_{DD} are sourced from a 3.3 V and 1.8 V voltage

source, is illustrated in the following figure. The component values in this example filter is system dependent and are still under characterization, component values may need adjustment based on the system or environment noise.

Where:

- C1 = 0.003 µF ± 10%, X5R, with ESL ≤ 0.5 nH
- C2 and C3 = 2.2 µF ± 10%, X5R, with ESL ≤ 0.5 nH
- F1 is an 0603 sized Ferrite SMD, like the Murata part BLM18PG121SH1. Its maximum DC resistance is 0.05Ω and it has about a 120+-25% Ω of AC impedance at 100 MHz with maximum DC current carrying capacity of 2Amps.
- Bulk and decoupling capacitors are added, as needed, per power supply design.

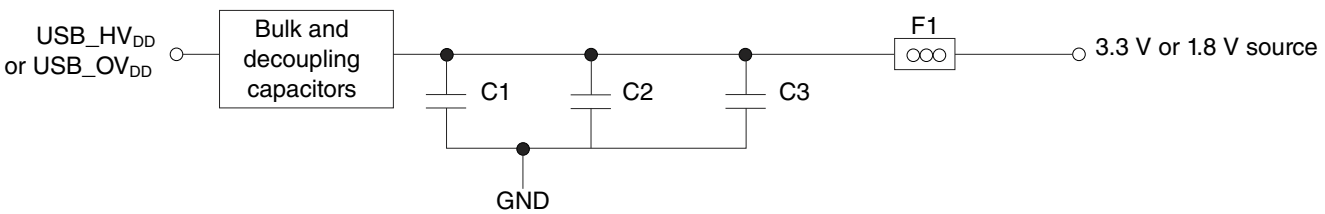


Figure 58. USB_HV_{DD} and USB_OV_{DD} power supply filter circuit

4.2.7 USB_SV_{DD} power supply filtering

USB_SV_{DD} must be sourced by a filtered V_{DD} using a star connection. An example solution for USB_SV_{DD} filtering, where USB_SV_{DD} is sourced from V_{DD}, is illustrated in the following figure. The component values in this example filter is system dependent and are still under characterization, component values may need adjustment based on the system or environment noise.

Where:

- C1 = 2.2 µF ± 20%, X5R, with Low ESL (for example, Panasonic ECJ0EB0J225M)
- F1 is an 0603 sized Ferrite SMD, like the Murata part BLM18PG121SH1. Its maximum DC resistance is 0.05Ω and it has about a 120+-25% Ω of AC impedance at 100 MHz with maximum DC current carrying capacity of 2Amps.
- Bulk and decoupling capacitors are added, as needed, per power supply design.

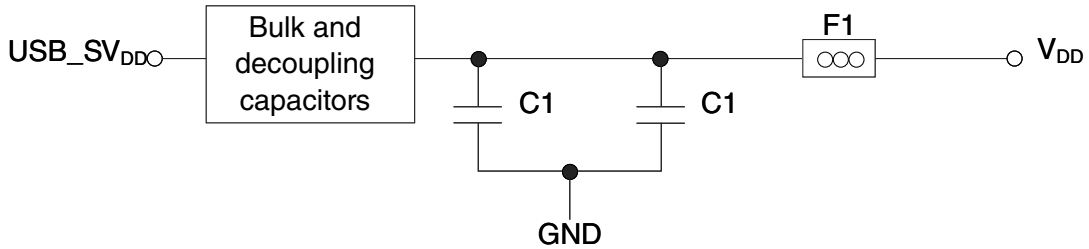


Figure 59. USB_SV_{DD} power supply filter circuit

4.3 Decoupling recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the chip system, and the chip itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, OV_{DD}, DV_{DD}, GnV_{DD}, and LV_{DD} pin of the device. These decoupling capacitors should receive their power from separate V_{DD}, OV_{DD}, DV_{DD}, GnV_{DD}, LV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.1 μF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

As presented in Core and platform supply voltage filtering, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} and other planes (for example, OV_{DD}, DV_{DD}, GnV_{DD}, and LV_{DD}), to enable quick recharging of the smaller chip capacitors.

4.4 SerDes block power supply decoupling recommendations

The SerDes block requires a clean, tightly regulated source of power (SnV_{DD} and XnV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

NOTE

Only SMT capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

1. The board should have at least 1 x 0.1-uF SMT ceramic chip capacitor placed as close as possible to each supply ball of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
2. Between the device and any SerDes voltage regulator there should be a lower bulk capacitor for example a 10-uF, low ESR SMT tantalum or ceramic and a higher bulk capacitor for example a 100uF - 300-uF low ESR SMT tantalum or ceramic capacitor.

4.5 Connection recommendations

The following is a list of connection recommendations:

- To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unless otherwise noted in this document, all unused active low and open drain I/O inputs should be pulled up to V_{DD}, OV_{DD}, DV_{DD}, GnV_{DD}, and LV_{DD} as required. All unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected. Power and ground connections must be made to all external V_{DD}, OV_{DD}, DV_{DD}, GnV_{DD}, LV_{DD} and GND pins of the device.
- The TEST_SEL pin must be tied to ground.
- The chip has temperature diodes that can be used to monitor its temperature by using some external temperature monitoring devices (such as Analog Devices, ADT7481A™). For more information, see AN4787. The following are the specifications of the chip temperature diodes:
  - Operating range: 10-230 µA
  - Non-ideality factor over temperature range 85C° to 105C°, n = 1.006 ± 0.003, with approximate error +/- 1 C° and error under +/- 3 C° for temperature range 0 C° to 85C°.

4.5.1 Legacy JTAG configuration signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 61. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The TRST_B signal is optional in the IEEE Std 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The device requires TRST_B to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert TRST_B during the power-on reset flow. Simply tying TRST_B to PORESET_B is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert PORESET_B or TRST_B in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 61 allows the COP port to independently assert PORESET_B or TRST_B, while ensuring that the target can drive PORESET_B as well.

The COP interface has a standard header, shown in Figure 60, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 60 is common to all known emulators.

4.5.1.1 Termination of unused signals

If the JTAG interface and COP header will not be used, NXP recommends the following connections:

- TRST_B should be tied to PORESET_B through a 0 kΩ isolation resistor so that it is asserted when the system reset signal (PORESET_B) is asserted, ensuring that the

JTAG scan chain is initialized during the power-on reset flow. NXP recommends that the COP header be designed into the system as shown in Figure 61. If this is not possible, the isolation resistor will allow future access to TRST_B in case a JTAG interface may need to be wired onto the system in future debug situations.

- No pull-up/pull-down is required for TDI, TMS or TDO.

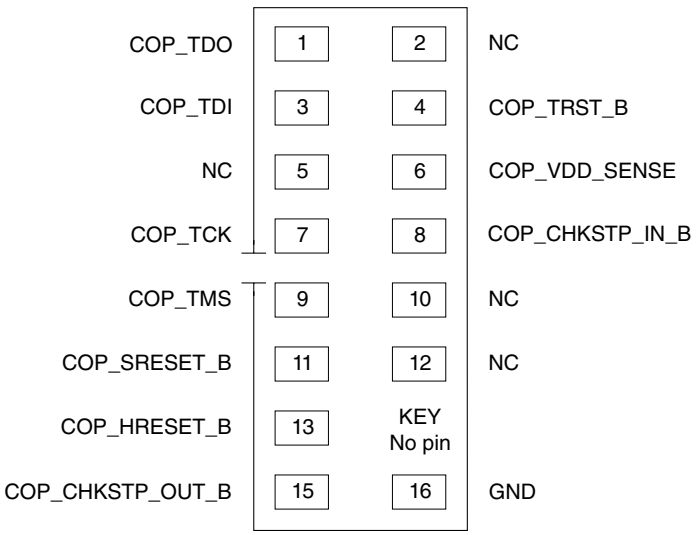
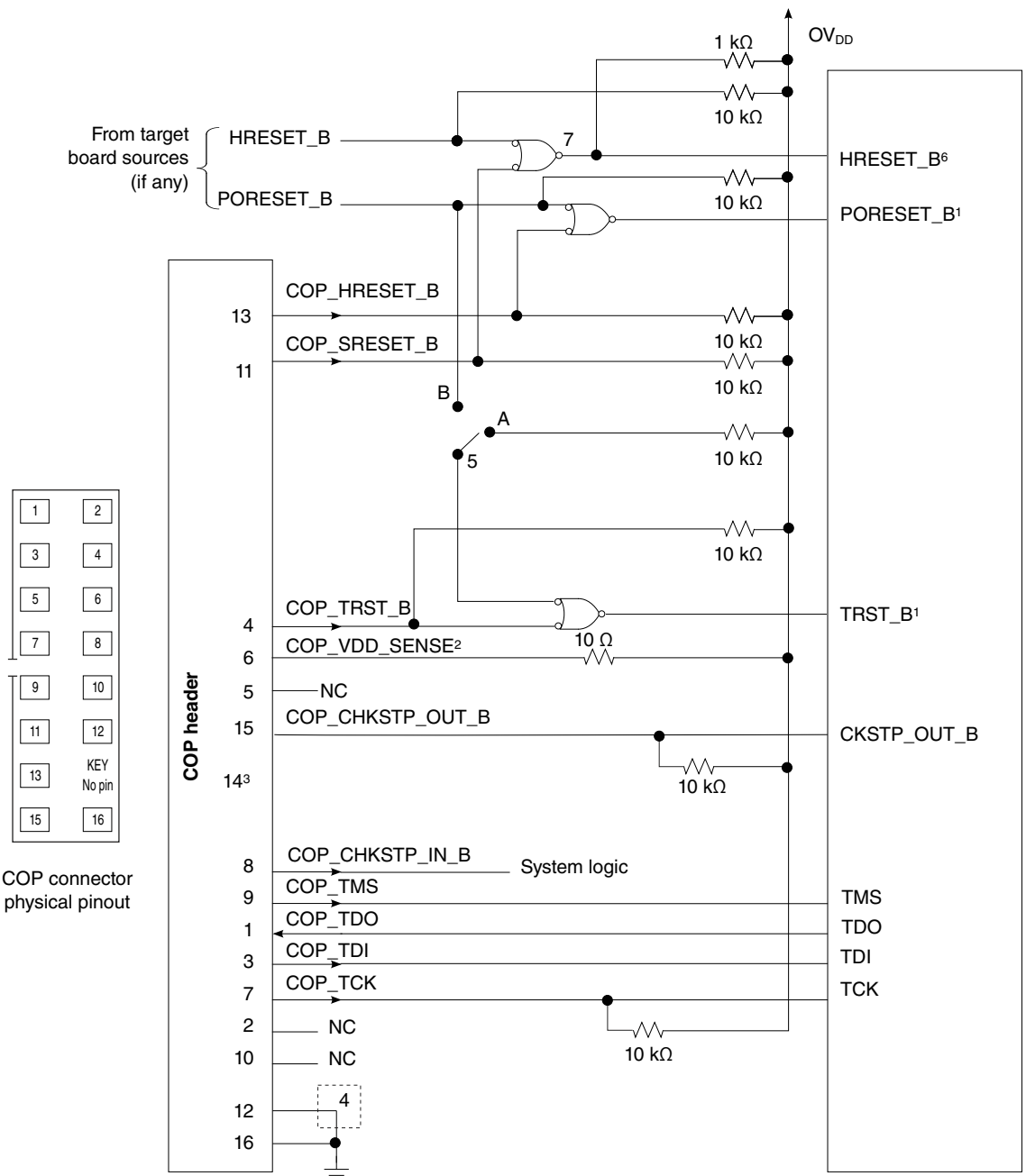


Figure 60. Legacy COP Connector Physical Pinout



Notes:

1. The COP port and target board should be able to independently assert PORESET_B and TRST_B to the processor in order to fully control the processor as shown here.

2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.

3. The KEY location (pin 14) is not physically present on the COP header.

4. Although pin 12 is defined as a no-connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.

5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the TRST_B line. If BSDL testing is not being performed, this switch should be closed to position B.

6. Asserting HRESET_B causes a hard reset on the device

7. This is an open-drain output gate.

Figure 61. Legacy JTAG Interface Connection

4.5.2 Aurora configuration signals

Correct operation of the Aurora interface requires configuration of a group of system control pins as demonstrated in the figures below. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

NXP recommends that the Aurora 34 pin duplex connector be designed into the system as shown in Figure 64 or the 70 pin duplex connector be designed into the system as shown in Figure 65.

If the Aurora interface will not be used, NXP recommends the legacy COP header be designed into the system as described in Termination of unused signals .

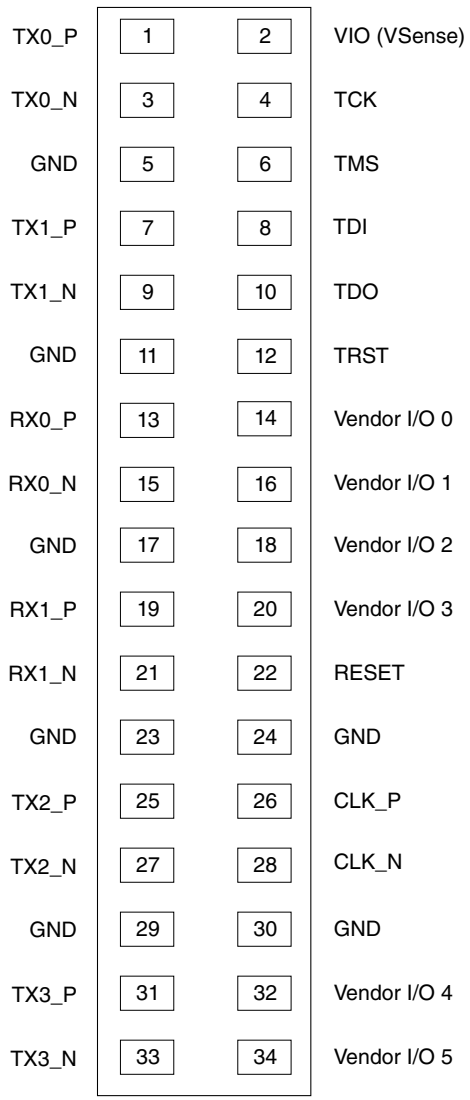


Figure 62. Aurora 34 pin connector duplex pinout

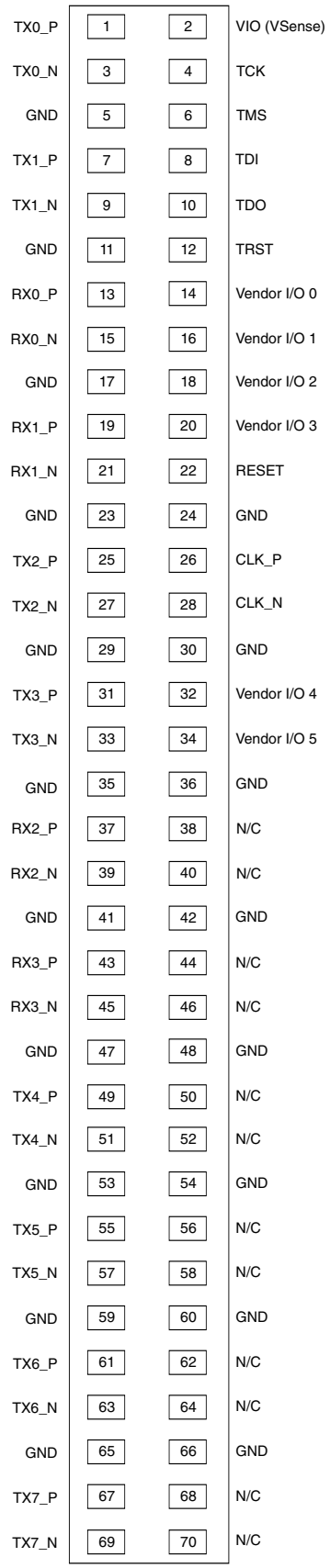
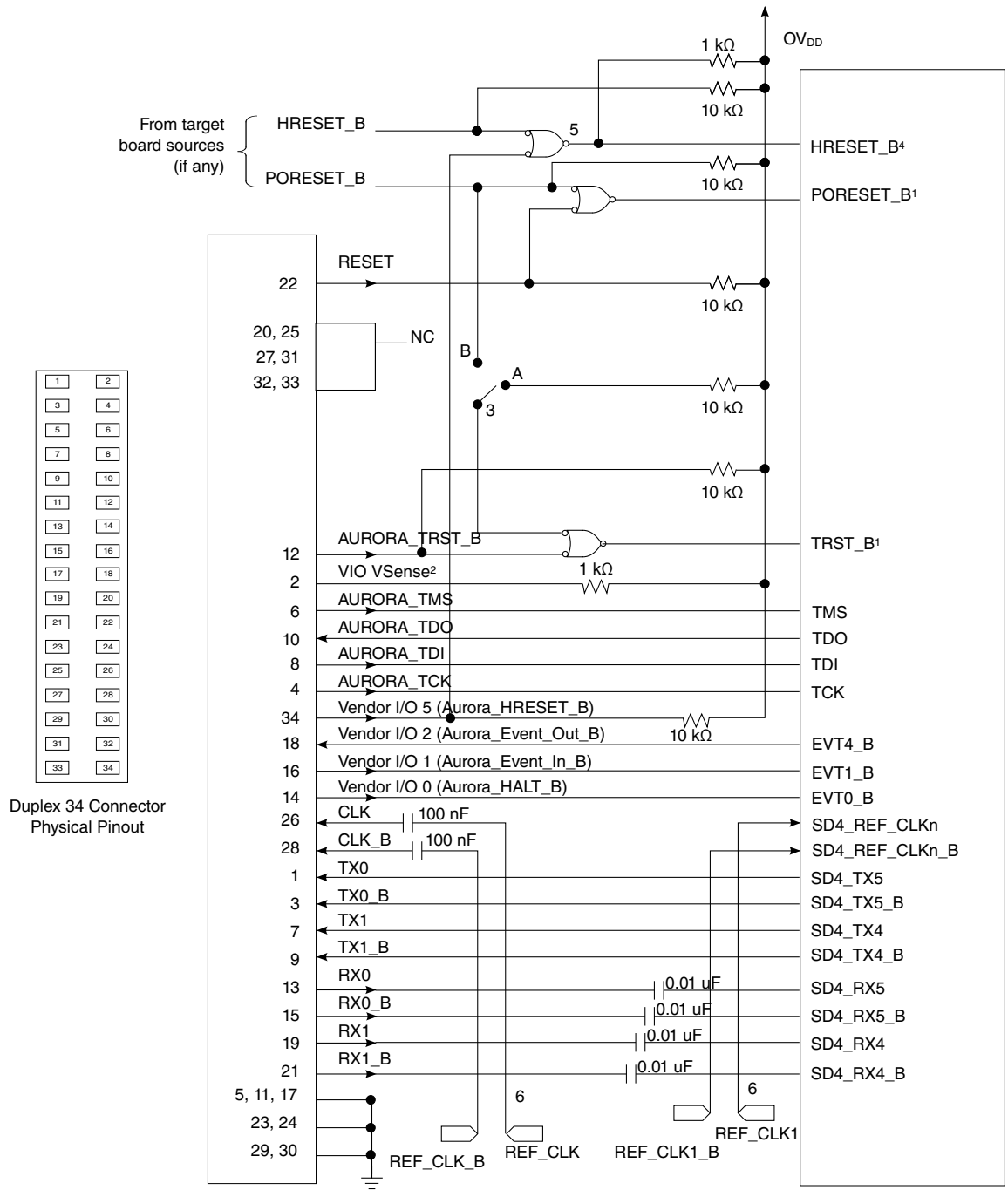


Figure 63. Aurora 70 pin connector duplex pinout



Notes:

1. The Aurora port and target board should be able to independently assert PORESET_B and TRST_B to the processor in order to fully control the processor as shown here.

2. Populate this with a 1 kΩ resistor for short-circuit/current-limiting protection.

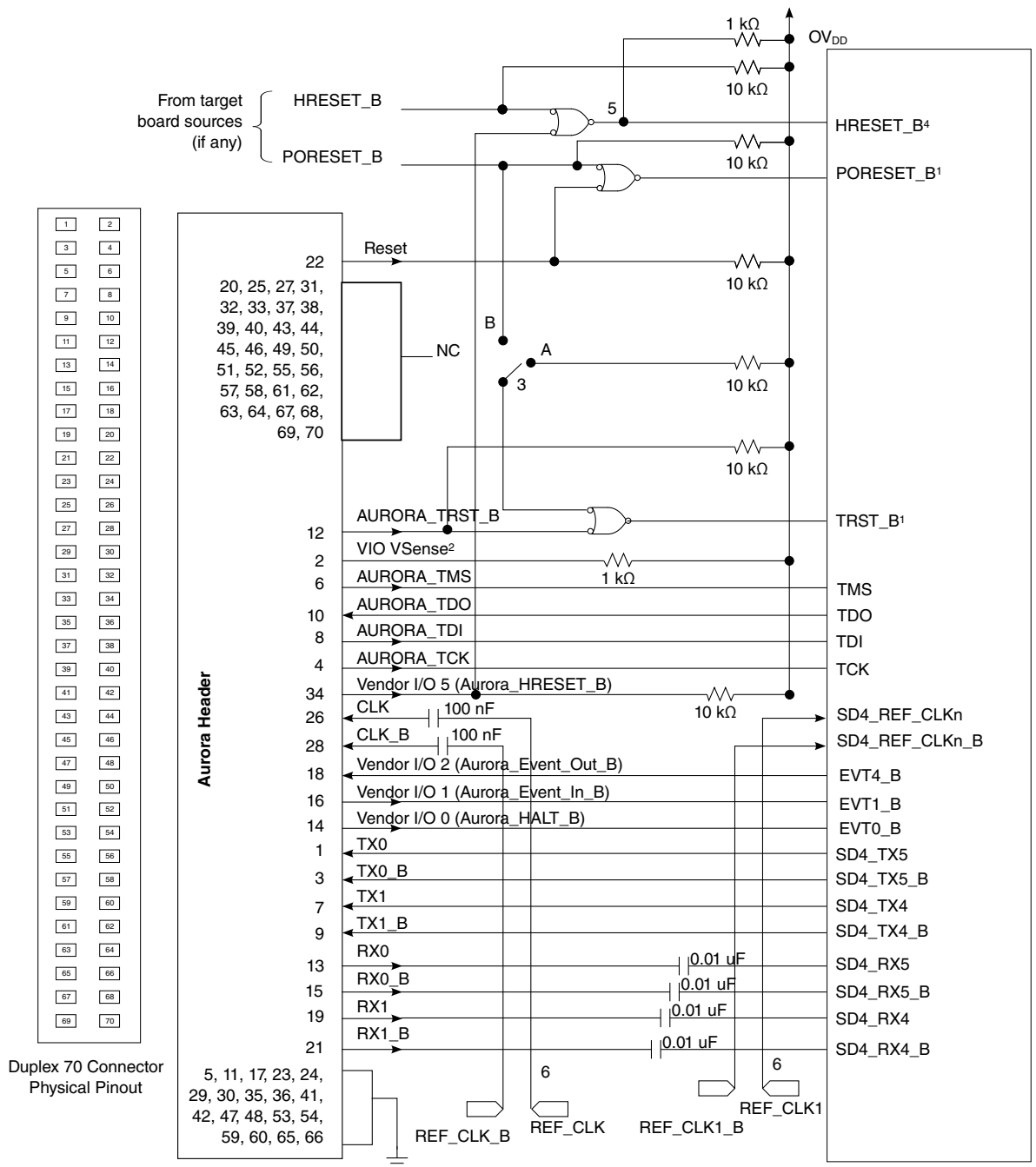
3. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the TRST_B line. If BSDL testing is not being performed, this switch should be closed to position B.

4. Asserting HRESET_B causes a hard reset on the device

5. This is an open-drain output gate.

6. REF_CLK/REF_CLK_B and REF_CLK1/REFCLK1_B are buffered clocks from the same common source.

Figure 64. Aurora 34 pin connector duplex interface connection



Notes:

1. The Aurora port and target board should be able to independently assert PORESET_B and TRST_B to the processor in order to fully control the processor as shown here.

2. Populate this with a 1 kΩ resistor for short-circuit/current-limiting protection.

3. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the TRST_B line. If BSDL testing is not being performed, this switch should be closed to position B.

4. Asserting HRESET_B causes a hard reset on the device

5. This is an open-drain output gate.

6. REF_CLK/REF_CLK_B and REF_CLK1/REFCLK1_B are buffered clocks from the same common source.

Figure 65. Aurora 70 pin connector duplex interface connection

4.5.3 Guidelines for high-speed interface termination

4.5.3.1 SerDes interface entirely unused

If the high-speed SerDes interface is not used at all, the unused pin should be terminated as described in this section.

Note that S*n*V_{DD}, X*n*V_{DD} and AVDD_SD*n*_PLL*n* must remain powered.

For AVDD_SD*n*_PLL*n*, it must be connected to X*n*V_{DD} through a zero ohm resistor (instead of filter circuit shown in Figure 55).

The following pins must be left unconnected:

- SD*n*_TX[7:0]
- SD*n*_TX[7:0]_B
- SD*n*_IMP_CAL_RX
- SD*n*_IMP_CAL_TX

The following pins must be connected to SnGND:

- SD*n*_REF_CLK1, SDn_REF_CLK2
- SD*n*_REF_CLK1_B, SDn_REF_CLK2_B

It is recommended for the following pins to be connected to SnGND:

- SD*n*_RX[7:0]
- SD*n*_RX[7:0]_B

It is possible to independently disable each SerDes module by disabling all PLLs associated with it.

SerDes *n* = 1:4 is disabled as follows:

- SRDS_PLL_PD_S*n* = 2'b11 (both PLLs configured as powered down, all data lanes selected by the protocols defined in SRDS_PRTCL_S*n* associated to the PLLs are powered down as well)
- SRDS_PLL_REF_CLK_SEL_S*n* = 2'b00
- SRDS_PRTCL_S*n* = 2 (no other values permitted when both PLLs are powered down

4.5.3.2 SerDes interface partly unused

If only part of the high speed SerDes interface pins are used, the remaining high-speed serial I/O pins should be terminated as described in this section.

Note that both SnV_{DD} and XnV_{DD} must remain powered.

If any of the PLLs are un-used, the corresponding AVDD_SD*n*_PLL*n* must be connected to XnV_{DD} through a zero ohm resistor (instead of filter circuit shown in Figure 55).

The following unused pins must be left unconnected:

- SDn_TX[*n*]
- SDn_TX[*n*]_B

The following unused pins must be connected to SnGND:

- SD1_REF_CLK[1:2], SD1_REF_CLK[1:2]_B (If entire SerDes 1 unused)
- SD2_REF_CLK[1:2], SD2_REF_CLK[1:2]_B (If entire SerDes 2 unused)
- SD3_REF_CLK[1:2], SD3_REF_CLK[1:2]_B (If entire SerDes 3 unused)
- SD4_REF_CLK[1:2], SD4_REF_CLK[1:2]_B (If entire SerDes 4 unused)

It is recommended for the following unused pins to be connected to SnGND:

- SDn_RX[*n*]
- SDn_RX[*n*]_B

In the RCW configuration field SRDS_PLL_PD_S*n*, the respective bits for each unused PLL must be set to power it down. A module is disabled when both its PLLs are turned off.

Unused lanes must be powered down through the SRDSx Lane m General Control Register 0 (SRDSxLNmGCR0) as follows:

- SRDSxLNmGCR0[RRST] = 0
- SRDSxLNmGCR0[TRST] = 0
- SRDSxLNmGCR0[RX_PD] = 1
- SRDSxLNmGCR0[TX_PD] = 1

Note that in the case where the SerDes pins are connected to slots , it is acceptable to have these pins unterminated when unused.

4.5.4 USB controller connections

This section details the hardware connections required for the USB controllers.

4.5.4.1 USB divider network

This figure shows the required divider network for the VBUS interface for the chip. Additional requirements for the external components are:

- Both resistors require 1% accuracy and a current capability of up to 1 mA. They must both have the same temperature coefficient and accuracy.
- The zener diode must have a value of 5 V–5.25 V.
- The 0.6 V diode requires an I_F = 10 mA, I_R < 500 nA and $V_{F(Max)}$ = 0.8 V. If the USB PHY does not support OTG mode, this diode can be removed from the schematic or made a DNP component.

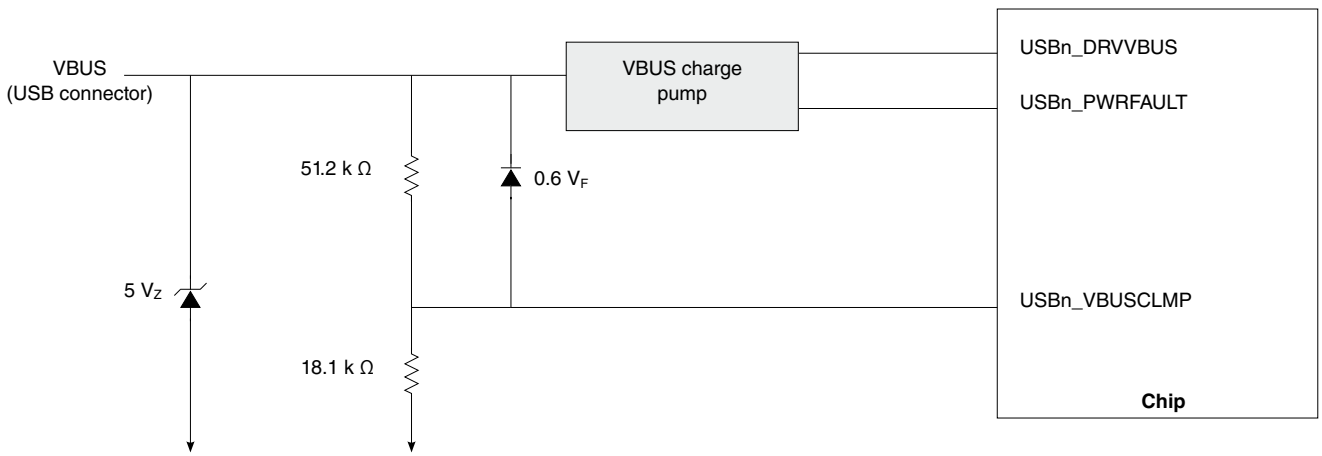


Figure 66. Divider network at VBUS

4.6 Thermal

This table shows the thermal characteristics for the chip. Note that these numbers are based on design estimates and are preliminary.

Table 151. Package thermal characteristics[6]

Rating	Board	Symbol	Value	Unit	Notes
Junction to ambient, natural convection	Single-layer board (1s)	$R_{\Theta JA}$	11	°C/W	1, 2
Junction to ambient, natural convection	Four-layer board (2s2p)	$R_{\Theta JA}$	9	°C/W	1, 3
Junction to ambient (at 200 ft./min.)	Single-layer board (1s)	$R_{\Theta JMA}$	8	°C/W	1, 2
Junction to ambient (at 200 ft./min.)	Four-layer board (2s2p)	$R_{\Theta JMA}$	6	°C/W	1, 2
Junction to board	-	$R_{\Theta JB}$	3	°C/W	3
Junction to case top	-	$R_{\Theta JCtop}$	0.3	°C/W	4
Junction to lid top	-	$R_{\Theta JClid}$	0.11	°C/W	5

Table continues on the next page...

Table 151. Package thermal characteristics[6] (continued)

Rating	Board	Symbol	Value	Unit	Notes
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.					
2. Per JEDEC JESD51-3 and JESD51-6 with the board (JESD51-9) horizontal.					
3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.					
4. Junction-to-case-top at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.					
5. Junction-to-lid-top thermal resistance determined using the using MIL-STD 883 Method 1012.1. However, instead of the cold plate, the lid top temperature is used here for the reference case temperature. Reported value does not include the thermal resistance of the interface layer between the package and cold plate.					
6. See Thermal management information, for additional details.					

4.7 Recommended thermal model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local NXP sales office.

4.8 Thermal management information

This section provides thermal management information for the flip-chip, plastic-ball, grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design-the heat sink, airflow, and thermal interface material.

The recommended attachment method to the heat sink is illustrated in Figure 67. The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 60 pounds force (270 Newtons).

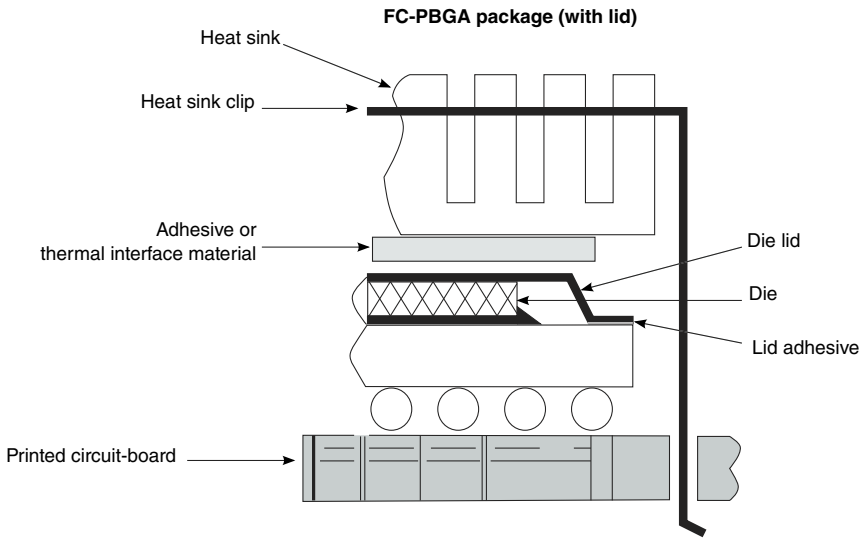


Figure 67. Package exploded, cross-sectional view-FC-PBGA (with lid)

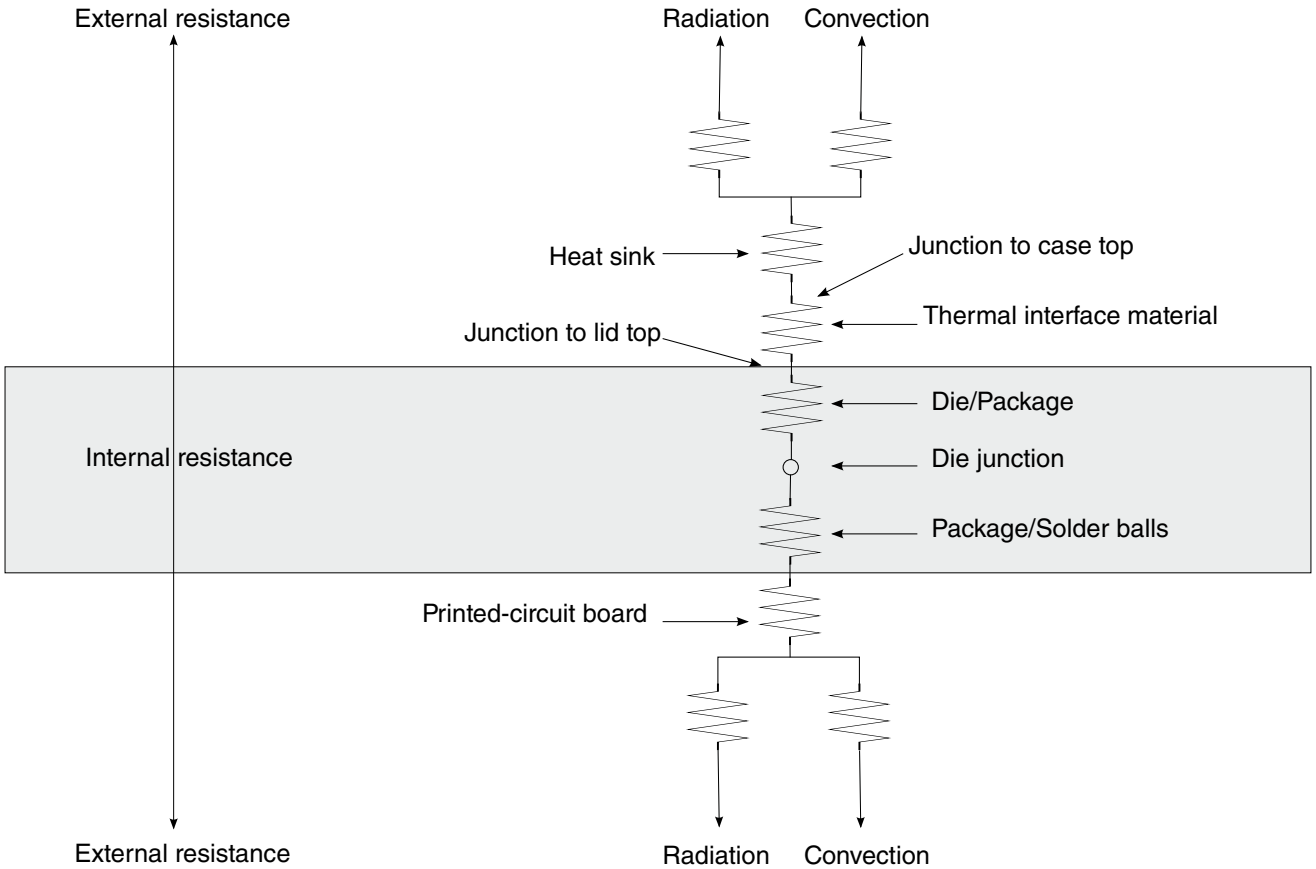
The system board designer can choose between several types of heat sinks to place on the device. There are several commercially-available thermal interfaces to choose from in the industry. Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

4.8.1 Internal package conduction resistance

For the package, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-lid-top thermal resistance
- The die junction-to-board thermal resistance

This figure depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.



(Note the internal versus external package resistance)

Figure 68. Package with heat sink mounted to a printed-circuit board

The heat sink removes most of the heat from the device. Heat generated on the active side of the chip is conducted through the silicon and through the heat sink attach material (or thermal interface material), and finally to the heat sink. The junction-to-case thermal resistance is low enough that the heat sink attach material and heat sink thermal resistance are the dominant terms.

4.8.2 Thermal interface materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. The performance of thermal interface materials improves with increasing contact pressure; this performance characteristic chart is generally provided by the thermal interface vendor. The recommended method of mounting heat sinks on the package is by means of a spring clip attachment to the printed-circuit board (see Figure 67).

The system board designer can choose among several types of commercially-available thermal interface materials.

5 Package information

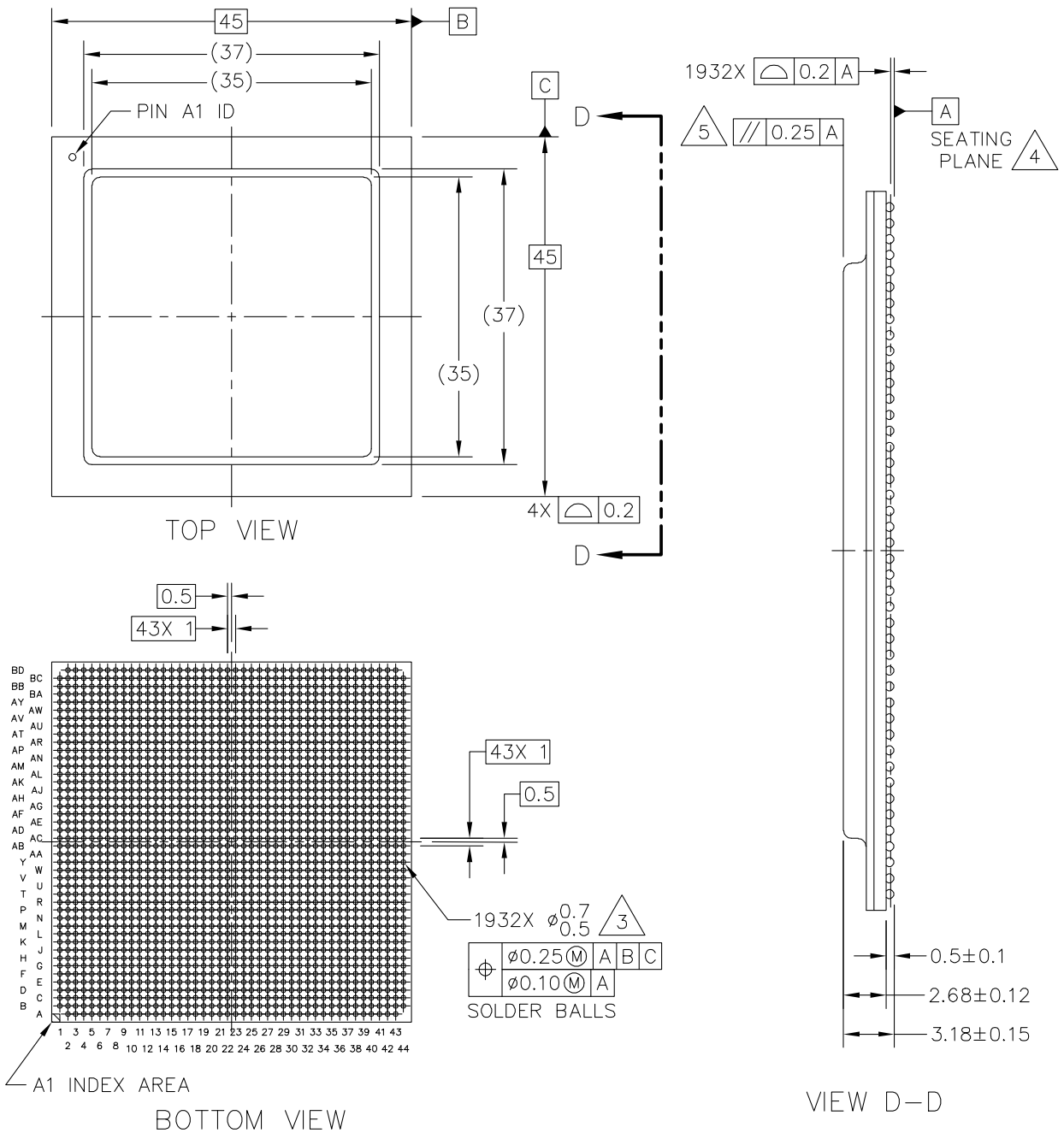
5.1 Package parameters for the FC-PBGA

The package parameters are as provided in the following list. The package type is 45 mm x 45 mm, 1932 flip-chip, plastic-ball, grid array (FC-PBGA).

- Package outline - 45 mm x 45 mm
- Interconnects - 1932
- Ball Pitch - 1.0 mm
- Ball Diameter (typical) - 0.60 mm
- Solder Balls - 96.5% Sn, 3% Ag, 0.5% Cu
- Module height (typical) - 3.03 mm to 3.33 mm (maximum)

5.2 Mechanical dimensions of the FC-PBGA

This figure shows the mechanical dimensions and bottom surface nomenclature of the chip.



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: FCPBGA, 1932 I/O, 45 X 45 X 3.18 PKG, 1 MM PITCH, WITH LID	DOCUMENT NO: 98ASA00384D	REV: A	
	CASE NUMBER: 2231–02	12 APR 2012	
	STANDARD: NON–JEDEC		

Figure 69. Mechanical dimensions of the FC-PBGA with full lid

NOTES:

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.

6 Security fuse processor

This chip implements the QorIQ platform's Trust Architecture, supporting capabilities such as secure boot. Use of the Trust Architecture features is dependent on programming fuses in the Security Fuse Processor (SFP). The details of the Trust Architecture and SFP can be found in the chip reference manual.

To program SFP fuses, the user is required to supply 1.8 V to the PROG_SFP pin per Power sequencing. PROG_SFP should only be powered for the duration of the fuse programming cycle, with a per device limit of two fuse programming cycles. All other times PROG_SFP should be connected to GND. The sequencing requirements for raising and lowering PROG_SFP are shown in Figure 9. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 3.

NOTE

Users not implementing the QorIQ platform's Trust Architecture features should connect PROG_SFP to GND.

7 Ordering information

Contact your local NXP sales office or regional marketing team for order information.

7.1 Part numbering nomenclature

This table provides the NXP QorIQ platform part numbering nomenclature.

Table 152. Part numbering nomenclature

pt or t	*n*	*nn*	*n*	*x*	*t*	*e*	*n*	*c*	*d*	*r*
Generation	**Platform**	**Number of virtual cores**	**Derivative**	**Qual status**	**Temperature range**	**Encryption**	**Package type**	**CPU speed**	**DDR data rate**	**Die revision**
PT = 28 nm (Prototype) T = 28 nm (Production)	4	24 = 24 virtual cores 16 = 16 virtual cores 08 = 8 virtual cores	0 = Standard power 1 = Low power	P = Prototype N = Qualified to industrial tier	S = Standard temp X = Extended temp	E = SEC present N = SEC not present	7 = FC-PBGA C4/C5 Pb-free	P = 1500 MHz Q = 1667 MHz T = 1800 MHz	Q = 1600 MT/s T= 1866 MT/s Z= TBD	A = Rev 1.0 B = Rev 2.0

7.2 Orderable part numbers addressed by this document

This table provides the NXP orderable part numbers addressed by this document for the chip.

Table 153. Orderable part numbers addressed by this document

Part number[1]	*pt or t*	*n*	*nn*	*n*	*x*	*t*	*e*	*n*	*c*	*d*	*r*
T4160NSE7PQB	T	4	16=16 virtual cores	0	N = Qualified	S= Std temp	E = SEC present	7	P=1500 MHz CPU	Q=1600 MT/s DDR	B= REV 2.0
T4160NSE7QTB	T	4	16=16 virtual cores	0	N = Qualified	S= Std temp	E = SEC present	7	Q=1667 MHz CPU	T=1866 MT/s DDR	B= REV 2.0
T4160NSN7PQB	T	4	16=16 virtual cores	0	N = Qualified	S= Std temp	N = SEC not present	7	P=1500 MHz CPU	Q=1600 MT/s DDR	B= REV 2.0
T4160NSN7QTB	T	4	16=16 virtual cores	0	N = Qualified	S= Std temp	N = SEC not present	7	Q=1667 MHz CPU	T=1866 MT/s DDR	B= REV 2.0
T4160NSE7TTB	T	4	16=16 virtual cores	0	N = Qualified	S= Std temp	E = SEC present	7	T=1800 MHZ CPU	T=1866 MT/s DDR	B= REV 2.0

Table continues on the next page...

Table 153. Orderable part numbers addressed by this document (continued)

Part number[1]	pt or t	n	nn	n	x	t	e	n	c	d	r
T4160NSN7TTB	T	4	16=16 virtual cores	0	N = Qualified	S= Std temp	N = SEC not present	7	T=1800 MHZ CPU	T=1866 MT/s DDR	B= REV 2.0
T4160NXE7PQB	T	4	16=16 virtual cores	0	N = Qualified	X = Extended temp	E = SEC present	7	P=1500 MHz CPU	Q=1600 MT/s DDR	B= REV 2.0
T4160NXN7PQB	T	4	16=16 virtual cores	0	N = Qualified	X = Extended temp	N = SEC not present	7	P=1500 MHz CPU	Q=1600 MT/s DDR	B= REV 2.0
T4161NSE7PQB	T	4	16=16 virtual cores	1	N = Qualified	S= Std temp	E=SEC present	7	P=1500 MHz CPU	Q=1600 MT/s DDR	B = Rev 2.0
T4161NSE7QTB	T	4	16=16 virtual cores	1	N = Qualified	S= Std temp	E=SEC present	7	Q=1667 MHz CPU	T=1866 MT/s DDR	B = Rev 2.0
T4161NSE7TTB	T	4	16=16 virtual cores	1	N = Qualified	S= Std temp	E=SEC present	7	T=1800 MHz CPU	T=1866 MT/s DDR	B = Rev 2.0
T4161NSN7PQB	T	4	16=16 virtual cores	1	N = Qualified	S= Std temp	N = SEC not present	7	P=1500 MHz CPU	Q=1600 MT/s DDR	B = Rev 2.0
T4161NSN7QTB	T	4	16=16 virtual cores	1	N = Qualified	S= Std temp	N = SEC not present	7	Q=1667 MHz CPU	T=1866 MT/s DDR	B = Rev 2.0
T4161NSN7TTB	T	4	16=16 virtual cores	1	N = Qualified	S= Std temp	N = SEC not present	7	T=1800MHz CPU	T=1866 MT/s DDR	B = Rev 2.0
T4161NXE7PQB	T	4	16=16 virtual cores	1	N = Qualified	X=extended temp	E=SEC present	7	P=1500 MHz CPU	Q=1600 MT/s DDR	B = Rev 2.0
T4161NXE7QTB	T	4	16=16 virtual cores	1	N = Qualified	X=extended temp	E=SEC present	7	Q=1667 MHz CPU	T=1866 MT/s DDR	B = Rev 2.0
T4161NXE7TTB	T	4	16=16 virtual cores	1	N = Qualified	X=extended temp	E=SEC present	7	T=1800 MHz CPU	T=1866 MT/s DDR	B = Rev 2.0
T4161NXN7PQB	T	4	16=16 virtual cores	1	N = Qualified	X=extended temp	N = SEC not present	7	P=1500 MHz CPU	Q=1600 MT/s DDR	B = Rev 2.0
T4161NXN7QTB	T	4	16=16 virtual cores	1	N = Qualified	X=extended temp	N = SEC not present	7	Q=1667 MHz CPU	T=1866 MT/s DDR	B = Rev 2.0
T4161NXN7TTB	T	4	16=16 virtual cores	1	N = Qualified	X=extended temp	N = SEC not present	7	T=1800 MHz CPU	T=1866 MT/s DDR	B = Rev 2.0

Notes:

1. The 1866 MT/s DDR rate is associated with 733 MHz platform frequency in high speed parts while the 1600 MT/s DDR rate is associated with 667 MHz platform clock frequency in lower speed parts in the part number encoding.

Table 153. Orderable part numbers addressed by this document

Part number[1]	pt or t	n	nn	n	x	t	e	n	c	d	r
2. The T4241/T4161/T4081 are identical to T4240/T4160/T4080 except they consume less power. See the power requirements in Power characteristics.											

Table 154. Orderable part numbers addressed by this document

Part number[1]	pt or t	n	nn	n	x	t	e	n	c	d	r
T4080NSE7PQB	T	4	8 = 8 virtual cores	0	N = Qualified	S= Std temp	E = SEC present	7	P=1500 MHz CPU	Q=1600 MT/s DDR	B= REV 2.0
T4080NSE7QTB	T	4	8 = 8 virtual cores	0	N = Qualified	S= Std temp	E = SEC present	7	Q=1667 MHz CPU	T=1866 MT/s DDR	B= REV 2.0
T4080NSN7PQB	T	4	8 = 8 virtual cores	0	N = Qualified	S= Std temp	N = SEC not present	7	P=1500 MHz CPU	Q=1600 MT/s DDR	B= REV 2.0
T4080NSN7QTB	T	4	8 = 8 virtual cores	0	N = Qualified	S= Std temp	N = SEC not present	7	Q=1667 MHz CPU	T=1866 MT/s DDR	B= REV 2.0
T4080NXE7PQB	T	4	8 = 8 virtual cores	0	N = Qualified	X = Extended temp	E = SEC present	7	P=1500 MHz CPU	Q=1600 MT/s DDR	B= REV 2.0
T4080NXN7PQB	T	4	8 = 8 virtual cores	0	N = Qualified	X = Extended temp	N = SEC not present	7	P=1500 MHz CPU	Q=1600 MT/s DDR	B= REV 2.0
T4081NSE7PQB	T	4	8 = 8 virtual cores	1	N = Qualified	S= Std temp	E = SEC present	7	P= 1500 MHz CPU	Q=1600 MT/s DDR	B = Rev 2.0
T4081NSE7QTB	T	4	8 = 8 virtual cores	1	N = Qualified	S= Std temp	E = SEC present	7	Q=1667 MHz CPU	T=1866 MT/s DDR	B = Rev 2.0
T4081NSE7TTB	T	4	8 = 8 virtual cores	1	N = Qualified	S= Std temp	E = SEC present	7	T=1800 MHz CPU	T=1866 MT/s DDR	B = Rev 2.0
T4081NSN7PQB	T	4	8 = 8 virtual cores	1	N = Qualified	S= Std temp	N = SEC not present	7	P= 1500 MHz CPU	Q=1600 MT/s DDR	B = Rev 2.0
T4081NSN7QTB	T	4	8 = 8 virtual cores	1	N = Qualified	S= Std temp	N = SEC not present	7	Q=1667 MHz CPU	T=1866 MT/s DDR	B = Rev 2.0
T4081NSN7TTB	T	4	8 = 8 virtual cores	1	N = Qualified	S= Std temp	N = SEC not present	7	T=1800 MHz CPU	T=1866 MT/s DDR	B = Rev 2.0
T4081NXE7PQB	T	4	8 = 8 virtual cores	1	N = Qualified	X=extended temp	E = SEC present	7	P= 1500 MHz CPU	Q=1600 MT/s DDR	B = Rev 2.0

Table continues on the next page...

Table 154. Orderable part numbers addressed by this document (continued)

Part number[1]	*pt or t*	*n*	*nn*	*n*	*x*	*t*	*e*	*n*	*c*	*d*	*r*
T4081NXE7QTB	T	4	8 = 8 virtual cores	1	N = Qualified	X=extended temp	E = SEC present	7	Q=1667 MHz CPU	T=1866 MT/s DDR	B = Rev 2.0
T4081NXE7TTB	T	4	8 = 8 virtual cores	1	N = Qualified	X=extended temp	E = SEC present	7	T=1800 MHz CPU	T=1866 MT/s DDR	B = Rev 2.0
T4081NXN7PQB	T	4	8 = 8 virtual cores	1	N = Qualified	X=extended temp	N = SEC not present	7	P= 1500 MHz CPU	Q=1600 MT/s DDR	B = Rev 2.0
T4081NXN7QTB	T	4	8 = 8 virtual cores	1	N = Qualified	X=extended temp	N = SEC not present	7	Q=1667 MHz CPU	T=1866 MT/s DDR	B = Rev 2.0
T4081NXN7TTB	T	4	8 = 8 virtual cores	1	N = Qualified	X=extended temp	N = SEC not present	7	T=1800 MHz CPU	T=1866 MT/s DDR	B = Rev 2.0

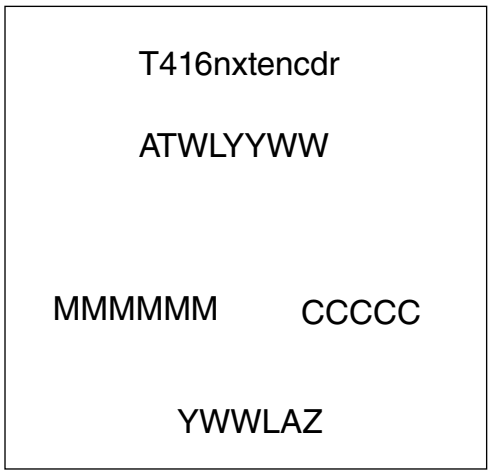
Notes:

1. The 1866 MT/s DDR rate is associated with 733 MHz platform frequency in high speed parts while the 1600 MT/s DDR rate is associated with 667 MHz platform clock frequency in lower speed parts in the part number encoding.

2. The T4241/T4161/T4081 are identical to T4240/T4160/T4080 except they consume less power. See the power requirements in Power characteristics.

7.2.1 Part marking

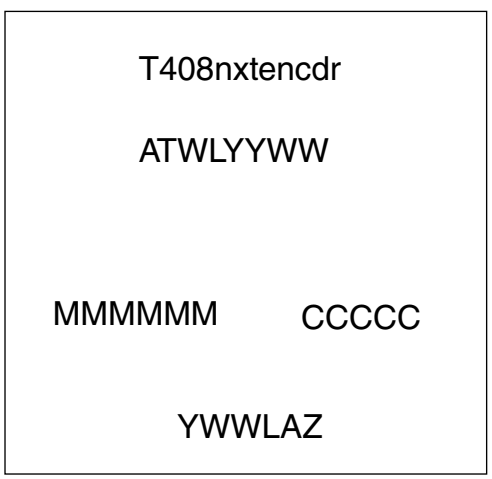
T4160 parts are marked as in the example shown in this figure.



Legend:
T416nxtencdr is the orderable part number.
ATWLYYWW is the test traceability code.
MMMMMM is the mask number.
CCCCC is th5e country code.
YWWLAZ is the assembly traceability code

Figure 70. Part marking for T416n FC-PBGA chip

T4080 parts are marked as in the example shown in this figure.



Legend:
T408nxtencdr is the orderable part number.
ATWLYYWW is the test traceability code.
MMMMMM is the mask number.
CCCCC is th5e country code.
YWWLAZ is the assembly traceability code

Figure 71. Part marking for T408n FC-PBGA chip

8 Revision history

This table summarizes revisions to this document.

Table 155. Revision history

Revision	Date	Description

1	05/2016	• Updated the document title to conform with new naming requirements.
		• Rebranded to NXP company name.
		• Removed all references to and sections for 10.3215G Interlaken.
		• Updated the speed units throughout the document.
		• In the pinout list table:
		  • Modified notes 6, 8, 23, and 24.
		  • Updated note 29 so the pull down resistance is 4.7 K instead of 10 to 50 kΩ.
		• In Table 2 :
		  • Changed format to group "Supply Voltage Levels," "Storage Temperature Conditions," and "Signal Voltage Levels."
		  • Reduced Maximum VDD, SnVDD supply voltage level from 1.1 V to 1.08 V.
		  • Reduced the max GnVDD I/O voltage levels from 1.65 to 1.58 (DDR3) and from 1.45 to 1.42 (DDR3L).
		  • Increased the storage temperature range max value from 150 to 155.
		  • Added "Min_DCV V_input," "Max_DCV V_input," and "Max Overshoot Voltage" columns for Signal Voltage level signals.
		  • In the SerDes signals, added additional rows for "No internal termination selected" and "50 ohm internal termination selected".
		  • Added the LP Trust signal LP_TMP_DETECT_B.
		  • Renamed "USBn_V_{IN}_3P3" and "USBn_V_{IN}_1P8" in note 5 and stressed the max slew rate of Dn_MVREF to 25 kv/s.
		  • Updated note 9 to include "See also note 6 in Table 3".
		  • Updated note 10 to include required biasing.
		  • Added notes 11, 12, and 13.
		• In Table 3, added table note 11 and added the LP Trust signal.
		• Updated Figure 8.
		• In Power sequencing, added a paragraph for V_{DD}_LP special power sequencing. Also relaxed power lines stability time from 75 ms to 400 ms.
		• In Table 6 :
		  • Added 1.8 GHz power numbers.
		  • Updated note 9.
		• In Table 7, updated note 9.
		• Added Table 8, Table 9, Table 12, and Table 13 for the T4161 and T4081 low power devices.
		• In Table 10 :
		  • Added 1.8 GHz power numbers.
		  • Updated note 9.
		• In Table 11 :
		  • Increased the 1667 MHz V_{DD} power max from 39.0 to 39.30.
		  • Updated note 9.
		• In Table 14 :
		  • Added the 1.8 GHz frequency.
		  • Added the T4160 and T4080 LPM20 data.
		  • Updated power numbers so they are relevant to 65°C.
		  • Added a note saying that these numbers are good for the T4161 and T4081 devices.
		• In Table 15 :
		  • Improved the PLL_SerDes typical value from 40 to 60.
		  • Added a formula for XV_{DD} and SV_{DD} typical power estimation rather than have multiple rows showing different SerDes configuration power.

Table continues on the next page...

Table 155. Revision history (continued)

Revision	Date	Description
		• Removed the note: "Maximum DDR power numbers are based on one 2-rank DIMM with 100% utilization," (previously note 5) and renumbered the notes. • Updated note 6 and added example. • Added low power devices to the table title. • In Table 17, included RTC clock DC specifications and updated the input capacitance data for both SYSCLK and RTC clock pins. • In "SYSCLK and RTC AC timing specifications," added Table 19, "RTC AC timing specification." • In Real-time clock (RTC) timing, removed the 50% duty cycle requirement from the RTC period minimum. • In Table 23, changed the DDRCLK input pin capacitance typical value from 7 to 11 and removed the max value. • In Table 24, changed the minimum DDRCLK cycle time from 5 ns to 7.5 ns. • In Table 25, relaxed HRESET_B signal rise/fall time to 4 SYSCLK cycles. • In Table 33, updated the SPI_MOSI hold time min and SPI_MOSI delay max formulas. • Updated the t_{MDKHDX} delay equation presentation in Table 42 and Table 43. (When MDIO_CFG[NEG] = 0 then Y = 0.5 and t_{MDKHDX} is Y x T_{MDC_CIK} ± 3 ns.) • In Table 46 : • Updated the TSEC_1588_CLK_IN clock period min value and removed the max value. • Updated the TSEC_1588_CLK_OUT clock period min value. • Added "hold time" to TSEC_1588_ALARM_OUT1/2. • Changed the TSEC_1588_TRIG_IN1/2 pulse width min value. • Removed notes 4 and 5 and updated notes 1 and 2. • Updated all note references. • In Table 50, changed VOH/VOL min and max from (0.8 x OVDD, 0.4) to (1.6 V, 0.32 V). • In "GPIO DC electrical characteristics," added Table 63, "LP_TMP_DETECT_B pin DC electrical characteristics." • In Table 109, changed the figure reference in note 2 from Figure 44 to Figure 43. • In Table 131, added the 1800 MHz data columns and added note 8 to describe why FMAN might have two different minimum frequencies. • In Table 136, changed the 133.333 MHz DDRCLK frequency example value to 1866.667. • In Table 140, added the 1800 MHz Core cluster: SYSCLK Ratio options. • In Minimum platform frequency requirements for high-speed interfaces, removed the SRIO equation that shows minimum platform frequency. • In Table 150, changed the VDD voltage note for "All other values". After the table, added paragraph for if DA_ALT_V is not all zeroes. • In PLL power supply filtering, updated the second NOTE. • Updated Figure 54 and Figure 55. • In Connection recommendations, added the expected temperature error to the non-ideality factor temperature range. • Updated Mechanical dimensions of the FC-PBGA to include package parameters. • In Table 152 : • Added "24 cores" to column nn. • Changed column n to "0 = Standard power; 1 = Low power". • Added symbol "T = 1800 MHz" to column C. • In Orderable part numbers addressed by this document, added two new orderable 1.8 G parts, removed prototype orderable part numbers, and added T4161 and T4081 part numbers. • Updated Part marking to include low power numbers.
0	07/2014	Initial release