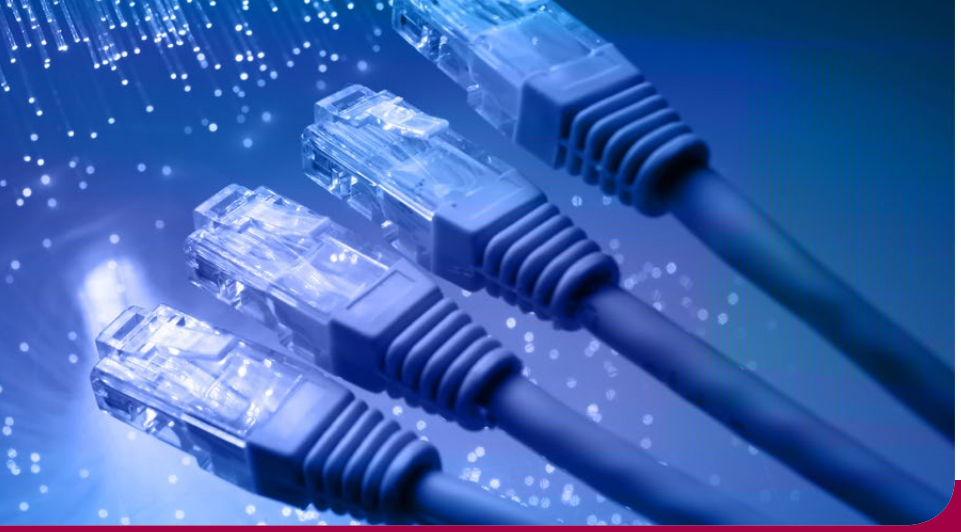


Multi-threaded SoCs deliver high performance per watt

QorIQ® T4240, T4160 and T4080 Multicore Processors

The QorIQ T4 family is the flagship of the QorIQ T series. Advanced 28 nm process technology, integration, new higher speed I/O, clustered memory subsystems, hardware acceleration and power management give the T4 family a very high performance profile in an embedded power envelope.

The T4240 advanced multicore processor features 12 physical and 24 virtual high performance cores scaling up to 1.8 GHz. The T4 family is joined by the T4160 (16 virtual cores) and T4080 (eight virtual cores) processors, and the family has a 3x performance scaling factor within a pin-compatible package. The T4 family features sophisticated support for hardware and software virtualization solutions.

TARGET MARKETS AND APPLICATIONS

The T4 family is ideal for combined control and data plane processing. Like other QorIQ devices, the T4 family of processors' high level of integration offers significant space, weight and power benefits compared to multiple discrete devices.

- Service provider networking: RNC, metro networking, gateway, core/edge router, EPC, CRAN, ATCA and AMC solutions
- Enterprise equipment: Router, switch services, UTM
- Data centers: NFV, SDN, ADC, WOC, UTM, proxy, server appliance, PCI Express® (PCIe) offload
- Storage controllers: FCoE bridging, iSCSI controller, SAN controller
- Aeronautics, defense and government: Radar imaging, ruggedized network appliance, cockpit display
- Industrial computing: Single-board computers, test equipment

FEATURES OF DISTINCTION

	T4080	T4160	T4240
Cores (Dual Threaded)	4	8	12
L2 Cache	2 MB	4 MB	6 MB
CoreNet Platform Cache	1 MB	1 MB	1.5 MB
DDR Controllers	2	2	3
SerDes Lanes	24	24	36
Max 10 Gbit/s Ethernet	2	2	4
Max 1 Gbit/s Ethernet	13	13	16
PCIe Controllers	3	3	4

ADVANCED CORES

The T4 family of processors are based on the new Power Architecture® e6500 core. The e6500 uses a 64-bit seven-stage pipeline for low latency response to unpredictable code execution paths, boosting single-threaded performance. The e6500 also offers higher aggregate instructions per clock at lower power with an innovative "fused core" approach to threading. The e6500 core's fully resourced dual threads provide 1.7 times the performance of a single thread.

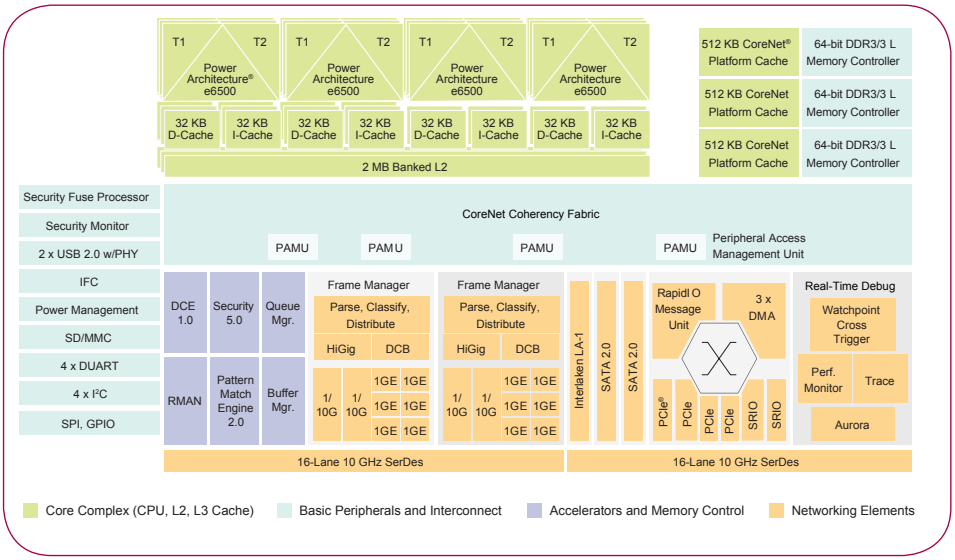
The e6500 cores are clustered in banks of four cores sharing a 2 MB L2 cache, allowing efficient sharing of code and data within a multicore cluster. Each e6500 core implements the AltiVec® technology SIMD engine, dramatically boosting the performance of heavy math algorithms with DSP-like performance. The e6500 core features include:

- Up to 1.8 GHz dual-threaded operation
- 7 DMIPS/MHz per core
- Advanced power saving modes, including state retention power gating

VIRTUALIZATION

The T4 family of processors includes support for hardware-assisted virtualization. The e6500 core offers an extra core privilege level (hypervisor) and hardware offload of logical to real address translation. In addition, the T4 family of processors includes platform-level enhancements supporting I/O virtualization with DMA memory protection through IOMMUs and configurable "storage profiles" that provide isolation of I/O buffers between guest environments. Virtualization software for the T4 family includes kernel virtualization machine (KVM), Linux® containers, hypervisor and commercial virtualization software from Enea®, Green Hills Software®, Mentor Graphics® and Wind River.

QorIQ T4240 PROCESSOR BLOCK DIAGRAM



DATA PATH ACCELERATION ARCHITECTURE (DPAA)

The T4 family of processors enhances the QorIQ DPAA, an innovative multicore infrastructure for scheduling work to cores (physical and virtual), hardware accelerators and network interfaces. The FMAN, a primary element of the DPAA, parses headers from incoming packets and classifies and selects data buffers with optional policing and congestion management. The FMAN passes its work to the QMAN, which assigns it to cores or accelerators with a multilevel scheduling hierarchy. The T4240 processor's implementation of the DPAA offers accelerators for cryptography, enhanced regular expression pattern matching and compression/decompression.

SYSTEM PERIPHERALS AND NETWORKING

For networking, there are dual FMANs with an aggregate of up to 16 any-speed MAC controllers that connect to PHYs, switches and backplanes over RGMII, SGMII, QSGMII, HiGig2, XAUI, XFI and 10Gbase-KR. The FMAN also supports new quality-of-service features through egress traffic shaping and priority flow control for data center bridging in converged data center networking applications. High-speed system expansion is supported through four PCI Express controllers that support varieties of lane lengths for PCIe specification 3.0, including endpoint SR-IOV with 128 virtual functions. Other peripheral interfaces include SRIO, Interlaken-LA, SATA, SD/MMC, I²C, UART, SPI, a NOR/NAND controller, GPIO and a 1866 MT/s DDR3L controller.

DPAA HARDWARE ACCELERATORS

Frame Manager (FMAN)	50 Gbit/s classify, parse and distribute
Buffer Manager (BMAN)	64 buffer pools
Queue Manager (QMAN)	Up to 2^{24} queues
RapidIO Manager (RMAN)	Seamless mapping to DPAA
Security (SEC)	40 Gbit/s: 3 DES, AES; 20 Gbit/s: Kasumi/F8
Pattern Matching Engine (PME)	10 Gbit/s
Data Compression Engine (DCE)	20 Gbit/s aggregate