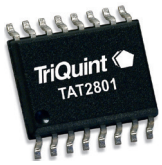
TAT2801

75 Ω CATV Output Stage Amplifier

Applications

- CATV Line Amplifiers
- HFC Nodes
- Head End Equipment

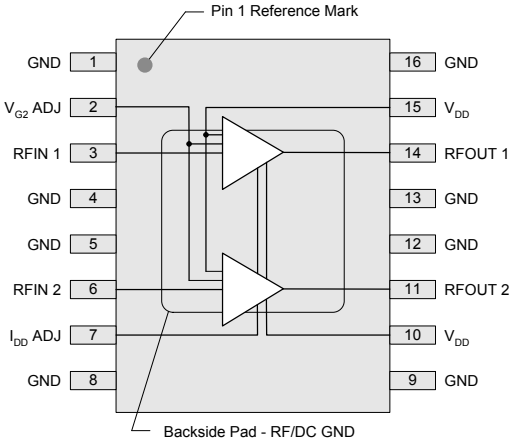


16-pin SOIC Wide Body Package
with Exposed Backside Ground Pad

Product Features

- Wide Bandwidth (40– 1000 MHz)
- 100% production tested for DOCSIS Edge QAM.
- In-package ESD protection
- Flat Gain
- High Power Compression
- Excellent Input/Output Match
- Low DC Power Consumption
- Bias optimization through external voltage

Functional Block Diagram



General Description

The TAT2801 is a high power, high linearity GaAs MMIC amplifier intended for output stage amplification in CATV infrastructure applications. Featuring a single die design and providing flat gain with low distortion, this amplifier is ideal for use in CATV distribution systems requiring high output powers and low distortion.

The TAT2801 draws 575 mA from a 12 V supply Bias current and voltage may be adjusted externally to optimize output performance for specific applications.

The TAT2801 integrates two TQP200002 ESD protection devices that provide bi-directional protection with very low leakage currents and extremely low capacitance.

The TAT2801 is packaged in an industry standard 16 pin SOIC WB package.

Pin Configuration

Pin No.	Label
1, 4-5, 8-9, 12-13, 16	GND
2	V_{G2} ADJ
3 / 6	RFIN1 / RFIN2
7	I_{DD} ADJ
10	V_{DD}
11 / 14	RFOUT2 / RFOUT1
15	V_{DD}
Backside Pad	RF/DC Gnd

Ordering Information

Part No.	Description
TAT2801	CATV Output Stage Amplifier
TAT2801-PCB	40-1000 MHz Evaluation Board

Standard T/R size = 1000 pieces on a 7” reel

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-40 to 150°C
Device Voltage (V_{DD})	+16 V
Device Current (I_{DD})	700 mA
RF Input Power (single tone)	75 dBmV

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Device Voltage (V_{DD})	11.7	12	12.3	V
Case Temperature	-40		+85	°C
Tj (for >10^6 hours MTTF)			200	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

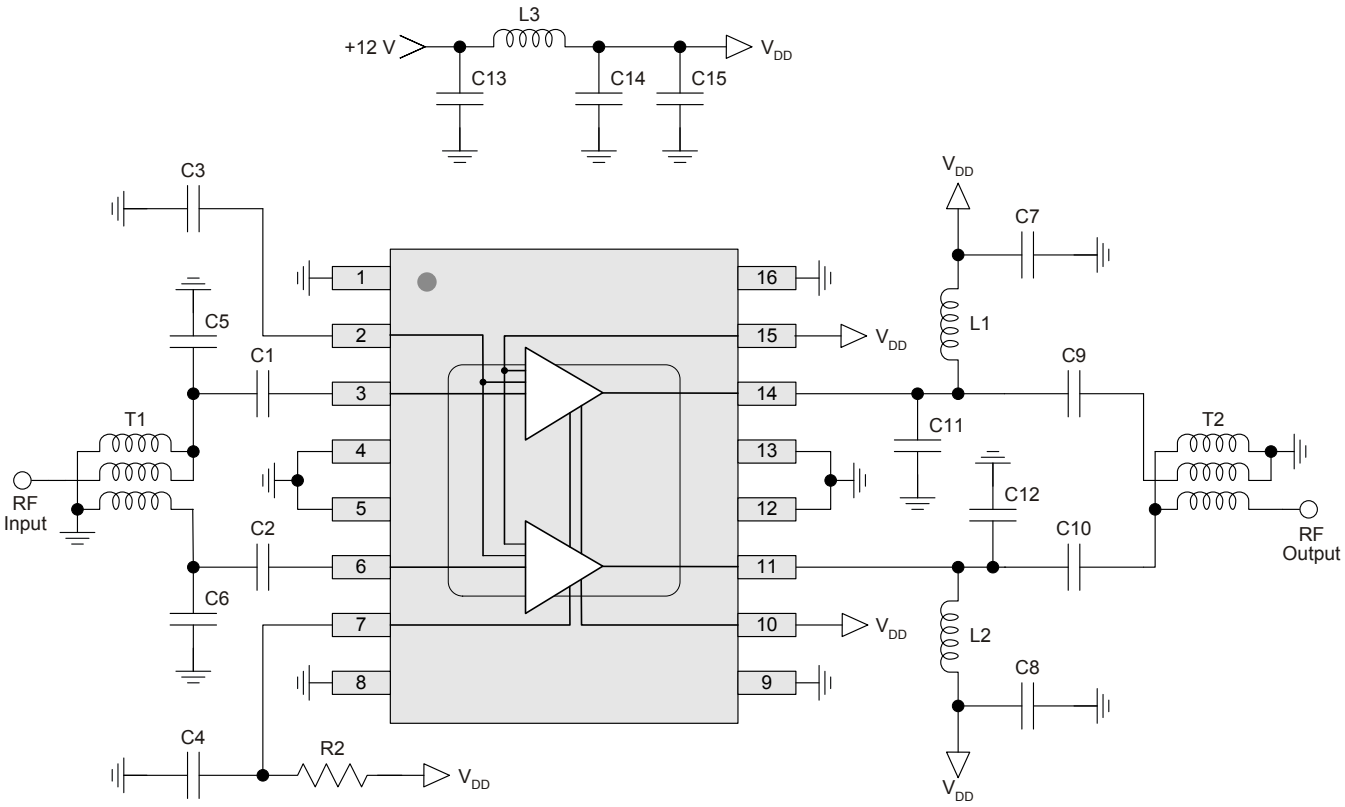
Electrical Specifications

Test conditions unless otherwise noted: V_{DD}=+12 V, I_{CC}=575 mA (typ.), $T_{AMBIENT}$=+25°C, 75 Ω system

Parameter	Conditions	Min	Typ	Max	Units
Operational Frequency Range		40		1000	MHz
Current			575		mA
Gain		10.6	11.2	12.0	dB
Gain Flatness	Peak deviation from least squared fit curve.		±0.25	±0.3	dB
Gain Slope		-1		0	dB
Input Return Loss			20		dB
Output Return Loss			20		dB
CSO	80 ch. NTSC, + 56 dBmV/ch at 1002 MHz, 15.6 dB tilt, QAM from 553 MHz to 1002 MHz at 6 dB offset.		-65		dBc
CTB			-76		dBc
XMOD			-70		dBc
CIN			58		dB
EQAM Vout 4−Ch. ACPR(1)	ACPR2 (750 kHz – 6 MHz) ACPR3 (6 MHz – 12 MHz) ACPR4 (12 MHz – 18 MHz)	60 60 60	61 61 61		dBmV/ch
1-Ch. Harmonics	Pout = 68 dBmV			-63	dBc
Output P1dB			31		dBm
Output IP3	f_1=950 MHz, f_2=1000 MHz, Pout=+17 dBm/tone		54		dBm
Thermal Resistance, θjc	Junction to case		12		°C/W

Notes:
1. Measured against DOCSIS 3.0 specified limits for out of band spurious emissions in adjacent channels

Application Circuit Schematic – TAT2801-PCB

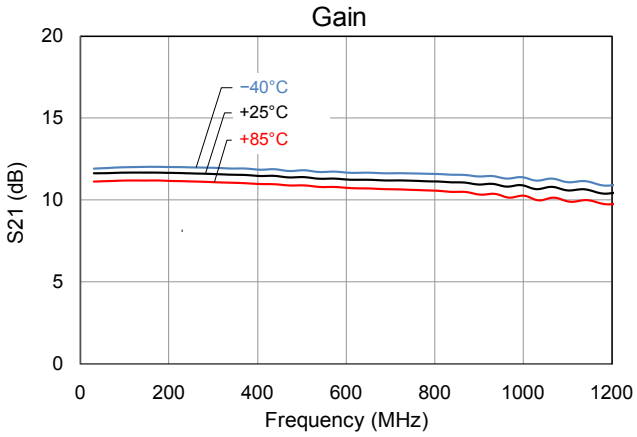


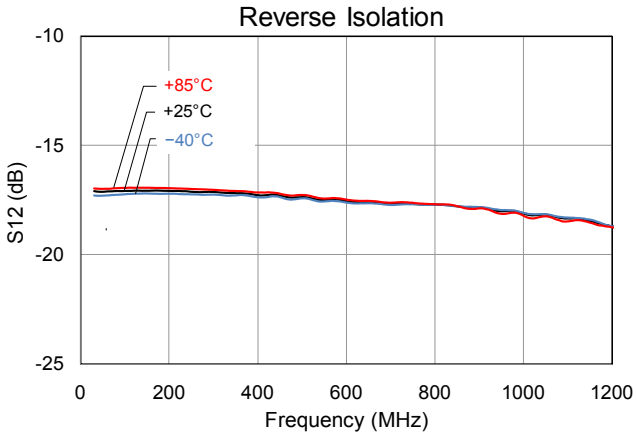
Bill of Material – TAT2801-PCB

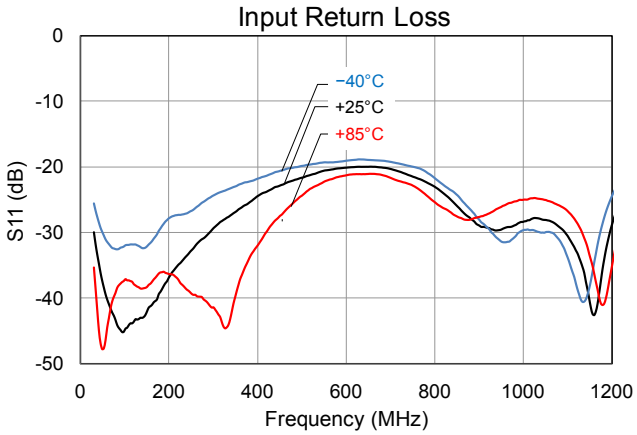
Reference	Value	Description	Manuf.	Part Number
U1	--	40 MHz – 1 GHz, CATV Gain Block	TriQuint	TAT2801
C1, C2, C3, C4	0.01 uF	Cap, Chip, 0402, 16V, 10%	Various	
C5, C6, C11, C12	0.7 pF	Cap, Chip, 0402, 25V, +/-0.075, NPO/COG	Various	
C7, C8, C13, C14	0.01 uF	Cap, Chip, 0603, 25V, 5%, X7R	Various	
C9, C10	330 pF	Cap, Chip, 0402, 50V, 10%, X7R	Various	
C15	DNP		Various	
R2	7.5 kΩ	Res, Chip, 0402, 1%, 1/16W	Various	
L1, L2	500 nH	Ind, Chip, Ferrite, 1206, 10%, 260mA	Various	
L3	0.9 uH	Ind, Chip, 1008, 5%, 1.4A	Coilcraft	1008AF-901XJL
TX1, TX2	1:1	SMT, 75 OHM, BALUN 1:1, SM-118A	M/A-COM	MABA-008483-CT1760

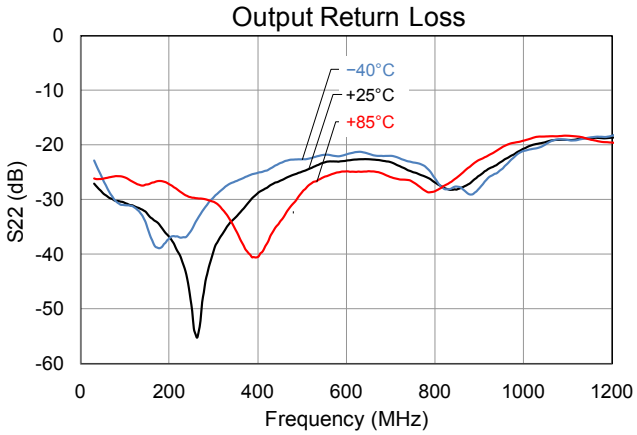
Performance Plots – TAT2801-PCB

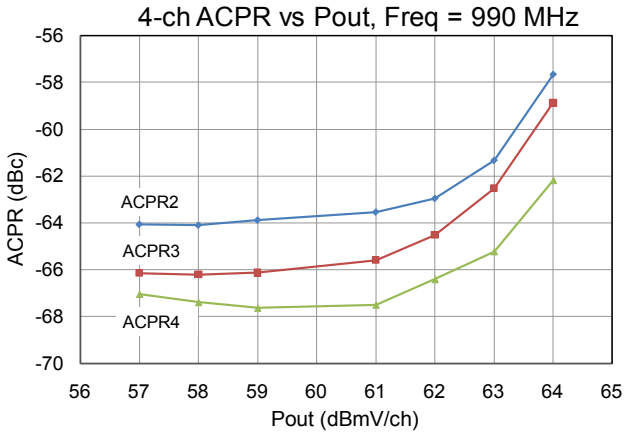
Test conditions unless otherwise noted: V_{DD}=+12 V, I_{CC} = 575 mA (typ.)

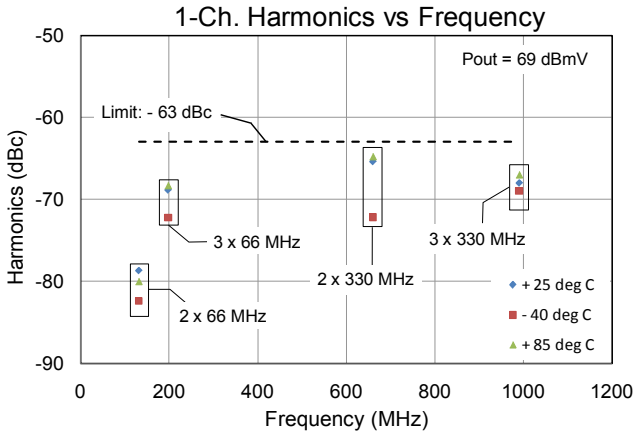






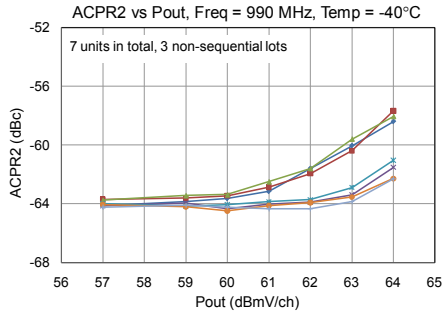


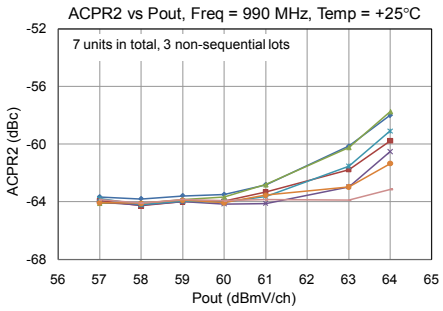


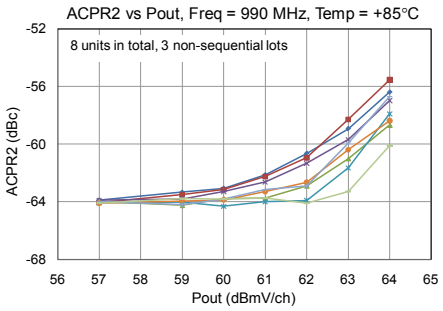


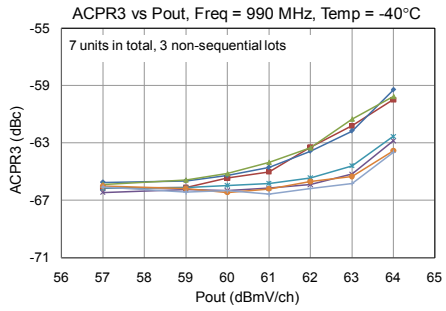
Distortion Performance: Lot to Lot Variation Over Temperature

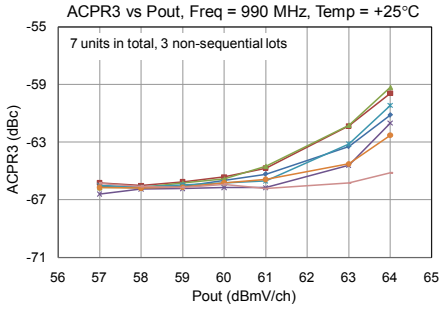
Test conditions unless otherwise noted: V_{DD}=+12 V, I_{CC} = 575 mA (typ.)

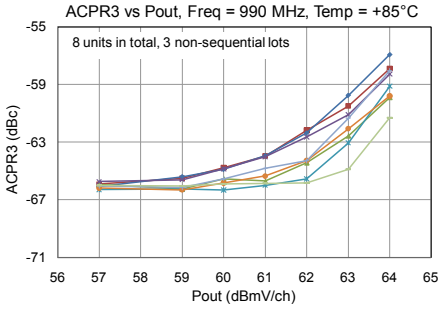


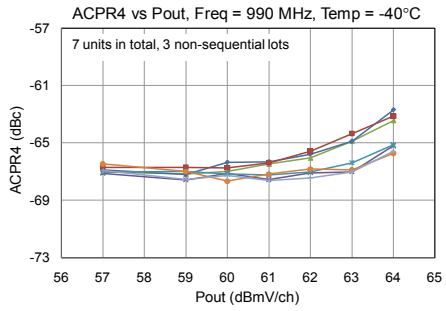


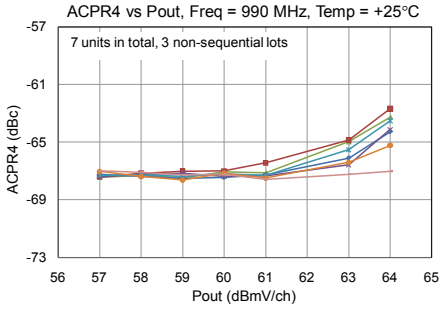


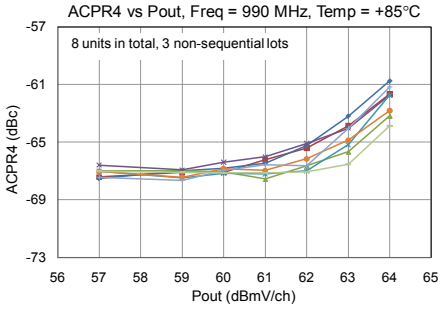






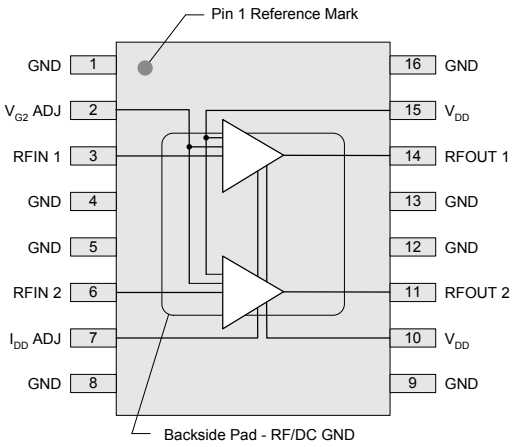






Note: ACPR performance measured using application circuit on pg. 3. ACPR performance at low output power levels is reflective of the limitations of the source. A better test source is likely to result in significantly better ACPR performance at these power levels.

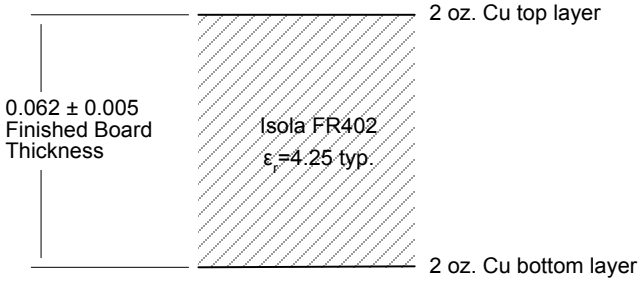
Pin Configuration and Description

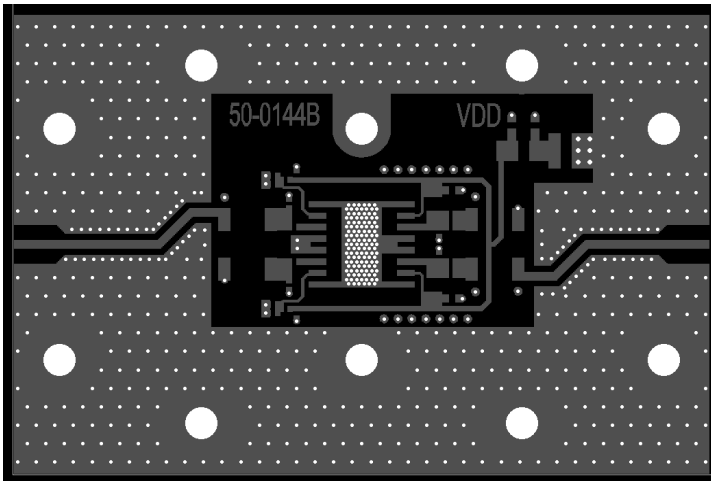


Pin No.	Label	Description
1, 4-5, 8-9, 12-13, 16	GND	Grounded internally within the package. Provide grounded land pads.
2	V_{G2} ADJ	Dropping resistor and bypass capacitor required.
3 / 6	RFINA / RFINB	RF Input A / RF Input B. Impedance matching and DC blocking capacitors required.
7	I_{DD} ADJ	IDD current adjustment. Dropping resistor and bypass capacitor required.
10	V_{DD}	VDD supply for internal biasing
11 / 14	RFOUTB / RFOUTA	RF Output / DC supply. Impedance matching , DC block and bias choke required
15	V_{DD}	VDD supply for internal biasing
Backside Pad	GND	RF/DC ground.

Evaluation Board PCB Information

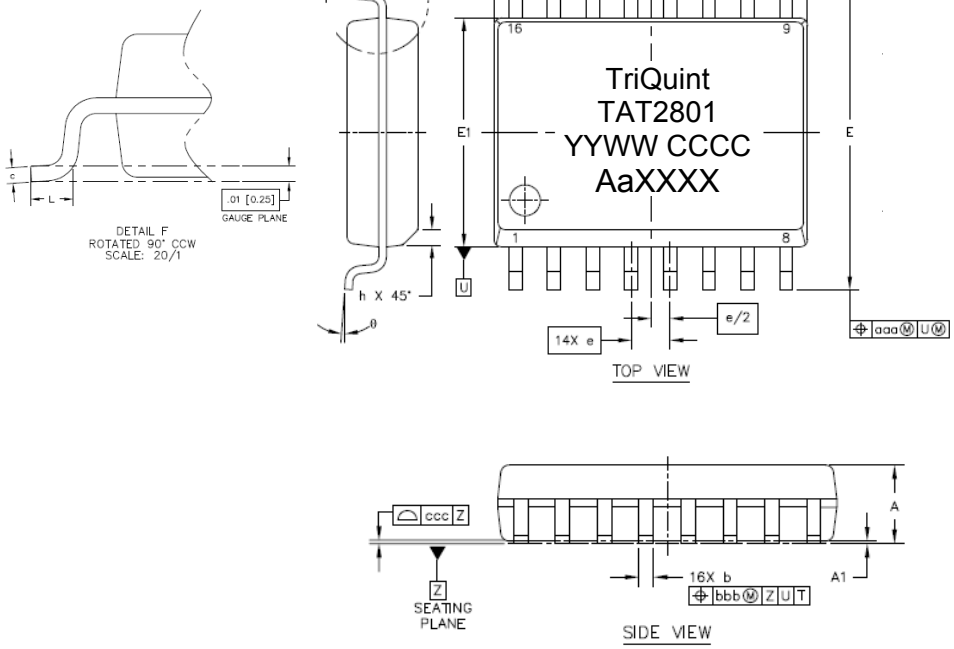
TriQuint Evaluation Board
PCB Material and Stack-up





Package Marking and Dimensions

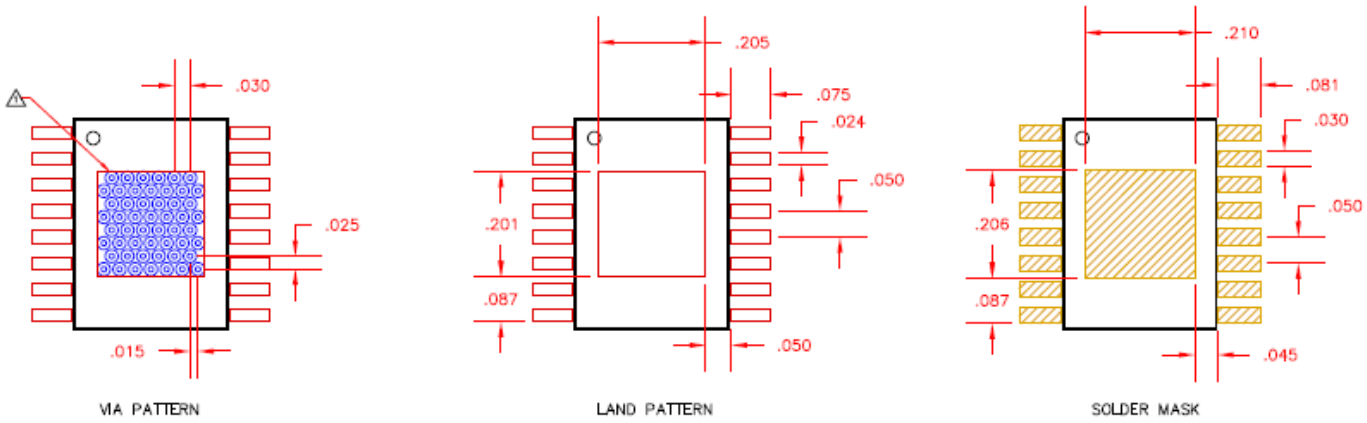
Marking: Part Number – TAT2801
Year/Week/Country Code – YYWW CCCC
Lot code – AaXXXX



Package Dimensions

	Symbol	MIN	TYP	MAX	MIN	TYP	MAX
TOTAL THICKNESS	A	.087		.098	2.2		2.5
STAND OFF	A1	0		.004	0		0.1
LEAD WIDTH	b	.014		.019	0.35		0.49
L/F THICKNESS	c	.009		.013	0.23		0.33
BODY SIZE	D	.400		.411	10.15		10.45
	E1	.291		.299	7.4		7.6
	E	.395		.415	10.05		10.55
LEAD PITCH	e		0.05 BSC			1.27 BSC	
	L	.016		.050	0.4		1.27
	h	.010		.030	0.25		0.75
	θ	0°		8°	0°		8°
EP SIZE	M	.196	.200	.204	4.98	5.08	5.18
	N	.200	.204	.208	5.08	5.18	5.28
LEAD EDGE OFFSET	aaa		.010			0.25	
LEAD OFFSET	bbb		.010			0.25	
COPLANARITY	ccc		.004			0.10	

PCB Mounting Pattern



Notes:

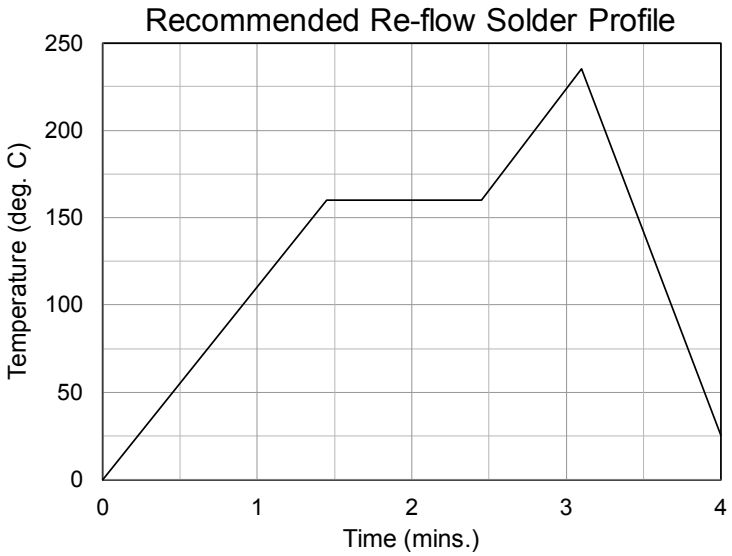
1. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25mm (0.10").
2. Ensure good package backside paddle solder attach for optimum electrical and thermal performance.
3. All dimensions are in millimeters. Angles are in degrees.

Recommended Soldering Temperature Profile

Solder paste manufacturers will recommend a "typical" solder reflow profile depending on their particular solder paste's flux and metal composition. This typical profile entails the parameters necessary for the solder to properly melt and reflow, and defines the thermal condition of the PCB soldering surface to be within an optimum temperature range. The profile is obtained by mounting a thermo couple directly to the solder surface area of the PCB, and recording the actual local surface temperature during the reflow process.

The solder reflow profile shown at right is for a typical SAC305 lead free solder paste application and assumes that standard PCB layout rules have been followed, such as solder mask to dam in molten solder during reflow to keep it from wicking away from the solder joint.

The "oven profile" required to achieve the "solder reflow profile" will vary depending on reflow equipment, PCB, components loaded on the PCB, and other factors such as fixturing.



Thermal Reliability