TAT7461

75 Ω RF Amplifier

Applications

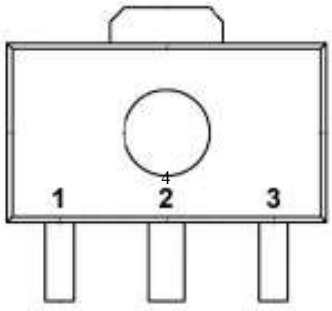
- Distribution Amplifiers
- Multi-Dwelling Units
- Drop Amplifiers
- Single-ended Gain Block

SOT-89 package

Product Features

- 50-1000 MHz bandwidth
- pHEMT device technology
- On-chip negative feedback providing excellent gain and return loss consistency.
- On-chip active bias for consistent bias current and repeatable performance.
- Simple external tuning allows excellent return loss.
- 6 V supply voltage
- 130 mA typical current consumption
- 16.1 dB typical gain
- 2.3 dB typical NF and < 2.6 dB up to 1000 MHz
- +39 dBm typical OIP3
- +22 dBm typical P1dB
- Low distortion: CSO -72 dBc, CTB -88 dBc
- (26 dBmV/ch at output, 80 ch)
- SOT-89 package

Functional Block Diagram



RF IN GND RFOUT

General Description

The TAT7461 is a 75 Ω RF Amplifier designed for CATV applications to 1000 MHz. The balance of low noise, excellent distortion, and high-gain is applicable for drop and other distribution amplifiers.

The TAT7461 is fabricated using 6-inch GaAs pHEMT technology to optimize performance and cost. It provides consistent gain and return loss from the use of extensive on-chip negative feedback. The TAT7461 also uses an on-chip active bias for consistent bias current and repeatable performance. Simple external tuning allows the TAT7461 to achieve excellent return loss.

Pin Configuration

Pin #	Symbol
1	RF IN
2	GND
3	RF OUT
4	GND PADDLE

Ordering Information

Part No.	Description
TAT7461	75 Ω High linearity pHEMT amplifier (lead-free/RoHS compliant SOT-89 Pkg)
TAT7461-EB	Amplifier Evaluation Board

Standard T/R size = 1000 pieces on a 7" reel.

Specifications

Absolute Maximum Ratings[1]

Parameter	Rating
Storage Temperature	-65 to +150 °C
Device Voltage	+10 V
Thermal Resistance[2] (jnt to case) θ_{jc}	42 °C/W

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{DD}		6		V
I_{DD}	100	130	150	mA
T_J (for > 10^6 hours MTTF)			150	°C

Notes:
1. Operation of this device outside the parameter ranges given above may cause permanent damage.
2. Refer to Thermal Analysis Report TAT7461, Report No. 30-0011 Rev B.

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

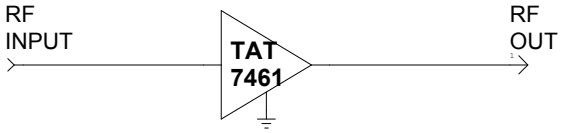
Test conditions unless otherwise noted: 25 ºC, +6 V V_{DD}

Parameter	Conditions	Min	Typical	Max	Units
Operational Frequency Range		50		1000	MHz
Gain			16.1		dB
Gain Flatness			+/- 0.3		dB
Noise Figure			2.3		dB
Input Return Loss			23		dB
Output Return Loss			23		dB
CSO	See Note 1.		-72		dBc
CTB	See Note 1.		-88		dBc
Output IP2	See Note 2.		+61		dBm
Output IP3	See Note 2.		+39		dBm
Vsupply			+6		V
I_{DD}		100	130	150	mA

Notes:
1. 26 dBmV/ch at output, 80 ch flat
2. At 5 dBm/tone
3. Electrical specifications are measured at specified test conditions.
4. Specifications are not guaranteed over all recommended operating conditions.

Device Characterization Data

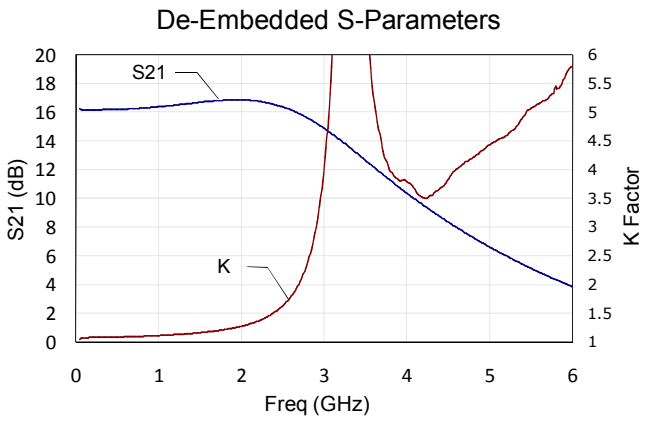
S PARAMETER SCHEMATIC

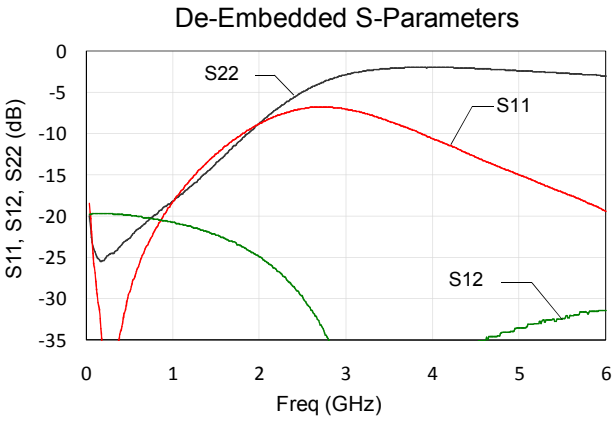


Measured in 50 ohms
Conversion to 75 ohms done in CAD package
Biasing done through Agilent 8753 Test Set

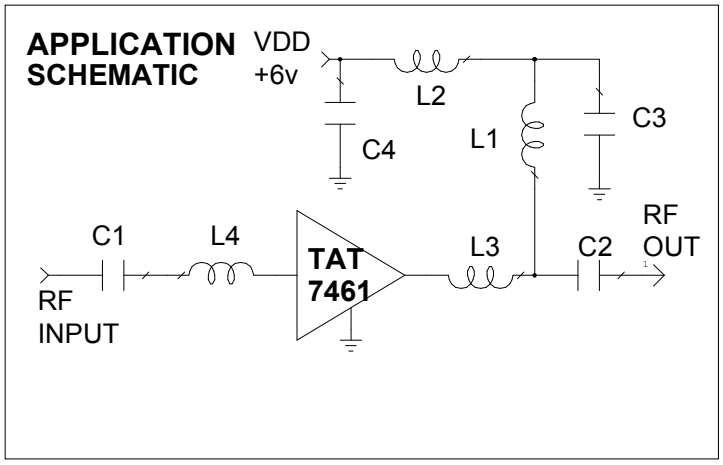
S-Parameter Data

V_{DD} = +6 V, I_{DD} = 130 mA





Application Circuit 50-1000 MHz



Notes:
1. See PC Board Layout, page 6 for more information.

Bill of Material

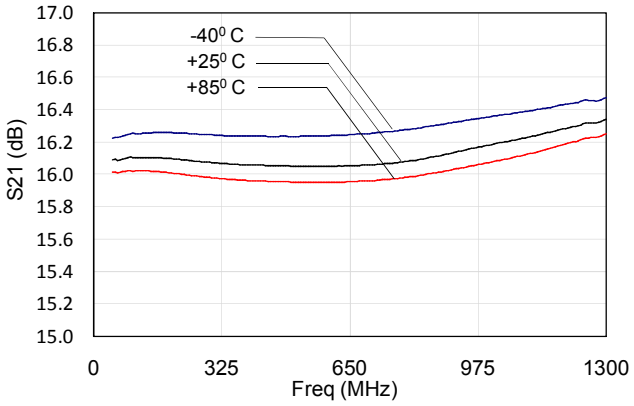
Ref. Desg.	Value	Description	Manufacturer	Part Number
U1		75 Ω High Linearity pHEMT Amplifier	TriQuint	TAT7461
L1, L2	880 nH	Chip Coil, Vertical Wire Wound Ferrite, 1206, 30 %	Murata[1]	LQH31HNR88K
L3	5.1 nH	Ceramic Chip Ind., Wire-wound, 0402, 5 %	Coilcraft	0402CS-5N1XJLW
L4	2.7 nH	Ceramic Chip Ind., Wire-wound, 0402, 5 %	Coilcraft	0402CS-2N7XJLW
C1	1000 pF	Ceramic Chip Cap., 0402, 50 V, 10 %, X7R	AVX[1]	04025C102KAT2A
C2	120 pF	Ceramic Chip Cap., 0402, 50 V, 5 %, NPO	AVX[1]	04025A121JAT2A
C3, C4	0.01 uF	Ceramic Chip Cap., 0402, 16 V, 10 %, X7R	AVX[1]	0402YC103KAT
J1, J2		75 Ω F connector	Lighthorse[1]	FSF55MGT-P-10A

Notes:
1. Or equivalent.

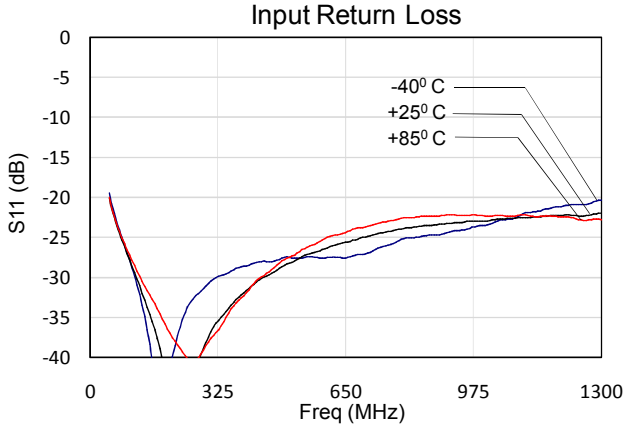
Application Board Typical Performance

V_{DD} = +6 V, I_{DD} = 130 mA

Gain

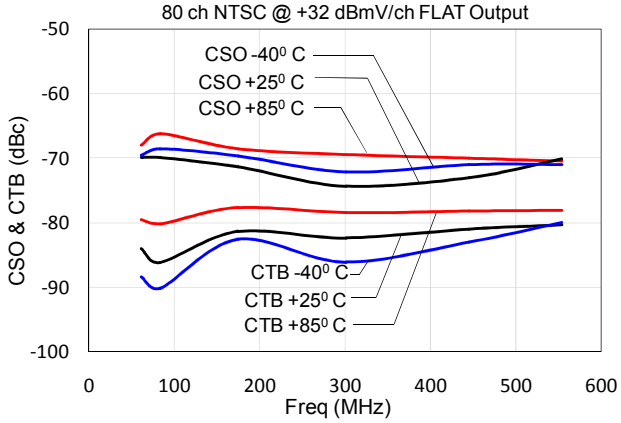


Input Return Loss

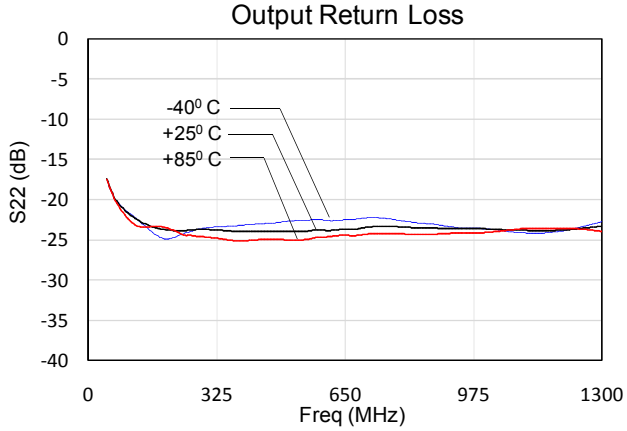


CSO & CTB

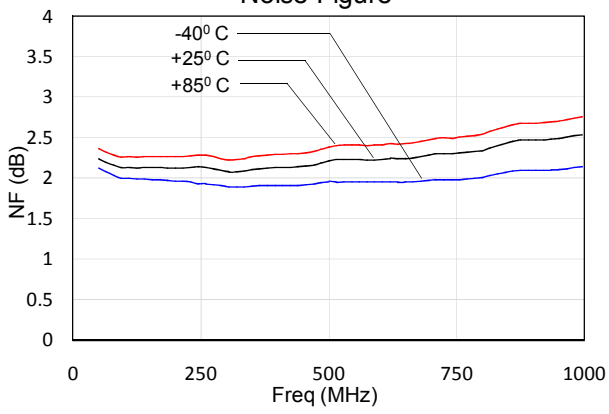
80 ch NTSC @ +32 dBmV/ch FLAT Output



Output Return Loss



Noise Figure



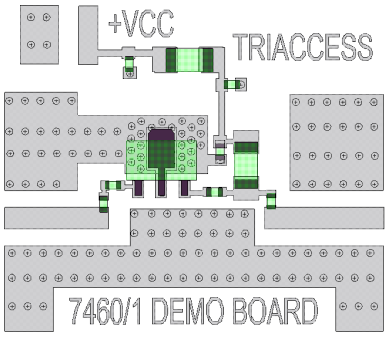
Applications Information

PC Board Layout

Core is .062" FR-4, ϵ_r = 4.7. Metal layers are 1-oz copper.

The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

For further technical information, refer to:
http://www.triquint.com/TAT7461



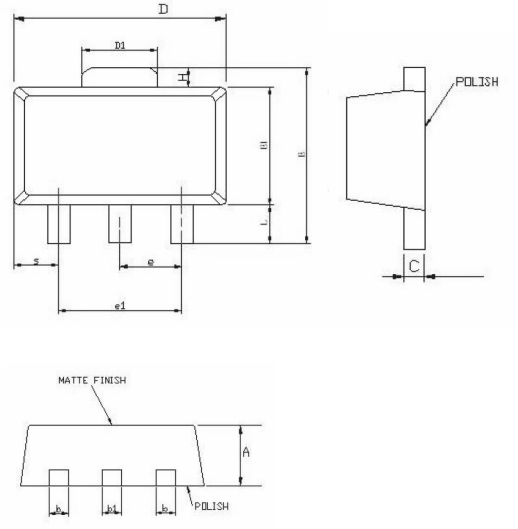
Mechanical Information

Package Information and Dimensions

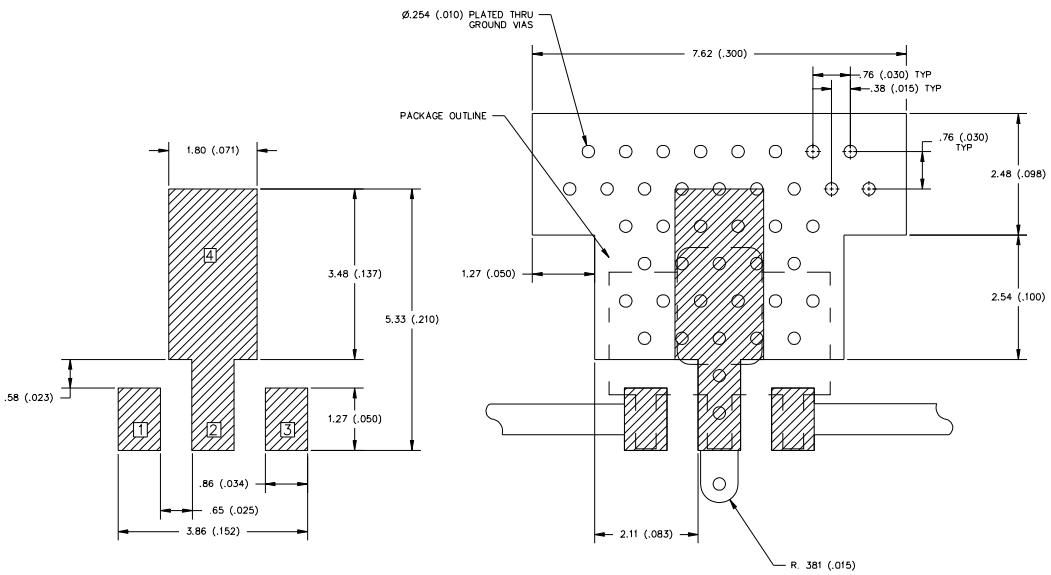
This package is lead-free/RoHS-compliant. The plating material on the leads is 100 % Matte Tin. It is compatible with both lead-free (maximum 260 °C reflow temperature) and lead (maximum 245 °C reflow temperature) soldering processes.

The TAT7461 will be marked with a "TAT7461" designator and an 8 digit alphanumeric lot code (XXXXYYWW). The first four digits are the lot code (XXXX). The last four digits are a date code consisting of the year and work week (YYWW) of assembly.

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.40	1.50	1.60	0.055	0.059	0.063
L	0.89	1.04	1.20	00350	0.041	0.047
b	0.36	0.42	0.48	0.014	0.016	0.018
b1	0.41	0.47	0.53	0.016	0.018	0.020
C	0.38	0.40	0.43	0.014	0.015	0.017
D	4.40	4.50	4.60	0.173	0.177	0.181
D1	1.40	1.60	1.75	0.055	0.062	0.069
E	3.64	—	4.25	0.143	—	0.167
E1	2.40	2.50	2.60	0.094	0.098	0.102
e1	2.90	3.00	3.10	0.114	0.118	0.122
H	0.35	0.40	0.45	0.014	0.016	0.018
S	0.65	0.75	0.85	0.026	0.030	0.034
e	1.40	1.50	1.60	0.054	0.059	0.063



Mounting Configuration



Notes:
1. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35 mm (#80/.0135") diameter drill and have a final, plated thru diameter of .25 mm (.010").
2. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
3. RF trace width depends upon the PC board material and construction.
4. All dimensions are in millimeters (inches). Angles are in degrees.

Product Compliance Information

ESD Information

Caution! ESD-Sensitive Device

ESD Rating:	Class 1 A
Value:	Passes ≥ 450 V min.
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114

ESD Rating:	Class IV
Value:	Passes ≥ 1000 V min.
Test:	Charged Device Model (CDM)
Standard:	JEDEC Standard JESD22-C101

MSL Rating

Level 3 at +260 °C convection reflow.
The part is rated Moisture Sensitivity Level 3 at 260 °C per JEDEC standard IPC/JEDEC J-STD-020.

Solderability

Compatible with the latest version of J-STD-020, Lead free solder, 260 °C.

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).