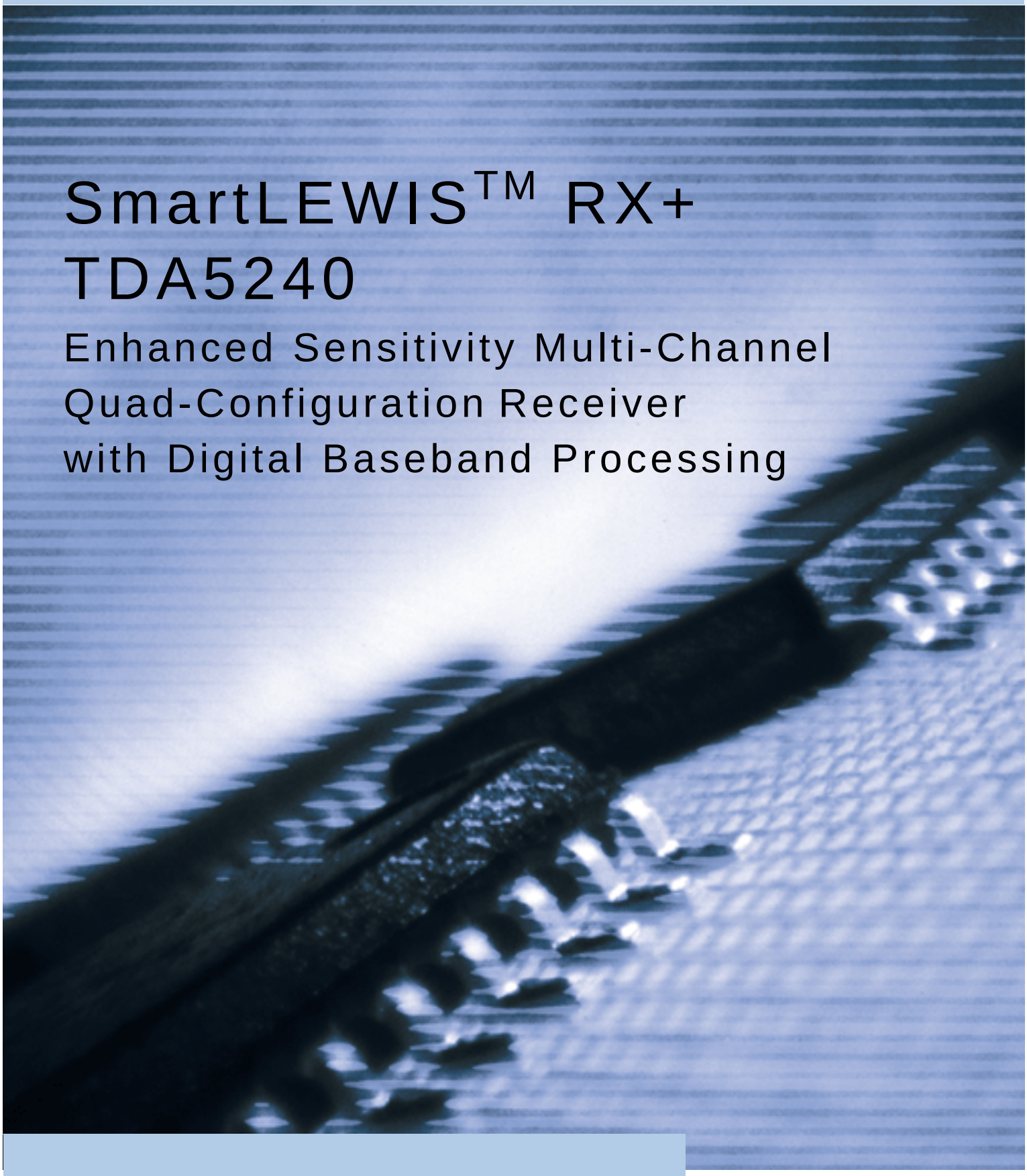

SmartLEWIS™ RX+ TDA5240

Enhanced Sensitivity Multi-Channel Quad-Configuration Receiver with Digital Baseband Processing

Wireless Control

Never stop thinking.

Edition February 19, 2010

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Enhanced Sensitivity Multi-Channel Quad-Configuration Receiver with Digital Baseband Processing

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TDA5240

Revision Number:	**010**	
Revision History:	**2010-02-19**	V4.0
Previous Version:	TDA5240_V3.4	

Page	Subjects (major changes since last revision)
Page 27	Update of Figure 9
Page 29	Update of Figure 10
Page 31	AFC limitation added
Page 33	AGC setting proposal added
Page 34	New Section 2.4.6.5 ADC added
Page 36	Additional information on RSSIPRX register inserted
Page 41	Signal and Noise Detector Procedure adapted
Page 45	x_CDRRI register recommendation changed
Page 49, 52, 56	Data Slicer Modes adapted; limitation added
Page 69	Update of Figure 41
Page 70	Update of Figure 42
Page 78	Additional hint on clock and data recovery algorithm of the user software inserted
Page 84	PLDLEN limitation added
Page 86	Limitation for ISx readout and Burst-read function added
Page 88	Limitation for Burst-read function added
Page 107	Description of “Parallel Wake-up Search” adapted
Page 125	Additional hints added
Page 127	Adaption of Section 4.1
Page 130	New item C7 added
Page 138 f	Comments added for items I6, I7, I8, I9, J11, J12
Page 138	Item J1 updated
Page 141 ff	General test conditions noted for parameters K, L and M
Page 147	BOM components C7, C8, L1, R2 and R3 updated

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Wirelesscontrol@infineon.com

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1 Product Description

1.1 Overview

The IC is a low power ASK/FSK Receiver for the frequency bands 300-320, 425-450, 863-870 and 902-928 MHz. Bi-phase modulation schemes, like Manchester, bi-phase mark, bi-phase space and differential Manchester are supported.

The chip offers best-in-class sensitivity performance at a very high level of integration and needs only a few external components.

The device is qualified to automotive quality standards and operates between -40 and +105°C at supply voltage ranges of 3.0-3.6 Volts or 4.5-5.5 Volts.

The receiver is realized as a double down conversion super-heterodyne/low-IF architecture each with image rejection supplemented by digital signal processing in the baseband. A fully integrated Sigma-Delta Fractional-N PLL Synthesizer allows for high-resolution frequency generation and uses a crystal oscillator as the reference. The on-chip temperature sensor may be utilized for temperature drift compensation via the crystal oscillator.

The digital baseband processing unit together with the high performance down converter is the key element for the exceptional sensitivity performance of the device which take it close to the theoretical top-performance limits. It comprises signal and noise detectors, matched data filter, clock and data recovery, data slicer and a format decoder. It demodulates the received ASK or FSK data stream independently and recovers the data clock out of the received data stream with very fast synchronization times which can then be either accessed via separate pins or used for further processing like frame synchronization and intermediate storage in the on-chip FIFO. The RSSI output signal is converted to the digital domain with an ADC. All these signals are accessible via the 4-wire SPI interface bus. Up to 4 pre-configured telegram formats can be stored into the device offering independent pre-processing of the received data to an extent not available till now. The down converter can be also configured in single-conversion mode at moderately reduced selectivity performance but at the advantage of omitting the IF ceramic filter.

1.2 Features

- Enhanced sensitivity receiver
- Multi-band/Multi-Channel (300-320, 425-450, 863-870 and 902-928 MHz)
- One crystal frequency for all supported frequency bands
- 21-bit Sigma-Delta Fractional-N PLL synthesizer with high resolution of 10.5 Hz
- Up to 4 parallel parameter sets for autonomous scanning and receiving from different sources reduces significantly host processor power consumption and system standby power consumption
- Up to 12 different frequency channels are supported with 10.5 Hz resolution each
- Autonomous receive mode leads to reduced noise of host processor and improved system performance
- Ultrafast Wake-up on RSSI
- Fast synchronization on incoming data stream typically within first 4 bits of a telegram
- Selectable IF filter bandwidth and optional external filters possible
- Double down conversion image reject mixer
- ASK and FSK capability
- Automatic Frequency Control (AFC) for carrier frequency offset compensation
- Supports bi-phase line codes like Manchester, bi-phase mark/space and differential Manchester
- NRZ data pre-processing capability
- Digital base band receiver with clock synch, frame synch, format decoding and FIFO
- Separate outputs for recovered data and clock
- RSSI peak detectors
- Wake-up generator and polling timer unit
- Message ID scanning
- Unique 32-bit serial number
- On-chip temperature sensor
- Integrated timer usable for external watch unit
- Integrated 4-wire SPI interface bus
- Supply voltage range 3.0 Volts to 3.6 Volts or 4.5 Volts to 5.5 Volts
- Operating temperature range -40 to +105°C
- ESD protection +/- 2 kV on all pins
- Package PG-TSSOP-28

1.3 Applications

- Remote keyless entry systems
- Remote start applications
- Tire pressure monitoring
- Short range radio data transmission
- Remote control units
- Cordless alarm systems
- Remote metering

2 Functional Description

2.1 Pin Configuration

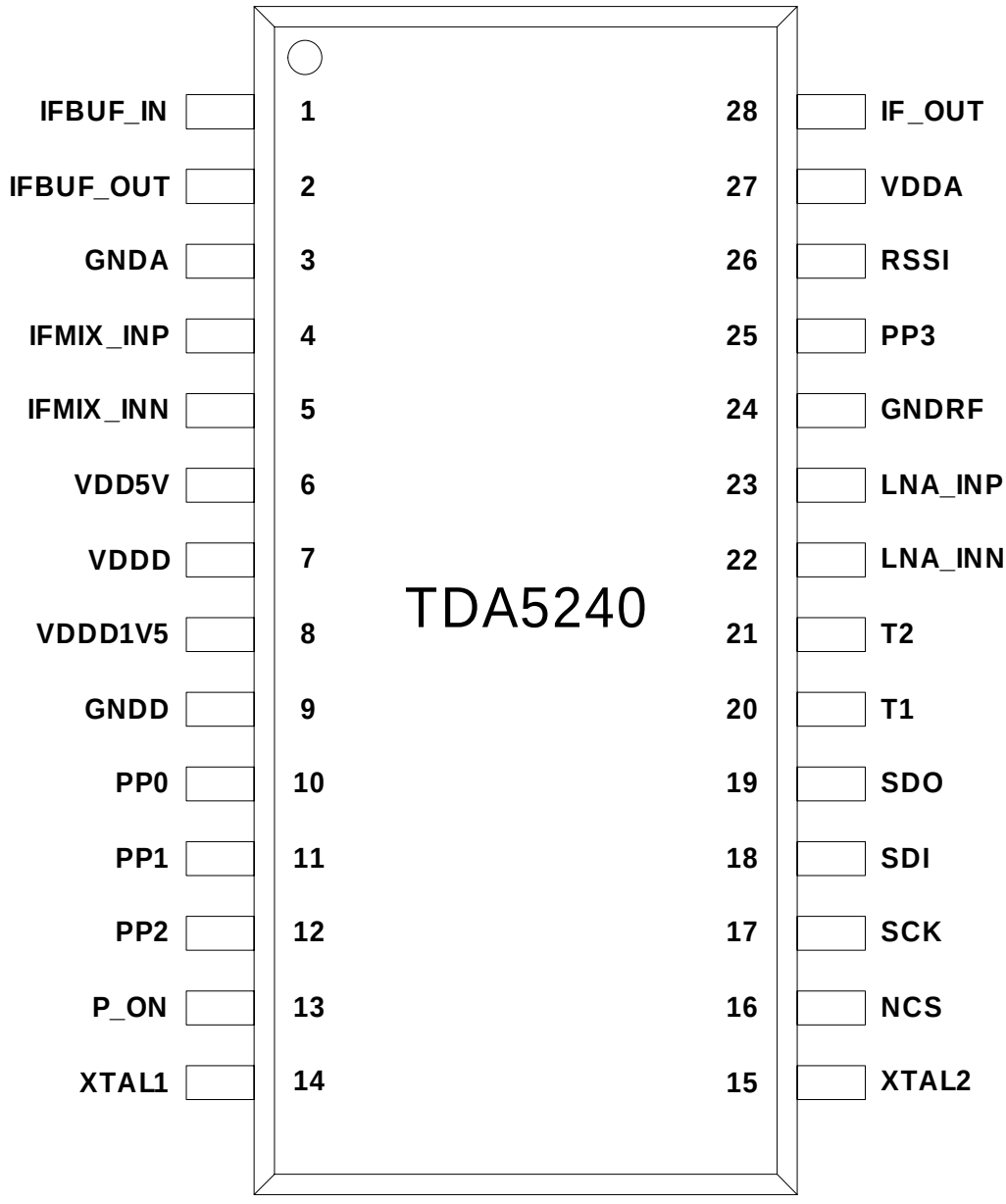
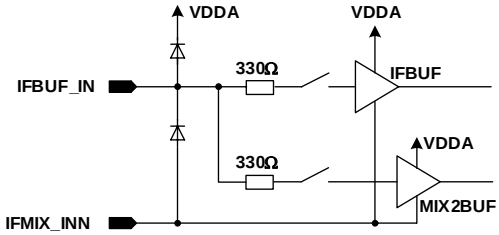
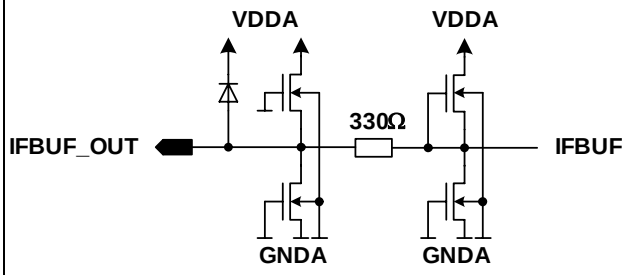
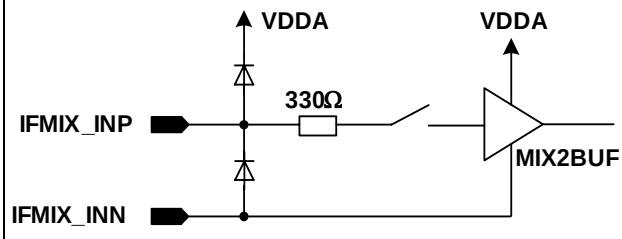
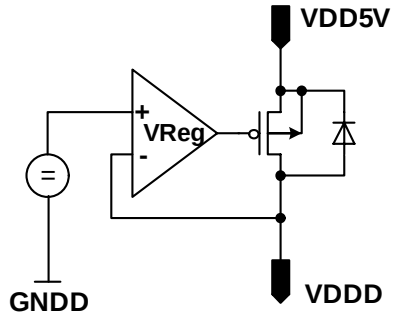
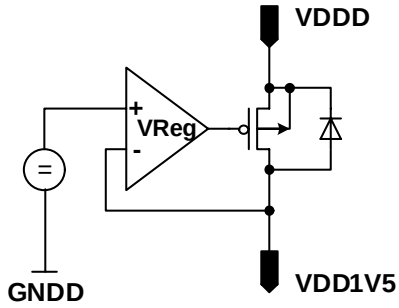
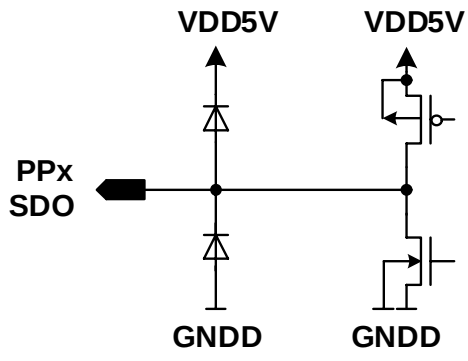


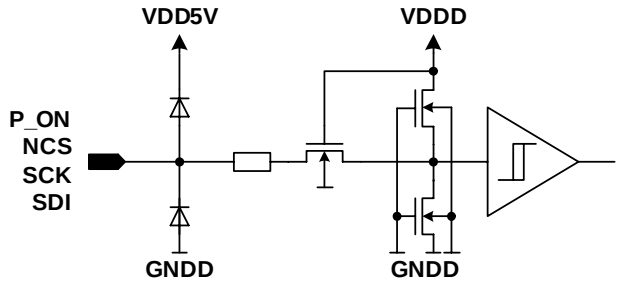
Figure 1 Pin-out

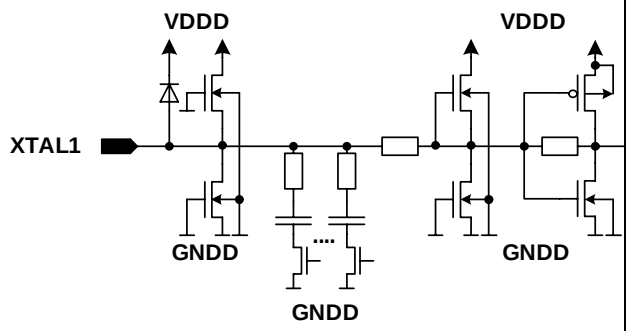
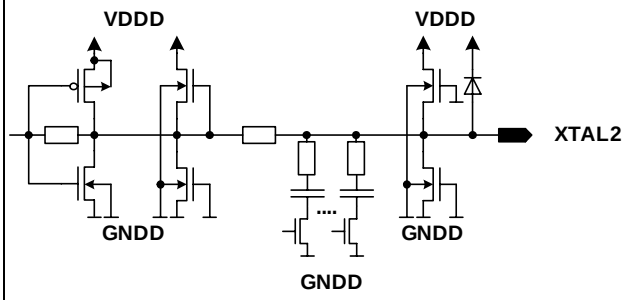
2.2 Pin Definition and Pin Functionality

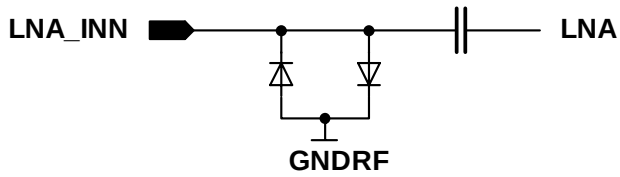
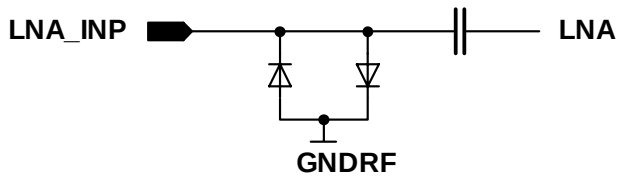
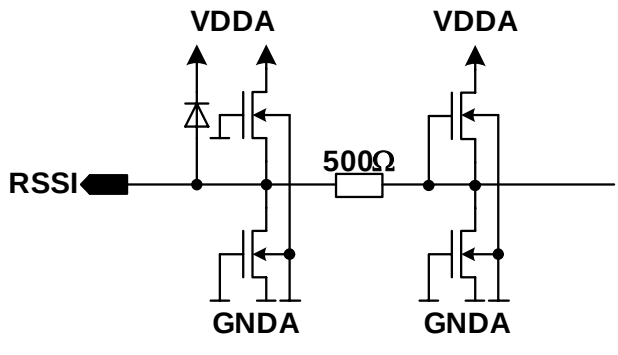
Table 1 Pin Definition and Function

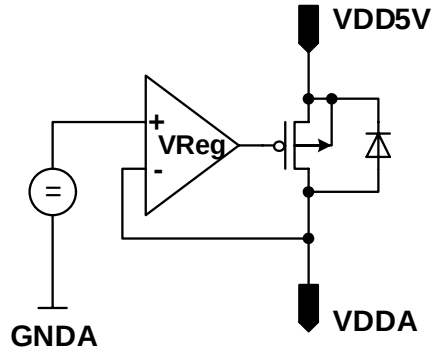
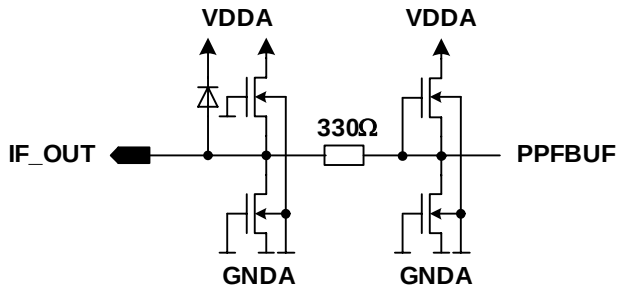
Pin No.	Pad name	Equivalent I/O Schematic	Function
1	IFBUF_IN		Analog input IF Buffer input Note: Input is biased at VDDA/2
2	IFBUF_OUT		Analog output IF Buffer output
3	GNDA		Analog ground
4	IFMIX_INP		Analog input + IF mixer input Note: Input is biased at VDDA/2
5	IFMIX_INN	see schematic of Pin 1 and 4	Analog input. - IF mixer input
6	VDD5V		Analog input 5 Volt supply input

Pin No.	Pad name	Equivalent I/O Schematic	Function
7	VDDD		Analog input digital supply input
8	VDDD1V5		Analog output 1.5 Volt voltage regulator
9	GNDD		Digital ground
10	PP0		Digital output CLK_OUT, RX_RUN, NINT, LOW, HIGH, DATA, DATA_MATCHFIL, CH_DATA, CH_STR, RXD and RXSTR are programmable via a SFR (Special Function Register), default = CLK_OUT

Pin No.	Pad name	Equivalent I/O Schematic	Function
11	PP1	see schematic of Pin 10	Digital output CLK_OUT, RX_RUN, NINT, LOW, HIGH, DATA, DATA_MATCHFIL, CH_DATA, CH_STR, RXD and RXSTR are programmable via a SFR, default = DATA
12	PP2	see schematic of Pin 10	Digital output CLK_OUT, RX_RUN, NINT, LOW, HIGH, DATA, DATA_MATCHFIL, CH_DATA, CH_STR, RXD and RXSTR are programmable via a SFR, default = NINT
13	P_ON		Digital input power-on reset

Pin No.	Pad name	Equivalent I/O Schematic	Function
14	XTAL1		Analog input crystal oscillator input
15	XTAL2		Analog output crystal oscillator output
16	NCS	see schematic of Pin 13	Digital input SPI enable
17	SCK	see schematic of Pin 13	Digital input SPI clock
18	SDI	see schematic of Pin 13	Digital input SPI data in
19	SDO	see schematic of Pin 10	Digital output SPI data out
20	T1		Digital input, connect to Digital Ground
21	T2		Digital input, connect to Digital Ground

Pin No.	Pad name	Equivalent I/O Schematic	Function
22	LNA_INN		Analog input - RF input
23	LNA_INP		Analog input + RF input
24	GNDRF		RF analog ground
25	PP3	see schematic of Pin 10	Digital output RX_RUN, NINT, LOW, HIGH, DATA, DATA_MATCHFIL, CH_DATA, CH_STR, RXD and RXSTR are programmable via a SFR, default = RX_RUN
26	RSSI		Analog output analog RSSI output/ analog test pin ANA_TST

Pin No.	Pad name	Equivalent I/O Schematic	Function
27	VDDA		Analog input Analog supply
28	IF_OUT		Analog output IF output

2.3 Functional Block Diagram

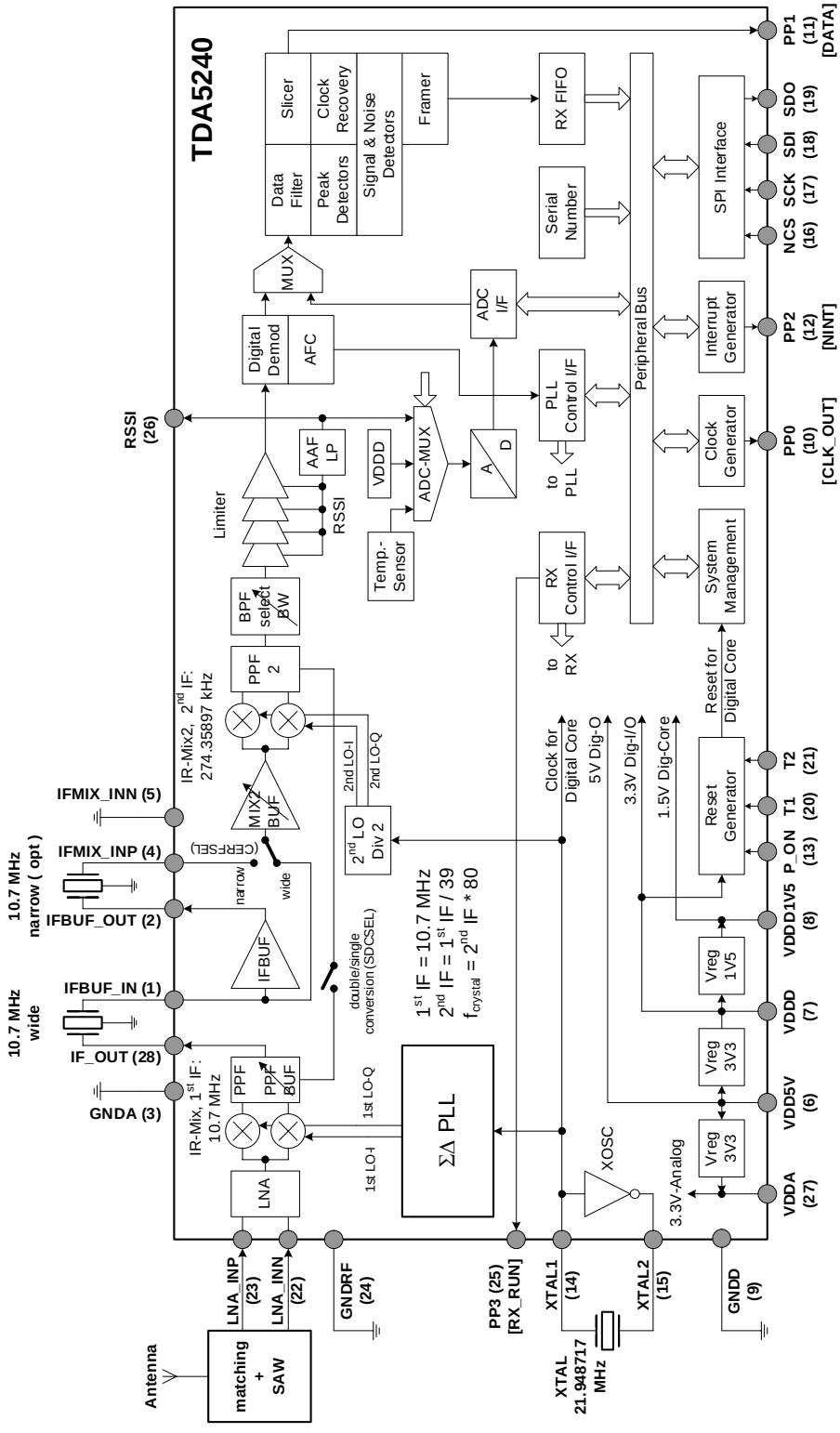


Figure 2 TDA5240 Block Diagram[1)]

1) The function on each PPx port pin can be programmed via SFR (see also **Table 1**). Default values are given in squared brackets in **Figure 2**.

2.4 Functional Block Description

2.4.1 Architecture Overview

A fully integrated Sigma-Delta Fractional-N PLL Synthesizer covers the frequency bands 300-320 MHz, 425-450 MHz, 863-870 MHz, 902-928 MHz with a high frequency resolution, using only one VCO running at around 3.6 GHz. This makes the IC most suitable for Multi-Band/Multi-Channel applications.
For Multi-Channel applications a very good channel separation is essential. To achieve the necessary high sensitivity and selectivity a double down conversion super-heterodyne architecture is used. The first IF frequency is located around 10.7 MHz and the second IF frequency around 274 kHz. For both IF frequencies an adjustment-free image frequency rejection feature is realized. In the second IF domain the filtering is done with an on-chip third order bandpass polyphase filter. A multi-stage bandpass limiter completes the RF/IF path of the receiver. For Single-Channel applications with relaxed requirements to selectivity, a single down conversion low-IF scheme can be selected.

For Multi-Channel systems where even higher channel separation is required, up to two (switchable) external ceramic (CER) filters can be used to improve the selectivity.
An RSSI generator delivers a DC signal proportional to the applied input power and is also used as an ASK demodulator. Via an anti-aliasing filter this signal feeds an ADC with 10 bits resolution.
The harmonic suppressed limiter output signal feeds a digital FSK demodulator. This block demodulates the FSK data and delivers an AFC signal which controls the divider factor of the PLL synthesizer.
A digital receiver, which comprises RSSI peak detectors, a matched data filter, a clock and data recovery, a data slicer, a frame synchronization and a data FIFO, decodes the received ASK or FSK data stream. The recovered data and clock signals are accessible via 2 separate pins. The FIFO data buffer is accessible via the SPI bus interface.
The crystal oscillator serves as the reference frequency for the PLL phase detector, the clock signal of the Sigma-Delta modulator and divided by two as the 2^{nd} local oscillator signal. To accelerate the start up time of the crystal oscillator two modes are selectable: a Low Power Mode (with lower precision) and a High Precision Mode.

2.4.2 Block Overview

The TDA5240 is separated into the following main blocks:

- **RF / IF Receiver**
- **Crystal Oscillator and Clock Divider**
- **Sigma-Delta Fractional-N PLL Synthesizer**
- **ASK / FSK Demodulator incl. AFC, AGC and ADC**
- **RSSI Peak Detector**
- **Digital Baseband Receiver**
- **Power Supply Circuitry**
- **System Interface**
- **System Management Unit**

2.4.3 RF/IF Receiver

The receiver path uses a double down conversion super-heterodyne/low-IF architecture, where the first IF frequency is located around 10.7 MHz and the second IF frequency around 274 kHz. For the first IF frequency an adjustment-free image frequency rejection is realized by means of two low-side injected I/Q-mixers followed by a second order passive polyphase filter centered at 10.7 MHz (PPF). The I/Q-oscillator signals for the first down conversion are delivered from the PLL synthesizer. The frequency selection in the first IF domain is done by an external CER filter (optionally by two, decoupled by a buffer amplifier). For moderate or low cost applications, this ceramic filter can be substituted by a simple LC Pi-filter or completely by-passed using the receiver as a single down conversion low-IF scheme with 274 kHz IF frequency. The down conversion to the second IF frequency is done by means of two high-side injected I/Q-mixers together with an on-chip third order bandpass polyphase filter (PPF2 + BPF). The I/Q-oscillator signals for the second down conversion are directly derived by division of two from the crystal oscillator frequency. The bandwidth of the bandpass filter (BPF) can be selected from 50 kHz to 300 kHz in 5 steps. For a frequency offset of -150 kHz to -120 kHz, the AFC (Automatic Frequency Control) function is mandatory. Activated AFC option might require a longer preamble sequence in the receive data stream.

The receiver enable signal (RX_RUN) can be offered at each of the port pins to control external components. Whenever the receiver is active, the RX_RUN output signal is active. Active high or active low is configurable via PPCFG2 register.

The frequency relations are calculated with the following formulas:

$$f_{IF1} = 10.7MHz$$

$$f_{IF2} = \frac{f_{IF1}}{39}$$

$$f_{crystal} = f_{IF2} \times 80$$

$$f_{LO2} = \frac{f_{crystal}}{2}$$

$$f_{LO1} = f_{crystal} \times NF_{divider}$$

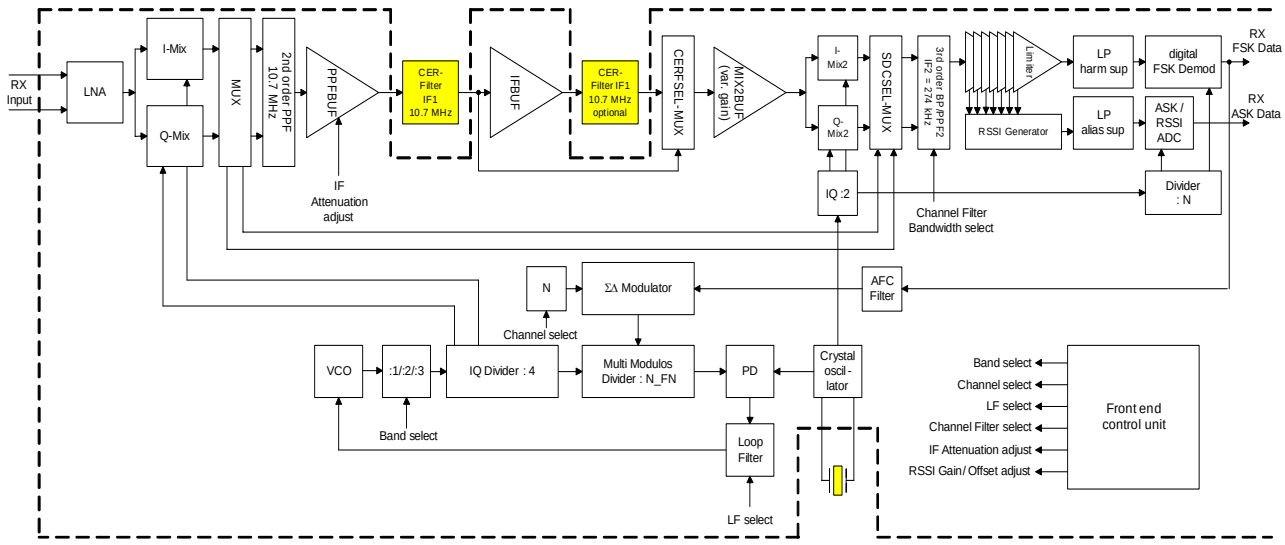


Figure 3 Block Diagram RF Section

The front end of the receiver comprises an LNA, an image reject mixer and a digitally gain controlled buffer amplifier. This buffer amplifier allows the production spread of the on-chip signal strip, of external matching circuitry and RF SAW and ceramic IF filters to be trimmed. The second image reject mixer down converts the first IF to the second IF.

The bandpass filter follows the subsequent formula:

$$f_{center} = \sqrt{f_{corner,\,low} \times f_{corner,\,high}}$$

Therefore asymmetric corner frequencies can be observed. The use of AFC results in more symmetry.

A multi-stage bandpass limiter at a center frequency of 274 kHz completes the receiver chain. The -3dB corner frequencies of the bandpass limiter are typically at 75 kHz and at 520 kHz.

An RSSI generator delivers a DC signal proportional to the applied input power and is also used as an ASK demodulator. Via a programmable anti-aliasing filter this signal is converted to the digital domain by means of a 10-bit ADC.

The limiter output signal is connected to a digital FSK demodulator.

The immunity against strong interference frequencies (so called blockers) is determined by the available filter bandwidth, the filter order and the 3rd order intercept point of the front end stages. For Single-Channel applications with moderate requirements to the selectivity the performance of the on-chip 3rd order bandpass polyphase filter might be sufficient. In this case no external filters are necessary and a single down conversion architecture can be used, which converts the input signal frequency directly to the 2nd IF frequency of 274 kHz.

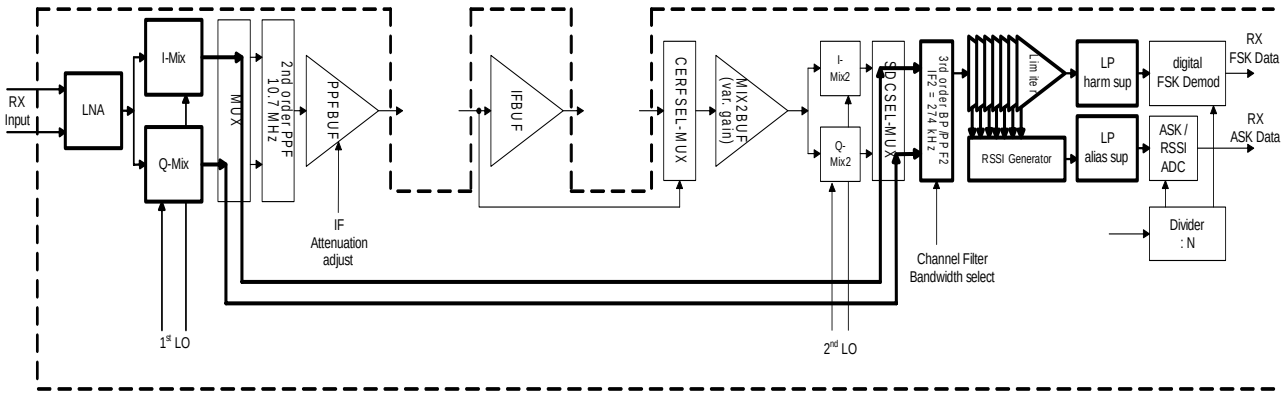


Figure 4 Single Down Conversion (SDC, no external filters required)

For Multi-Channel applications or systems which demand higher selectivity the double down conversion scheme together with one or two external CER filters can be selected. The order of such ceramic filters is in a range of 3, so the selectivity is further improved and a better channel separation is guaranteed.

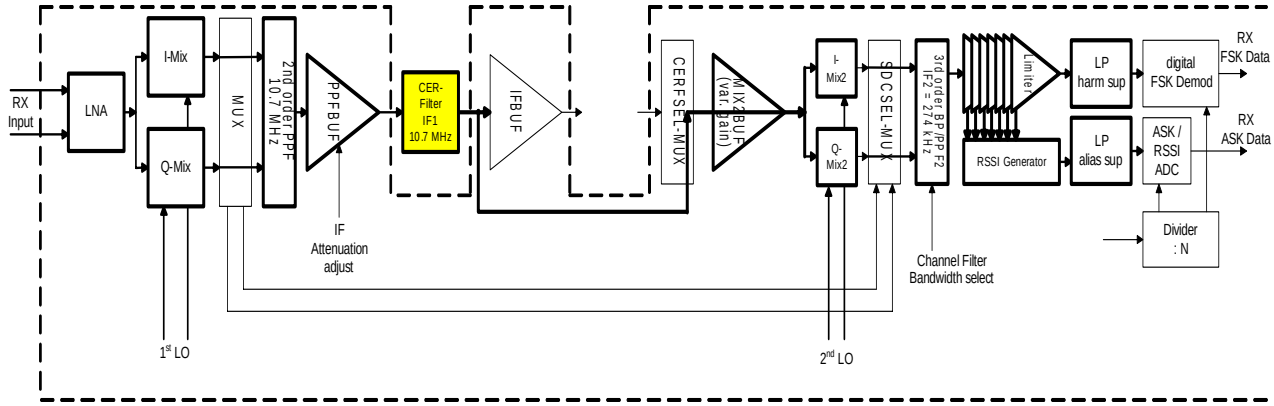


Figure 5 Double Down Conversion (DDC) with one external filter

For applications which demand very high selectivity and/or channel separation even two CER filters may be used. Also in applications where one channel requires a wider bandwidth than the other (e.g. TPMS and RKE) the second filter can be by-passed.

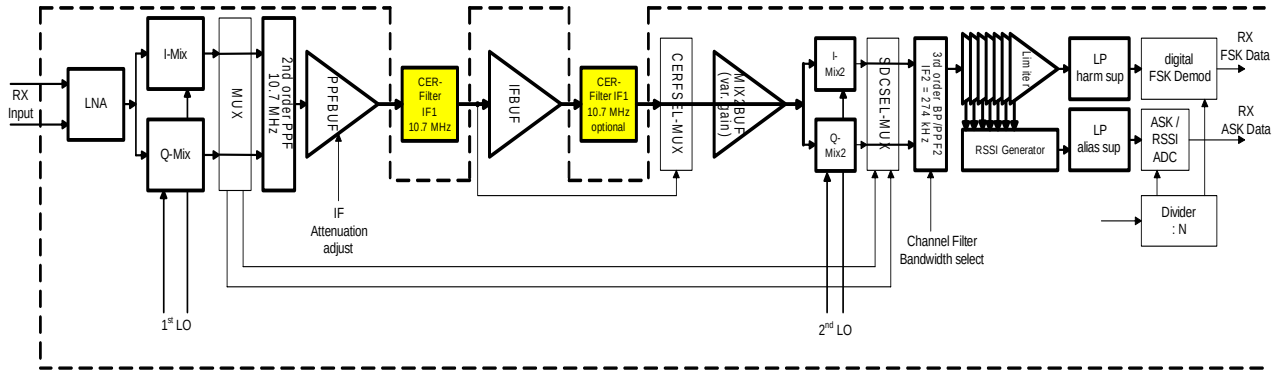


Figure 6 Double Down Conversion (DDC) with two external filters

2.4.4 Crystal Oscillator and Clock Divider

The crystal oscillator is a Pierce type oscillator which operates together with the crystal in parallel resonance mode. An automatic amplitude regulation circuitry allows the oscillator to operate with minimum current consumption. In SLEEP Mode, where the current consumption should be as low as possible, the load capacitor must be small and the frequency is slightly detuned, therefore all internal trim capacitors are disconnected. The internal capacitors are controlled by the crystal oscillator calibration registers XTALCALx. With a binary weighted capacitor array the necessary load capacitor can be selected.

Whenever a XTALCALx register value is updated, the selected trim capacitors are automatically connected to the crystal so that the frequency is precise at the desired value. The SFR control bit XTALHPMS can be used to activate the High Precision Mode also during SLEEP Mode.

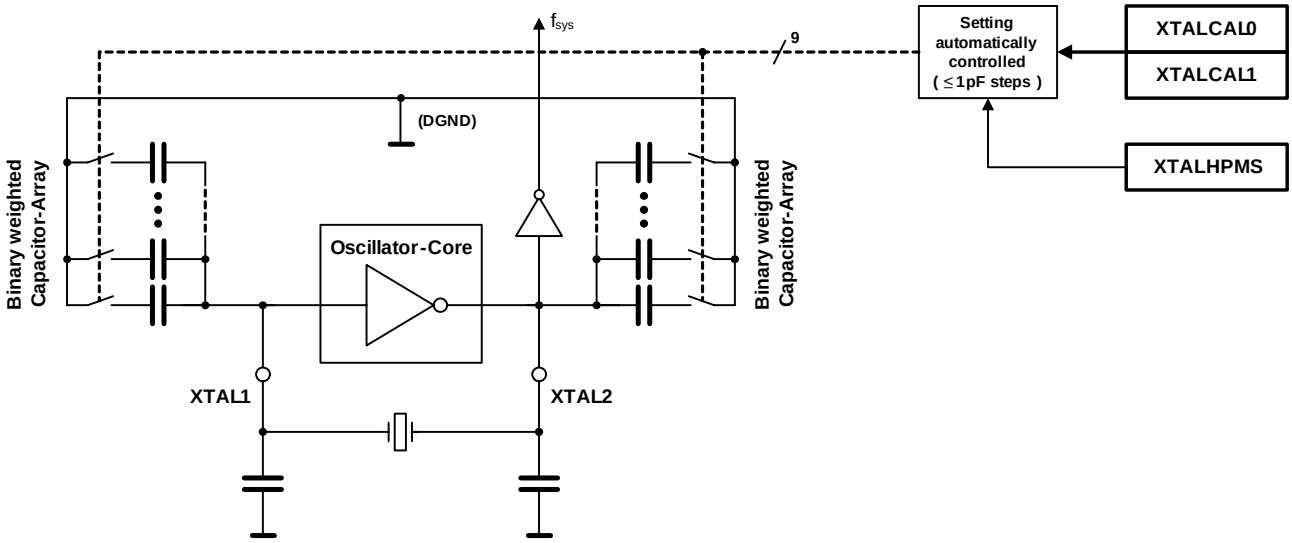


Figure 7 Crystal Oscillator

Recommended Trimming Procedure

- Set the registers XTALCAL0 and XTALCAL1 to the expected nominal values
- Set the TDA5240 to Run Mode Slave
- Wait for 0.5ms minimum
- Trim the oscillator by increasing and decreasing the values of XTALCAL0/1
- Register changes larger than 1 pF are automatically handled by the TDA5240 in 1pF steps
- After the Oscillator is trimmed, the TDA5240 can be set to SLEEP mode and keeps these values during SLEEP mode
- Add the settings of XTALCAL0/1 to the configuration. It must be set after every power up or brownout!

Using the High Precision Mode

As discussed earlier, the TDA5240 allows the crystal oscillator to be trimmed by the use of internal trim capacitors. It is also possible to use the trim functionality to compensate temperature drift of crystals.

During Run Mode (always when the receiver is active) the capacitors are automatically connected and the oscillator is working in the High Precision Mode.

On entering SLEEP Mode, the capacitors are automatically disconnected to save power.

If the High Precision Mode is also required for SLEEP Mode, the automatic disconnection of trim capacitors can be avoided by setting XTALHPMS to 1 (enable XTAL High Precision Mode during SLEEP Mode).

External Clock Generation Unit

A built in programmable frequency divider can be used to generate an external clock source out of the crystal reference. The 20 bit wide division factor is stored in the registers CLKOUT0, CLKOUT1 and CLKOUT2. The minimum value of the programmable frequency divider is 2. This programmable divider is followed by an additional divider by 2, which generates a 50% duty cycle of the CLK_OUT signal. So the maximum frequency at the CLK_OUT signal is the crystal frequency divided by 4. The minimum CLK_OUT frequency is the crystal frequency divided by 2^{21}.

To save power, this programmable clock signal can be disabled by the SFR control bit CLKOUTEN. In this case the external clock signal is set to low.

The resulting CLK_OUT frequency can be calculated by:

$$f_{CLKOUT} = \frac{f_{sys}}{2 \cdot divisionfactor}$$

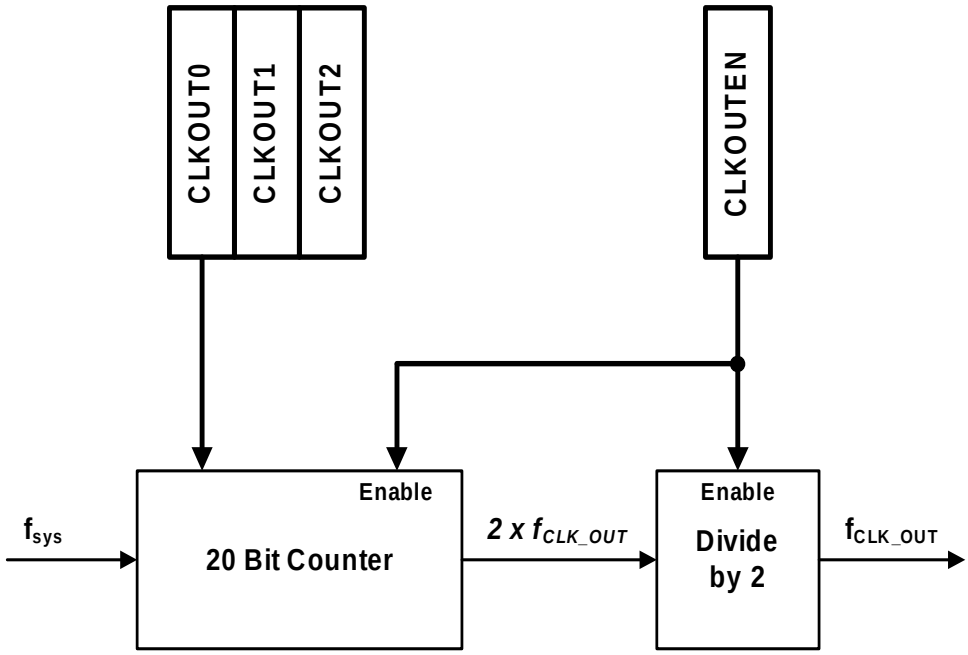


Figure 8 External Clock Generation Unit

The maximum CLK_OUT frequency is limited by the driver capability of the PPx pin and depends on the external load connected to this pin. Please be aware that large loads and/or high clock frequencies at this pin may interfere with the receiver and reduce performance.

After Reset the PPx pin is activated and the division factor is initialized to 11 (equals f_{CLK_OUT} = 998 kHz).

A clock output frequency higher than 1 MHz is not supported.

For high sensitivity applications, the use of the external clock generation unit is not recommended.

2.4.5 Sigma-Delta Fractional-N PLL Block

The Sigma-Delta Fractional-N PLL is fully integrated on chip. The ***V****oltage* ***C****ontrolled* ***O****scillator* (VCO) with on-chip LC-tank runs at approximately 3.6 GHz and is first divided with a band select divider by 1, 2 or 3 and then with an I/Q-divider by 4 which provides an orthogonal local oscillator signal for the first image reject mixer with the necessary high accuracy.
The multi-modulus divider determines the channel selection and is controlled by a 3rd order Sigma-Delta Modulator (*SDM*). A type IV phase detector, a charge pump with programmable current and an on-chip loop filter closes the phase locked loop.

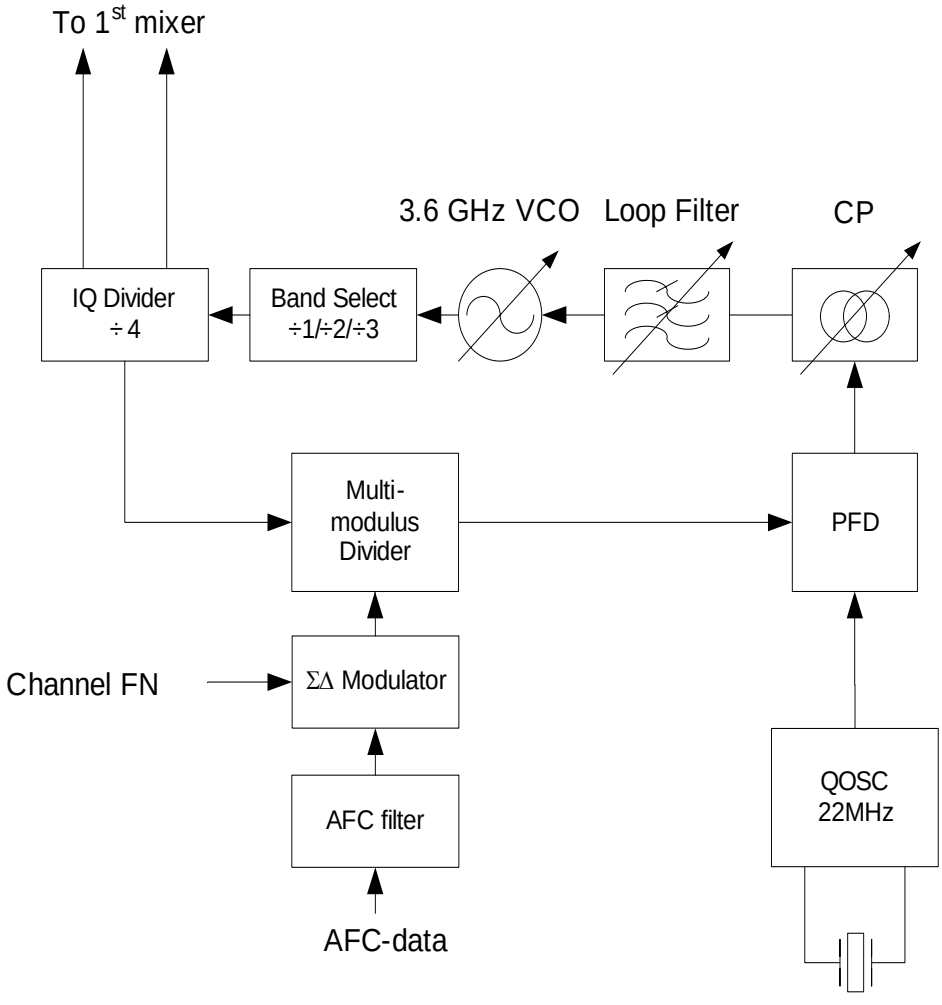


Figure 9 Synthesizer Block Diagram

When defining a Multi-Channel system, the correct selection of channel spacing is extremely important. A general rule is not possible, but following must be considered:

• If an additional SAW filter is used, all channels including their tolerances have to be inside the SAW filter bandwidth.

• The distance between channels must be high enough, that no overlapping can occur. Strong input signals may still appear as recognizable input signal in the neighboring channel because of the limited suppression of IF Filters. Example: a typical 330kHz IF filter has at 10.3 MHz (10.7 MHz - 0.4 MHz) only 30 dB suppression. A -70 dBm input signal appears like a -100 dBm signal, which is inside the receiver sensitivity. In critical cases the use of two IF filters must be considered. See also **Chapter 2.4.3 RF/IF Receiver**.

2.4.5.1 PLL Dividers

The divider chain consists of a band select divider 1/2/3, an I/Q-divider by 4 which provides an orthogonal 1st local oscillator signal for the first image reject mixer with the necessary high accuracy and a multi-modulus divider controlled by the Sigma-Delta Modulator. With the band select divider, the wanted frequency band is selected. Divide by 1 selects the 915 MHz and 868 MHz band, divide by 2 selects the 434 MHz band and divide by 3 selects the 315 MHz band. The ISM band selection is done via bit group BANDSEL in x_PLLINTC1 register.

2.4.5.2 Digital Modulator

The 3rd order ***Sigma-Delta Modulator (SDM)*** has a 22 bit wide input word, however the LSB is always high, and is clocked by the XTAL oscillator. This determines the achievable frequency resolution.

The ***Automatic Frequency Control Unit*** filters the actual frequency offset from the FSK demodulator data and calculates the necessary correction of the divider factor to achieve the nominal IF center frequency.

2.4.6 ASK and FSK Demodulator

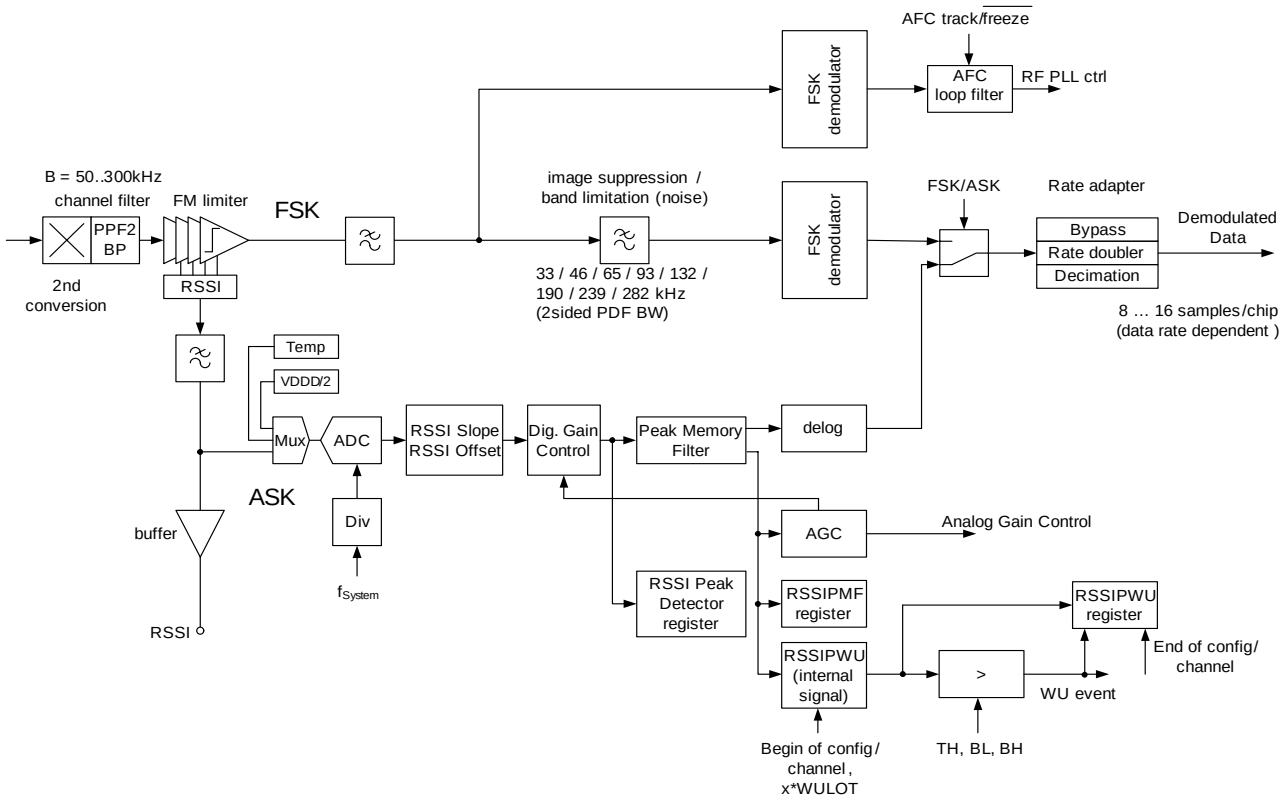


Figure 10 Functional Block Diagram ASK/FSK Demodulator

The IC comprises two separate demodulators for ASK and FSK.
After combining FSK and ASK data path, a sampling rate adaptation follows to meet an output oversampling between 8 and 16 samples per chip. Finally, an oversampling of 8 samples per chip can be achieved using a fractional sample rate converter (SRC) with linear interpolation (for further details see **Figure 15**).

2.4.6.1 ASK Demodulator

The RSSI generator delivers a DC signal proportional to the applied input power at a logarithmic scale (dBm) and is also used as an ASK demodulator. Via a programmable anti-aliasing filter this signal is converted to the digital domain by means of a 10-bit ADC. For the AM demodulation a signal proportional to the linear power is required. Therefore a conversion from logarithmic scale to linear scale is necessary. This is done in the digital domain by a nonlinear filter together with an exponential function. The analog RSSI signal after the anti-aliasing filter is available at the RSSI pin via a buffer amplifier. To enable this buffer the SFR control bit RSSIMONEN must be set. The anti-aliasing filter can be by-passed for visualization on the RSSI pin (see AAFBYP control bit).

2.4.6.2 FSK Demodulator

The limiter output signal, which has a constant amplitude over a wide range of the input signal, feeds the FSK demodulator. There is a configurable lowpass filter in front of the FSK demodulation to suppress the down conversion image and noise/limiter harmonics (FSK Pre-Demodulation Filter, PDF). This is realized as a 3rd order digital filter. The sampling rate after FSK demodulation is fixed and independent from the target data rate.

2.4.6.3 Automatic Frequency Control Unit (AFC)

In front of the image suppression filter a second FSK demodulator is used to derive the control signal for the **Automatic Frequency Control Unit**, which is actually the DC value of the FSK demodulated signal. This makes the AFC loop independent from signal path filtering and allow so a wider frequency capture range of the AFC. The derivation of the AFC control signal is preferably done during the DC free preamble and is then frozen for the rest of the datagram.

Since the digital FSK demodulator determines the exact frequency offset between the received input frequency and the programmed input center frequency of the receiver, this offset can be corrected through the sigma delta control of the PLL. As shown in **Figure 10**, for AFC purposes a parallel demodulation path is implemented. This path does not contain the digital low pass filter (PDF, Pre-Demodulation Filter). The entire IF bandwidth, filtered by the analog bandpass filter only, is processed by the AFC demodulator.

There are two options for the active time of the AFC loop:

- 1. always on
- 2. active for a programmable time relative to a signal identification event (several options can be programmed in SFR).

In the latter case the AFC can either be started or frozen relative to the signal identification. After the active time the offset for the sigma-delta PLL (SD PLL) is frozen.

The programming of the active time is especially necessary in case the expected frame structure contains a gap (noise) between wake-up and payload in order to avoid the AFC from drifting.

AFC works both for FSK and ASK. In the latter case the AFC loop only regulates during ASK data = high.

The maximum frequency offset generated by the AFC can be limited by means of the x_AFCLIMIT register. This limit can be used to avoid the AFC from drifting in the presence of interferers or when no RF input signal is available (AFC wander). A maximum AFC limit of 42 kHz is recommended. AFC wandering needs to be kept in mind especially when using Run Mode Slave.

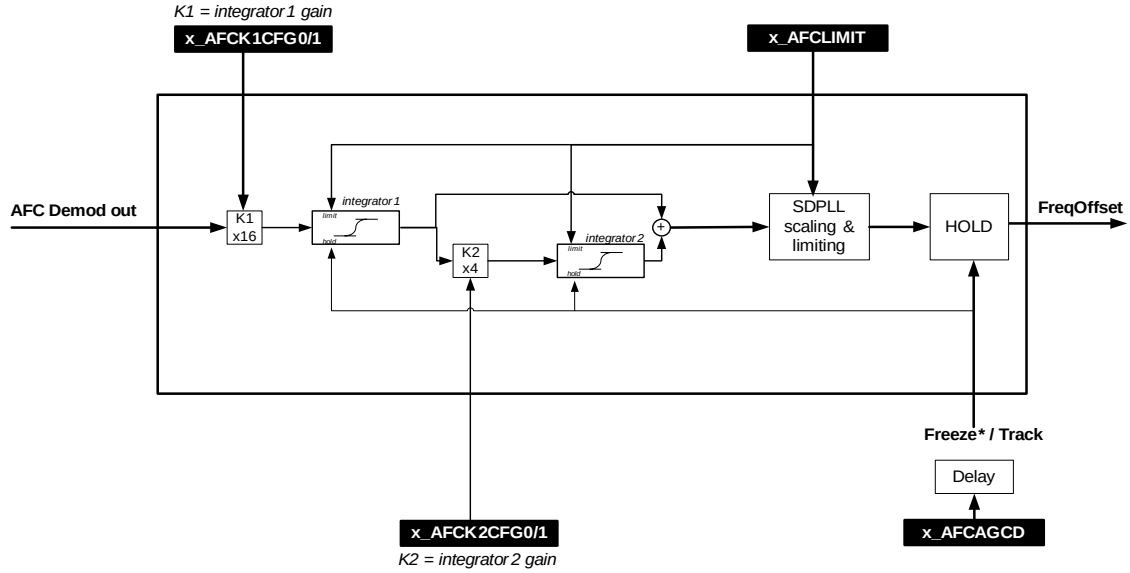


Figure 11 AFC Loop Filter (I-PI Filtering and Mapping)

The bandwidth (and thus settling time) of the loop is programmed by means of the integrator gain coefficients K1 and K2 (x_AFCK1CFG and x_AFCK2CFG register).

K1 mainly determines the bandwidth. K2 influences the dynamics/damping (overshoot) - smaller K2 means smaller overshoot, but slower dynamics. The bandwidth of the AFC loop is approximately 1.3*K1.

To avoid residual FM, limiting the AFC BW to 1/20 ~ 1/40 of the bit rate is suggested, therefore K1 must be set to approximately 1/50 ~ 1/100 of the bit rate. For most applications K2 can be set equal to K1 (overshoot is then <25%).

When very fast settling is necessary K1 and K2 can be increased up to bit rate/10, however, in this case approximately 1dB sensitivity loss is to be expected due to the AFC counteracting the input FSK signal.

AFC limitation at Local Oscillator (LO) frequencies at multiples of reference frequency (f_xtal). When AFC is activated and AFC drives the wanted LO frequency over the integer limit of Sigma Delta (SD) modulator, the SD modulator stucks at frac=1.0 or frac=0.0 due to saturation. So when AFC can change the integer value for the LO (register x_PLLINTCy) within the frequency range LO-frequency +/- AFC-limit, a change of the LO injection side or a smaller AFC-limit is recommended.

The frequency offset found by AFC (AFC loop filter output) can be readout via register AFCOFFSET, when AFC is activated. The value is in signed representation and has a frequency resolution of 2.68 kHz/digit. The output can be limited by the x_AFCLIMIT register.

2.4.6.4 Digital Automatic Gain Control Unit (AGC)

Automatic Gain Control (AGC) is necessary mainly because of the limited dynamic range of the on-chip bandpass filter (BPF). The dynamic range reduces to less than 60dB in case of minimum BPF bandwidth.

AGC is used to cover the following cases:

1. ASK demodulation at large input signals
2. RSSI reading at large input signals
3. Improve IIP3 performance in either FSK or ASK mode

The 1st IF buffer (PPFBUF, see **Figure 3**) can be fine tuned "manually" by means of 4 bits thus optimizing the overall gain to the application (attenuation of 0dB to -12dB by means of IFATT0 to IFATT15 in DDC mode; SDC mode has lower IFATT range). This buffer allows the production spread of external components to be trimmed.

The gain of the 2nd IF path is set to three different values by means of an AGC algorithm. Depending on whether the receiver is used in single down conversion or in double down conversion mode the gain control in the 2nd IF path is either after the 2nd poly-phase network or in front of the 2nd mixer.

The AGC action is illustrated in the RSSI curve below:

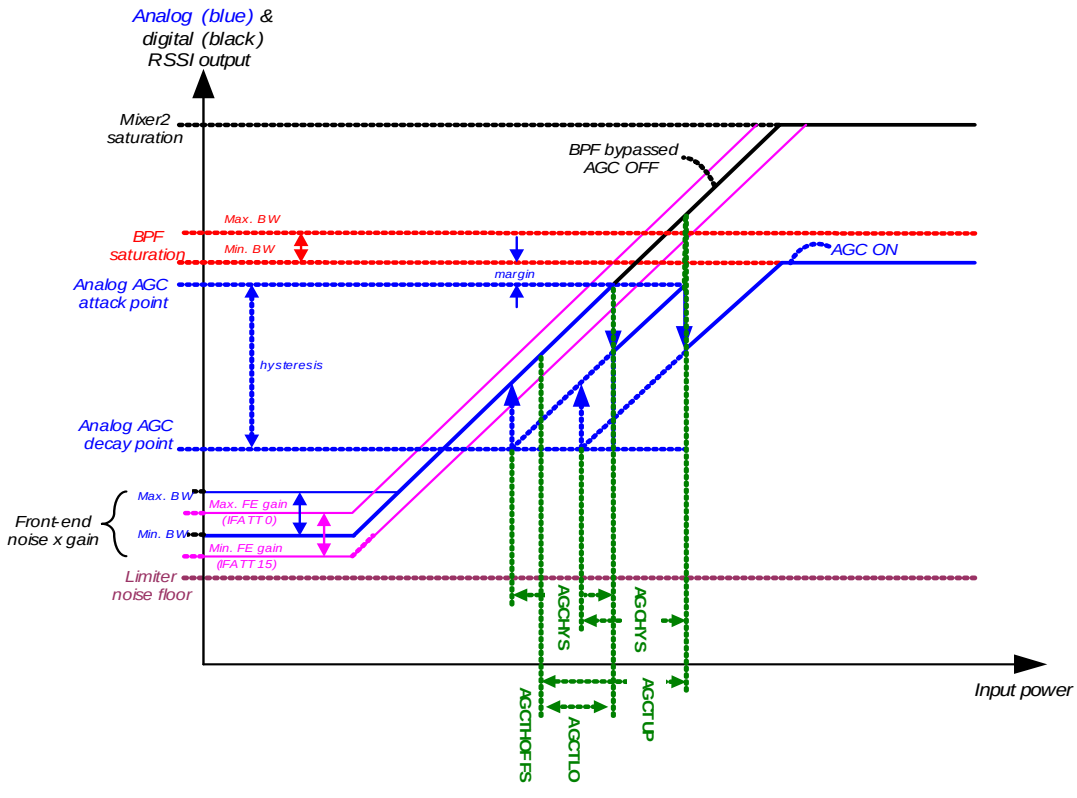


Figure 12 Analog RSSI output curve with AGC action ON (blue) vs. OFF (black)

Digital RSSI, AGC and Delog:

In order to match the analog RSSI signal to the **digital RSSI** output a correction is necessary. It adds an offset (RSSIOFFS) and modifies the slope (RSSISLOPE) such that standardized AGC levels and an appropriate DELOG table can be applied.

Upon entering the **AGC unit** the digital RSSI signal is passed through a Peak Memory Filter (PMF). This filter has programmable up and down integration time constants (PMFUP, PMFDN) to set attack respectively decay time. The integration time for decay time must be significantly longer than the attack time in order to avoid the AGC interfering with the ASK modulation.

The integrator is followed by two digital Schmitt triggers with programmable thresholds (AGCTLO; AGCTUP) - one Schmitt trigger for each of the two attack thresholds (two digital AGC switching points). The hysteresis of the Schmitt triggers is programmable (AGCHYS) and sets the decay threshold. The Schmitt triggers control both the analog gain as well as the corresponding (programmable) digital gain correction (DGC).

The difference ("error") signal in the PMF is actually a normalized version of the modulation. This signal is then used as input for the **DELOG** table.

AGC threshold programming

The SFR description for the AGC thresholds are in dBs. The first value to set is the AGC threshold offset in AGCTHOFFS.

This value is the offset relative to 0 input (no noise, no signal), which for the default setting of gain, and assuming typical insertion loss of matching network and ceramic filter, can be extrapolated to be approximately -143dBm.

In this case the default setting of the AGCTHOFFS of 63.9dB corresponds to an input power of approximately -79dBm (= -143dBm + 63.9dB).

The low (digital) AGC threshold is then -79 + 12.8dB (default AGCTLO) = -66dBm and the upper (digital) AGC threshold is -79 + 25.6 (default AGCTUP) = -53dBm.

Therefore a margin of about 6dB is indicated before a degradation of the linearity of the 2^{nd} IF can be observed when using the 50kHz BPF or even about 16dB when using the 300kHz BPF.

The input power level at which the AGC switches back to maximum gain is -66dBm - 21.3dB (default AGCHYS) = -87dBm. This provides enough margin against the minimum sensitivity.

When AGC is activated, RSSI is untrimmed, IFATT <= 5.6dB and the same RSSI offset should be applied for all bandpass filter settings, then the settings in **Table 2** can be applied, where a small reduction of the RSSI input range can be observed.

Table 2 AGC Settings 1

AGC Threshold Hysteresis = 21.3 dB					
AGC Digital RSSI Gain Correction = 15.5 dB					
BPF	**RSSI Offset Compensation (untrimmed) 1)**	**AGC Threshold Offset**	**AGC Threshold Low**	**AGC Threshold Up**	**RSSI Input Range Reduction**
300 kHz	32	63.9 dB	8	4	5 dB
200 kHz	32	63.9 dB	6	2	5 dB
125 kHz	32	63.9 dB	5	0	5 dB
80 kHz	32	51.1 dB	11	6	2.8 dB
50 kHz	32	51.1 dB	9	5	0 dB

1) Note: This value needs to be used for calculating the register value

For the full RSSI input range, the values in **Table 3** can be applied.

Table 3 AGC Settings 2

AGC Threshold Hysteresis = 21.3 dB				
AGC Digital RSSI Gain Correction = 15.5 dB				
BPF	**RSSI Offset Compensation (untrimmed) 1)**	**AGC Threshold Offset**	**AGC Threshold Low**	**AGC Threshold Up**
300 kHz	-18	63.9 dB	5	1
200 kHz	-18	51.1 dB	11	7
125 kHz	-18	51.1 dB	10	5
80 kHz	4	51.1 dB	9	5
50 kHz	32	51.1 dB	9	5

1) Note: This value needs to be used for calculating the register value

Attack and Decay coefficients PMF-UP & PMF-DOWN:

The settling time of the loop is determined by means of the integrator gain coefficients PMFUP and PMFDN, which need to be calculated from the wanted attack and decay times.

The ADC is running at a fixed sampling frequency of 274kHz. Therefore the integrator is integrating with PMFUP*274k per second, i.e. time constant is 1/(PMFUP*274k). The attack times are typically 16 times faster than the decay times.

Typical calculation of the coefficients by means of an example:

- PMFUP = 2^-round(ln(AttTime / BitRate * 274kHz) / ln(2))
- PMFDN = 2^-round(ln(DecTime / BitRate * 274kHz) / ln(2)) / PMFUP

where AttTime, DecTime = attack, decay time in number of bits

Note: PMFDN = overall_PMFDN / PMFUP

Example:

BitRate = 2kbps

AttTime = 0.1 bits

=> PMFUP = 2^-round(ln(0.1bit/2kbps*274kHz)/ln(2)) = 2^-round(3.8) = 2^-4

DecTime = 2 bits

=> PMFDN = 2^-round(ln(2bit/2kbps*274kHz)/ln(2))/PMFUP = 2^-round(8.1)/2^-4 = 2^-4

Note: In case of ASK with large modulation index the attack time (PMFUP) can be up to a factor 2 slower due to the fact that the ASK signal has a duty cycle of 50% - during the ASK low duration the integrator is actually slightly discharged due to the decay set by PMFDN.

The AGC start and freeze times are programmable. The same conditions can be used as in the corresponding AFC section above. They will however, be programmed in separate SFR registers.

2.4.6.5 Analog to Digital Converter (ADC)

In front of the AD converter there is a multiplexer so that also temperature and VDDD can be measured (see **Figure 10**).

The default value of the ADC-MUX is RSSI (register ADCINSEL: 000 for RSSI; 001 for Temperature; 010 for VDDD/2).

After switching ADC-MUX to a value other than RSSI in SLEEP Mode, the internal references are activated and this ADC start-up lasts 100µs. So after this ADC start-up time the readout measurements may begin. The chip stays in this mode until reconfiguration of register ADCINSEL to setting RSSI. However, it is recommended to measure temperature during SLEEP mode (This is also valid for VDDD).

Readout of the 10-bit ADC has to be done via ADCRESH register (the lower 2 bits in ADCRESL register can be inconsistent and should not be used).

Typical the ADC refresh rate is 3.7 µs. Time duration between two ADC readouts has to be at least 3.7 µs, so this is already achieved due to the maximum SPI rate (16 bit for SPI command and address last 8µs at an SPI rate of 2MBit/s). The EOC bit (end of conversion) indicates a successful conversion additionally. Repetition of the readout measurement for several times is for averaging purpose.

The input voltage of the ADC is in the range of 1 .. 2 V. Therefore VDDD/2 (= 1.65 V typical) is used to monitor VDDD.

Further details on the measurement and calibration procedure for temperature and VDDD can be taken from the corresponding application note.

2.4.7 RSSI Peak Detector

The IC possesses several digital RSSI peak level detectors. The RSSI level is averaged over 4 samples before it is fed to any of the peak detectors. This prevents the evaluated peak values to be dominated by single noise peaks.

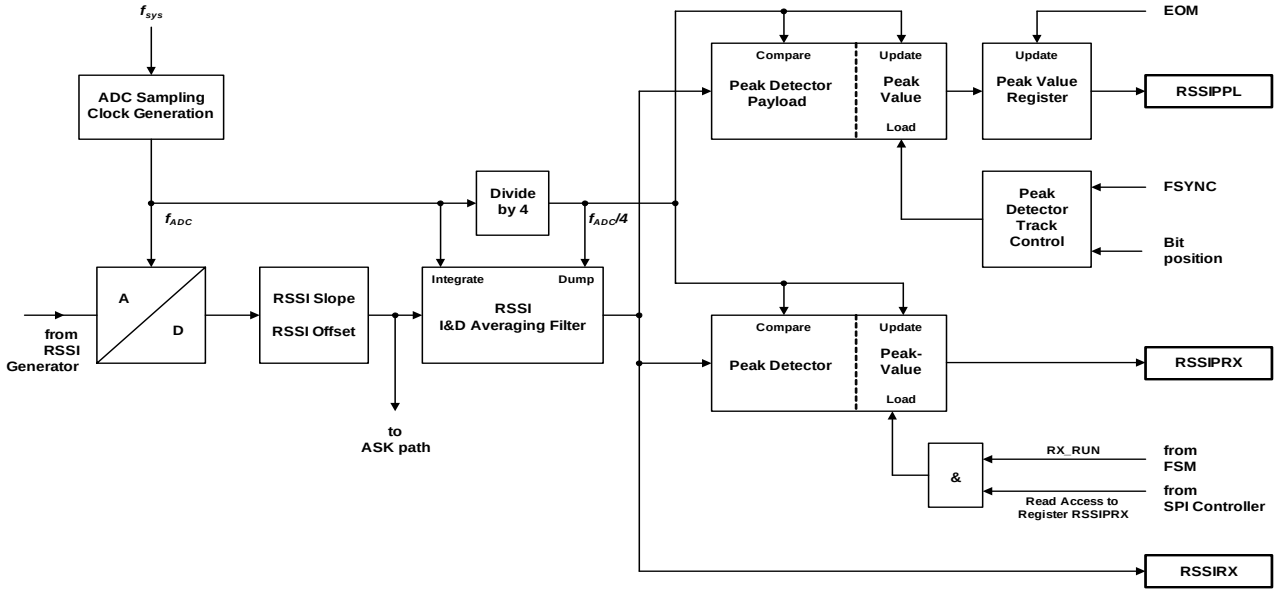


Figure 13 Peak Detector Unit

Peak Detector Payload is used to measure the input signal power of a received and accepted data telegram. It is read via SFR RSSIPPL.

Observation of the RSSI signal starts at the detection of a TSI (FSYNC) and ends with the detection of EOM. The internal RSSIPPL value is cleared after FSYNC. The evaluated RSSI peak level RSSIPPL is transferred to the RSSIPPL register at EOM. Starting the observation of the RSSI level can be delayed by a selectable number of data bits and is controlled by the register x_PKBITPOS. A latency in the generation of FSYNC and EOM of approx. 2..3 bits in relation to the contents of the Peak Detector must be considered. Within the boundaries described, the register RSSIPPL always contains the peak value of the last completely received data telegram. The register RSSIPPL is reset to 0 at power up reset only.

Peak Detector is used to measure RSSI independent of a data transfer and to digitally trim RSSI. It is read via SFR RSSIPRX.

Observation of the RSSI signal is active whenever the RX_RUN signal is high. The RSSIPRX register is refreshed and the Peak Detector is reset after every read access to RSSIPRX.

It may be required to read RSSIPRX twice to obtain the required result. This is because, for example, during a trim procedure in which the input signal power is reduced, after

reading RSSIPRX, the peak detector will still hold the higher RSSI level. After reading RSSIPRX the lower RSSI level is loaded into the Peak Detector and can be read by reading RSSIPRX again.

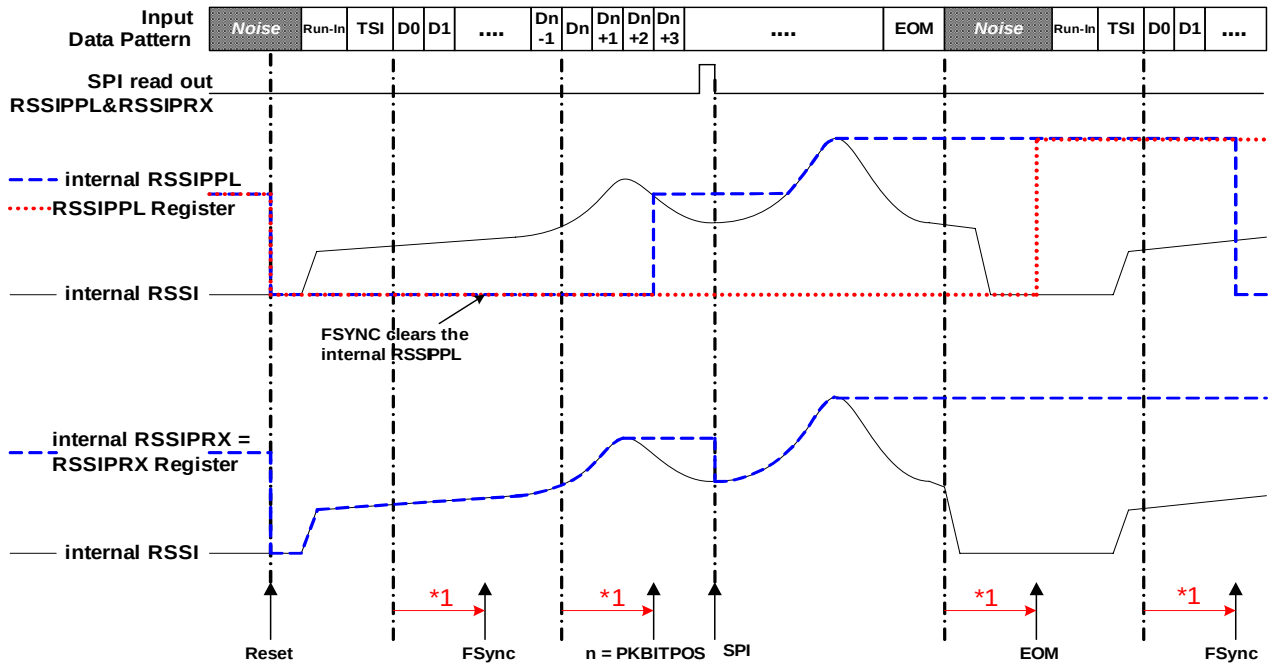
Register RSSIPRX should not be read-out faster than 41µs in case AGC is ON (as register value would not represent the actual, but a lower value).

When the RX_RUN signal is inactive, a read access has no influence to the peak detector value. The register RSSIPRX is reset to 0 at power up reset.

Peak Detector Wake-Up RSSIPWU (see **Figure 10**) is used to measure the input signal power during Wake-Up search. The internal signal RSSIPWU gets initialized to 0 at start of the first observation time window at the beginning of each configuration/channel. The peak value of this signal is tracked during Wake-Up search.

In case of a Wake-Up, the actual peak value is written in the RSSIPWU register. Even in case no Wake-Up occurred, actual peak value is written in the RSSIPWU register at the end of the actual configuration/channel of the Self Polling period. So if no Wake-Up occurred, then the RSSIPWU register contains the peak value of the last configuration/channel of the Self Polling period, even in a Multi-Configuration/Multi-Channel setup. This functionality can be used to track RSSI during unsuccessful Wake-Up search due to no input signal or due to blocking RSSI detection.

For further details please refer to **Chapter 2.4.8.5 Wake-Up Generator** and **Chapter 2.6.2 Polling Timer Unit**.



*1 Computation Delay due to filtering and signal calculation.

Figure 14 Peak Detector Behavior

Recommended Digital Trimming Procedure

- Download configuration file (Run Mode Slave; RSSISLOPE, RSSIOFFS set to default, i.e. RSSISLOPE=1, RSSIOFFS=0)
- Turn off AGC (AGCSTART=0) and set gain to AGCGAIN=0
- Apply P_{IN1} = -85 dBm RF input signal
- Read RSSIRX eleven times (minimum 10 ms in-between readings), use average of last ten readings (always), store as RSSIM1
- Apply P_{IN2} = -65 dBm RF input signal
- Read RSSIRX eleven times (minimum 10 ms in-between readings), use average of last ten readings (always), store as RSSIM2
- Calculate measured RSSI slope SLOPEM=(RSSIM2-RSSIM1)/(P_{IN2}-P_{IN1})
- Adjust RSSISLOPE for required RSSI slope SLOPER as follows: RSSISLOPE=SLOPER/SLOPEM
- Adjust RSSIOFFS for required value RSSIR2 at P_{IN2} as follows: RSSIOFFS=(RSSIR2-RSSIM2)+(SLOPEM-SLOPER)*P_{IN2}
- The new values for RSSISLOPE and RSSIOFFS have to be added to the configuration!

Notes:

1. The upper RF input level must stay well below the saturation level of the receiver (see **Chapter 2.4.6.4 Digital Automatic Gain Control Unit (AGC)**)

2. The lower RF input level must stay well above the noise level of the receiver

3. If IF Attenuation is trimmed, this has to be done before trimming of RSSI

4. If RSSI needs to be trimmed in a higher input power range the AGCGAIN must be set accordingly

2.4.8 Digital Baseband (DBB) Receiver

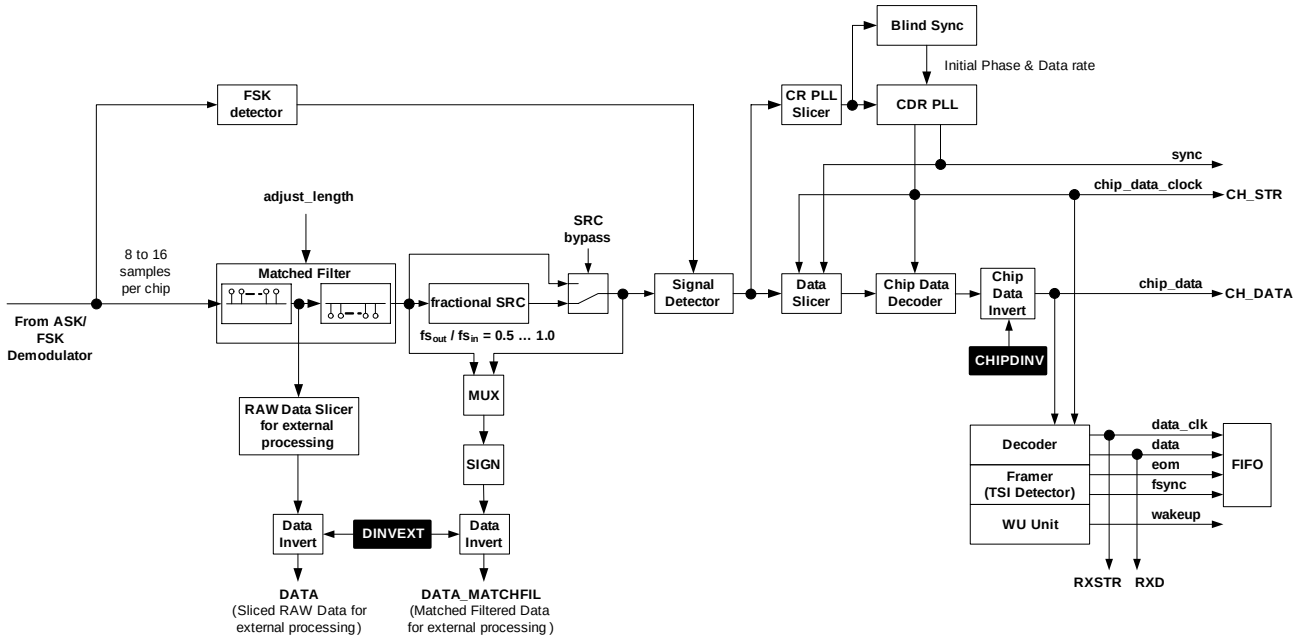


Figure 15 Functional Block Diagram Digital Baseband Receiver

The digital baseband receiver comprises a matched data filter, a clock and data recovery, a data slicer, a line decoder, a wake-up generator, a frame synchronization and a data FIFO. The recovered data and clock signals are accessible via 2 separate pins. The FIFO data buffer is accessible via the SPI bus interface.

2.4.8.1 Data Filter and Signal Detection

The data filter is a matched filter (*MF*). The frequency response of a matched filter has ideally the same shape as the power spectral density (*PSD*) of the originally transmitted signal, therefore the signal-to-noise ratio (*SNR*) at the output of the matched filter becomes maximum. The input sampling rate of the baseband receiver has to be between 8 and 16 samples per chip. The oversampling factor within this range is depending on the data rate (see **Figure 10**). The MF has to be adjusted accordingly to this oversampling. After the MF a fractional sample rate converter (SRC) is applied using linear interpolation. Depending on the data rate decimation is adjusted within the range 1...2. Finally, at the output of the fractional SRC the sampling rate is adjusted to 8 samples per chip for further processing.

To distinguish whether the incoming signal is really a signal or only noise adequate detectors for ASK and FSK are built in.

Signal and Noise Detector

The Signal Detector decides between acceptable and unacceptable data (e.g. noise). This decision is taken by comparing the signal power of the actually received data (register SPWR) with a configurable threshold level (registers x_SIGDET0/1), which must be evaluated. In case the actual signal power is above the threshold, acceptable data has been detected.

To decide in case of FSK whether there is a data signal or simply noise at the output of the rate adapter, there is a Noise Detector implemented. The principle is based on a power measurement of the demodulated signal. The current noise power is stored in the NPWR register and is updated at every SPI controller access. The Noise Detector is useful if data signal is transmitted with small FSK deviations. In case the current noise power (register NPWR) is below the configurable threshold (register x_NDTHRES), a data signal has been detected.

The Signal Recognition mode must be configured based on whether ASK or FSK modulation is used. Signal Recognition can be a combination of Signal Detector and Noise Detector:

- Signal Detector (=Squelch) only (related registers: x_SIGDET0, x_SIGDET1 and SPWR). This mode is generally used for ASK and recommended for FSK.
- Noise Detector only (related registers: x_NDTHRES and NPWR).
- Signal and Noise Detector simultaneously.
- Signal and Noise Detector simultaneously, but the FSK noise detect signal is valid only if the x_SIGDETLO threshold is exceeded. This is the recommended FSK mode, if minimum FSK deviation is not sufficient to use Signal Detector only.

Signal Recognition can also be used as Wake-up on Level criterion (see **Chapter 2.4.8.5**).

Figure 16 shows the system characteristics to consider in choosing the best Signal Detector level. On the one hand, a higher SIGDET threshold level must be set for achieving good FAR (False Alarm Rate) performance, but then the MER/BER (Message Error Rate/Bit Error Rate) performance will decrease. On the other hand, the MER/BER performance can be increased by setting smaller SIGDET threshold levels but then the FAR performance will worsen.

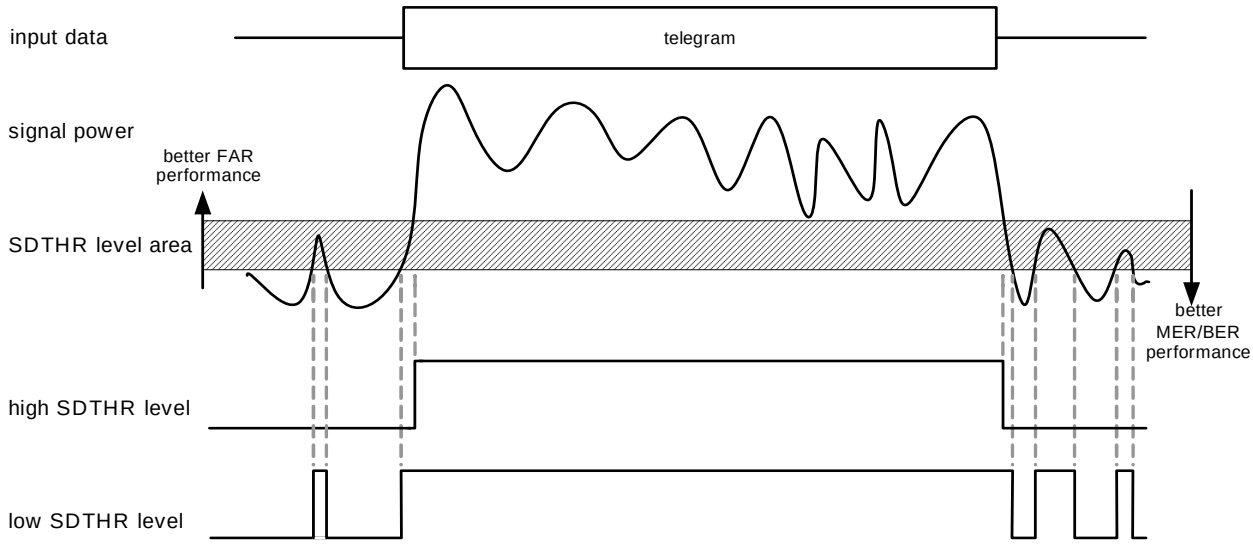


Figure 16 Signal Detector Threshold Level

Quick Procedure to Determine Signal and Noise Detector Thresholds

Preparation

A setup is required with original RF hardware as in the final application. The values of SPWR and NPWR can be read via the final application.

A complete configuration file using right modulation, data rate and Run Mode Slave, must be prepared and downloaded to the TDA5240.

Signal Detector Threshold for ASK

Take 500 readings of SPWR (50 are also possible, but this leads to less accurate results) with no RF input signal applied (=noise only). Calculate average and Standard Deviation. Signal Detector Threshold is average plus 2 times the Standard Deviation. To load the x_SIGDET0/1 register the calculated value must be rounded and converted to hexadecimals. For a final application, the Signal Detector Threshold should be varied to optimize the false alarm rate and the sensitivity.

Signal and Noise Detector Thresholds for FSK

Signal Detector Threshold

Do 500 (50) readings of SPWR with no RF input signal applied (=noise only). Calculate average and Standard Deviation. Signal Detector Threshold is average plus 2 times the Standard Deviation. Of course this value has to be rounded and converted to

hexadecimals. For a final application the Signal Detector Threshold should be varied to optimize the false alarm rate and the sensitivity.

Verification if Squelch only is possible

Apply a bit pattern (e.g. PRBS9) with correct data rate at about -80 dBm input signal power and minimum FSK deviation to the RF input. Do 500 (50) readings of SPWR, calculate average minus three times the Standard Deviation. This value should be higher than the calculated Signal Detector Threshold calculated above. If this is not the case, Signal Detector AND Noise Detector must be used.

Noise Detector Threshold

Do 500 (50) readings of NPWR with no RF input signal applied (=noise only). Calculate average and Standard Deviation. Noise Detector Threshold is average minus the Standard Deviation. Round this value and convert it to hexadecimals. For a final application, the Noise Detector Threshold should be varied to optimize false alarm rate and sensitivity.

Signal Detector Low Threshold

The Signal Detector Low Threshold is always required in combination with the Noise Detector.

Set register bit SDLORE to 1 and set bit group SDLORSEL to 00. Apply a bit pattern (e.g. PRBS9) at correct data rate at about -80 dBm input signal power and minimum FSK deviation to the RF input. Do 500 (50) readings of SPWR, calculate average. If average is larger than 200 dec (=0xC8), SDLORSEL has to be increased to the next larger value until average is smaller than 200 dec. x_SIGDETLO = 0.8 * (average - 3 * Standard Deviation). Set register SDLORE back to 0. The last setting of bit group SDLORSEL must also be used for configuration!

Verification

Threshold settings should be verified by testing receiver sensitivity over the input frequency range, with a step size of 100Hz, at minimum FSK deviation with all combinations of minimum and maximum data rate and duty cycle.

Further detailed information can be taken from the corresponding Application Note.

2.4.8.2 Encoding Modes

The IC supports the following Bi-phase encodings:

- Manchester code
- Differential Manchester code
- Bi-phase space code
- Bi-phase mark code

The encoding mode is set and enabled by bit group CODE in x_DIGRXC configuration register.

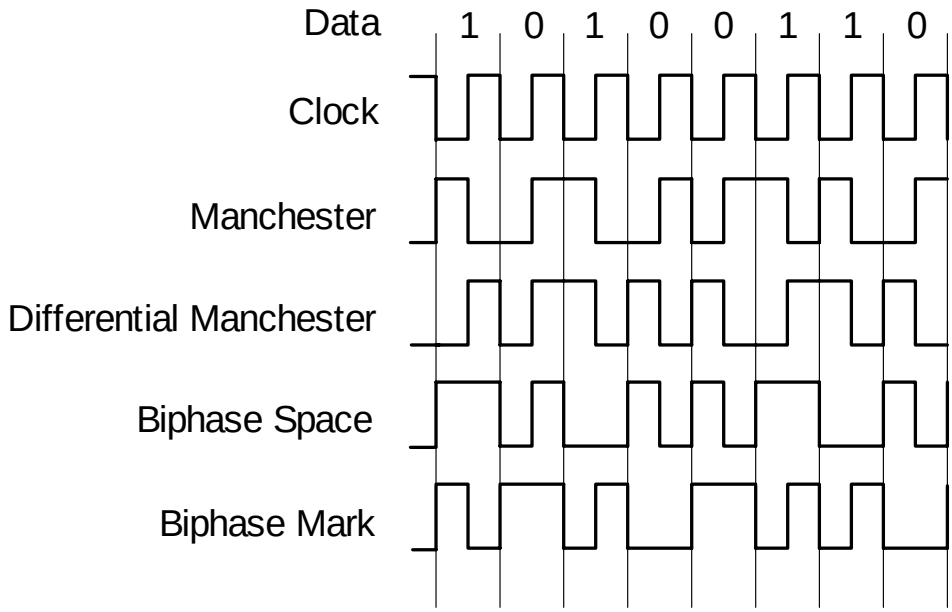


Figure 17 Coding Schemes

The encoding modes Inverted Manchester and Inverted Differential Manchester can also be decoded internally by usage of CHIPDINV bit in x_DIGRXC register (see **Figure 15**).

All the Manchester symbol combinations including Code Violations are shown in **Figure 18**. Digital 0 and 1 are coded with the change of the amplitude in the middle of the symbol period. The Code Violations (CV) M (mark) and S (space), are coded as low/high signal levels.

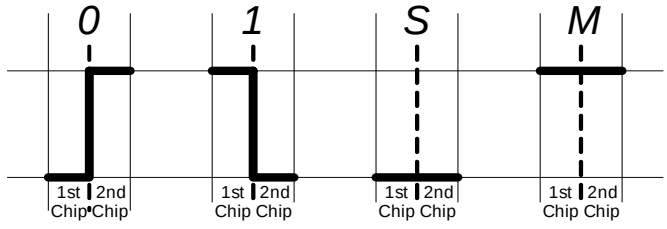


Figure 18 Manchester Symbols including Code Violations

2.4.8.3 Clock and Data Recovery

An all-digital PLL *(*ADPLL*)* recovers the data clock from the incoming data stream. The second main function is the generation of a signal indicating symbol synchronization. Synchronization on the incoming data stream generally occurs within the first 4 bits of a telegram.

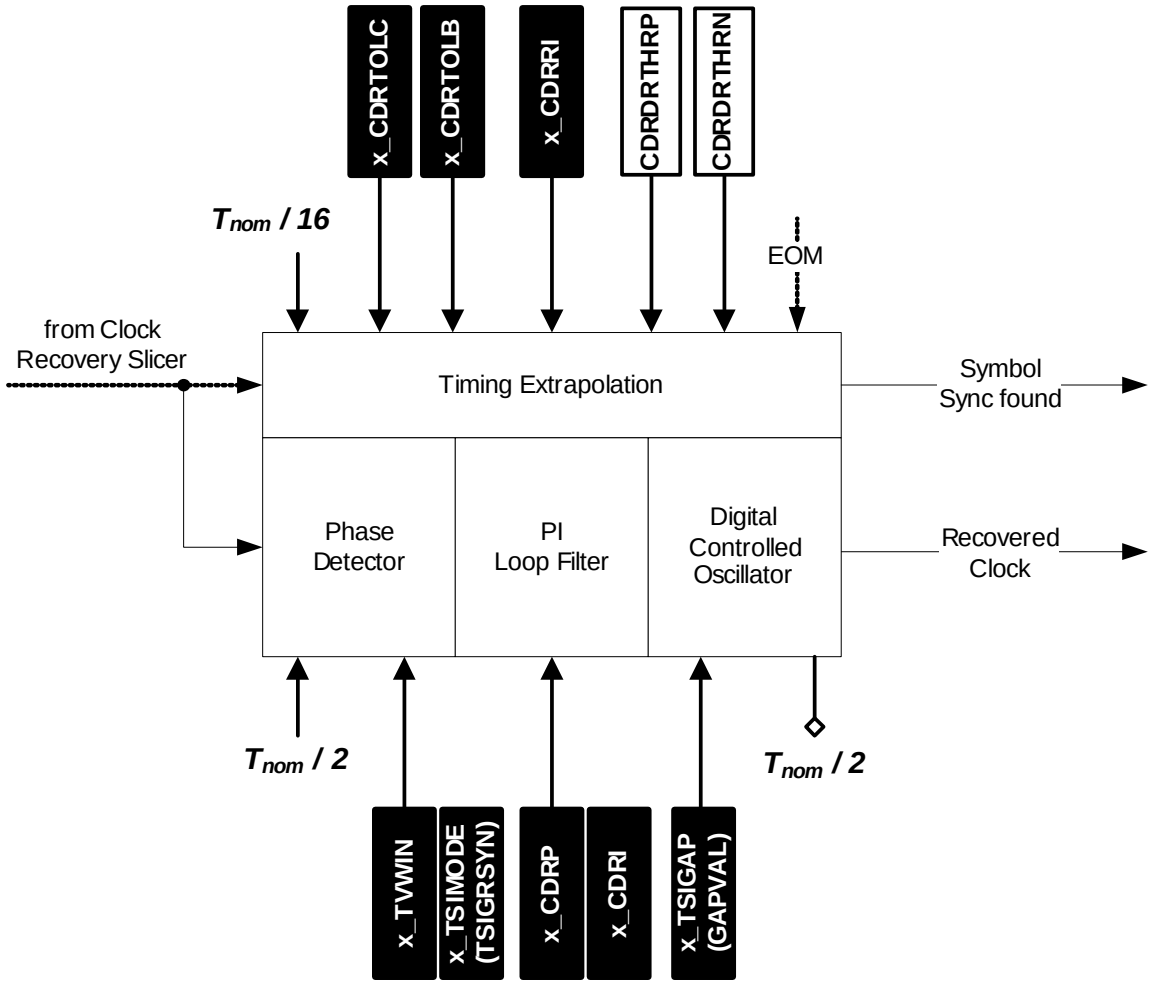


Figure 19 Clock Recovery (ADPLL)

Clock Recovery is implemented as standard ADPLL PI regulator with Timing Extrapolation Unit for fast settling.

In the unlocked state, the Timing Extrapolation Unit calculates the frequency offset for the incoming data stream. If the defined number of Bi-phase encoded bits are detected (the RUNIN length can be set in the x_CDRRI register), the I-part and the PLL oscillator will be set and the PLL will be locked.

When x_CDRRI.RUNLEN is set to small values, then the I-part is less accurate (residual error) and can lead to a longer needed PLL settling time and worse performance in the

first following bits. Therefore the selected default value is a good compromise between fast symbol synchronization and accuracy/performance.

Duty cycle and data rate acceptance limits are adjustable via registers. After locking, the clock must be stable and must follow the reference input. Therefore, a rapid settling procedure (Timing Extrapolation Unit) and a slow PLL are implemented.

If the PLL is locked, the reference signal from the Clock Recovery Slicer is used in the phase detector block to compute the actual error. The error is used in the PI loop filter to set the digital controlled oscillator running frequency. For the P, I and Timing Extrapolation Unit settings, the default values for the x_CDRP and x_CDRI control registers are recommended.

The PLL will be unlocked, if a code violation of more than the defined length is detected, which is set in the x_TVWIN control register. Another criterion for PLL resynchronization is an End Of Message (EOM) signalled by the Framer block.

The PLL oscillator generates the chip clock (2 * f_{data}).

The internal PLL lock signal used by the Framer is generated up to 1 bit before RUNIN ends. The Timing Extrapolation Unit counts the incoming edges and interprets the delay between two edges as a bit or a chip. Due to the fact that the first edge of a “Low” bit, coded as ’0’ and ’1’, rises one chip later than a “High” bit, the PLL locks later in this case (see **Figure 20**). The real needed RUNIN time can be shorter than the configured RUNIN length in the x_CDRRI register by up to two chips. This should be considered when setting the TSI pattern and/or TSI length. See also **Chapter 2.4.8.6 Frame Synchronization**.

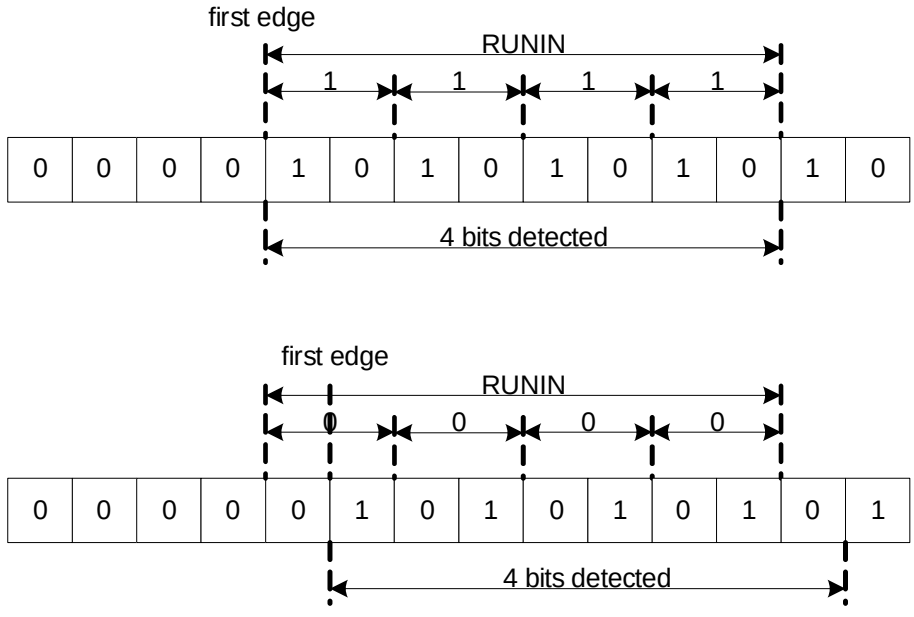


Figure 20 RUNIN Generation Principle

Number of Required RUNIN Bits

The number of RUNIN bits specified in x_CDRRI register should always be 3.0. This setting defines the duration of the internal synchronization. Because of internal processing delays, the pattern length that must be reserved for RUNIN is longer.

The ideal RUNIN pattern is a series of either Manchester 1's or Manchester 0's. This pattern includes the highest number of edges that can be used for synchronization. In this case, the number of physically sent RUNIN bits is 4.

For any other RUNIN pattern, 5.5 bits should be reserved for RUNIN.

TVWIN (Timing Violation WINdow length)

The PLL unlocks if the reference signal is lost for more than the time defined in the x_TVWIN register. During the TSI Gap (see TSI Gap Mode in **Chapter 2.4.8.6 Frame Synchronization**), the PLL and the TVWIN are frozen.

TVWIN time is the time during which the Digital Baseband Receiver should stay locked without any incoming signal edges detected. The time resolution is T/16.

Calculation of TVWIN can be seen at the end of subsection TSI Gap Mode in **Chapter 2.4.8.6 Frame Synchronization**.

Duty Cycle Variation

Ideally, the input signal to the Clock and Data Recovery (CDR) would have a chip width of 8 samples and a bit width of 16 samples and the CDR would not lock onto any input that violates this. However, due to variations in the duty cycle this stringent assumption for the pulse widths will in general not be true. Therefore it is necessary to loosen this requirement by using tolerance windows.

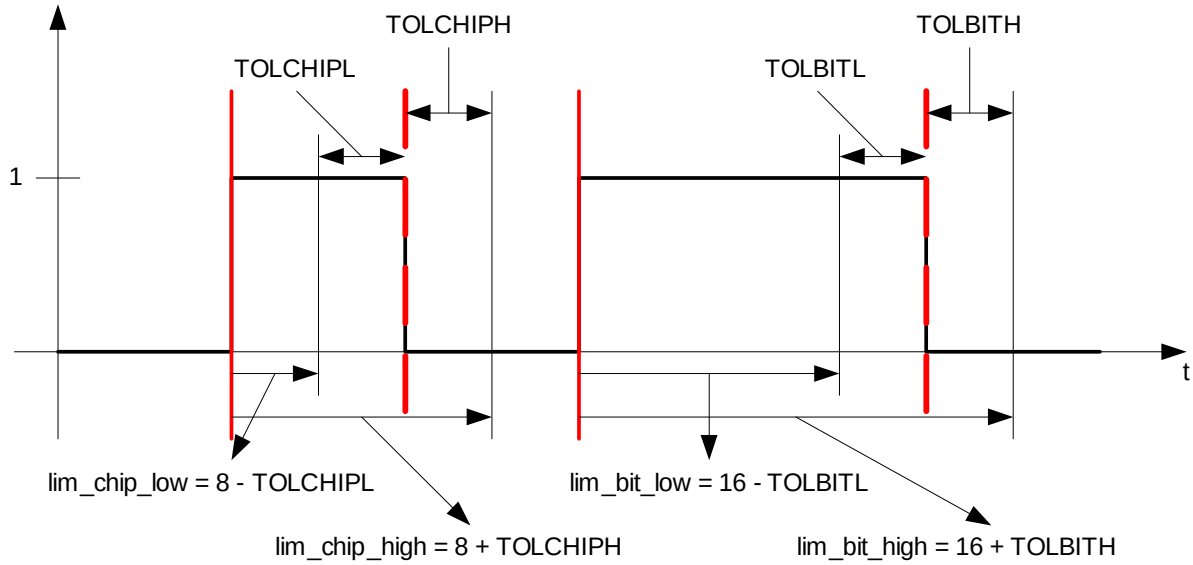


Figure 21 Definition of Tolerance Windows for the CDR

There exist now two registers - x_CDRTOLC for the chip width tolerance and x_CDRTOLB for the bit width tolerance - that can be used to tighten or loosen the windows around the ideal pulse widths. As it can easily be seen from **Figure 21**, tighter windows will result in more stringent requirements for the input data to have a 50% duty cycle and bigger windows will allow the duty cycle to vary more. **Figure 21** also depicts the meaning of the bits in the registers x_CDRTOLC and x_CDRTOLB.

Data Rate Acceptance Limitation

The Clock and Data Recovery is able to accept data rate errors of more than +/-15% with a certain loss of performance. There exist Multi-Configuration applications where the data rate of both configurations are within this range. So the adjacent data rates of these configurations are disturbing each other. The limitation of the data rate acceptance can be activated in this case.

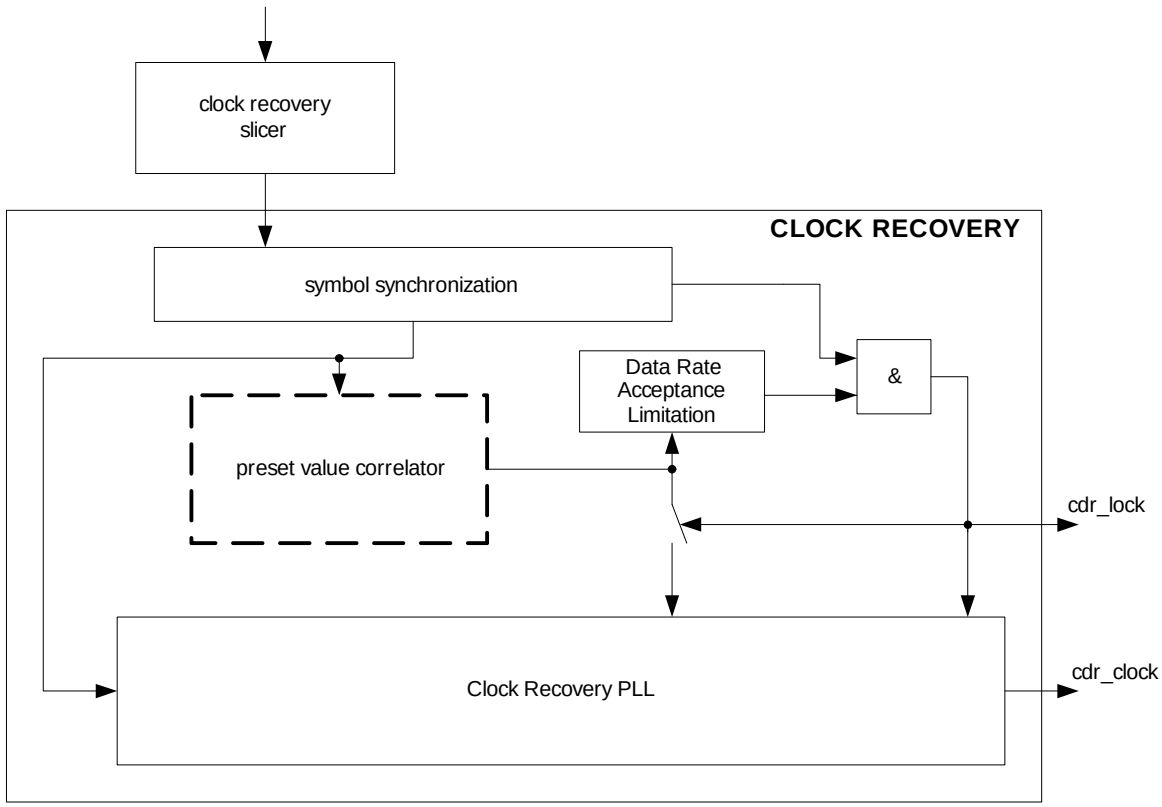


Figure 22 Data Rate Acceptance Limitation

The clock and data recovery (CDR) regenerates the clock based on the input data delivered from the clock recovery (CR) slicer. Symbol synchronization (cdr_lock) is achieved when a specified number of chips (can be set via register x_CDRRI.RUNLEN) has a valid pulse width. In parallel the preset value correlator estimates a preset value for the clock recovery PLL so that a shorter settling time is achieved. This preset value is also proportional to the data rate and is therefore used in the data rate acceptance limitation block. If the preset value is outside a certain range (positive and negative threshold configurable via registers CDRDRTHRP and CDRDRTHRN), the CDR does not go into lock and no symbol synchronization is generated.

For each configuration there exists one bit (register x_CDRRI.DRLIMEN) to switch the data rate acceptance limitation functionality on or off. Data rate acceptance limitation is disabled by default. All configurations share the same threshold registers, the default

thresholds are set so that almost all packets with a data rate error of +/-10% and larger are rejected.

The following statements summarize some important aspects that need to be kept in mind when using the described functionality:

- The output of the estimator must be described on statistical terms - this means that it can not be guaranteed that all packets with a certain data rate outside the allowed range will be rejected
- The quality of the estimated data rate value is mainly influenced by the setting of the signal and noise detectors
- Reducing the RUNIN length in register x_CDRRI reduces the quality of the data rate estimation, resulting in a degradation of the performance of the data rate acceptance limitation block
- The same threshold can be used for FSK and ASK
- If the thresholds are too small it may happen that also packets with a valid data rate are rejected

2.4.8.4 Data Slicer and Line Decoding

The output signal of the matched filter within the internal data processing path is in the range of +x to -x (x is the maximum value of the internal bit width). If Code Violations within a Manchester encoded bitstream have to be detected, the data slicer has to recover the underlying chipstream instead of the bitstream. In this case zero values at the matched filter output lead to an additional slicing threshold and an implicit sensitivity loss. To provide the full reachable sensitivity for applications which do not need the symbols S (space) and M (mark), the data slicer has two different operating modes:

- Chip mode (Code Violations are allowed)
- Bit mode (without Code Violations)

The chip mode introduces an implicit sensitivity loss compared to the bit mode, because a zero-crossing in the 2-chip matched filter signal must be detectable. This is only possible when an additional slicing level is introduced in the data slicer.

The data slicer internally maps a positive value to a 1 and a negative value to a -1. Everything inside the zero thresholds (zero-tube) becomes a 0. After that, the decoding to the chip-level representation is done by mapping the -1 to a "0" chip and the 1 to a "1" chip. A zero out of the data slicer is decoded to chip-level by referencing to the previous chip value.

In bit mode the data slicer has only one threshold (zero) to distinguish between the two levels of the matched filter output. The data slicer internally maps a positive value to a 1 and a negative value to a -1. After that, the selected line decoding is applied.

Summary of data slicer modes in the TDA5240:

Data Slicer Chip mode:

- Code violations detectable (TSI, or EOM)
- Performance loss compared to bit mode
- Activation via setting register x_SLCCFG to a value of
  + 0x90 (Chip Mode EOM-CV: For patterns with code violations in data packet and optimized for activated EOM code violation criterion (and optional EOM data length criterion))
  + 0x94 (Chip Mode EOM-Data length: For patterns with code violations in data packet and optimized for activated EOM data length criterion only)
  + 0x95 (Chip Mode Transparent: When Framer is not used, but CH_DATA / CH_STR are used for data processing)

Data Slicer Bit mode:

- No code violations detectable
- Full performance
- In case of Bi-phase mark and Bi-phase space an additional bit must be sent to ensure correct decoding of the last bit
- Activation via setting register x_SLCCFG to a value of 0x75

In Data Slicer Bit mode an even number of TSI chips needs to be used.

When Data Slicer Bit mode is selected, then the the last chip of RUNIN must be different from first chip of TSI (e.g. Runin-bit sequence 000000 and TSI bit sequence 0xx...xxx is OK). Otherwise the TSI will not be detected correctly.

On using Data Slicer Bit Mode, the Wake-up criteria Equal Bits Detection and Pattern Detection cannot be applied.

A line decoder decodes the incoming data chips according to the encoding scheme (see **Chapter 2.4.8.2**).

2.4.8.5 Wake-Up Generator

A wake-up generation unit is used only in the Self Polling Mode for the detection of a predefined wake-up criterion in the received pattern.

There are two groups of configurable wake-up criteria:

- Wake-up on Level criteria
- Wake-up on Data criteria

The search for the wake-up data criterion is started if data chip synchronization has occurred within the predefined number of symbols, otherwise the wake-up search is aborted. Several different wake-up patterns, like random bit, equal bit, bit pattern or bit synchronization, are programmable.

Additional level criterion fulfilment for RSSI or Signal Recognition can lead to a fast wake-up and to a change to Run Mode Self Polling. Whenever one of these Wake-up Level criteria is enabled and exceeds a programmable threshold, a wake-up has been detected.

The Wake-up Level criterion can be used very effectively in combination with the Ultrafast Fall Back to SLEEP Mode (see **Chapter 2.6.2.3**) for further decreasing the needed active time of the autonomous receive mode. A configurable observation time for Wake-up on Level can be set in the x_WULOT register. The Wake-up on Level criterion can be handled very quickly for FSK modulation, while in case of ASK the nature of this modulation type has to be kept in mind.

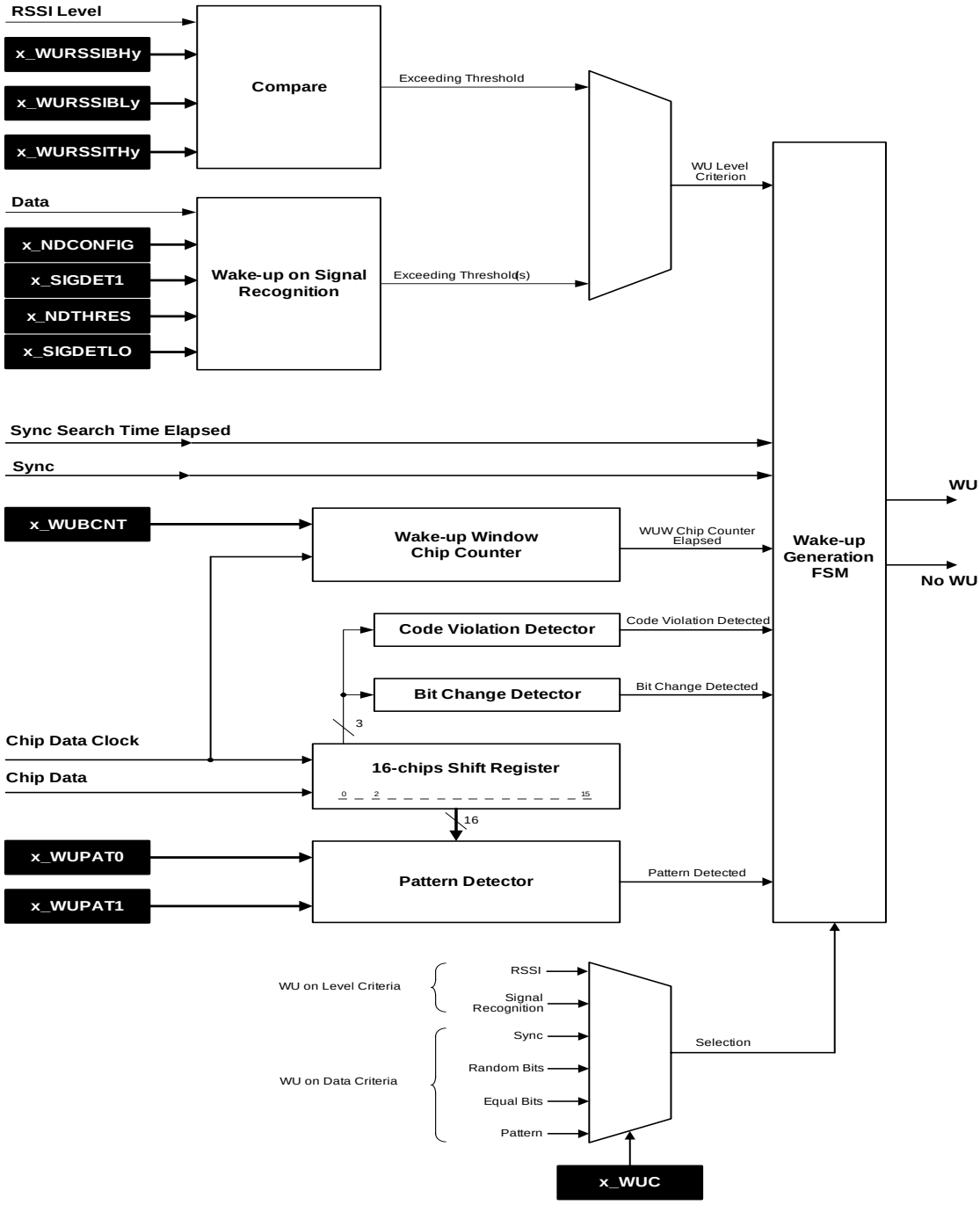


Figure 23 Wake-Up Generation Unit

Wake-Up on RSSI

The threshold x_WURSSITHy is used to decide whether the actual signal is a wanted signal or just noise. Any kind of interfering RSSI level can be blocked by using an RSSI blocking window. This window is determined by the thresholds x_WURSSIBLy and

x_WURSSIBHy, where y represents the actual RF channel. These two thresholds can be evaluated during normal operation of the application to handle the actual interferer environment.

The blocking window can be disabled by setting x_WURSSIBHy to the minimum value and x_WURSSIBLy to the maximum value.

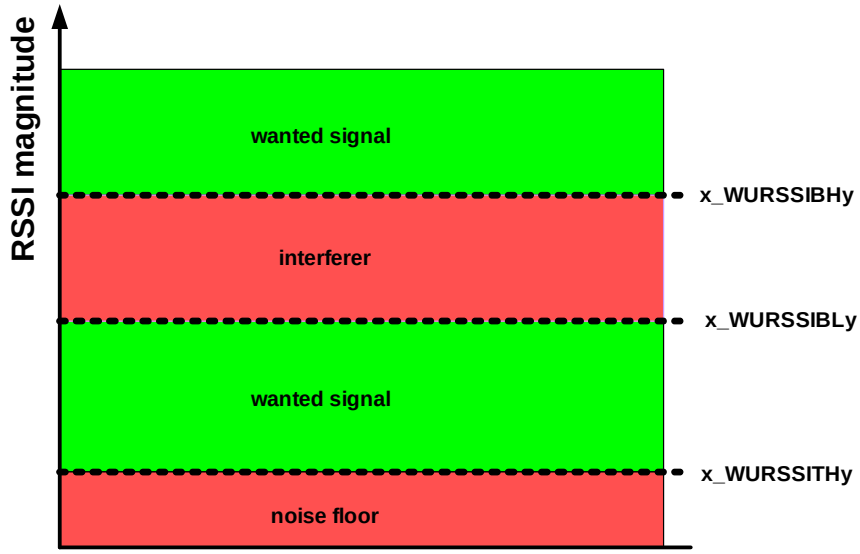


Figure 24 RSSI Blocking Thresholds

Threshold evaluation procedure

A statistical noise floor evaluation using read register RSSIPMF (RMS operation) leads to the threshold x_WURSSITHy. The interferer thresholds x_WURSSIBLy and x_WURSSIBHy are disabled when they are set to their default values.

For evaluation of the interferer thresholds, either use register RSSIPMF for RMS operation or during SPM and WU (Wake-Up) on RSSI use register RSSIPWU to statistically evaluate the interferer band. Finally the thresholds x_WURSSIBLy and x_WURSSIBHy can be set.

Wake-Up on RSSI can also be applied as additional criterion when already using a Wake-Up on Data criterion in Constant On-Off (COO) Mode.

Further details can be seen in **Figure 10**, **Chapter 2.4.7 RSSI Peak Detector**, **Chapter 2.6.2.2 Constant On-Off Time (COO)** and **Chapter 2.6.2.3 Fast Fall Back to SLEEP (FFB)**.

NOTE: If e.g. an interferer ends/starts too close after/to the beginning/end of the observation time, then a decision level error can arise. This is due to the filter dynamics (settling time). Further, for interferer thresholds evaluation in SPM this changes interferer statistics. Several interferer measurements are recommended to suppress this, what makes sense anyway for a better distribution.

Wake-Up on Signal Recognition

Instead of the previously mentioned RSSI criterion, the Signal Recognition criterion (see **Chapter 2.4.8.1**) can be applied for Wake-Up search. So the x_SIGDET1, x_SIGDETLO and x_NDTHRES threshold registers can be used.

The observation time has to be specified in the register x_WULOT. This observation time has to contain the delay in the signal path (12.5 µs + 2.25*T_{bit}) and the duration for the comparison of the Signal Recognition criterion.

The number of consecutive valid Signal Recognition samples/levels is compared vs. a threshold defined in x_WURSSIBHy register. Please note that x_WURSSIBHy register is used for both Wake-Up on RSSI and Wake-Up on Signal Recognition function. This threshold has an influence on the false alarm rate. So x_WURSSIBHy defines the minimum needed consecutive T/16 samples of the Signal Recognition output to be at high level for a positive Wake-Up event generation.

Wake-Up on Data Criterion

All SFRs configuring the Wake-up Generation Unit support the Multi-Configuration capability. The search for a wake-up data criterion is started if symbol synchronization is given within a certain duration (see **Chapter 2.4.8.8 RUNIN, Synchronization Search Time and Inter-Frame Time**); otherwise the wake-up search is aborted. During the observation period, the wake-up data search is aborted immediately if symbol synchronization is lost. If this is not the case, the wake-up search will last for the number of chips/bits defined in the register x_WUBCNT.

The Wake-up Window (WUW) Chip/Bit Counter counts the number of received chips/bits and compares this number vs. the number of chips/bits defined in the register x_WUBCNT.

The Code Violation Detector checks the incoming chip data stream for being Bi-Phase coded. A Code Violation is given if three consecutive chips are ’One’ or ’Zero’.

The Bit Change Detector checks the incoming Bi-phase coded bit data stream for changes from 'Zero' to 'One' or 'One' to 'Zero'.

The Pattern Detector searches for a pattern with 16 chips/bits length within the Wake-up Window. The pattern is configurable via the registers x_WUPAT0 and x_WUPAT1.

On using Data Slicer Bit Mode, the Wake-up criteria Equal Bits Detection and Pattern Detection cannot be applied. Further details can be seen at the end of **Chapter 2.4.8.4**.

The selection of 1 out of 4 wake-up data criteria is done via the x_WUC register.

Details on the four wake-up data criteria

Pattern Detection

The incoming signal must match a dedicated pattern of up to 8 bits or 16 chips in Wake-Up Pattern Chip Mode. When the WUW chip counter elapses, the search is stopped. The higher the setting of WUBCNT the longer it is possible to search for the wake-up pattern. The minimum for the WUBCNT is 0x11!

The pattern detection is stopped either when WUW elapses, or when symbol synchronization is lost.

The Wake-Up pattern can be extended from 16 chips to 16 bits on activation of WUPMSEL bit (Wake-Up Pattern Bit Mode). In this Bit Mode no Code Violations (CV) are allowed and thus Pattern Detection is aborted, when a CV is detected.

Equal Bits Detection

Wake-up condition is fulfilled if all received bits inside of WUW are either 0 or 1. WUBCNT holds the number of required equal bits. The higher the setting of WUBCNT the lower the number of wrong wake-ups.

Equal bits detection is stopped if a bit change or a CV has been detected, or symbol synchronization is lost.

Random Bits Detection

Wake-up condition is fulfilled if there is no code violation inside of WUW. WUBCNT holds the number of required Bi-phase coded bits. The higher the setting of WUBCNT, the lower the number of wrong wake-ups.

Random bits detection is stopped if a code violation has been detected, or symbol synchronization is lost.

Valid Data Rate Detection

Wake-up condition is fulfilled if symbol synchronization is possible inside of Sync Search Time out (see **Chapter 2.4.8.8 RUNIN, Synchronization Search Time and Inter-Frame Time**). WUBCNT is not used.

This is the weakest wake-up data criterion, and should be avoided.

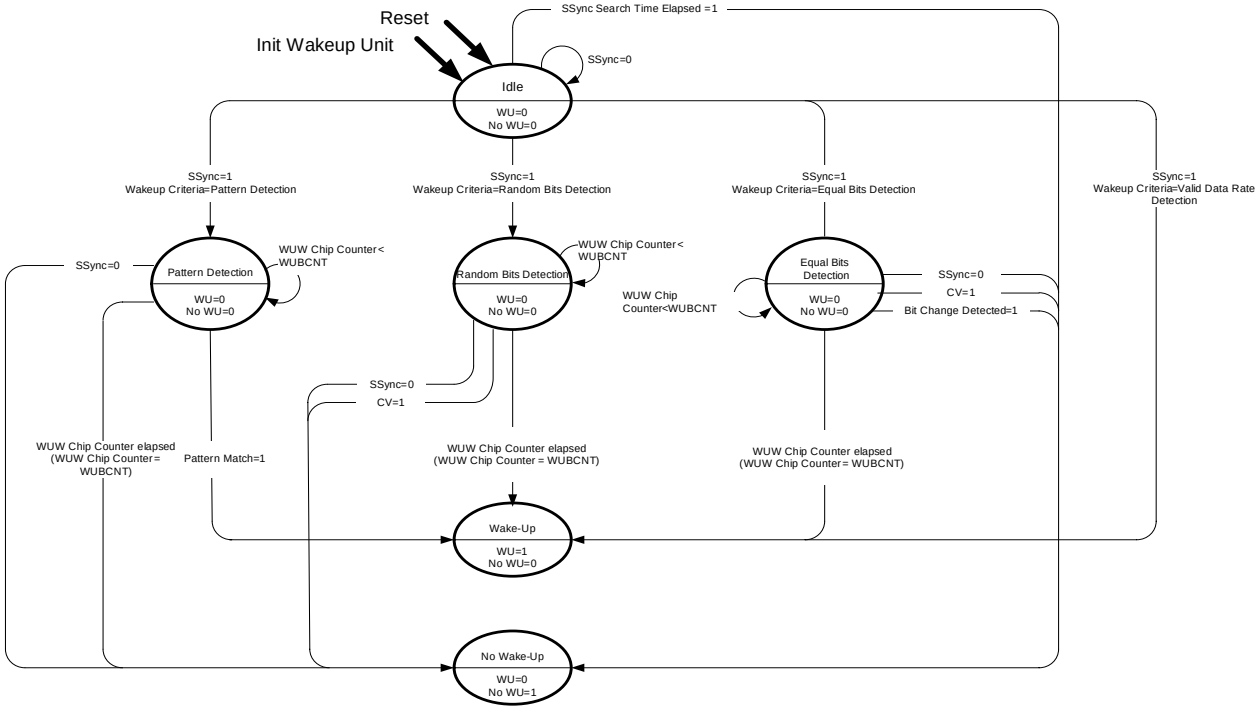


Figure 25 Wake-Up Data Criteria Search

2.4.8.6 Frame Synchronization

The Frame Synchronization Unit (Framer) synchronizes to a specific pattern to identify the exact start of a payload data frame within the data stream. This pattern is called Telegram Start Identifier (TSI).

There are different TSI modes selectable via the configuration:

- 16-Bit TSI Mode, supporting a TSI length of up to 16 bits or 32 chips
- 8-Bit Parallel TSI Mode, supporting two independent TSI pattern of up to 8 bits length each. Different payload length is possible for these two TSI pattern.
- 8-Bit Extended TSI Mode, identical to 8-Bit Parallel TSI Mode, but identifies which pattern matches by adding a single bit at the beginning of the data frame
- 8-Bit TSI Gap Mode, supporting two independent TSI pattern separated by a discontinuity

All SFRs configuring the Frame Synchronization Unit support the Multi-Configuration capability (Config A, B, C and D). The Framer starts working in Run Mode Slave after Symbol Sync found and in Self Polling Mode after wake-up found and searches for a frame until TSI is found or synchronization is lost. The input of the Framer is a sequence

of Bi-phase encoded data (chips). Basically the Framer consists of two identical correlators of 16 chips in length. It allows a Telegram Start Identifier (TSI) to be composed of Bi-phase encoded “Zeros” and “Ones”. The active length of each of the 16 chips correlators is defined independently in the x_TSILENA and x_TSILENB registers. The pattern to match is defined as a sequence of chips in the x_TSIPTA0, x_TSIPTA1, x_TSIPTB0 and x_TSIPTB1 registers.

Note that the RUNIN length shown in the figures below is the maximum needed RUNIN with the length of 8 chips. Further details on the needed RUNIN time of the receiver can be seen in **Chapter 2.4.8.3 Clock and Data Recovery**.

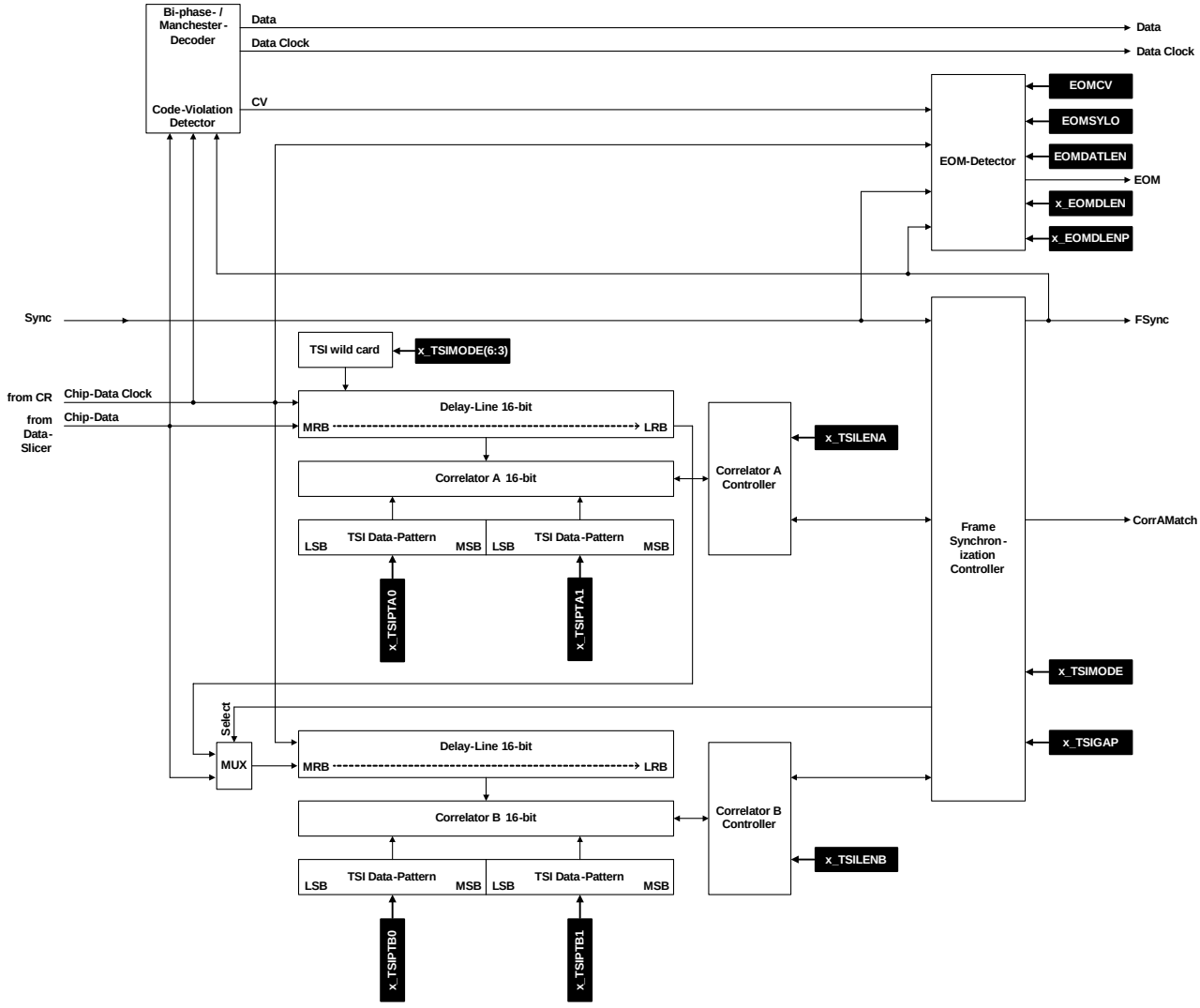


Figure 26 Frame Synchronization Unit

Please note that for Data Slicer Bit Mode a special constellation of RUNIN bits and TSI bits has to be ensured. Further details can be seen at the end of **Chapter 2.4.8.4**.

The two independent correlators can be configured in the x_TSIMODE register to work in one of the following four TSI modes:

16-Bit Mode: As a single correlator of up to 32 chips

The length of the x_TSILENA register must be set to 16d whenever x_TSILENB is higher than 0.

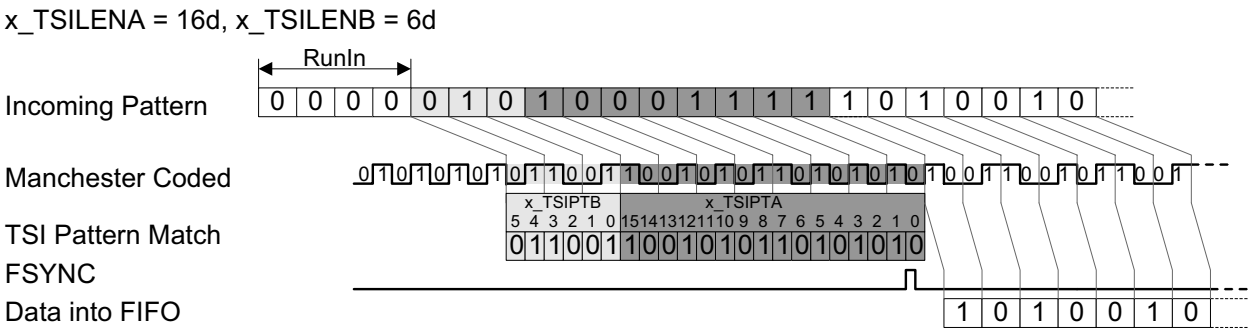


Figure 27 16-Bit TSI Mode

8-Bit Parallel Mode: As two correlators of up to 16 chips length each working simultaneously in parallel

In the following example, TSI Pattern B matches first and generates an FSYNC. The lengths of both TSI Patterns are now independent from each other. The payload length for these two TSI Pattern may be different.

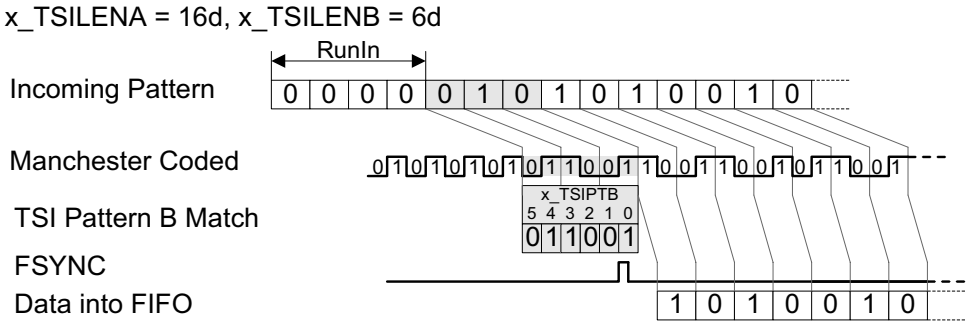


Figure 28 8-Bit Parallel TSI Mode

8-Bit Extended Mode: As two correlators of up to 16 chips length each working simultaneously in parallel, with matching information insertion

This bit is inserted at the beginning of the payload. “0” is inserted, when correlator A has matched and “1” when correlator B has matched. The payload length for these two TSI Pattern may be different.

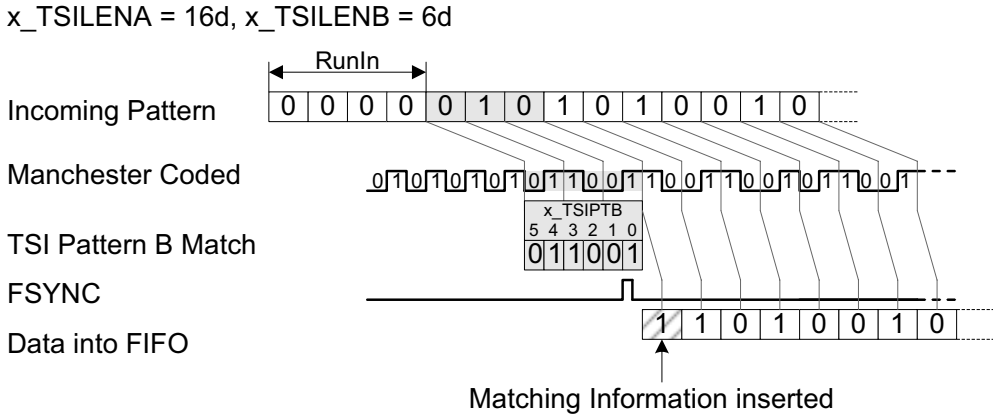


Figure 29 8-Bit Extended TSI Mode

8-Bit Gap Mode: As two sequentially working correlators of up to 16 chips length each

This mode is only used in combination with the TSI Gap Mode shown below!

This mode is used to define a gap between the two patterns which is preset in the x_TSIGAP register. To identify exactly the beginning of the gap it would be helpful on occasion to place the first CV of the gap into the TSI Pattern A. In this case, the gap length needed for the x_TSIGAP register must be shortened and the x_TVWIN length must be extended.

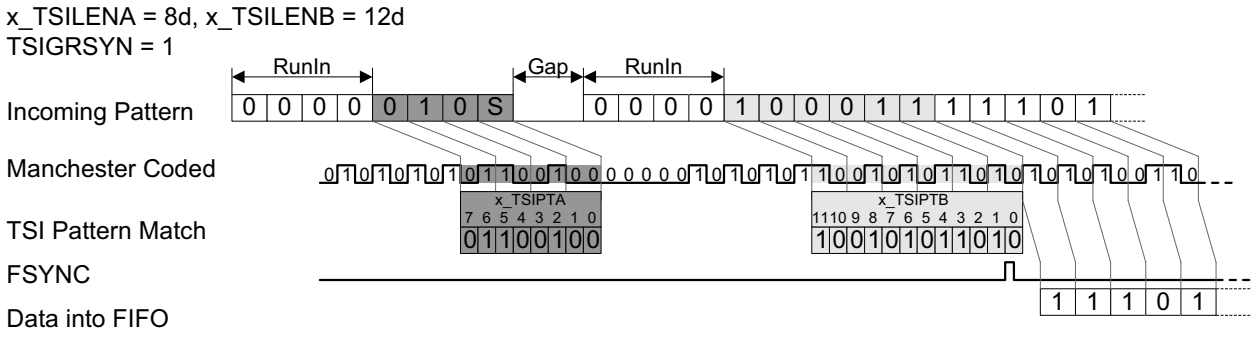


Figure 30 8-Bit Gap TSI Mode

Selection of a TSI Pattern

TSI patterns must be different to the wake-up bit stream and the RUNIN to clearly mark the start of the following payload data frame. It should be considered that the synchronization has a tolerance of about one bit. In addition, synchronization is related to data chips, and may occur in the middle of a data bit. This all must be tolerated by the data framer. Further details can be seen in **Chapter 2.4.8.3 Clock and Data Recovery**.

Ideal TSI patterns have a unique bit combination at their end, which may also contain a number of code violations (CVs), when possible (see **Chapter 2.4.8.4 Data Slicer and Line Decoding**).

Some examples of TSI patterns:

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1

0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1

0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0

1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0

When CVs are used:

0 0 0 0 0 0 0 0 0 0 0 0 0 M 1

1 1 1 1 1 1 1 1 1 1 1 1 1 M 0

Note: CVs in a TSI are practical for better differentiation to the real data, especially if repetition of data frames is used for wake-up.

End of Message (EOM) Detection

An End Of Message (EOM) detection feature is provided by the EOM detector. Three criteria can be selected to indicate EOM.

The first is based on the number of received bits since frame synchronization. The number of expected bits is preset in the x_EOMDLEN register. Sending fewer bits as defined in the register will result in no EOM. The EOM counter will be reset after new frame synchronization.

In 8-Bit Parallel TSI Mode and 8-Bit Extended TSI Mode, the payload length for the two independent TSI pattern may be different. Therefore the payload length for TSI B pattern can be preset in the x_EOMDLENP register, while payload length for TSI A pattern can be preset in the x_EOMDLEN register.

The second criterion is the detection of a Code Violation. This EOM criterion is not applicable for Data Slicer Bit mode.

The third criterion is the loss of symbol synchronization. Depending on the x_TVWIN register, the Sync signal persists for a certain amount of time after the end of the pattern has been reached. Therefore, more bits could be written into the FIFO than sent. The three EOM criteria can be combined with each other. If one of the selected EOM criteria is fulfilled, an EOM signal will be generated.

TSI Gap Mode

The TSI Gap Mode is only used if TSI patterns contain a gap that is not synchronous to the data rate, e.g. if a gap is 7.7 data bits, or if a gap is longer than 10 data bits. In all other cases, gaps should be included in the TSI pattern as code violations.

Because of its complexity in configuration, TSI Gap Mode should be only used in applications as noted above!

For these special protocols, it is possible to lock the actual data frequency during a long Code Violation period inside a TSI (x_TSIGAP must have a minimum of 8 chips). TSIGAP is used to lock the PLL after TSI A was found. After the lock period, two different resynchronization modes are available (TSI Gap ReSYNchronization, TSIGRSYN):

- Frequency readjustment (PLL starts from the beginning), TSIGRSYN = 1. In this mode the T/2 gap resolution can be set in the 5 MSB x_TSIGAP register bits. The value in GAPVAL (3 LSB in x_TSIGAP register) is not used. This is the preferred mode in TSI Gap Mode.

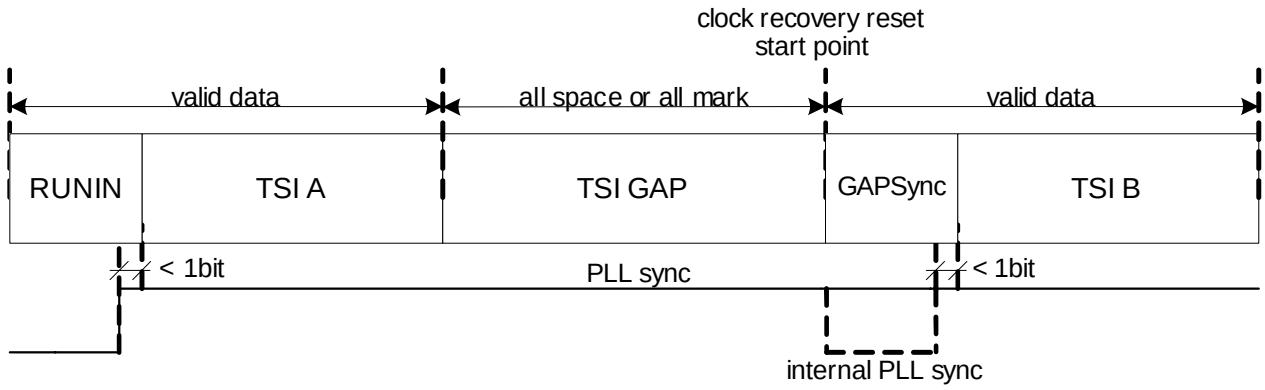


Figure 31 Clock Recovery Gap Resynchronization Mode TSIGRSYN = 1

- Phase readjustment only, TSIGRSYN = 0. In this mode, the value in GAPVAL is used to correct the phase after the gap phase. Overall gap time can be defined in T/16

steps. The 5 MSB bits (TSIGAP) define the real gap time and the 3 LSB bits (GAPVAL) the DCO (digital controlled oscillator) phase correction value.

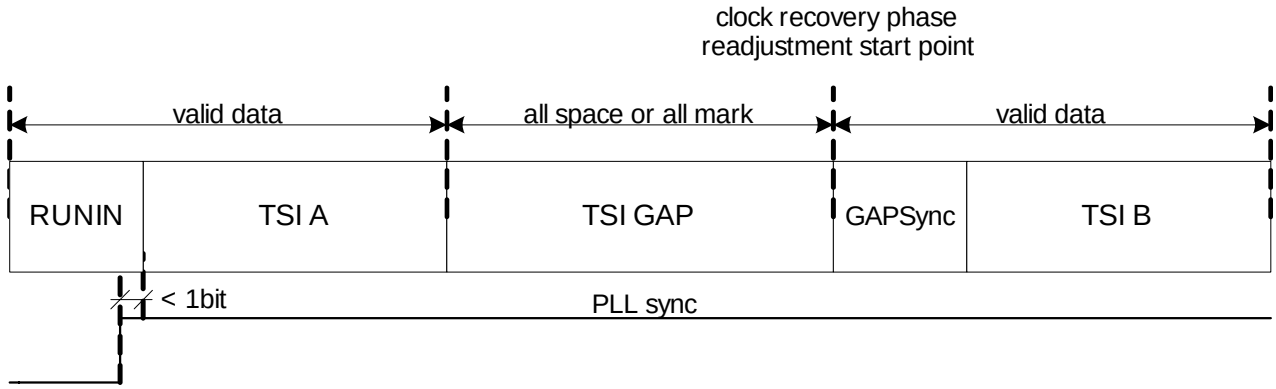


Figure 32 Clock Recovery Gap Resynchronization Mode TSIGRSYN = 0

When the time TSI GAP in the start sequence of the transmitted telegram has elapsed, the receiver needs a certain time (GAPSync = 5...6 chips) to readjust the PLL settings.

Behavior of the system at the starting position of the TSI B:

The starting position (TSI B start) for the TSI B comparison is independent from the RUNIN settings (x_CDRRI register) and the resynchronization mode (x_TSIMODE register):

$$TSIBstart[chips] = TSIGAP[chips] + 6...8$$

The incoming chips at TSI B start and the following incoming chips are compared with the contents of the register TSI B. Please notice that the receiver's PLL runs at the data rate determined before the gap. Therefore, the receiver calculates the gap based on this data rate.

Behavior of the system at the ending position of TSI B:

The system checks for the TSI B to match within a limited time. If there is no match within this time, then the receiver starts again to search for the TSI A pattern at the following incoming chips:

$$TSIBstop[chips] = TSIGAP[chips] + TSILENB[chips] + 11$$

For a successful TSI B pattern match, the defined TSI B pattern must be between "Start of TSI B" and "Stop of TSI B". In the example below, the earliest possible start position would be the 18^{th} chip and the latest possible start position would be the 22^{nd} chip.

Please note that after a gap, the internal TSI comparison register is cleared (all chips set to ’0’). In this case, a TSI B criteria of “0000” would always match at the beginning. To avoid such an unwanted matching, set the highest TSI B match chip to ’1’.

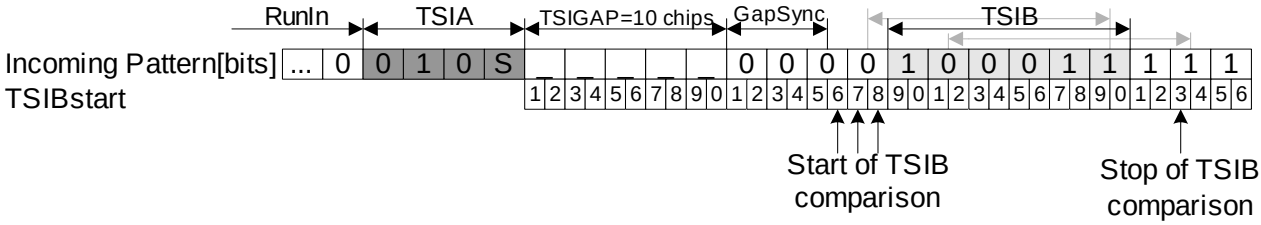


Figure 33 TSIGap TSIB Timing

The TVWIN (Timing Violation WINdow) and TSIGAP dependency is shown in **Figure 34**.

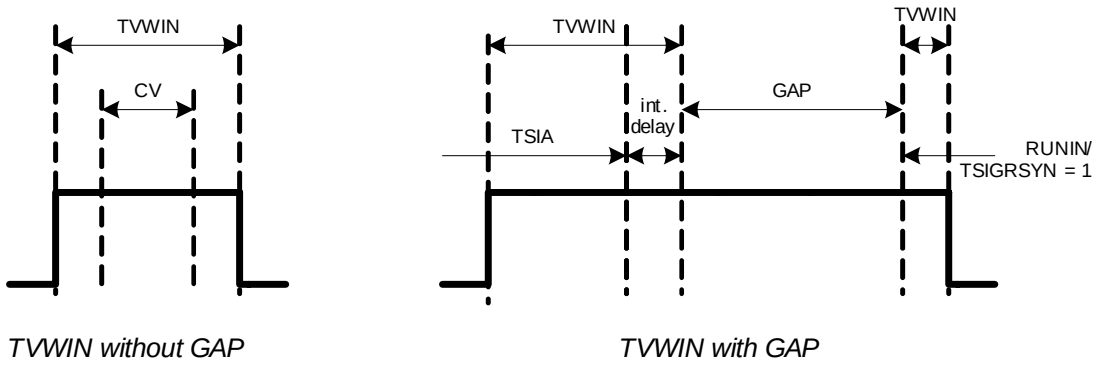


Figure 34 TVWIN and TSIGAP dependency example

TVWIN calculation for pattern without Gap time:

$$TVWIN = round((8 + 16 \cdot CV + 8) \cdot 1.25)$$

The entire TVWIN time is made up of the CV[1)] number itself, the half bit before CV and the half bit after the CV. To reach all frequency and duty cycle errors, 25% of the overall sum must be added.

TVWIN calculation with Gap time:

$$TVWIN = round(max\{((8 + 16 \cdot CV + 8) \cdot 1.25), (8 + 16 \cdot TSIA_{CV} + 16 \cdot 1 + 8) \cdot 1.25\})$$

1) CV...number of bits containing manchester code violations

2.4.8.7 Message ID Scanning

This unit is used to define an ID or special combination of bits in the payload data stream, which identifies the pattern. All SFRs configuring the Message ID Scanning Unit feature the Multi-Configuration capability. Furthermore, it is available in the Slave and Self Polling Mode. The MID Unit can be mainly configured in two modes: 4-Byte and 2-Byte organized Message ID. For each configuration there are 20 8-bit registers designed for ID storage. SFRs are used to configure the MID Unit: Enabling of the MID scanning, setting of the ID storage organization, the starting position of the comparison and number of bytes to scan.

When the Message ID Scanning Unit is activated, the incoming data stream is compared bit-wise serially with all stored IDs. If the Scan End Position is reached and all received data have matched the observed part of at least one MID the Message ID Scanning Unit indicates a successful MID scanning to the Master FSM, which generates an MID interrupt.

Please note that the default register value of the MID registers is set to 0x00. All MID registers must be set to a pattern value to avoid matching to default value 0x00.

If the MID Unit finishes ID matching without success, the data receiving is stopped and the FSM waits again for a Frame Start criterion. The received bits are still stored in the FIFO.

4-Byte Organized Message ID:

In this mode four bytes are merged to define an ID-Pattern. This does not mean that the ID must be exact four bytes long. The number of bytes used is defined in register x_MIDC1. Up to 5 ID Patterns are available.

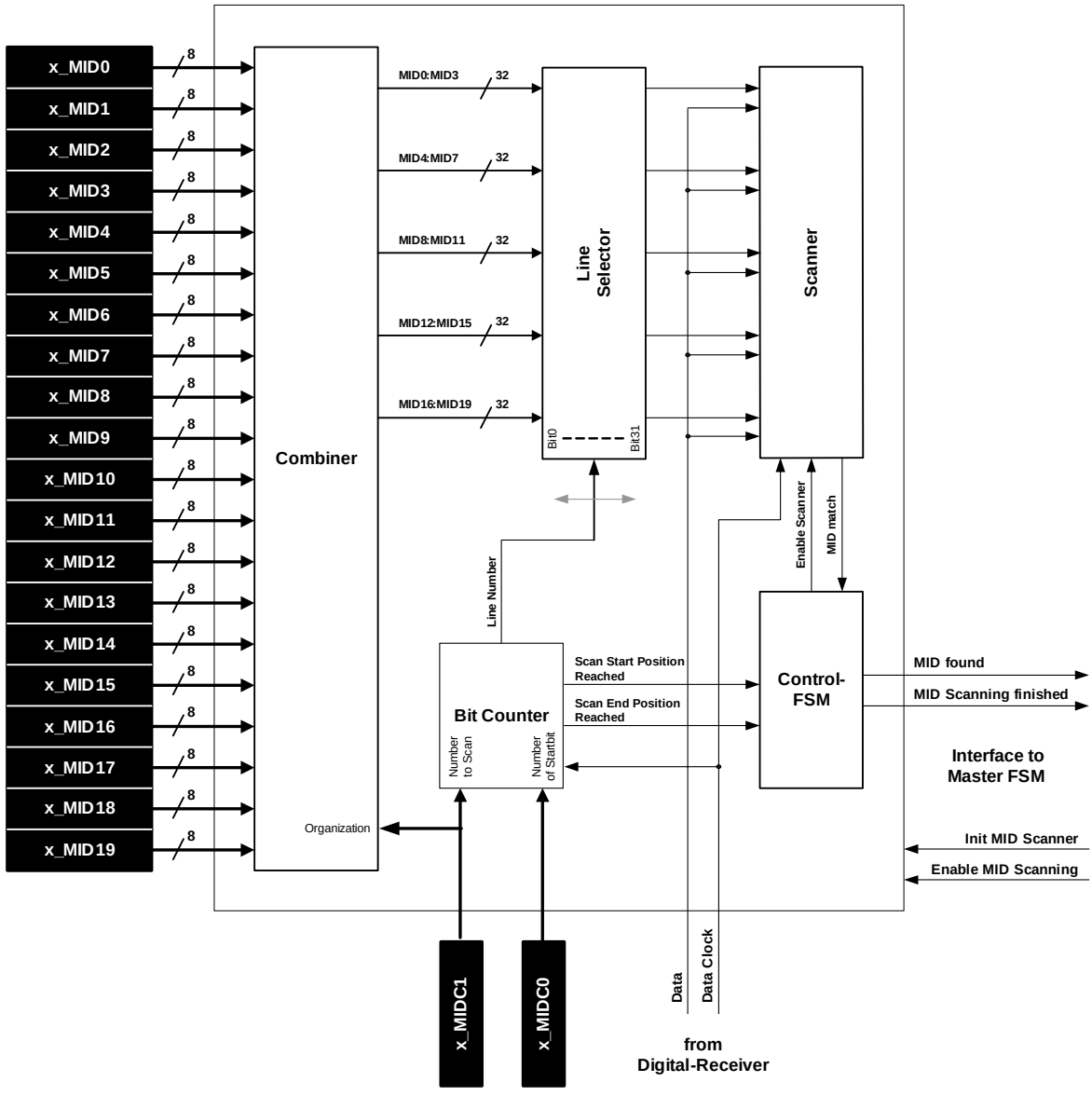


Figure 35 4-Byte Message ID Scanning

2-Byte Organized Message ID:

In this mode two bytes are merged to define an ID Pattern. Up to 10 patterns are possible.

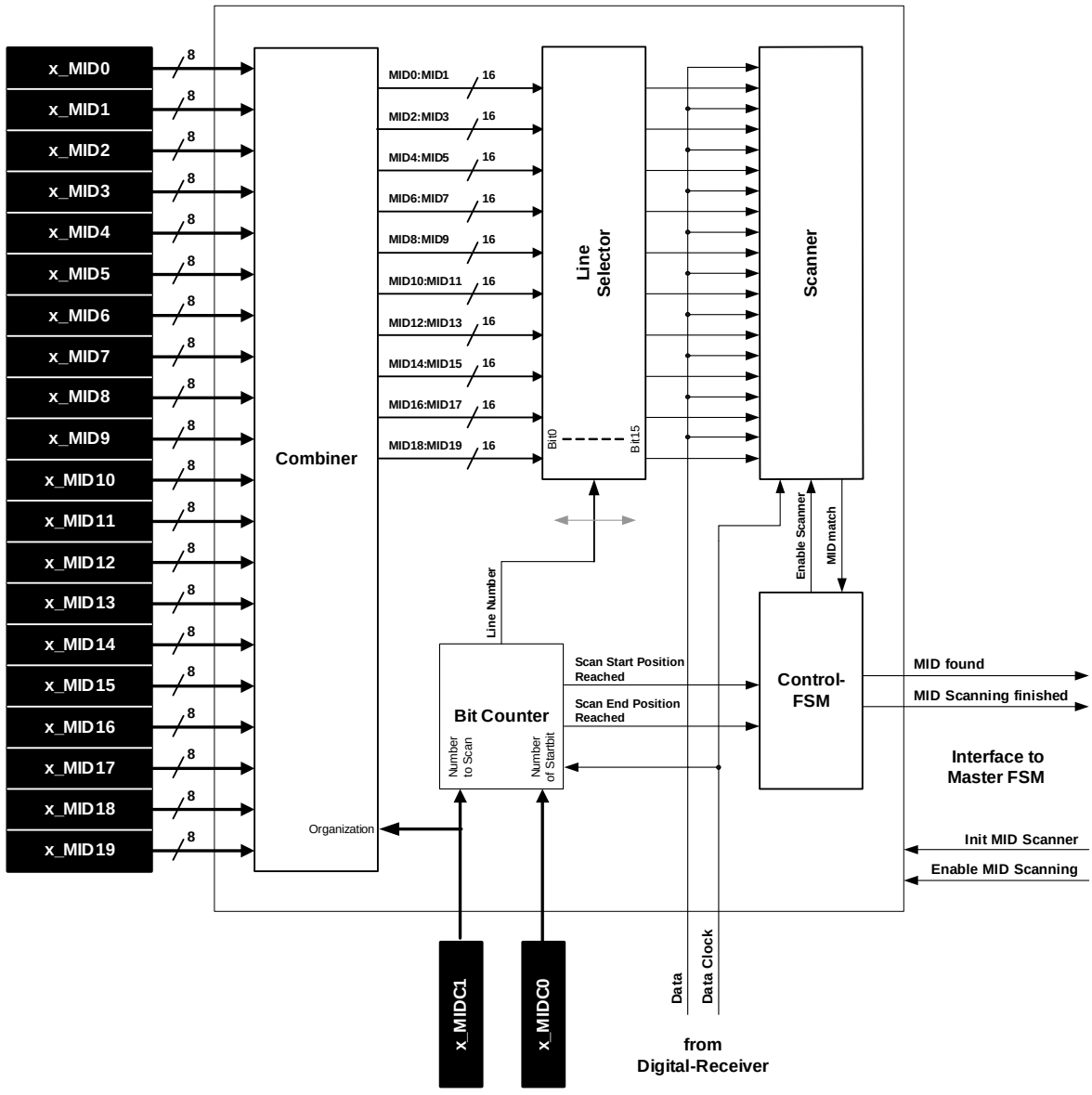


Figure 36 2-Byte Message ID Scanning

ID Position Configuration:

It is possible to choose which part of the incoming data stream is compared against the stored MIDs. The register x_MIDC0 contains the Scan Start Position. If the Bit Counter detects the Scan Start Position, the Control FSM enables the Scanner. The register x_MIDC1 contains the number of bytes to scan. During the observation period, the

Message ID Scanning is aborted immediately by the Master FSM, if symbol synchronization is lost or an EOM (End Of Message) is detected.

Example:

Start Selection: 00010001b

Number to scan: 00b, 01b, 10b, 11b

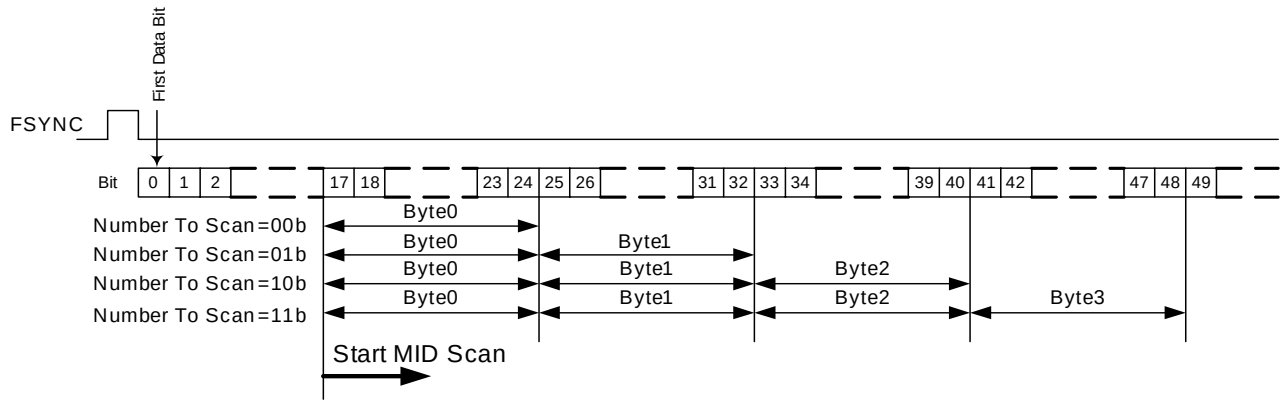


Figure 37 MID Scanning

The starting position in this case is Bit 17. Depending on the number to scan, the corresponding number of bytes is compared with the stored MIDs.

2.4.8.8 RUNIN, Synchronization Search Time and Inter-Frame Time

The functionality of the Digital Baseband Receiver is divided into four consecutive data processing stages; the data filter, clock and data recovery, data slicer and frame synchronization unit. The architecture of the Digital Baseband Receiver is optimized for processing bi-phase coded data streams.

The basic structure of a payload frame is shown in **Figure 38**. The protocol starts with a so called RUNIN. The RUNIN with the minimum length of four bi-phase coded symbols is used for internal filter settling and frequency adjustment. The TSI (Telegram Start Identifier), which is used as framing word, follows the RUNIN sequence. The payload contains the effective data. The length of the valid payload data is defined as the length itself or additional criteria (e.g. loss of Sync).

Please note that almost all transmitted protocols send a wake-up sequence before the payload frame (see also **Figure 72**). This wake-up sequence allows a very fast decision, whether there is a suitable message available or not. Further details on this topic can be gained from **Chapter 2.6.1.5** and **Chapter 2.4.8.5**.

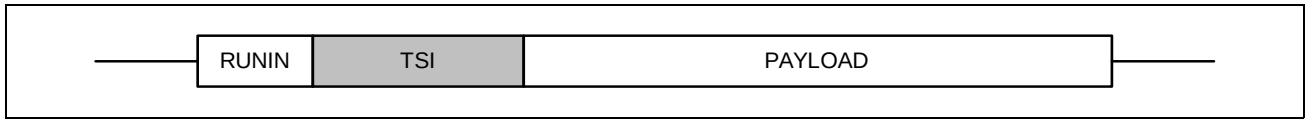


Figure 38 Structure of Payload Frame

Two important system parameters are described in this section: the **Sy**nchronization **Sea**r**ch** **T**ime **O**ut (SYSRCTO) and the Inter-Frame Time. The processing sequence of a payload frame is shown in **Figure 39**.

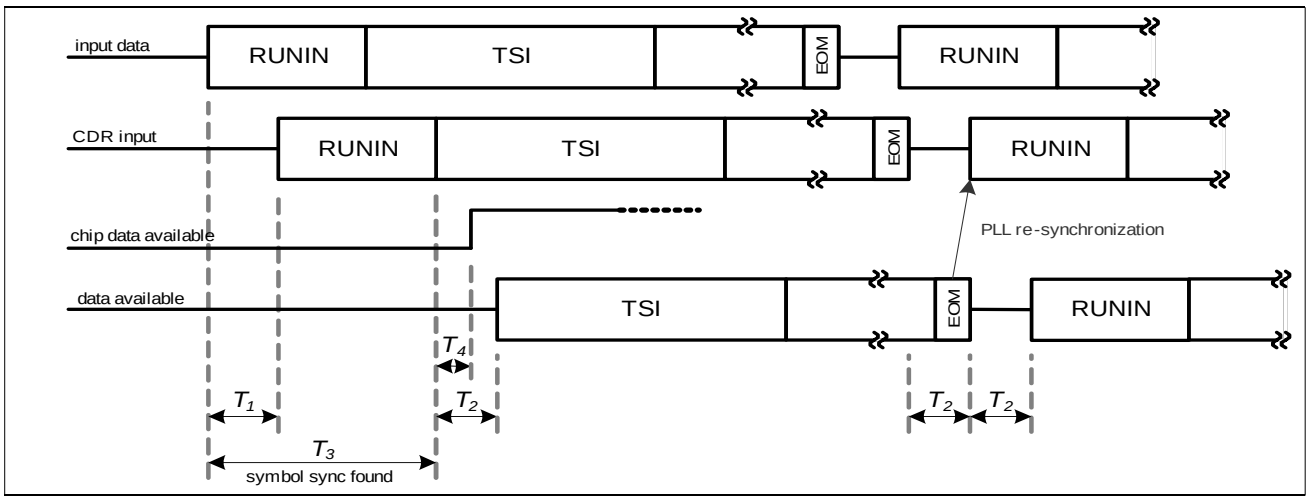


Figure 39 Data Latency

The overall system latency time is calculated in two steps: T_1 is the delay between ADC input (ASK) / limiter output (FSK) and the CDR input, and T_2 is the time between Symbol Sync Found and the Framer output (decoded data available).

T_4 is the time between Symbol Sync Found and Chip Data output (RX mode TMCDS). T_4 = 1 T. T is the nominal duration of one data bit.

T_1 latency time include: (T_1 = 12.5µs + 2 T)

- digital frontend processing delay
- matched filter computation time
- signal detector delay

T_2 latency time include: (T_2 = 1.5 T + 0.5 T[1)])

- Data Slicer computation time
- Framer computation time.

1) The 0.5 T have to be added in case of activation of Bi-phase mark / space decoding mode and Data Slicer Bit mode without Code Violation (see register x_SLCCFG)

The synchronization search time T_3 is the time the receiver requires to search for a pattern in an incoming data stream and needs to be considered in the receivers start-up phase. The minimum value of the search time out length is the consequence of the system latency time T_1, the RUNIN length and the time of asynchronism between transmitter and receiver.

This means, that for the minimum length of register value for SYSRCTO, the value 2 bits plus 12.5 µs plus the RUNIN length, which is set in the x_CDRRI register, plus 2 bits (to consider worst case RUNIN patterns and TX-RX asynchronism) have to be used. To reach data rate and duty cycle errors, 10% of the overall sum must be added.

$$SYSRCT0 = roundup\left(\left(\left(\frac{12.5\mu s}{T_{bit}} + 2 + RUNLEN + 2\right) \cdot 16\right) \cdot 1.1\right)$$

A second important system parameter that must be considered, is the minimal Inter-Frame Time (time between two data frames). This time is equal to the time T_2 and has a length of 1.5 or 2 bits[1)]. The EOM to PLL resynchronization time is negligible in case INITDRXES is disabled. Otherwise T_1 has to be added.[2)]

Note that the described Inter-Frame Time is based on the input pattern with equal signal power in the following data frame; in other cases, the Inter-Frame Time can vary from the calculated value.

$$T_{Inter-Frame} = 1.5T_{bit} + \begin{pmatrix} 0.5T_{bit}^{1)} \\ 0 \end{pmatrix} + \begin{pmatrix} T_1^{2)} \\ 0 \end{pmatrix}$$

1) see previous footnote

2) in case INITDRXES is enabled

2.4.9 Power Supply Circuitry

The chip may be operated within a 5 Volts or a 3.3 Volts environment.

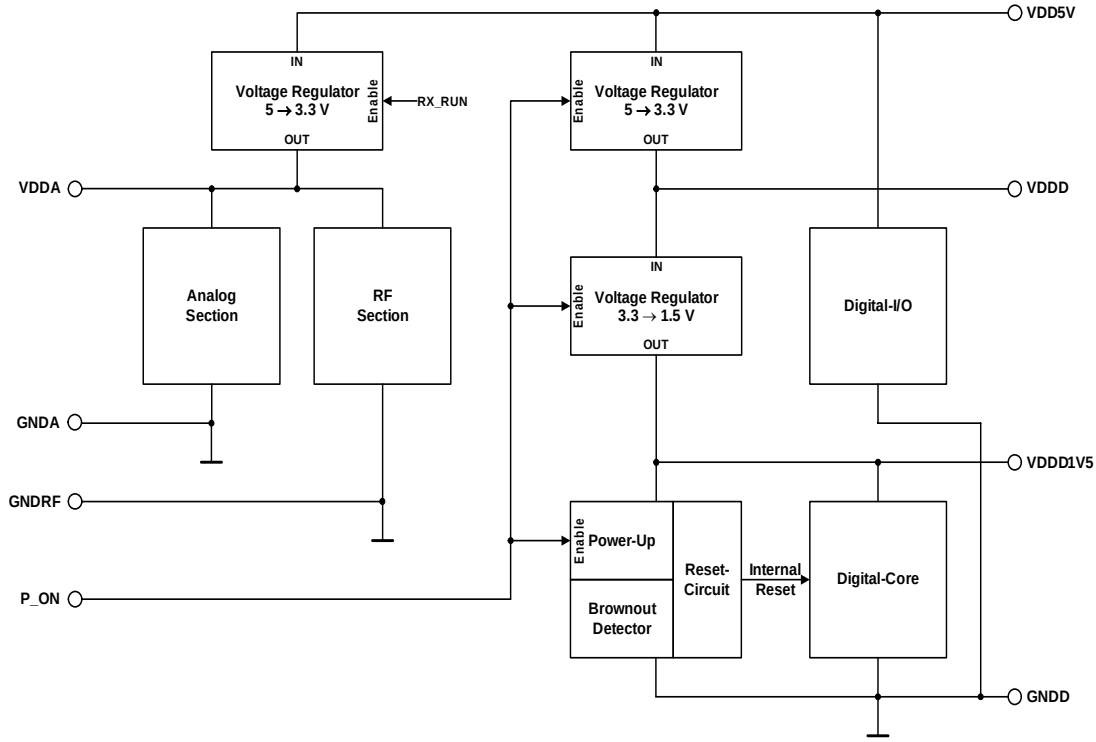


Figure 40 Power Supply

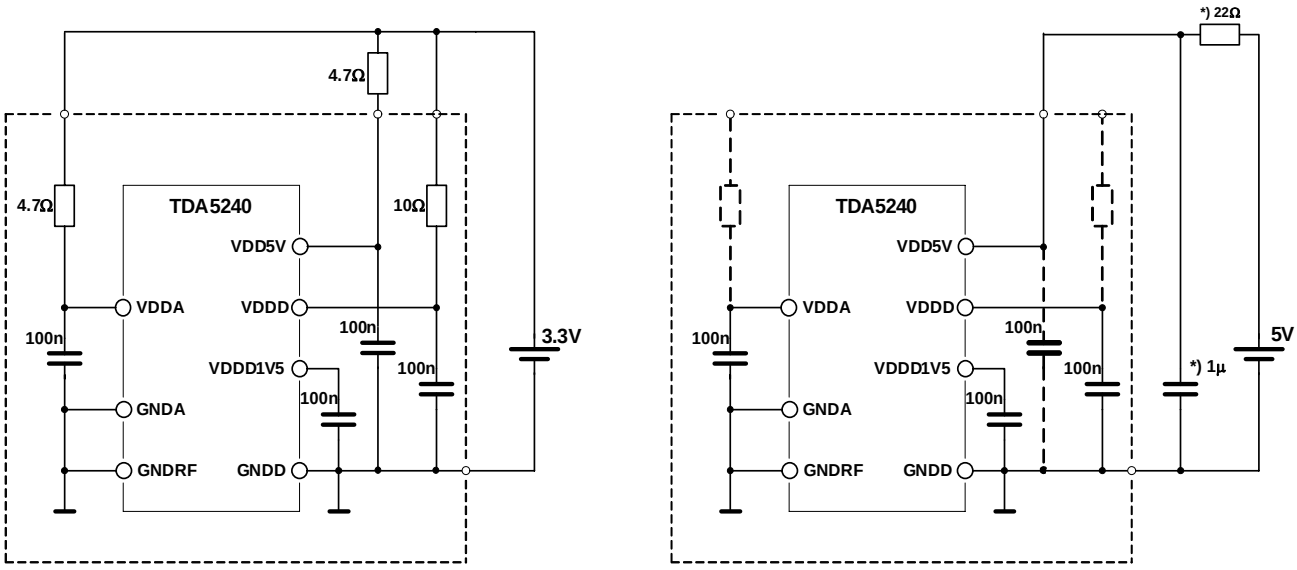
For operation within a 5 Volts environment (supply voltage range 1), the chip is supplied via the VDD5V pin. In this configuration the digital I/O pads are supplied via VDD5V and a 5 V to 3.3 V voltage regulator supplies the analog/RF section (only active in Run Modes).
When operating within a 3.3 Volts environment (supply voltage range 2), the VDD5V, VDDA and VDDD pins must be supplied. The 5 V to 3.3 V voltage regulators are inactive in this configuration.

The internal digital core is supplied by an additional 3.3 V to 1.5 V regulator.

The regulators for the digital section are controlled by the signal at P_ON (Power On) pin. A low signal at P_ON disables all regulators and set the IC in Power Down Mode. A low to high transition at P_ON enables the regulators for the digital section and initiates a power on reset. The regulator for the analog section is controlled by the Master Control Unit and is active only when the RF section is active.

To provide data integrity within the digital units, a brownout detector monitors the digital supply. In case a voltage drop of VDDD below approximately 2.45 V is detected a RESET will be initiated.

A typical power supply application for a 3.3 Volts and a 5 Volts environment is shown in the figure below.



Supply-Application in 3.3V environment

Supply-Application in 5V environment

*) When operating in a 5V environment, the voltage-drop across the voltage regulators 5 → 3.3V has to be limited, to keep the regulators in a safe operating range. Resistive or capacitive loads (in excess to the scheme shown above) on pins VDDA and VDDD are not recommended.

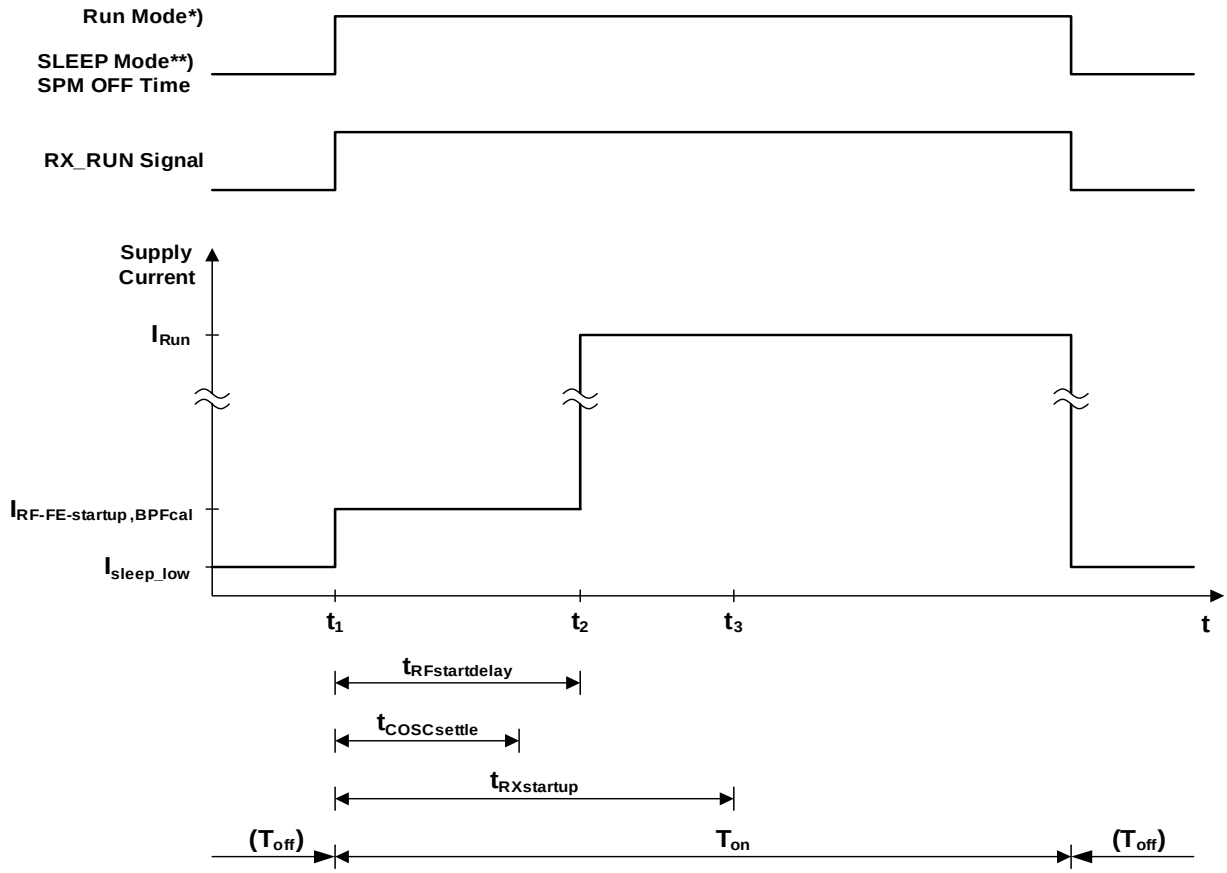
Figure 41 3.3 Volts and 5 Volts Applications

2.4.9.1 Supply Current

In SLEEP Mode, the Master Control Unit switches the crystal oscillator into Low Power Mode (all internal load capacitors are disconnected) to minimize power consumption. This is also valid for Self Polling Mode during Off time (SPM_OFF).

Whenever the chip leaves the SLEEP Mode/SPM_OFF (t_1), the crystal oscillator resumes operation in High Precision Mode and requires $t_{COSCsettle}$ to settle at the trimmed frequency. At t_2 the analog signal path (RF and IF section) and the RF PLL are activated. At t_3 the chip is ready to receive data. The chip requires $t_{RXstartup}$ when leaving SLEEP Mode/SPM_OFF until the receiver is ready to receive data.

A transient supply current peak may occur at t_1, depending on the selected trimming capacitance. The average supply current drawn during $t_{RFstartdelay}$ is $I_{RF\text{-}FE\text{-}startup,BPFcal}$.



*) Run Mode covers the global chip states Run Mode Slave/ Receiver active in Self Polling Mode/ Run Mode Self Polling
**) I_{sleep_low} is valid in the chip states SLEEP / Off time during Self Polling Mode

Figure 42 Supply Current Ramp Up/Down

If the IF buffer amplifier or the clock generation feature (PPx pin active) are enabled, the respective currents must be added.

2.4.9.2 Chip Reset

Power down and power on are controlled by the P_ON pin. A LOW at this pin keeps the IC in Power Down Mode. All voltage regulators and the internal biasing are switched off. A high transition at P_ON pin activates the appropriate voltage regulators and the internal biasing of the chip. A power up reset is generated at the same time.

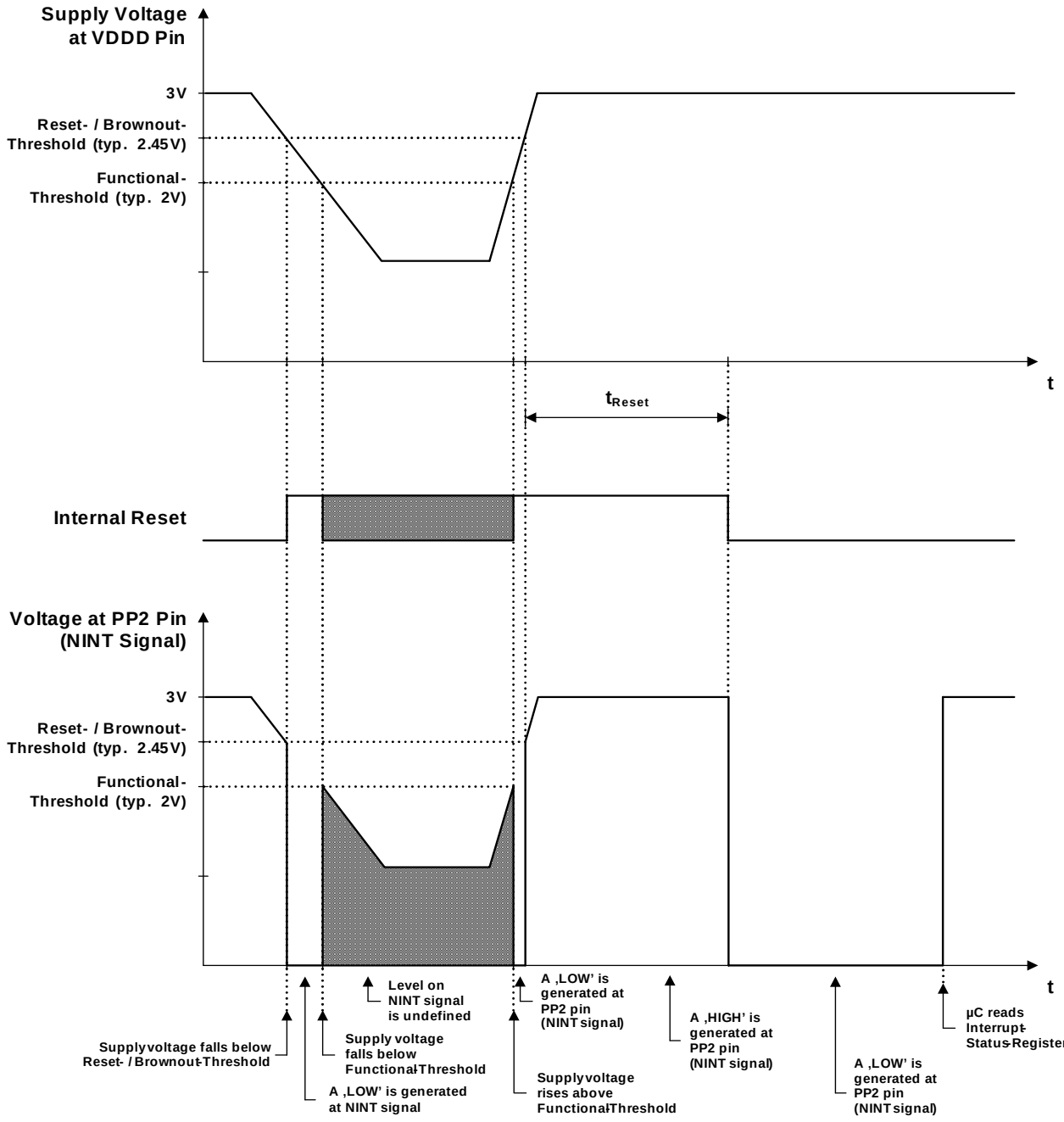


Figure 43 Reset Behavior

A second source that can trigger a reset is a brownout event. Whenever the integrated brownout detector measures a voltage drop below the brownout threshold on the digital

supply, the integrity of the stored data and configuration can no longer be guaranteed; thus a reset is generated. While the supply voltage stays between the brownout and the functional threshold of the chip, the NINT signal is forced to low. When the supply voltage drops below the functional threshold, the levels of all digital output pins are undefined.

When the supply voltage raises above the brownout threshold, the IC generates a high pulse at NINT and remains in the reset state for the duration of the reset time. When the IC leaves the reset state, the Interrupt Status registers (IS0 and IS1) are set to 0xFF and the NINT signal is forced to low. Now, the IC starts operation in the SLEEP Mode, ready to receive commands via the SPI interface. The NINT signal will go high, when one of the Interrupt Status registers is read for the first time.

2.5 System Interface

In most applications, the TDA5240 receiver IC is attached to an external microcontroller. This so-called Application Controller executes a firmware which governs the TDA5240 by reading data from the receiver when data has been received on the RF channel and by configuring the receiver device. The TDA5240 features an easy to use System Interface, which is described in this chapter.

Transparent Mode

The TDA5240 supports two levels of integration. In the most elementary fashion, it provides a rather rudimentary interface by which the incoming RF signal is demodulated and the corresponding data is made available to the Application Controller. Optionally, a chip clock is generated by the TDA5240. Since the data signal is always directly the baseband representation of the RF signal, we call this mode the Transparent Mode. The usage of the Transparent Mode will be described in **Chapter 2.5.1.2**.

Packet Oriented Mode

Alternatively, the TDA5240 features the so-called Packet Oriented Mode which supports the autonomous reception of data telegrams. The Packet Oriented Mode provides a high-level System Interface which greatly simplifies the integration of the receiver in data-centric applications. In Packet Oriented Mode, the data interface is based on chunks of synchronous data which are received in packets. In the easiest way, the Application Controller only reacts on the synchronous data it receives. The receiver autonomously handles the line decoding and the deframing of these data, and supports the timed reception of packets. Data is buffered in a receive FIFO and can be read out via the data interface. Further, the receiver provides support for the identification of wake-up signals. Details on the usage of the Packet Oriented Mode of the receiver are given in **Chapter 2.5.1.2**.

2.5.1 Interfacing to the TDA5240

The TDA5240 is interfacing with an application by three logical interfaces, see **Figure 44**. The RF/IF interface handles the reception of RF signals and is responsible for the demodulation. Its physical implementation has been described in **Chapter 2.4.3** and **Chapter 2.4.8**, respectively. The other two logical interfaces establish the connection to the Application Controller. Note that due to the high level of integration of the receiver, these interfaces impose minor requirements on the Application Controller, which can be as simple as an 8-bit microcontroller operated at low clock rate. As will be shown later, the physical implementation of the data interface depends on whether the receiver is operated in Packet Oriented or in Transparent Mode.

For the sake of clarity, the communication between the TDA5240 and the Application Controller is split into **control flow** and **data flow**. This separation leads to an independent definition of the data interface and the control interface, respectively.

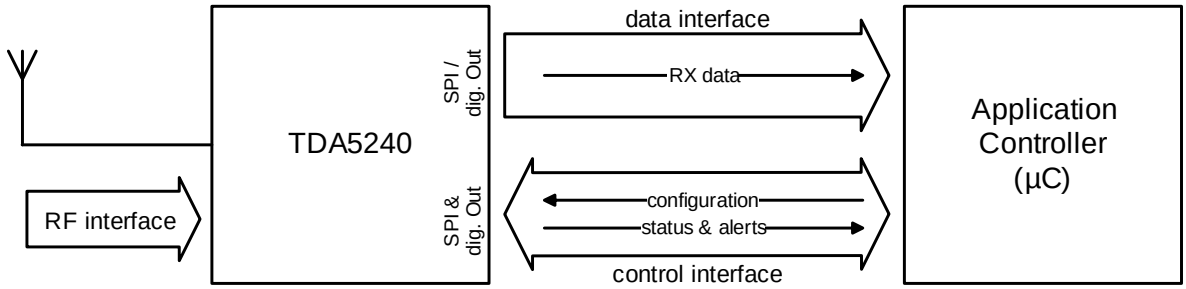


Figure 44 Logical and electrical System Interfaces of the TDA5240

2.5.1.1 Control Interface

The control interface is used in order to configure the TDA5240 after start-up or to re-configure it during run-time, as well as to properly react on changes in the status of the receiver in the Application Controller's firmware. The control interface offers a bi-directional communication link by which

- **configuration data** is sent from the Application Controller to the TDA5240,
- the receiver provides **status information** (e.g. the status of a data reception) as response to a request it has received from the Application Controller, and
- the TDA5240 autonomously **alerts** the Application Controller that a certain, configurable event has occurred (e.g. that a packet has been received successfully).

Configuration and status information are sent via the 4-wire SPI interface as described in **Chapter 2.5.5**. The configuration data determines the behavior of the receiver, which comprises

- scheduling the inactive power-saving phases as well as the active receive phases,
- selecting the properties of the RF/IF interface configuration (e.g. carrier frequency selection, filter settings),
- configuring the properties of the frames (e.g. wake-up patterns, Telegram Start Identifier (TSI), and optionally specifying the position, format and content of patterns within packets that stimulate a certain, configurable alerting behavior (Message ID)).

Note that the TDA5240 receiver IC supports reception of multiple configuration sets on multiple channels in a time-based manner without reconfiguration. Thus, the RF/IF interface as well as the frame format properties support alternative settings, which can be activated autonomously by the receiver as part of the scheduling process.

In contrast to the high-level interface used for communicating configuration instructions and status information, alerts are emitted by the receiver on a digital output pin that may trigger external interrupts in the Application Controller. Note that the alerting conditions as well as the polarity of the output pin are configurable, see **Chapter 2.5.4**.

2.5.1.2 Data Interface

The data interface between the Application Controller and the TDA5240 receiver IC is used for the transport of the received data, see **Figure 44**. The physical implementation as well as the features of the data interface depend on the selected mode of operation.

There are 5 possible receive modes:

- Packet Oriented FIFO Mode (POF)
- Packet Oriented Transparent Payload Mode (POTP)
- Transparent Mode - Chip Data and Strobe (TMCDS)
- Transparent Mode - Matched Filter (TMMF)
- Transparent Mode - Raw Data Slicer (TMRDS)

Access points for these receive modes can be seen in **Figure 15**.

The possible combinations of receive modes and polling mode setup is noted in **Figure 45**.

Self Polling Mode / RX Mode - available signal	Const ON-OFF					Fast Fall Back (UFFB), Mixed, PWUS			
	WU on Level criterion		WU on data criterion			WU on Level criterion		WU on data criterion	
	RSSI	Signal Recognition	Sync	Random, Equal, Pattern		RSSI	Signal Recognition	Sync	Random, Equal, Pattern
POF - FIFO	√	√	√	√		√	√	√	√
POTP - RXD - RXSTR	√	√	√	√		√	√	√	√
TMCDS - CH_DATA - CH_STR	√	√	√	-		√	√	√	-
TMMF - DATA_MATCHFIL	√	-	-	-		-	-	-	-
TMRDS - DATA	√	-	-	-		-	-	-	-

Legend:

√ ... available

- ... not available

Figure 45 Receive Modes

Packet Oriented FIFO Mode (POF)

In Packet Oriented FIFO Mode, data is transferred via the 4-wire SPI bus. During receive operation, the incoming RF signal is demodulated in the RF/IF interface, the line decoding is performed and the data, of which wake-up frames, data frame headers and optional footers have been stripped off, is stored in the RX FIFO. Then, the received data can be read from the RX FIFO using the “read FIFO” command described in

Chapter 2.5.2 and Chapter 2.5.5. The data which is read from the RX FIFO is accompanied by information which contains the status of the respective receive operation. Note that the availability of received data packets is communicated via alerts in the control interface.

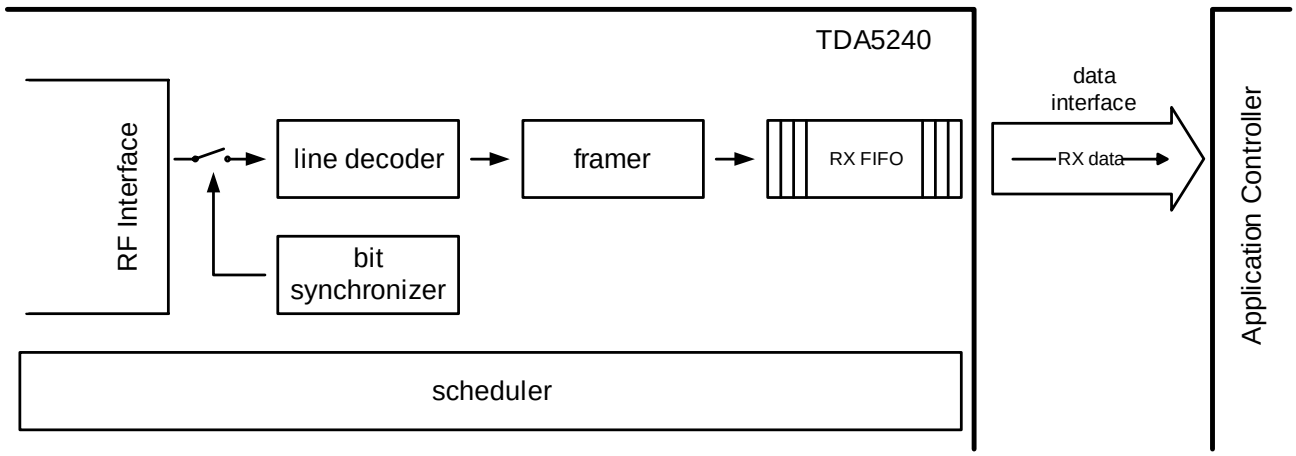


Figure 46 Data interface for the Packet Oriented FIFO Mode

Packet Oriented Transparent Payload Mode (POTP)

This mode is very similar to POF Mode as data which is going into FIFO is also available via RXD and RXSTR signals (see Chapter 2.5.3 Digital Output Pins).

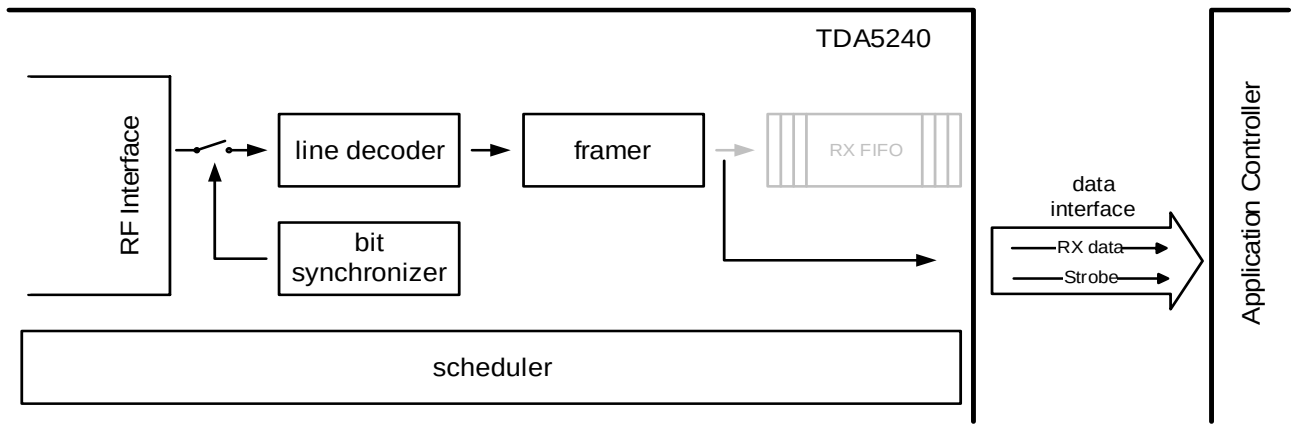


Figure 47 Data interface for the Packet Oriented Transparent Payload Mode

In the TDA5240, there are specific digital output lines (PPx pin) for the Bi-phase decoded data and an appropriate Strobe signal. During inactivity of the receiver, the line is in default mode switched to low.

In default mode the Strobe signal is active high and has a delay of $T_{BIT}/16$ relative to the data bit and a duration of $T_{BIT}/2$. The polarity of the Strobe signal is programmable, this can be done via PPCFG2 register.

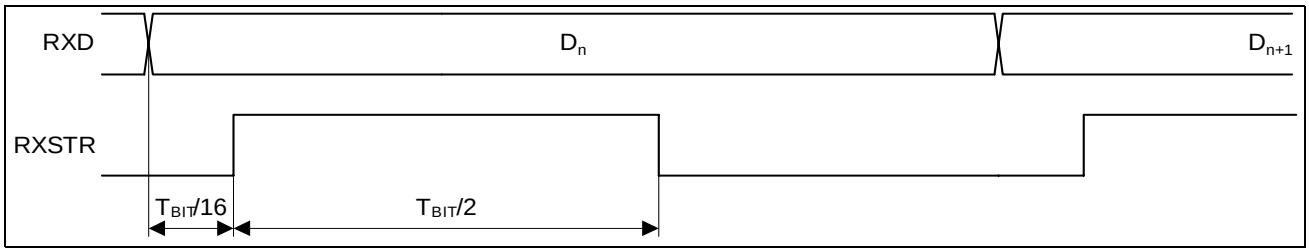


Figure 48 Timing of the Packet Oriented Transparent Payload Mode

Transparent Mode - Chip Data and Strobe (TMCDS)

The receiver's simple plain data interface in this Transparent Mode is shown in **Figure 49**. In this mode, the demodulated data signal is made directly available on the data output pin of the data interface. Concurrently, an estimate of the chip clock is optionally provided on the respective clock output line. Note that a sensible chip clock can only be generated if the selected line encoding exhibits a constant chip rate. The chip clock generation can be significantly improved by using a run-in signal of alternating one-zero chips (maximum number of transitions within a data stream).

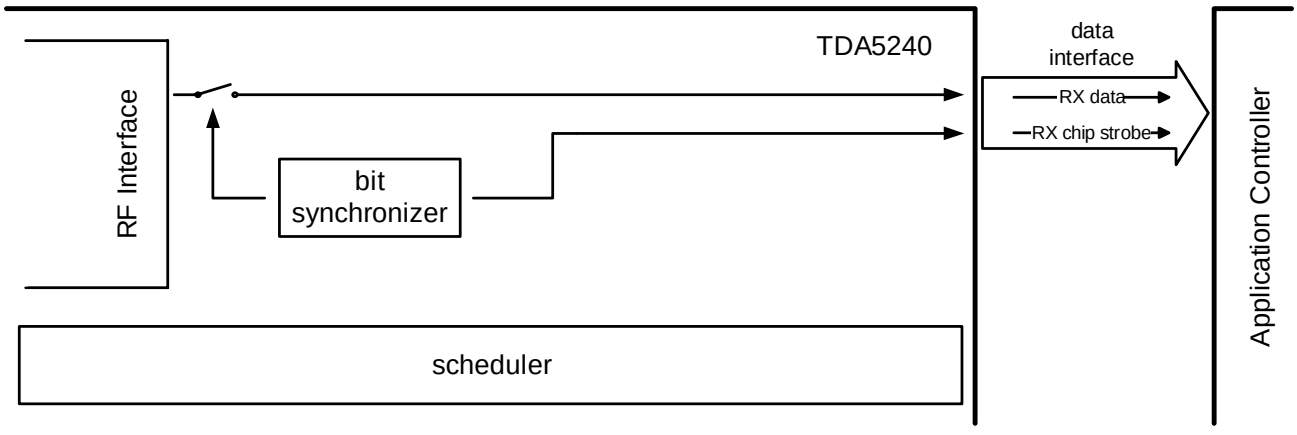


Figure 49 Data interface for the Transparent Mode - Chip Data and Strobe

In the TDA5240, there is a specific digital output line for the chip clock estimate as well as for the data output line, which delivers the encoded chip data. During inactivity of the receiver, the line is in default mode switched to low.

The PPx pin provides the estimated chip clock, if CH_STR is selected. Further details are given in **Chapter 2.5.3**.

In default mode the CH_STR signal is active high and has a delay of $T_{CHIP}/8$ relative to the data chip and a duration of $T_{CHIP}/2$. The polarity of the CH_STR signal is programmable, this can be done via PPCFG2 register.

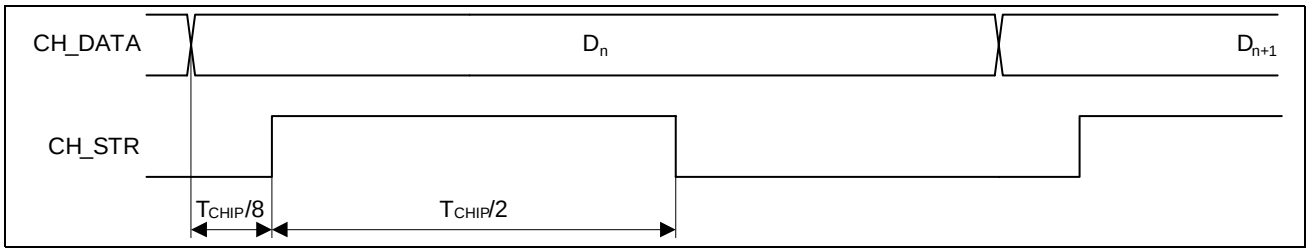


Figure 50 Timing of the Transparent Mode - Chip Data and Strobe

Transparent Mode - Matched Filter (TMMF)

The received data after the Matched Filter (Two-Chip Matched Filter) with an additional SIGN function is provided via the DATA_MATCHFIL signal (PPx pin). In this mode sensitivity measurements with ideal data clock can be performed very simple. For further details see the block diagram in **Figure 15**.

Sensitivity in this transparent mode is significantly depending on the implemented clock and data recovery algorithm of the user software in the application controller.

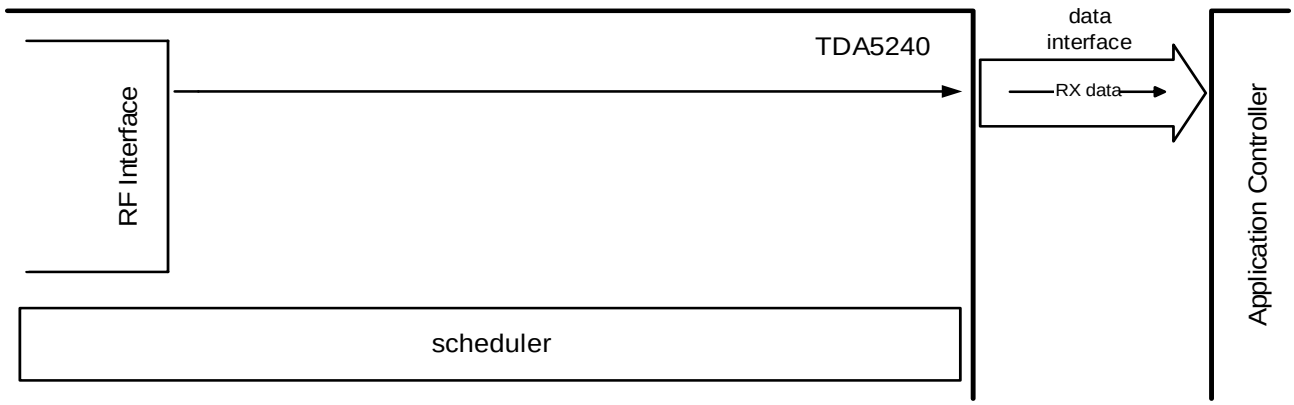


Figure 51 Data interface for the Transparent Modes TMMF / TMRDS

Transparent Mode - Raw Data Slicer (TMRDS)

This mode supports processing of data even without bi-phase encoding (e.g. NRZ coding) by providing the received data via the One-Chip Matched Filter on the DATA signal (PPx pin). See more details in the block diagram in **Figure 15**.

Sensitivity in this transparent mode is significantly depending on the implemented clock and data recovery algorithm of the user software in the application controller.

The data interface can be seen from **Figure 51**.

Self Polling capabilities are possible as well, but only Constant On-Off Mode and Wake-up on RSSI makes sense. Assume one of the TDA5240 configurations (e.g. Configuration B) is set for external data processing mode. See also example in **Figure 52**. The needed On time (latency through TDA5240) is configured in the corresponding On time registers of the chip. The interrupt for Wake-Up Config B (WUB) is enabled and suitable RSSI thresholds are set.

If the RSSI signal is in a valid threshold area, the TDA5240 changes to Run Mode Self Polling and an interrupt can be signaled to the Application Controller.

In case the RSSI signal is outside the valid threshold area, the chip stays in Self Polling Mode and the external controller gets no interrupt (as the desired RSSI level is not reached).

It should be mentioned that all Timeout Timers (TOTIMs) should be disabled in the configuration set of the external processing mode as the microcontroller takes over the control (see SFR bit group EXTPROC in the x_CHCFG register).

It is recommended to put this external configuration at the end of the On time within the polling cycle (so right before the Off time). This is helpful when using the "EXTTOTIM" command (goto Self Polling Mode, next programmed channel or Configuration A; see **Figure 77**). When the external configuration is the last configuration before the Off time, then the next programmed channel within the polling cycle would be the sequence of the Off time.

When data is available and the RSSI is within a valid threshold area, an interrupt is generated (NINT). So the Application Controller can process the data and decide about valid data.

In case the controller decides that wrong data was sent, the microcontroller can send the register command "EXTTOTIM" (see **Figure 77** and EXTPCMD register).

When the microcontroller detects valid data, then the controller can send the register command "EXTEOM found" (see **Figure 77** and EXTPCMD register) after completing the data reception.

The functionality described above can also be used for other receive modes (mainly TMMF, TMCDS), where the external microcontroller takes on responsibility for further data processing.

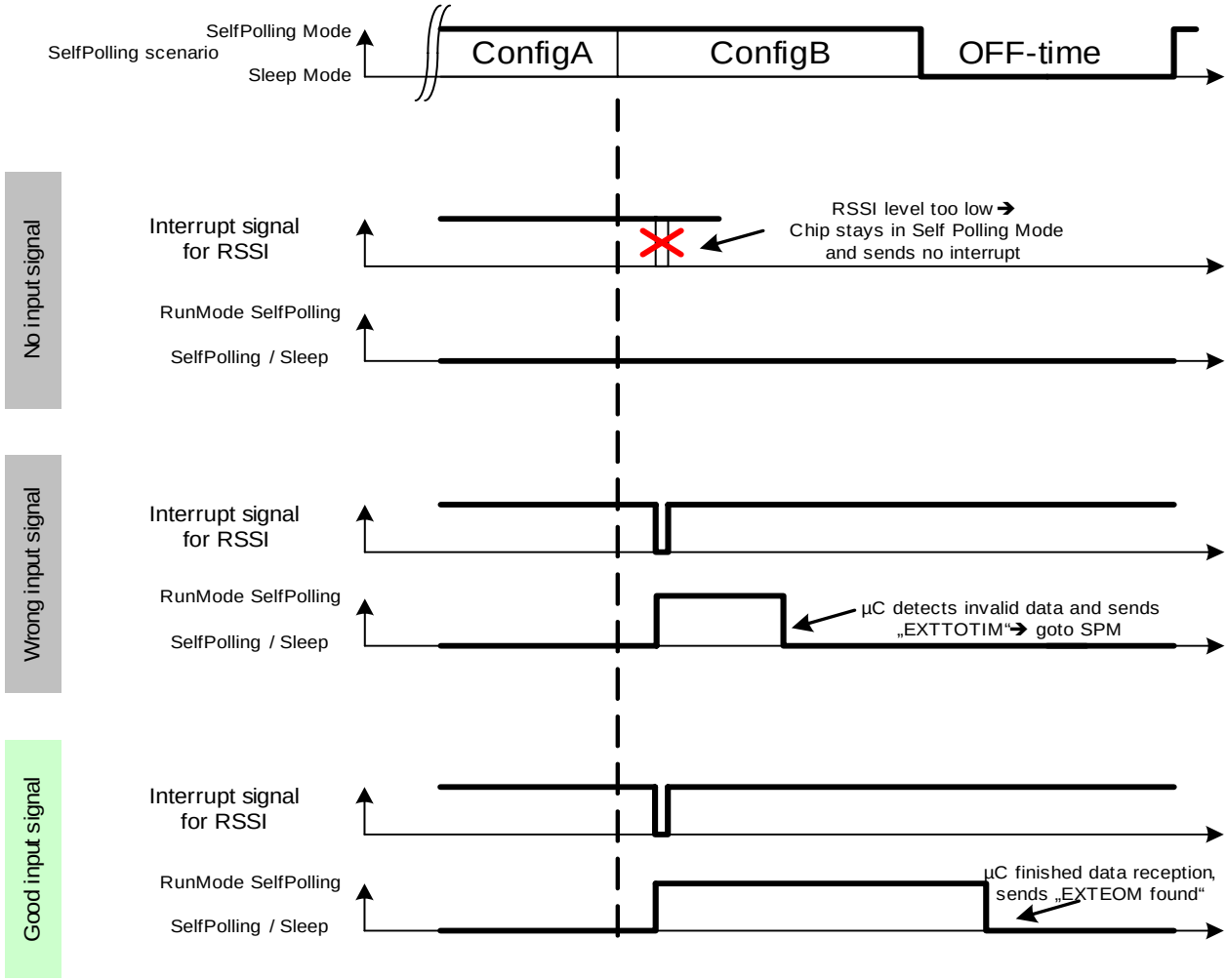


Figure 52 External Data Processing

The SFR bit group EXTPROC in the x_CHCFG register can be activated for each configuration set for an easier handling of external data processing by the Application Controller. Depending on the intended transparent receive mode an activation of this function means:

- Data path in front of Framer Unit is no longer closed (so that no data is going into Framer Unit accidentally)
- Interrupts for FSync, MID and EOM are deactivated internally
- Some/all TOTIM counters are deactivated
- Some/all Wake-up on Data Criteria are disabled
- Wake-up on Signal Recognition is/is not disabled

2.5.2 Receive FIFO

The Receive FIFO is the storage of the received data frames and is only used in the POF Mode. It is written during data reception. The host microcontroller is able to start reading via SPI right after frame sync (interrupt) or in the most common case right after detection of EOM (interrupt). The FIFO can store up to 256 received data bits. If the expected data transmission contains more bits (note that in TSI 8-bit Extended Mode one bit is added in front of the real payload to indicate which of the two TSI pattern has matched), reading from FIFO must start a certain time after frame sync to prevent an overrun.

Architecture

The 256-bit receive FIFO is based on a bit-addressable 2-port memory architecture.

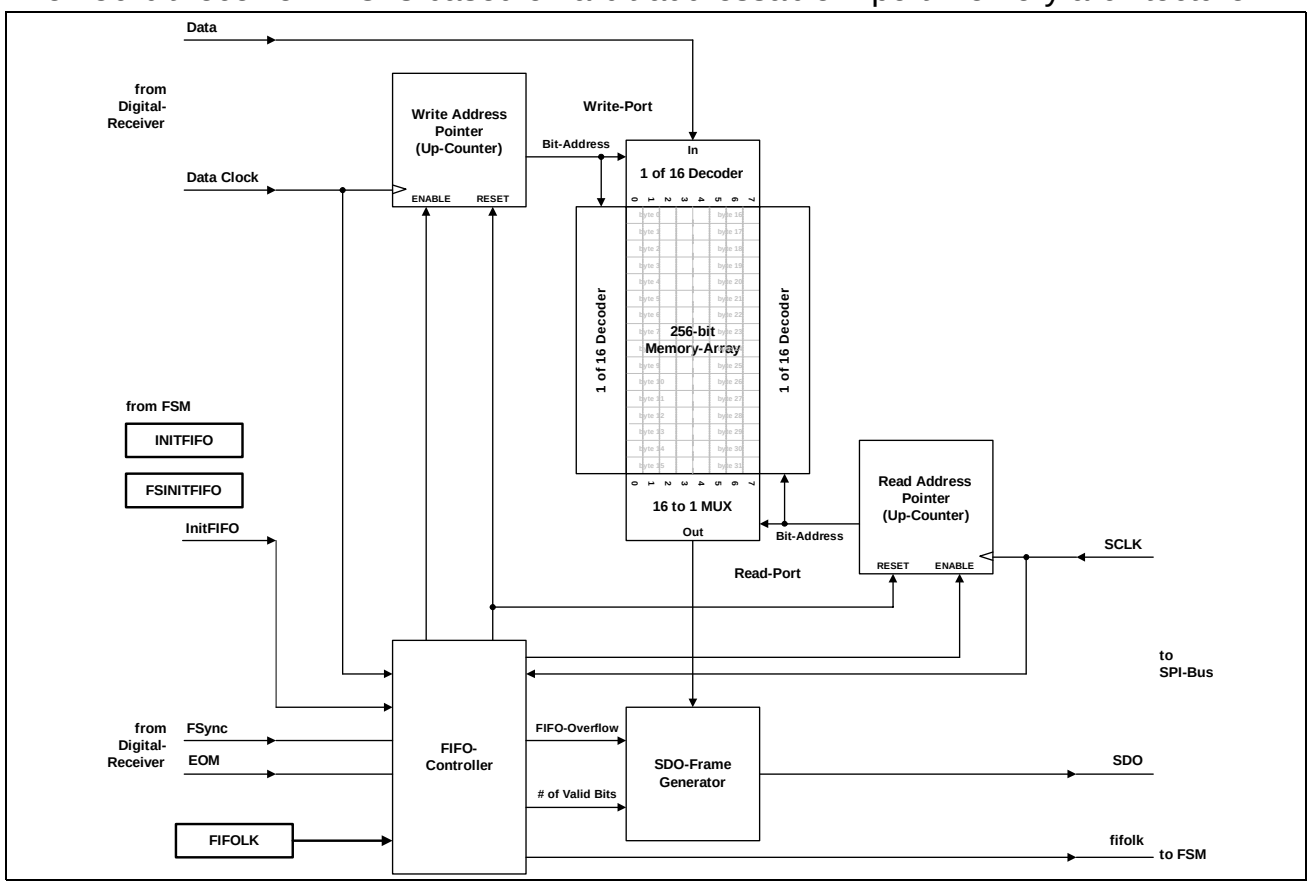


Figure 53 Receive FIFO

The write port is controlled by the Digital Receiver using the Write Address Pointer. Writing data into the FIFO starts with the detection of a TSI. The Write Address Pointer is incremented with each data clock signal generated by the Digital Receiver. The read port is controlled by the SPI controller using the Read Address Pointer. Each bit read from the SPI controller increments the Read Address Pointer. The Read and Write Address Pointers jump from their maximum value (255_d) to address zero. Writing to the FIFO stops at EOM or after Sync loss.

FIFO Lock Behavior

The FIFO possesses a lock mechanism that is enabled via the SFR control bit FIFOLK in the CMC1 register. If this mechanism is enabled, the FIFO will enter a FIFO Lock state at the detection of the EOM criterion. During the time that the FIFO is locked, it is not possible to receive additional data in Run Mode Self Polling. This means that it is only possible to detect another wake-up in the Self Polling Mode, but no more data in the Run Mode Self Polling. This will guarantee that only the first complete data packet is stored in the FIFO. Enabling FIFOLK also locks the digital receive chain at EOM until release from FIFO lock state.

The FIFO will remain locked unless one of three conditions occurs:

1.) The remaining contents of the FIFO are completely read out via the SPI

2.) The SFR control bit FIFOLK is cleared

3.) INITFIFO at Cycle Start is set in the CMC1 register and

a) FSM is switched to Run Mode Slave or

b) FSM switches from Self Polling Mode to Run Mode Self Polling

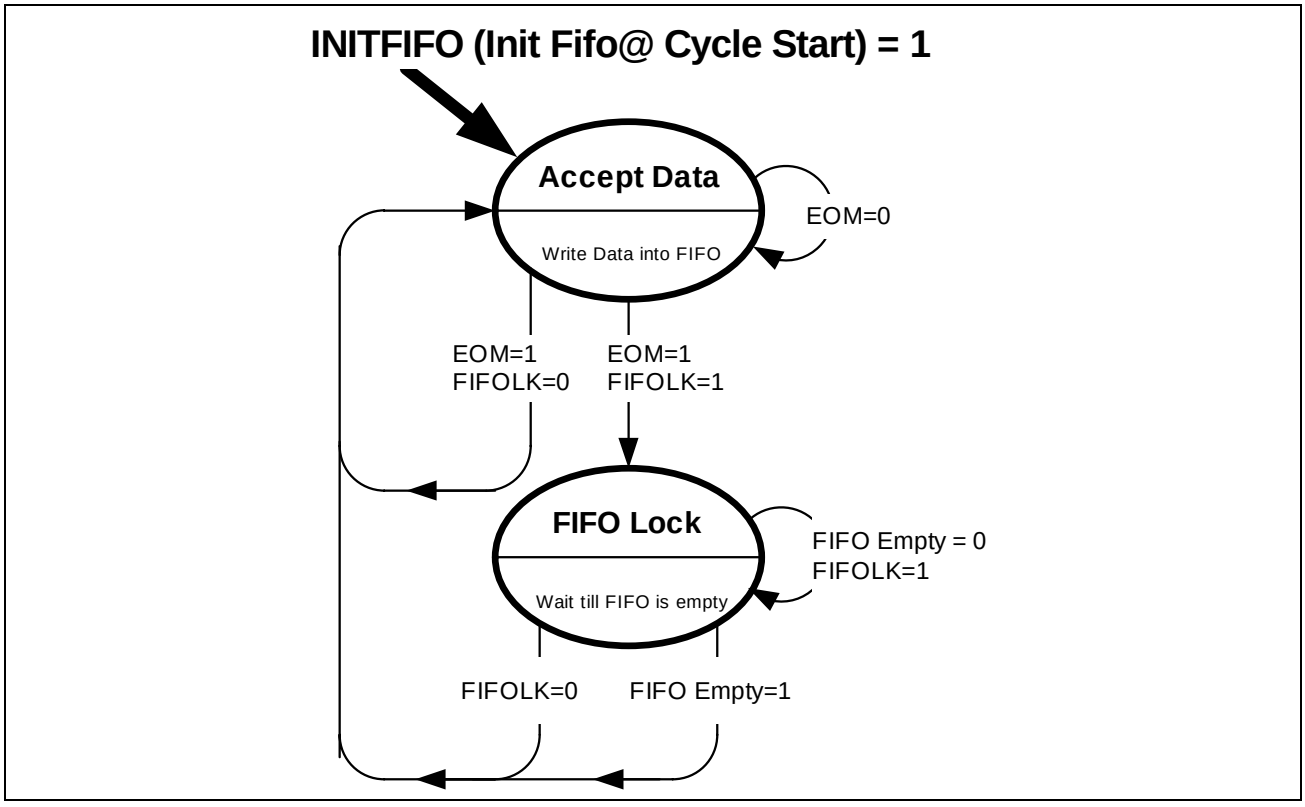


Figure 54 FIFO Lock Behavior

FIFO Status Word

The FIFO Status Word is attached at the end of a FIFO SPI transmission, and shows if there was an overflow, and how many valid data bits were transmitted. The number of valid FIFO bits is indicated at bit positions S0 to S5. S6 of the Status Word is always undefined.

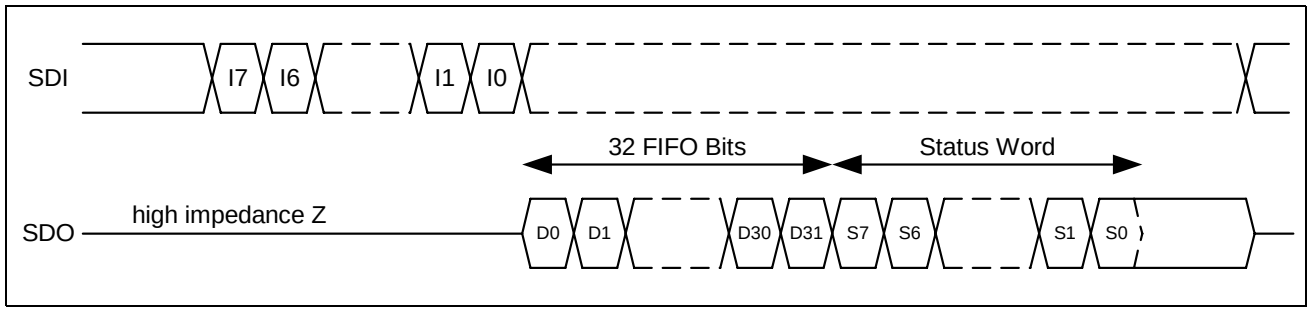


Figure 55 SPI Data FIFO Read

If the Write Address Pointer outruns the Read Address Pointer, an overflow is indicated in the FIFO Overflow Status bit in the FIFO Read Status Word at position S7. All 32 FIFO bits and the bits S5 to S0 of the Status Word are undefined while the Overflow Status bit is set.

If a TSI is detected after an overflow, the FIFO Overflow Status bit is cleared and the entire receive FIFO is initialized.

Initialization

Additionally, there are two possibilities to initialize the receive FIFO.

- If the INITFIFO bit is set in the CMC1 register (“Init FIFO at Cycle Start”) the entire receive FIFO is always initialized

  a.) after switching to Run Mode Slave or

  b.) switching from Self Polling Mode to Run Mode Self Polling.
- If the FSINITFIFO bit in CMC1 register is set, the entire receive FIFO is initialized when a TSI is detected and the receive FIFO is not locked (“Init FIFO at Frame Start”).

Last received message length

For application protocols with several payload frames and only a short pause in-between, the microcontroller would have to read out the FIFO very fast after detection of an EOM. Thus even slow or overloaded Application Controllers have the possibility now to determine the end of the last message, when reading out the FIFO, while the next payload frame gets already received and payload data is further stored in the FIFO.

Therefore the last received message length (e.g. after an EOM event) is stored in register PLDLEN and the upper two bits of register RFPLLACC at TSI detection of the next message. The upper two bits of register RFPLLACC hold the MSBs, thus a message length of 256 up to 1023 payload bits can be depicted. A saturation of the message length at the maximum value of 1023 is realized. Storage at TSI of the next message ensures that even wrong payload data (e.g. if MID is not matching, no EOM will be generated, but payload is kept in FIFO. Or EOM data length criterion is selected only and a sync loss prevents from generating an EOM event) can be identified.

On initialization of the FIFO, the register PLDLEN and the upper two bits of register RFPLLACC are cleared. The corresponding internal counter is cleared with every TSI detection and initialization of the FIFO.

PLDLEN will work correctly in case:

(INITDRXES = 0) AND ((Data rate > 22kBit/s) OR (EOM2SPM = 0))

If the condition above is not fulfilled, then the chip internal state machine can set PLDLEN to 0 and a correct function of PLDLEN cannot be guaranteed.

2.5.3 Digital Output Pins

As long as the P_ON pin is high, all digital output pins operate as described. If the P_ON pin is low, all digital output pins are switched to high impedance mode.

The digital outputs PP0, PP1, PP2 and PP3 are configurable, where each of the signals CLK_OUT, RX_RUN, NINT, a LOW level (GND) and a HIGH level, DATA, DATA_MATCHFIL, CH_DATA, CH_STR, RXD and RXSTR can be routed to any of the four output pins. There is only one exception, CLK_OUT is not available on PP3. The default configuration for these four output pins can be seen in **Table 1**.

Each port pin can be inverted by usage of PPCFG2 register.

The RX_RUN signal is active high for all Configurations by default. It can be deactivated for every Configuration separately. Every PPx can be configured with an individual RX_RUN setup. This can be set in RXRUNCFG0 and RXRUNCFG1 registers.

Interfacing to 3.3V Logic:

The TDA5240 is able to interface directly to a 3.3V logic, when chip is operated in 3.3V environment.

Interfacing to 5V Logic:

The TDA5240 is able to interface directly to a 5V logic, when chip is operated in 5V environment.

EMC Reduction of Digital I/Os:

Because electromagnetic distortion generated by digital I/Os may interfere with the high sensitivity radio receiver, it is recommended that all inputs are filtered by adding an RC low pass circuit.

2.5.4 Interrupt Generation Unit

The TDA5240 is able to signal interrupts (NINT signal) to the external Application Controller on one of the PPx port pins (for further details see **Chapter 2.5.3 Digital Output Pins**). The Interrupt Generation Unit receives all possible interrupts and sets the NINT signal based on the configuration of the Interrupt Mask registers (IM0 and IM1). The Interrupt Status registers (IS0 and IS1) are set from the Interrupt Generation Unit, depending on which interrupt occurred. The polarity of the interrupt can be changed in the PPCFG2 register. Please note that during power up and brownout reset, the polarity of NINT signal is always as described in **Chapter 2.4.9.2 Chip Reset**.

A Reset event has the highest priority. It sets all bits in the Status registers to “1” and sets the interrupt signal to “0”. The first interrupt after the Reset event will clear the Status registers and will set the interrupt signal to “1”, even if this interrupt is masked.

A Wake-up interrupt clears the FsyncA, FsyncB, FsyncC, FsyncD and the complementary Wake-up flag. An Fsync interrupt clears the EOMA, EOMB, EOMC, EOMD, MIDA, MIDB, MIDC, MIDD and the complementary Fsync flags.

The Interrupt Status register is always cleared after read out via SPI.

It is not possible to disable the Power On Reset Indicator Interrupt using the Interrupt Mask registers.

Some interrupts are not usable depending on the selected receive mode, which is described in **Chapter 2.5.1.2 Data Interface**.

Interrupts for WU can be used in all receive modes.

Interrupts for FSync, MID and EOM can only be used in the receive modes POTP and POF.

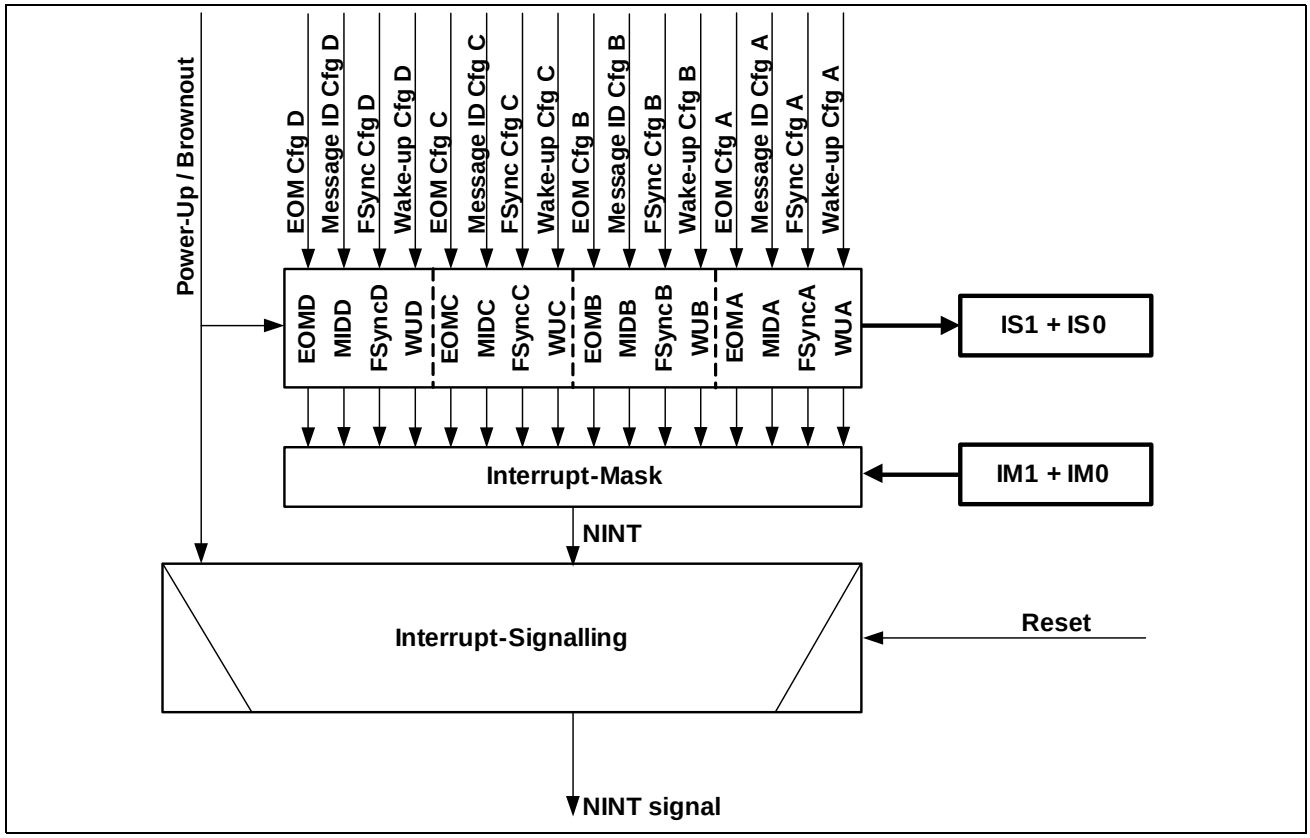


Figure 56 Interrupt Generation Unit

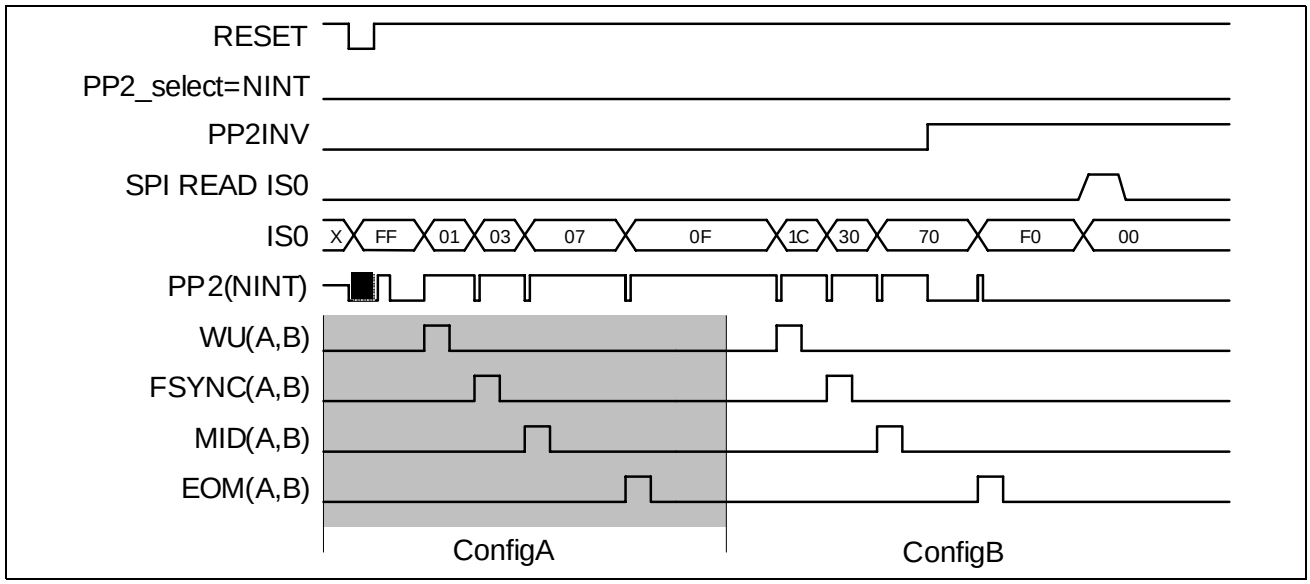


Figure 57 Interrupt Generation Waveform (Example for Configuration A+B)

The following handling mechanism for read-clear registers was chosen due to implementation of the Burst Read command:

- the current Interrupt Status (ISx) register 8-bit content is **latched** into the SPI shift register after the last address bit is clocked-in (**point A** in **Figure 58**)
- the IS register is then **cleared** after last IS register bit is clocked out of the SPI interface (**point B** in **Figure 58**)

Consequence: any interrupt event occurring in the window-time between points A and B is cleared at point B and not stored/shown in an later readout of ISx.

(However: NINT signal is toggling in any case, if occurring interrupt is not masked in IMx register)

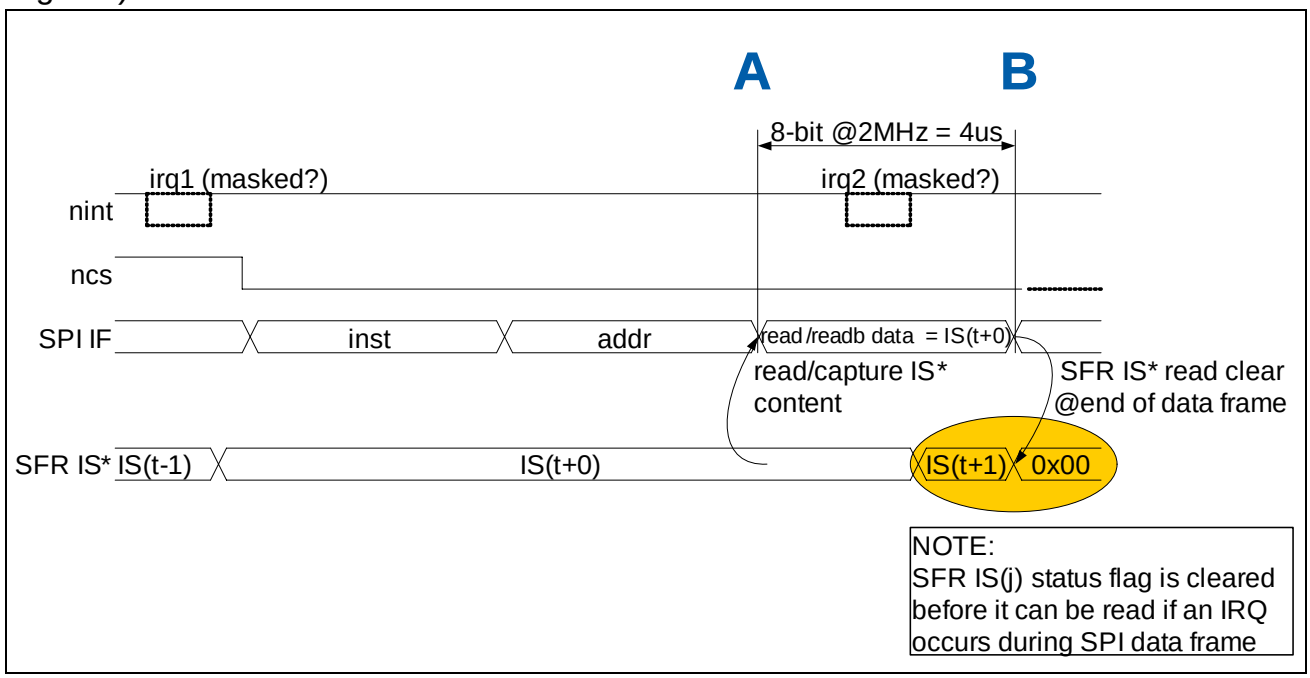


Figure 58 ISx Readout Set Clear Collision

Please see also the **IMPORTANT NOTE** in the Burst Read section !

2.5.5 Digital Control (4-wire SPI Bus)

The control interface used for device control and data transmission is a 4-wire SPI interface.

- *NCS* - select input, active low
- *SDI* - data input
- *SDO* - data output
- SCK - clock input: Data bits on *SDI* are read in at rising *SCK* edges and written out on *SDO* at falling *SCK* edges.

Level definition:
logic 0 = low voltage level
logic 1 = high voltage level

Note for non-Burst modes: It is possible to send multiple frames while the device is selected. It is also possible to change the access mode while the device is selected by sending a different instruction.

Note: In all bus transfers MSB is sent first, except for the received data read from the FIFO. There the bit order is given as first bit received is first bit transferred via the bus.

To **read from the device**, the SPI master has to select the SPI slave unit first. Therefore, the master must set the *NCS* line to low. After this, the instruction byte and the address byte are shifted in on *SDI* and stored in the internal instruction and address register. The data byte at this address is then shifted out on *SDO*. After completing the read operation, the master sets the *NCS* line to high.

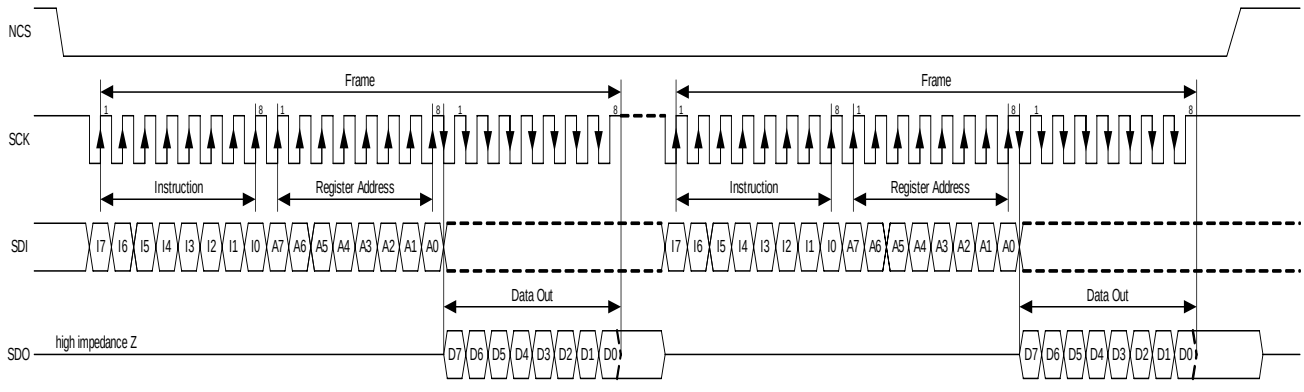


Figure 59 Read Register

To **read from the device in Burst mode**, the SPI master has to select the SPI slave unit first. Therefore the master has to drive the NCS line to low. After the instruction byte and the start address byte have been transferred to the SPI slave (MSB first), the slave unit will respond by transferring the register contents beginning from the given start address (MSB first). Driving the NCS line to high will end the Burst frame.

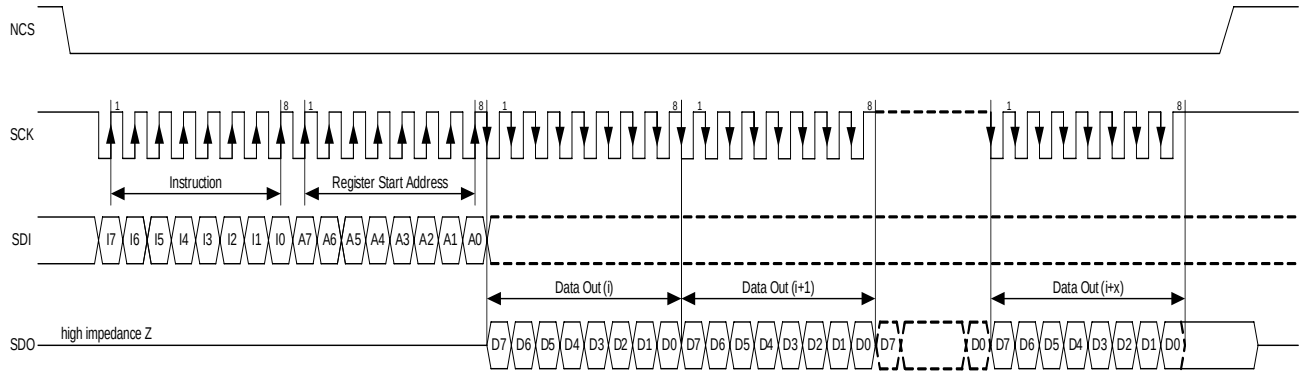


Figure 60 Burst Read Registers

IMPORTANT NOTE - for being upwards compatible with further versions of the product, we give following strong recommendation:

For read-clear registers at address (N), no read-burst access stopping at address (N-1) is allowed, because read-clear register will be cleared without being read out. Use single read command to read out the register at address (N-1) or extend the burst read to include the read-clear register at address (N).

To **write to the device,** the SPI master has to select the SPI slave unit first. Therefore, the master must set the *NCS* line to low. After this, the instruction byte and the address byte are shifted in on *SDI* and stored in the internal instruction and address register. The following data byte is then stored at this address.
After completing the writing operation, the master sets the *NCS* line to high.

Additionally the received address byte is stored into the register *SPIAT* and the received data byte is stored into the register *SPIDT*. These two **trace registers** are readable.

Therefore, an external controller is able to check the correct address and data transmission by reading out these two registers after each write instruction. The trace registers are updated at every write instruction, so only the last transmission can be checked by a read out of these two registers.

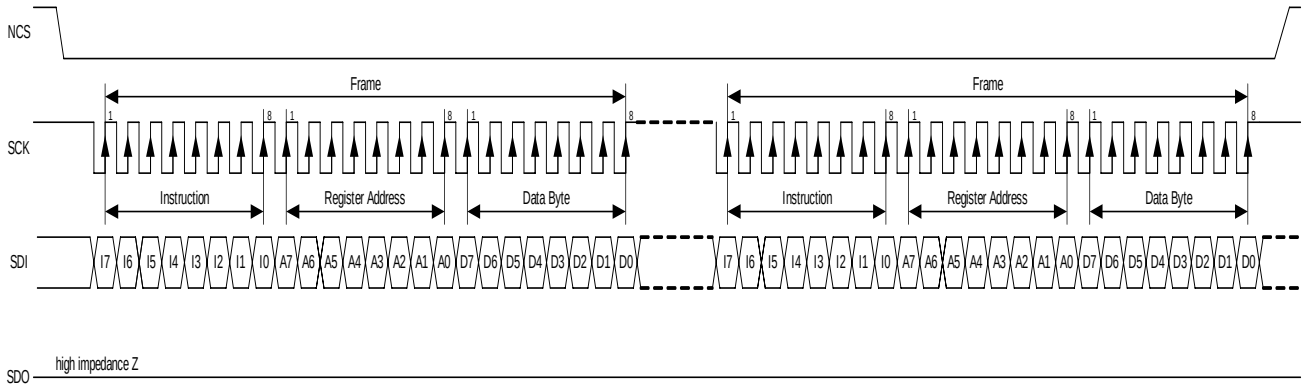


Figure 61 Write Register

To **write to the device in Burst mode**, the SPI master has to select the SPI slave unit first. Therefore the master has to drive the NCS line to low. After the instruction byte and the start address byte have been transferred to the SPI slave (MSB first) the successive data bytes will be stored into the automatically addressed registers.

To verify the SPI Burst Write transfer, the current address (start address, start address + 1, etc.) is stored in register SPIAT and the current data field of the frame is stored in register SPIDT. At the end of the Burst Write frame the latest address as well as the latest data field can be read out to verify the transfer. Note that some error in one of the intermediate data bytes can not be detected by reading SPIDT.

Driving the NCS line to high will end the Burst frame.

A single SPI Burst Write command can be applied very efficiently for data transfer either within a register block of configuration dependent registers or within the block of configuration independent registers.

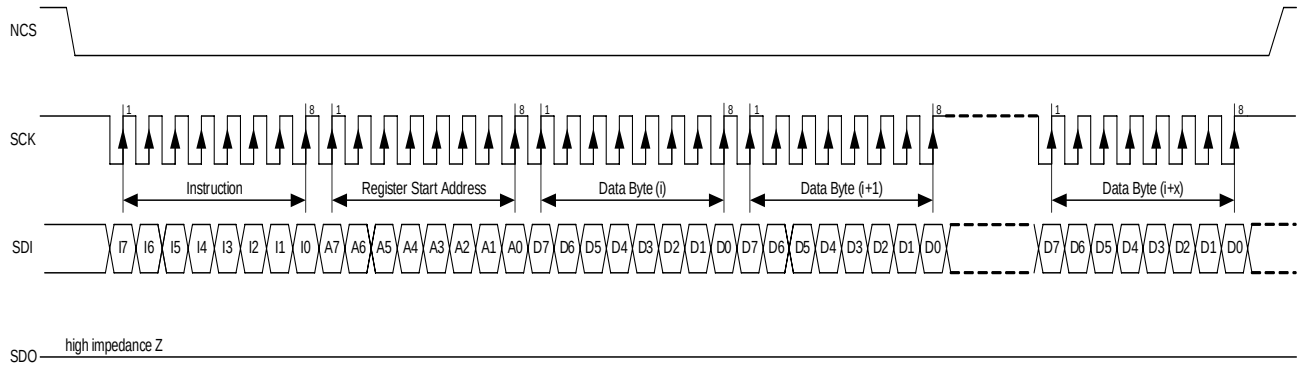


Figure 62 Burst Write Registers

The SPI also includes a safety feature by which the **checksum is calculated** with an XOR operation from the address and the data when writing SFR registers. The checksum is in fact an XOR of the data 8-bitwise after every 8 bits of the SPI write command. The calculated checksum value is automatically written in the SPICHKSUM register and can be compared with the expected value. After the SPICHKSUM register is read, its value is cleared.

In case of an SPI Burst Write frame, a checksum is calculated from the SPI start address and consecutive data fields.

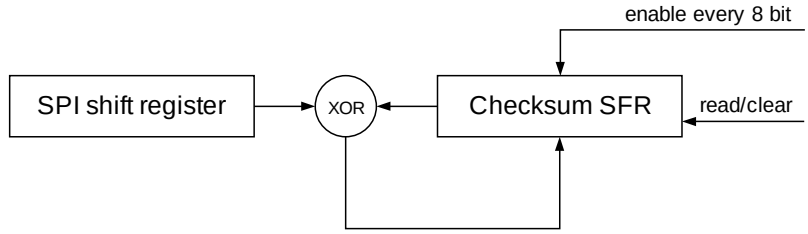


Figure 63 SPI Checksum Generation

To **read the FIFO,** the SPI master has to select the SPI slave unit first. Therefore, the master must set the *NCS* line to low. After this, the instruction byte is shifted in on *SDI* and stored in the internal instruction register. The data bits of the FIFO are then shifted out on *SDO*. The following byte is a status word that contains the number of valid bits in the data packet. After completing the read operation, the master sets the *NCS* line to high.

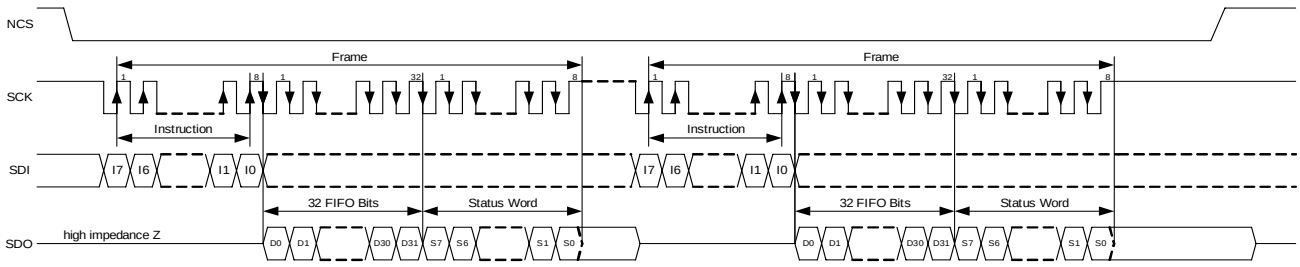


Figure 64 Read FIFO

Table 4 Instruction Set

Instruction	Description	Instruction Format
WR	Write to chip	0000 0010
RD	Read from chip	0000 0011
RDF	Read FIFO from chip	0000 0100
WRB	Write to chip in Burst mode	0000 0001
RDB	Read from chip in Burst mode	0000 0101

2.5.5.1 Timing Diagrams

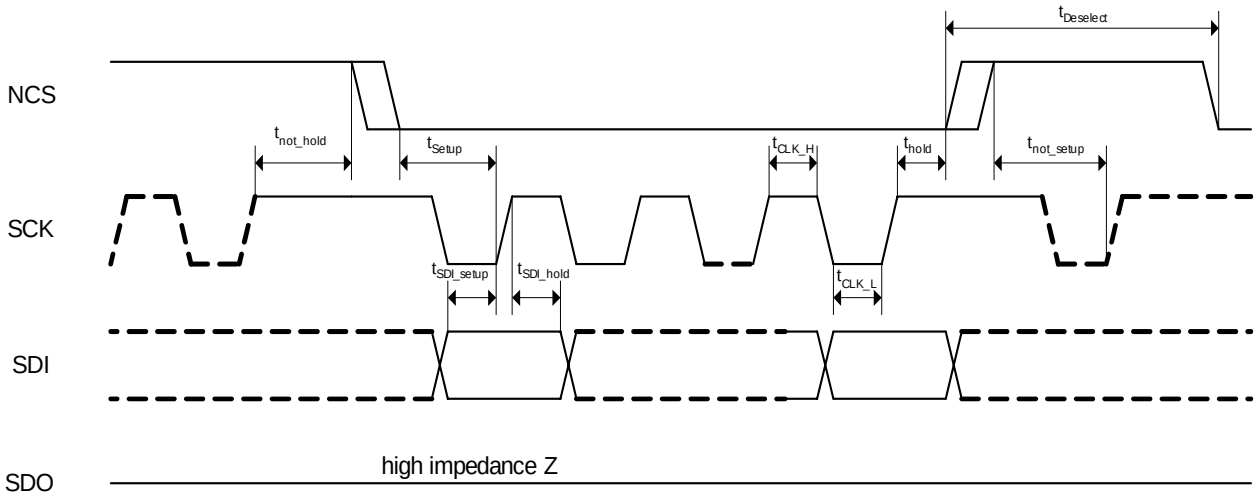


Figure 65 Serial Input Timing

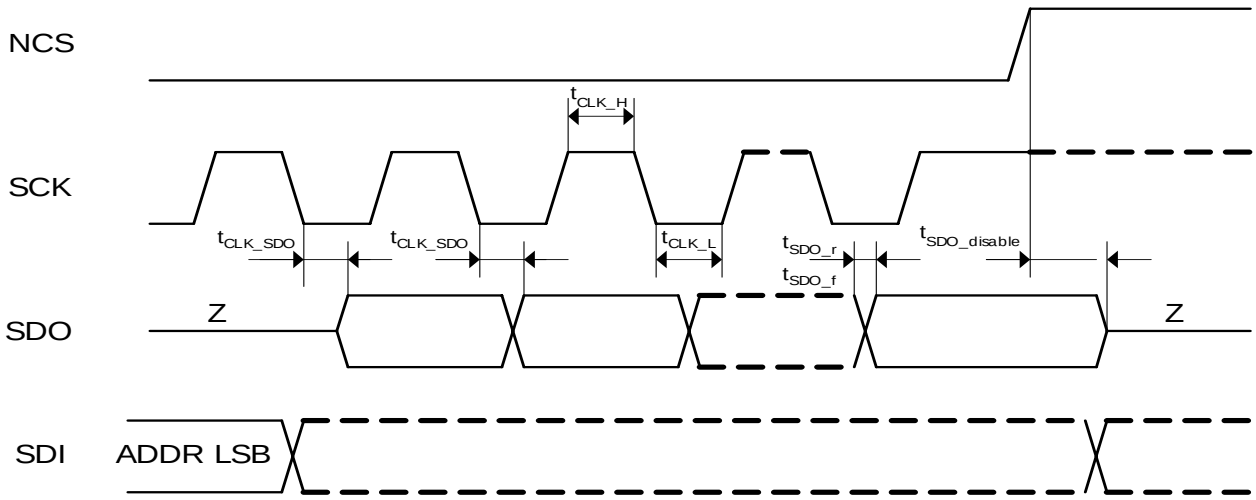


Figure 66 Serial Output Timing

Table 5 SPI Bus Timing Parameter

Symbol	Parameter
f_{clock}	Clock frequency
t_{CLK_H}	Clock High time
t_{CLK_L}	Clock Low time
t_{setup}	Active setup time
t_{not_setup}	Not active setup time
t_{hold}	Active hold time
t_{not_hold}	Not active hold time
$t_{Deselect}$	Deselect time
t_{SDI_setup}	SDI setup time
t_{SDI_hold}	SDI hold time
t_{CLK_SDO}	Clock low to SDO valid
t_{SDO_r}	SDO rise time
t_{SDO_f}	SDO fall time
$t_{SDO\_disable}$	SDO disable time

2.5.6 Chip Serial Number

Every device contains a unique, preprogrammed 32-bit wide serial number. This number can be read out from SN3, SN2, SN1 and SN0 registers via the SPI interface. The TDA5240 always has SN0.6 set to 1 and SN0.5 set to 1.

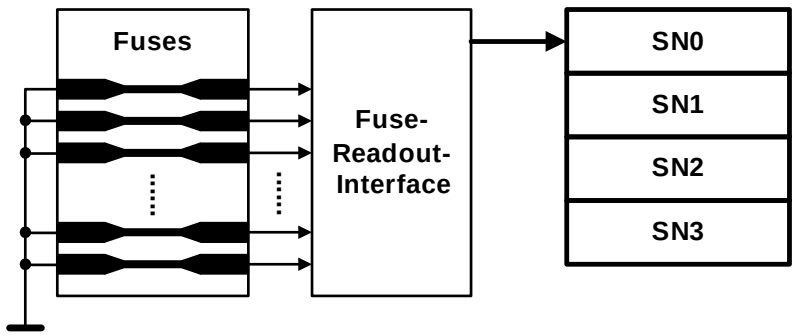


Figure 67 Chip Serial Number

2.6 System Management Unit (SMU)

The System Management Unit consists of two main units:

- **Master Control Unit**, where the various operating modes can be configured.
- **Polling Timer Unit**, where the receiver's On and Off times and modes are defined. The Polling Timer Unit is only working in the Self Polling Mode.

2.6.1 Master Control Unit (MCU)

2.6.1.1 Overview

The Master Control Unit controls the operation modes, the global states, and is generally responsible for automating data reception, verification, identification, extraction, and storage into the FIFO. The payload data without RUNIN, TSI and optional EOM can be read from the FIFO via SPI by the external microcontroller.

Alternatively, a transparent data stream can also be processed externally by the Application Controller (see **Chapter 2.5.1.2 Data Interface**).

The following operation modes and the behavior of the Master Control Unit are fully automatic and only influenced by SFR settings and by incoming RF data streams.

The TDA5240 has two major operation modes, which are switched by SFR bit MSEL.

In **Slave Mode** the device is controlled via SPI by the external microcontroller. This mode supports:

- **Run Mode Slave (RMS)**, where the receiver is continuously active
- **SLEEP Mode**, where the receiver is switched off for power saving. This mode can also be used to change register settings
- **HOLD Mode**, allows register settings to be changed. The change to HOLD Mode and back to RMS is faster than changing to SLEEP Mode and back to RMS.

In Slave Mode, switching between configurations and channels, as well as between Run and SLEEP Mode must be initiated by the microcontroller.

In **Self Polling Mode,** TDA5240 autonomously polls for incoming RF signals. The receiver switches automatically between up to four configurations (Configuration A, B, C and D) and up to 3 channels per configuration (Further information can be found in **Chapter 2.6.2**).

Between the RF signal scans, the receiver is automatically switched to Low Power Mode for reducing the average power consumption. If an incoming signal fulfills the selected wake-up criterion an interrupt can be generated and Run Mode Self Polling will be entered. If the following received data matches to the TSI pattern, and passes the optional message ID screening, the payload is loaded into the FIFO, and, if not masked, an interrupt is generated. Then the payload data can be read via SPI.

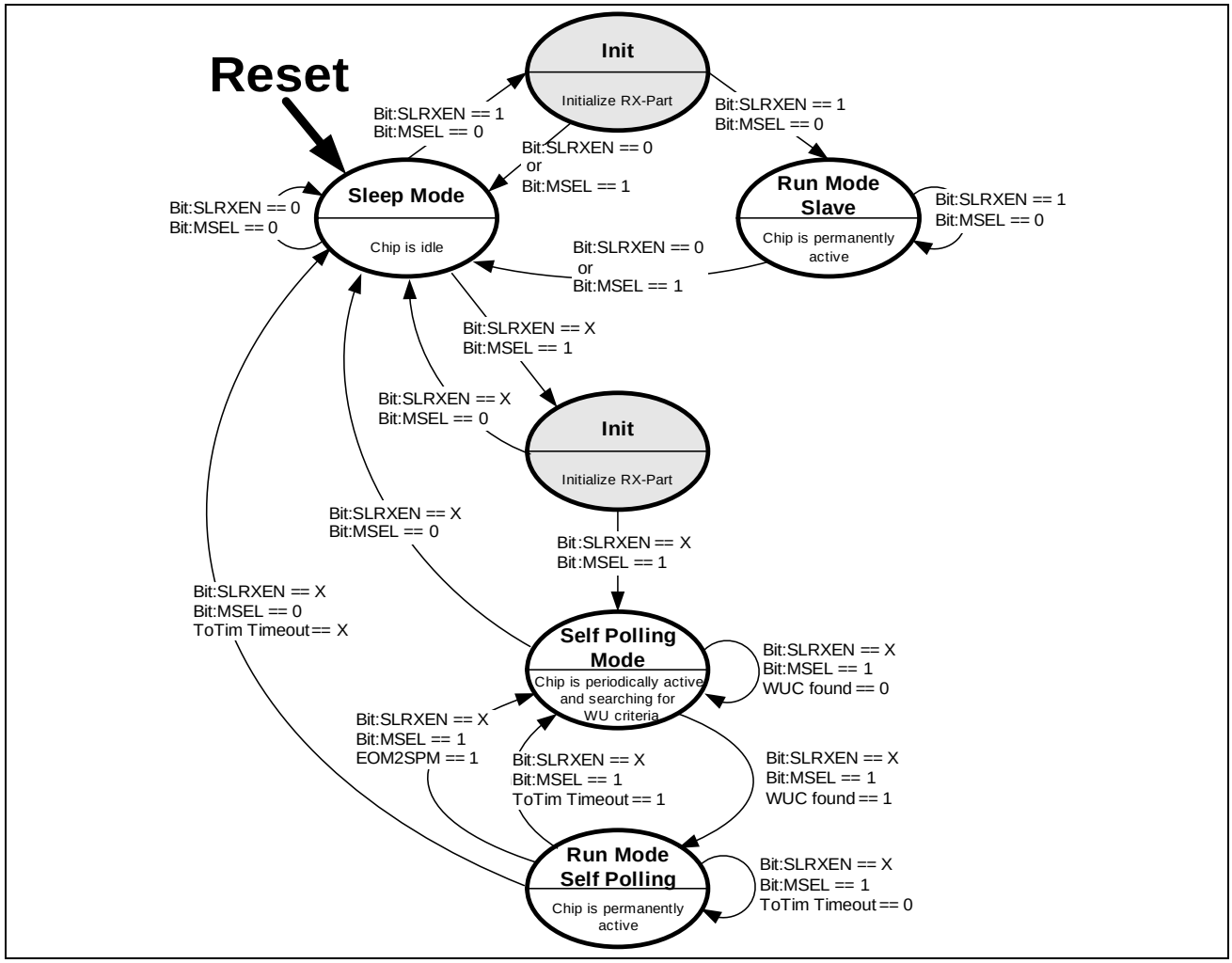


Figure 68 Global State Diagram

2.6.1.2 Run Mode Slave (RMS)

In Run Mode Slave, the receiver is able to continuously scan for incoming data streams. Detection and validation of a wake-up criterion are not performed, but RUNIN and TSI are required.

Recognition of TSI and validation of the optional MID (Message IDentification) are done automatically. The data payload is extracted from the data stream, and moved to the FIFO.

The various recognition steps are communicated by interrupts. Interrupts can be generated at frame-start (when a valid TSI has been detected), when a valid MID has been found and at EOM (End of Message).

Alternatively, a transparent data stream can also be processed externally by the Application Controller (see **Chapter 2.5.1.2 Data Interface**).

Run Mode Slave is entered by setting SFR CMC0 bits MSEL to 0 and SLRXEN to 1.

Configurations are switched via SFR bit group MCS in the CMC0 register. The RF channel in use can be selected in the x_CHCFG register, the frequency selection is defined by SFRs x_PLLINTCy, x_PLLFRAC0Cy, x_PLLFRAC1Cy, x_PLLFRAC2Cy, where x = A, B, C or D and y = 1, 2 or 3.

The configuration may be changed only in SLEEP or in HOLD Mode before returning to the previously selected operation mode. This is necessary to restart the state machine with defined settings at a defined state. Otherwise the state machine may hang up. Reconfigurations in HOLD Mode are faster, because there is no Start-Up sequence.

The following flowchart and explanation show and help to understand the internal behavior of the Finite State Machine (FSM) in Run Mode Slave.

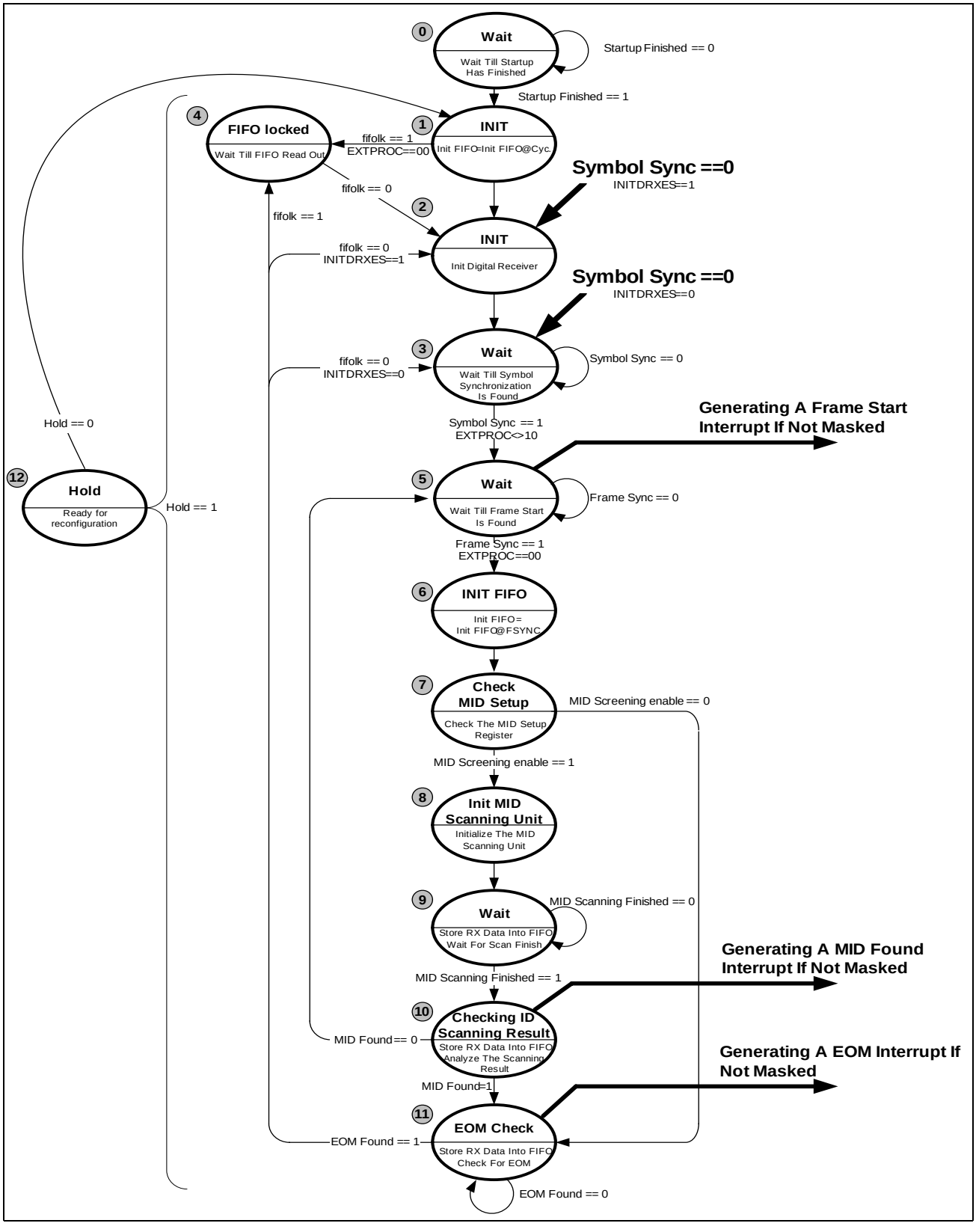


Figure 69 Run Mode Slave

2.6.1.3 HOLD Mode

This state (item 12 in **Figure 69**) is used for fast reconfiguration of the chip in Run Mode Slave. This state can be reached after the Start-Up Sequencer and Initialization of the chip have been completed from any state from 3 to 11. To reconfigure the chip the SFR control bit HOLD must be set. After reconfiguration in this state the SFR control bit HOLD must be cleared again. After leaving the HOLD state, the INIT state is entered and the receiver can work with the new settings. Be aware that the time between changing the configuration and reinitialization of the chip has to be at least 40us. Take note that one SPI command for clearing the SFR control bit HOLD needs 24 bits or 12µs at an SPI data rate of 2.0Mbit/s. The remaining 28µs must be guaranteed by the application.

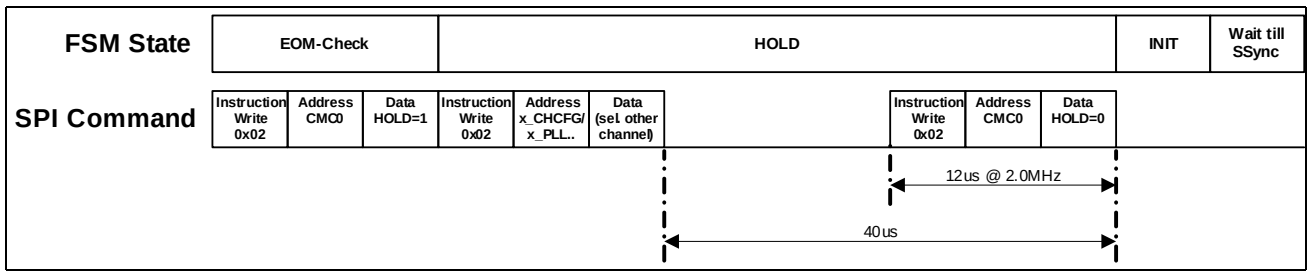


Figure 70 HOLD State Behavior (INITPLLHOLD disabled)

In case of large frequency steps, an additional VAC routine (VCO Automatic Calibration) has to be activated when recovering from HOLD Mode (INITPLLHOLD bit). The maximum allowed frequency step in HOLD Mode without activation of VAC routine is depending on the selected frequency band. The limits are +/- 1 MHz for the 315 MHz band, +/- 1.5 MHz for the 434 MHz band and +/- 3 MHz for the 868/915 MHz band.

When this additional VAC routine is enabled, the TDA5240 starts initialization of the Digital Receiver block after release from HOLD and an additional Channel Hop time.

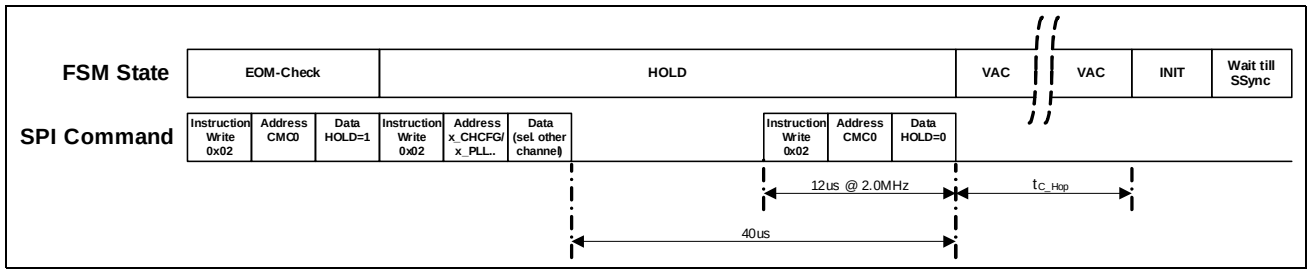


Figure 71 HOLD State Behavior (INITPLLHOLD enabled)

HOLD Mode is only available in Run Mode Slave. Configuration changes in Self Polling Mode have to be done by switching to SLEEP Mode and returning to Self Polling Mode after reconfiguration.

2.6.1.4 SLEEP Mode

The SLEEP Mode is a power save mode. The complete RF part is switched off and the oscillator is in Low Power Mode. As in HOLD Mode, the chip can be reconfigured. When switching from SLEEP to Run Mode Slave, the state machine starts with the internal Start-Up Sequence.

2.6.1.5 Self Polling Mode (SPM)

In Self Polling Mode TDA5240 autonomously polls for incoming RF wake-up data streams. There is no processing load on the host microcontroller. When a wake-up criterion has been found, an interrupt can be generated and the TDA5240 mode is changed to Run Mode Self Polling for automatic verification of TSI, optional MIDs and for transfer of payload data into the FIFO.

A general overview on a typically transmitted protocol and the behaviour of the TDA5240 is given in **Figure 72**.

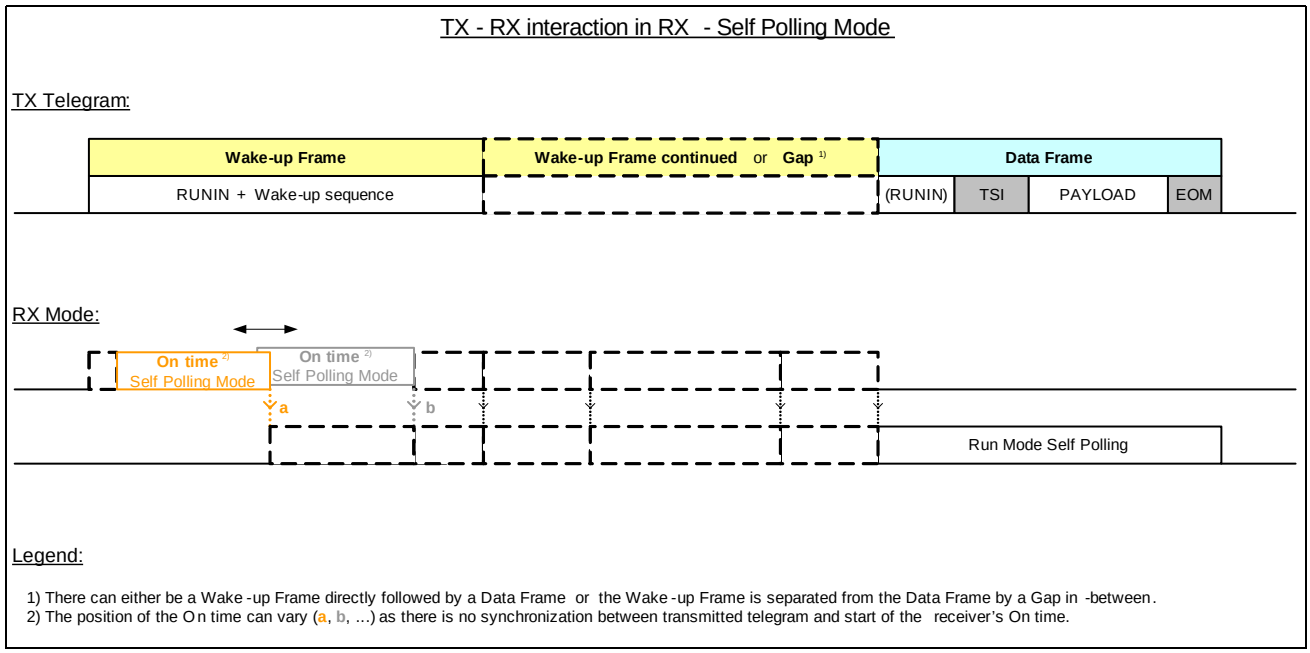


Figure 72 SPM - TX-RX Interaction

Alternatively, a transparent data stream can also be processed externally by the Application Controller (see **Chapter 2.5.1.2 Data Interface**).

Self Polling Mode is entered by setting the MSEL register bit to 1.

Configuration changes are allowed only by switching to SLEEP Mode, and returning to Self Polling Mode after reconfiguration.

The **Polling Timer Unit** controls the timing for scanning (On time) and sleeping (Off time, SPM_OFF). Up to four independent configuration sets (A, B, C and D) can automatically be processed, thus enabling scanning from different transmit sources. Additionally, up to 3 different frequency channels within each configuration may be scanned to support Multi-Channel applications. See also **Chapter 2.6.2 Polling Timer Unit**. So a total number of up to 12 different frequency channels is supported.

The **Wake-Up Generation Unit** identifies, whether an incoming data stream matches the configurable wake-up criterion.

After fulfillment of the wake-up criterion, modulation can be switched automatically.

See also **Chapter 2.6.1.6 Automatic Modulation Switching**, **Chapter 2.4.8.5 Wake-Up Generator** and **Chapter 2.5.1.2 Data Interface** (in Subsection TMRDS).

The following state diagrams and explanations help to illustrate the behavior during Self Polling Mode. First there is a search for a wake-up criterion according to Configuration A on up to three different channels. Then, there is an optional search for a wake-up criterion according to Configuration B, C and D, again including up to 3 channels.

In applications using only Single-Configuration, settings are always taken from Configuration A.

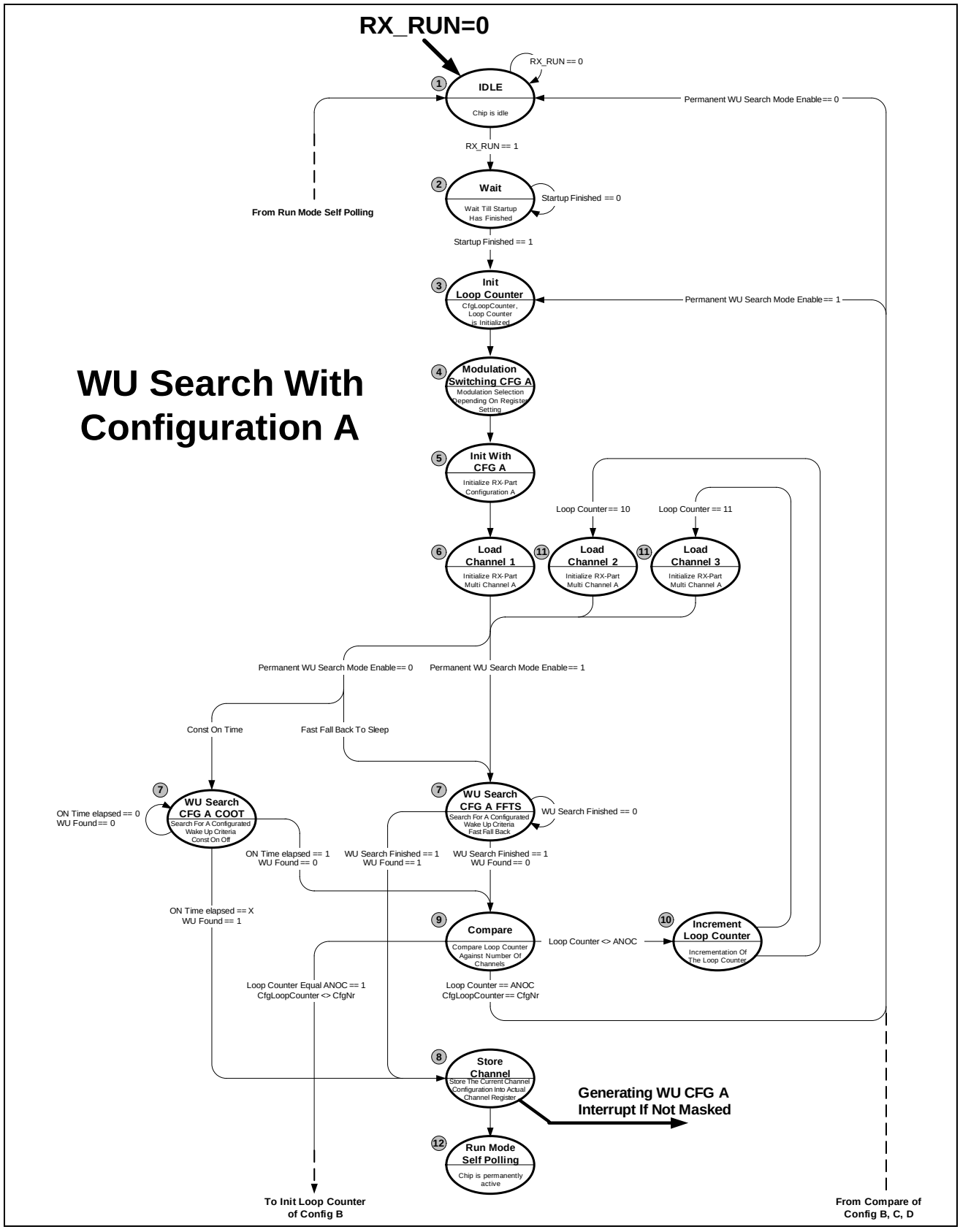


Figure 73 Wake-up Search with Configuration A

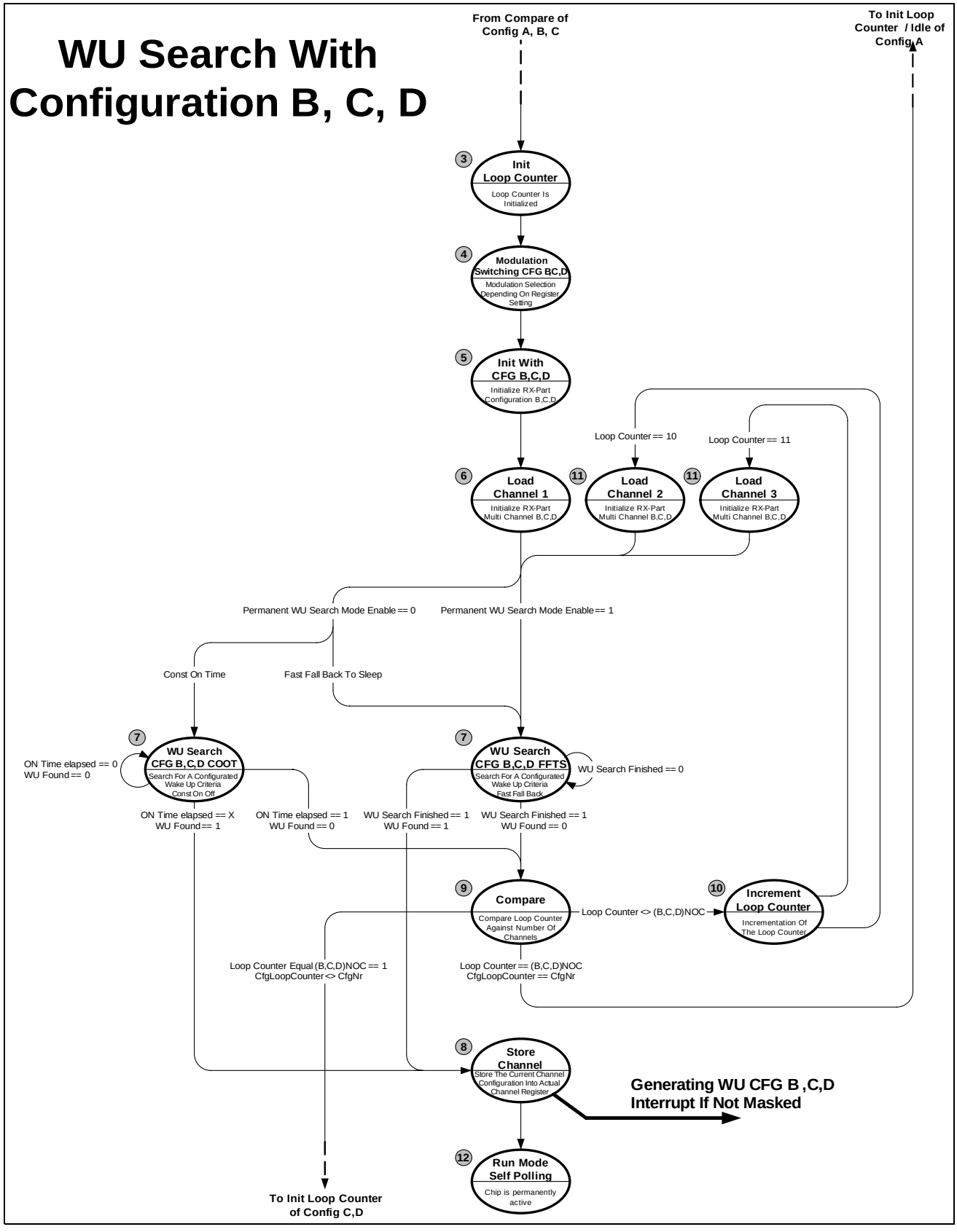


Figure 74 Wake-up Search with Configuration B, C, D

2.6.1.6 Automatic Modulation Switching

In **Self Polling Mode**, the chip is able to automatically change the type of modulation after a **wake-up** criterion was fulfilled in a received data stream. The type of modulation used in the different operational modes is selected by the SFR control bit MT.

2.6.1.7 Multi-Channel in Self Polling Mode

As previously mentioned, in Self Polling Mode the TDA5240 allows RF scans on up to three RF channels per configuration, this can be defined in the x_CHCFG register. Channel frequencies are defined in registers x_PLLINTCy, x_PLLFRAC0Cy, x_PLLFRAC1Cy, x_PLLFRAC2Cy, where x = A, B, C or D and y = 1, 2 or 3.

The channel number at which a wake-up criterion has been found is available in register RFPLLACC. See also **Chapter 2.4.5 Sigma-Delta Fractional-N PLL Block**.

2.6.1.8 Run Mode Self Polling (RMSP)

The chip enters **Run Mode Self Polling** after a successful fulfillment of a **wake-up** criterion in Self Polling Mode.

When Wake-Up criterion for RSSI or Signal Recognition (see **Chapter 2.4.8.1**) is selected and fulfilled, this leads to a change to **Run Mode Self Polling**. This will be interesting especially in case of a transparent data stream being processed externally by the Application Controller (see **Chapter 2.5.1.2 Data Interface**).

The following steps are performed automatically, depending on register settings:

- Modulation switching (see **Chapter 2.6.1.6 Automatic Modulation Switching**)
- Wait for valid TSI (see **Chapter 2.4.8.6 Frame Synchronization**)
- Initialize FIFO (see **Chapter 2.5.2 Receive FIFO**) and write data to FIFO
- Scan for MIDs (see **Chapter 2.4.8.7 Message ID Scanning**)

Depending on interrupt masking, the host microcontroller is alerted when

- a data frame has started,
- an MID has been found, (if enabled) or
- EOM (End of Message) has been detected.

See also **Chapter 2.5.4 Interrupt Generation Unit**

Run Mode Self Polling is left, when synchronization is lost and the timeout timer for loss of synchronization (TOTIM_SYNC) has elapsed, or when one of the other timeout timers (TOTIM_TSI, TOTIM_EOM) for each configuration (A, B, C, D) has elapsed, or when an EOM occurred and the SFR bit EOM2SPM is activated, or when the operating mode is switched to SLEEP or Run Mode Slave by the host microcontroller.

Timeout timers for getting no TSI or getting no EOM within a certain time period can be used to avoid a deadlock situation, e.g. TOTIM_TSI can be used in case an interfering transmit signal fulfilled the wake-up criterion and keeps on transmitting, but no TSI can be found in this data stream within a certain programmable time period. TOTIM_EOM might be used in case EOM criterion “EOM by payload data length” cannot be applied.

The timeout timer functionality in the absence/presence of an interfering signal is shown in **Figure 75** and **Figure 76**.

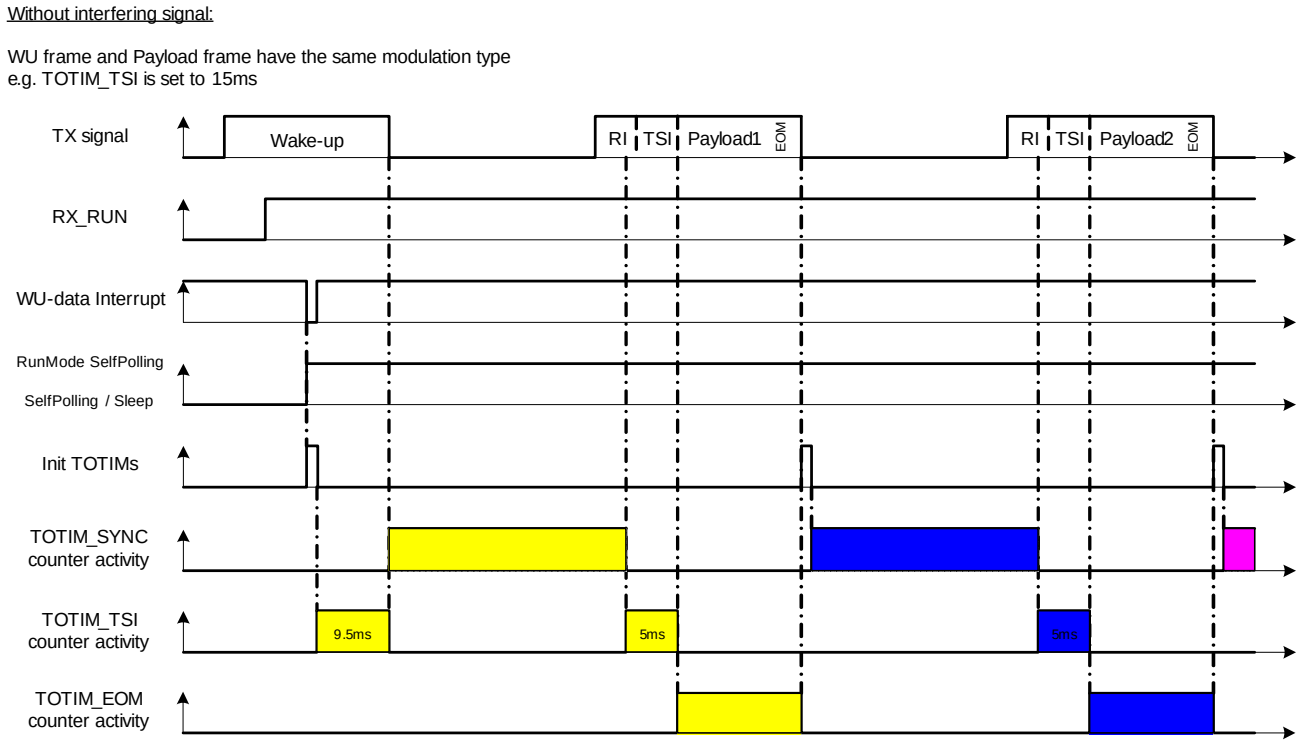


Figure 75 TOTIM Behavior without Presence of Interferer

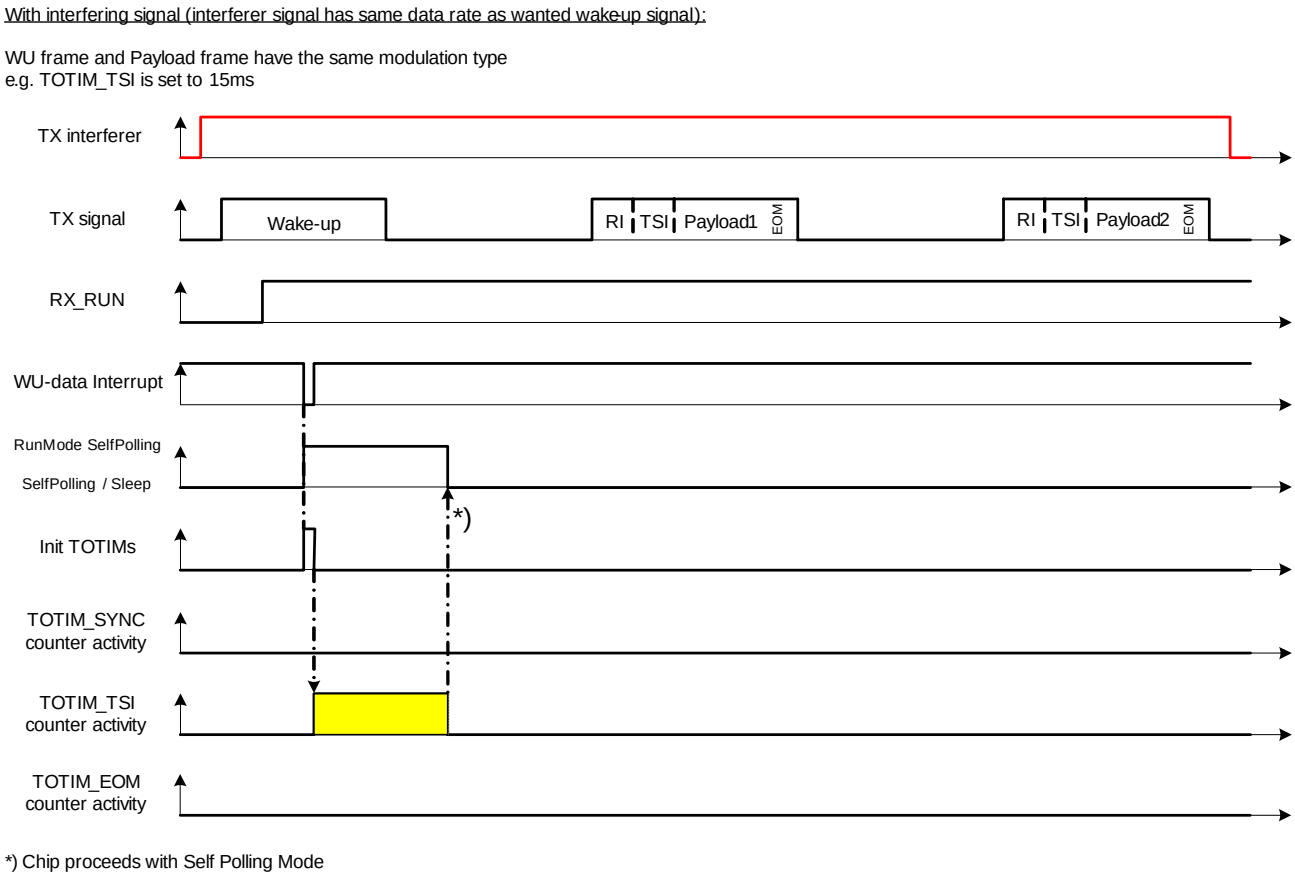


Figure 76 TOTIM Behavior in Presence of Interferer

On expiring of one of the timeout timers, the receiver proceeds with Self Polling Mode and with searching for a suitable wake-up criterion on the next programmed channel (either next RF channel or next configuration, depending on the selected mode - Multi-Configuration or Multi-Channel or a mix of both) or a search for a wake-up criterion in Configuration A is initiated.

As long as the chip is in Run Mode Self Polling, incoming data frames (including a RUNIN sequence and TSI, but without necessity of additional wake-up patterns) can be received and stored.

The data FIFO can be initialized and cleared either at

- Cycle Start, that means whenever Run Mode Self Polling is entered or
- Frame Start, when a TSI has been successfully identified (and Receive FIFO is not locked).

Further information about the Receive FIFO can be found in the **Chapter 2.5.2 Receive FIFO**.

After an EOM was found, the information about the RF channel and the configuration of the actual payload data is saved in the RFPLLACC register.

After detection of EOM the TDA5240 can either proceed with a search for a wake-up criterion in the next configuration or a search for wake-up in Configuration A can follow or the TOTIMs of the current configuration are reloaded for being prepared to receive another (redundant) payload data frame within the same configuration.

Alternatively, a transparent data stream can also be processed externally by the Application Controller. Therefore the external controller needs the possibility to send following commands, which would normally be generated by the TDA5240 itself (see **Figure 77** and EXTPCMD register as well):

- EXTTOTIM: So the TDA5240 can proceed with Self Polling Mode (either with the next programmed channel or with Configuration A).
- EXTEOM found: In this case the TDA5240 can either proceed with Self Polling Mode (either with the next configuration or with Configuration A) or stay in Run Mode Self Polling.

EXTTOTIM and EXTEOM are only available, when the external processing mode is deactivating functional blocks (see bit group x_CHCFG.EXTPROC).

When the actual processed configuration is right before the Off time and the Application Controller sends one of the above mentioned commands, then the TDA5240 can proceed with the Off time (in case next configuration is selected).

If the autonomous Wake-up Search with Configuration A follows a TOTIM or EOM event, then also the Polling Timer is initialized, this means a new On period is started. In case the Wake-up Search is started with Next Programmed Channel (after a TOTIM event) or Wake-up Search gets started with Next Configuration (after an EOM event), then the Polling Timer is not initialized. This means that the On time counter proceeds with the old value from leaving the previous Wake-up search period successfully. This is the case for Fast Fall Back to SLEEP Mode.

In Constant On-Off Time Mode the Polling Timer is always initialized after a TOTIM or EOM event.

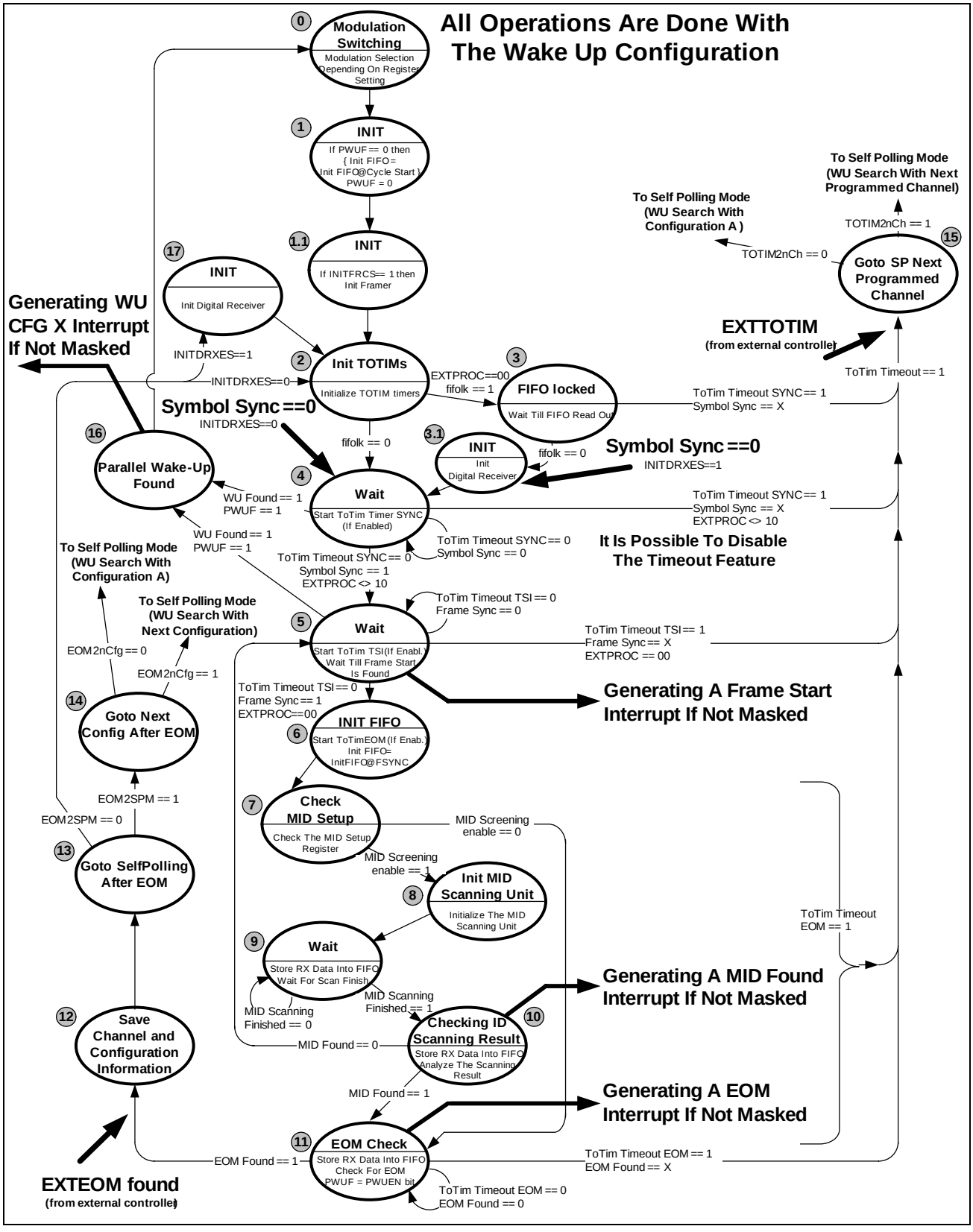


Figure 77 Run Mode Self Polling

While the TDA5240 is in Run Mode Self Polling, further Wake-ups would normally not be detected by the receiver. If the functionality of a parallel Wake-up search during the search for a TSI is desired, this can be activated by the PWUEN bit. In this case the Wake-up search is not active during a recognized payload and is only active after the first received payload frame, as can be seen from **Figure 77**. This feature can only be used, when modulation type is the same for SPM and RMSP.

So after a reception of the EOM from the current payload, the parallel WU search can take place in this mode. The WU search will be active after Symbol Sync has been detected. The WU search will be active until the Synchronization gets lost or wake-up is generated. After the Synchronization gets lost the WU search will be finished and wake-up can not be detected any more (the TSI search continues as usual).

Following procedure can be applied with help of 3 SPI Write command sequences.

The idea is to generate external EOM every time the Symbol Sync goes to inactive state and no interrupt (TSI or WU) has been detected. This will bring the MCU to the cycle start and reinitialize the WU search.

Configuration:

Write x_WUC.PWUEN = 1

// Enable Parallel Wake-up search

Write x_WURSSITHx 0xFF

// Set RSSI threshold to max value (avoid WU during the reinitialization procedure)

Write x_WULOT 0xFF

// Set WULOT to max value (avoid WU during the reinitialization procedure)

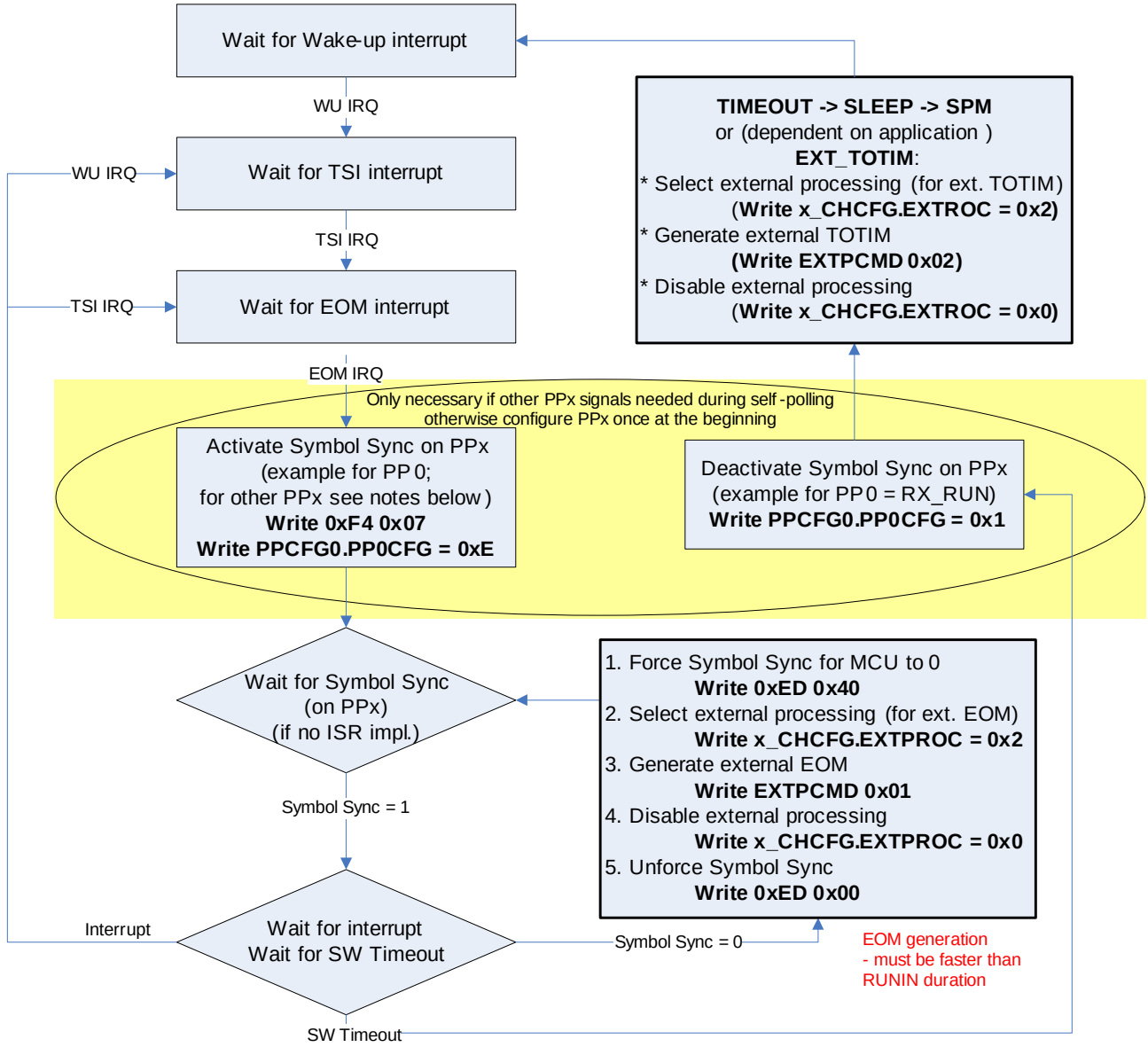


Figure 78 Parallel Wake-up Search

Notes:

- Symbol Sync can be activated on any PPx port

  PP0: Write 0xF4 0x07 & Write PPCFG0 0x0E

  PP1: Write 0xF4 0x70 & Write PPCFG0 0xE0

  PP2: Write 0xF5 0x01 & Write PPCFG1 0x0E

  PP3: Write 0xF5 0x10 & Write PPCFG1 0xE0

- Symbol Sync monitoring necessary only in run mode between frames and WU pattern or till software timeout generated

- generation of external EOM will reinitialize also the TOTIM timers
- external EOM generation period should be smaller than the RUNIN length
  (7 chips RUNIN = ~62 us @ 112 kchip/s , 5 SPI write commands = ~ 60 us @ 2 Mbit)
- minimal Symbol Sync active period = TVWIN, minimal Symbol Sync inactive period = RUNIN

For protocols where no ASK/FSK switching is required between the Wake-up and payload frame, the Wake-up and TSI pattern can share the same bits (e.g. Wake-up pattern = ..00000, TSI = 000001, all bits Manchester encoded). This function can be activated by the INITFRCS bit, so then there is no reset of the framer compare shift register after a Wake-up event, which can shorten the required processing time.

2.6.2 Polling Timer Unit

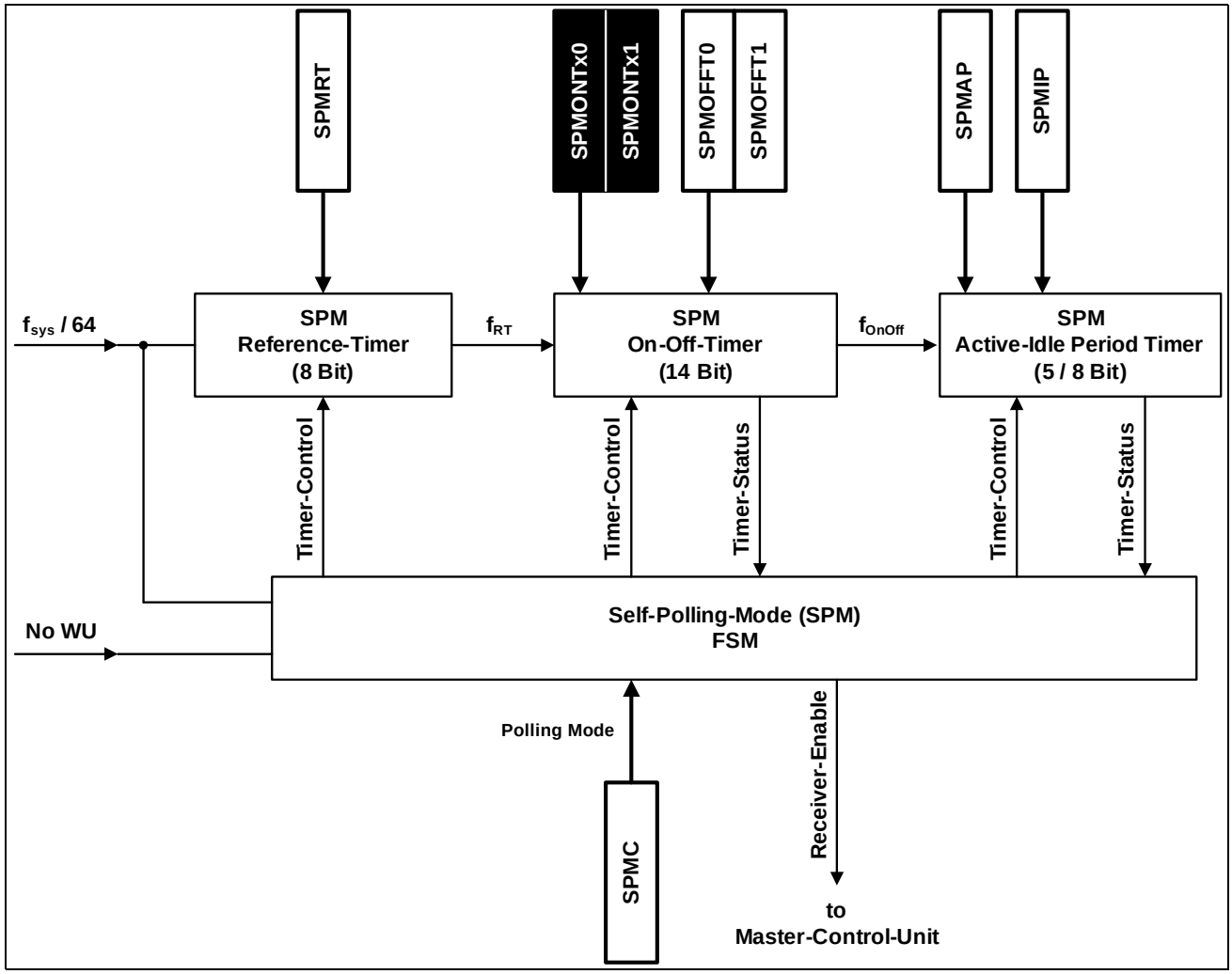


Figure 79 Polling Timer Unit

The Polling Timer Unit consists of a Counter Stage and a Control FSM (Finite State Machine).

The Counter Stage is divided into three sub-modules.

The **Reference Timer** is used to divide the state machine clock (f_{sys}/64) into the slower clock required for the SPM timers.

The **On-Off Timer** and the **Active Idle Period Timer** are used to generate the polling signal. The entire unit is controlled by the SPM FSM.

The TDA5240 is able to handle up to four different sets of configurations automatically. However, the examples and figures in this subsection only show up to two configuration sets for the sake of clarity.

2.6.2.1 Self Polling Modes

Four polling modes are available to fit the polling behavior to the expected wake-up patterns and to optimize power consumption in Self Polling Mode.

The following 4 Polling Modes are available and can be configured via 2 bits in the configuration register SPMC:

- Constant On-Off (COO)
- Fast Fall Back to SLEEP (FFB)
- Mixed Mode (MM)
- Permanent Wake-Up Search (PWUS)

A detected wake-up data sequence or an actual value for RSSI or Signal Recognition (a combination of Signal Detector and Noise Detector, see **Chapter 2.4.8.1**) exceeding a certain adjustable threshold forces the TDA5240 into Run Mode Self Polling.

In all modes the timing resolution is defined by the Reference Timer, which scales the incoming frequency (f_{sys}/64) corresponding to the value, which is defined in the Self Polling Mode Reference Timer (SPMRT) register. Changing values of SPMRT helps to fit the final On-Off timing to the calculated ideal timing.

2.6.2.2 Constant On-Off Time (COO)

In this mode there is a constant On and a constant Off time. Therefore also the resulting master period time is constant. The On and Off time are set in the SPMONTA0, SPMONTA1, SPMONTB0, SPMONTB1, SPMONTC0, SPMONTC1, SPMONTD0, SPMONTD1, SPMOFFT0 and SPMOFFT1 registers. The On time configuration is done separately for Configuration A, B, C and D.

When **Single-Configuration** is selected then only Configuration A is used. The number of RF channels is defined in the A_CHCFG register (**Single-Channel** or **Multi-Channel** Mode).

Multi-Configuration Mode allows reception of up to 4 different transmit sources. The corresponding RF channels can be defined in the A_CHCFG, B_CHCFG, C_CHCFG and D_CHCFG registers. In the case of Multi-Channel or combination of Multi-Channel and Multi-Configuration Mode, the configured On time is used for each RF channel in a configuration. The diagram below shows possible scenarios.

All receive modes described in **Chapter 2.5.1.2 Data Interface** can be used.

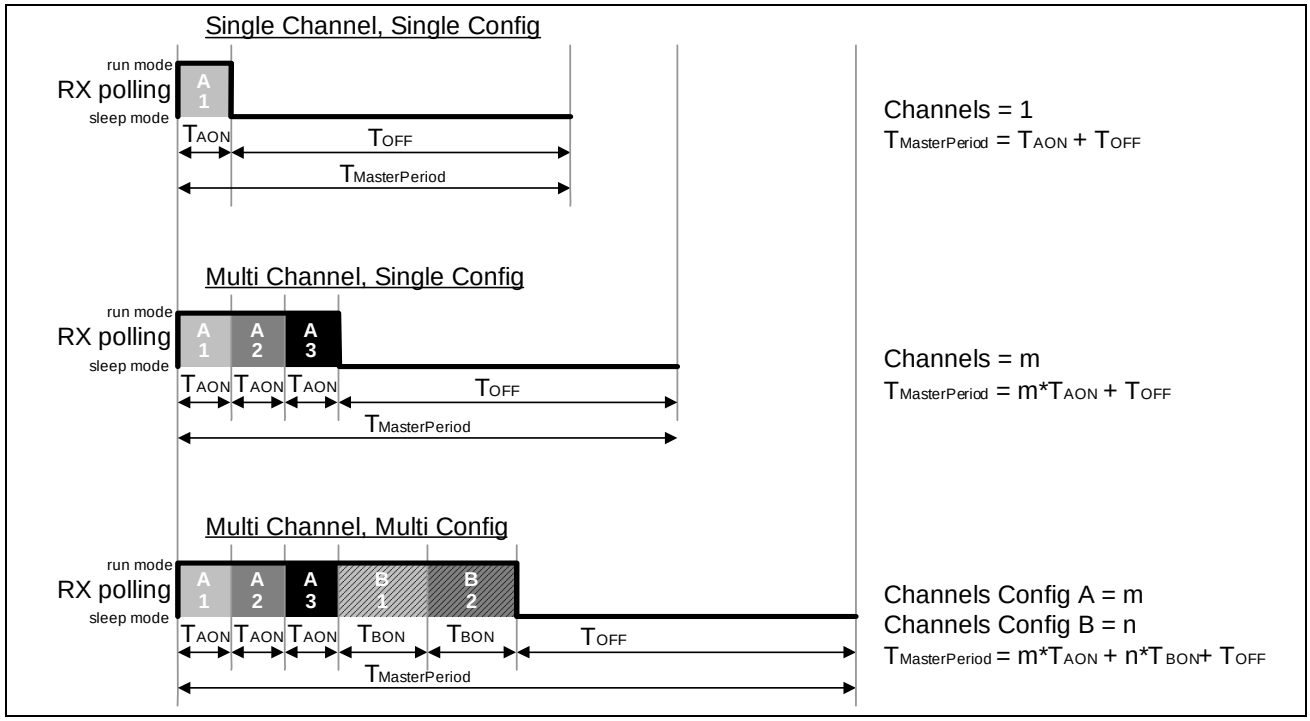


Figure 80 Constant On-Off Time

Calculation of the On time:

The On time for each channel must be long enough to ensure proper detection of a specified wake-up criterion. Therefore the On time depends on the wake-up pattern, and the wake-up criterion. It has to include transmitter data rate tolerances.

A widely used wake-up pattern is a sequence of equal Bi-phase encoded bits or a certain Bi-phase encoded bit pattern.

T_{ON} also must include the relevant start-up times. In case of the first channel after T_{OFF}, this is the Receiver Start-Up Time. In case of following channels (RF Receiver is already on, there is only a change of the channel or the configuration), e.g. if Configuration B is used, this is the Channel Hop Latency Time. In addition, it has to be considered that some data bits are required for synchronization and internal latency, see **Chapter 2.4.8.8 RUNIN, Synchronization Search Time and Inter-Frame Time**.

There are other wake-up patterns in use as well, which have several (up to 10 and more) short wake-up sequences (a few byte each) that are separated by a certain pause (again a few byte each). In this case the On time has to be set, so that a possible wake-up can be found within two wake-up sequences including the pause in-between.

Calculation of the Off time:

The longer the Off time, the lower the average power consumption in Self Polling Mode. On the other hand, the Off time has to be short enough that no transmitted wake-up

pattern is missed. Therefore the Off time depends mainly on the duration of the expected wake-up pattern.

If there are further channels scanned, T_{OFF} has to be reduced by the related additional On times.

For basic timing of WU on RSSI in COO mode, please see **Figure 81**.

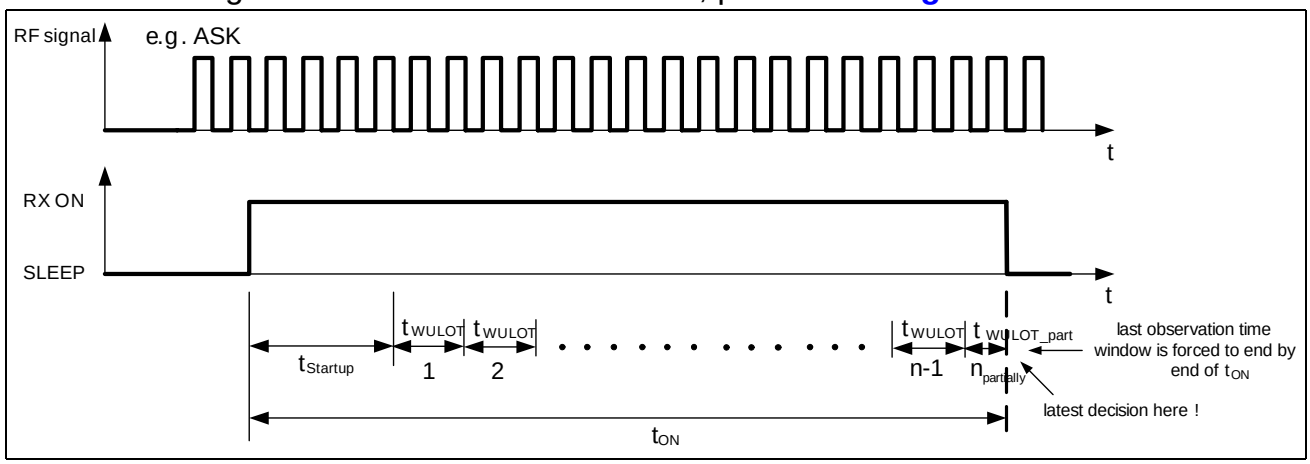


Figure 81 COO Polling in WU on RSSI Mode

Always check at the end of the current observation time window, if there is a WU (Wake-Up) event or NOT. This means, in algorithmic description (see also **Figure 10**, **Chapter 2.4.7 RSSI Peak Detector** and **Chapter 2.4.8.5 Wake-Up Generator**):

if (RSSIPWU_value > x_WURSSITHy) and (RSSIPWU_value > x_WURSSIBHy)

then WU

else NOT

Here, ‘NOT‘ means to keep on evaluating and move on to the next observation time window, also keep on peak value tracking of RSSIPWU signal. Keep on walking through the observation time windows until there is a WU event from the algorithm above or finally decide at the end of the On time with the following algorithm:

if (RSSIPWU_value > x_WURSSITHy) and (RSSIPWU_value < x_WURSSIBLy or RSSIPWU_value > x_WURSSIBHy)

then WU

else NOT

If there is a WU event at the end of an observation time window while walking through the observation time windows, freeze/hold this decision/peak value in register RSSIPWU for optional read out and switch to run mode self polling.

Instead of the single RSSI criterion also the Signal Recognition criterion can be activated.

Combined Level and Data criterion in COO mode

On using the Wake-Up on Data criterion in COO mode, the RSSI criterion (including the RSSI blocking window) can be applied additionally by setting the bit x_WUC.UFFBLCOO. This means that a Wake-Up interrupt will not be generated, when a blocking RSSI level (e.g. an interfering signal) is detected even when the Data criterion is fulfilled.

The behavior of the additional RSSI criterion is similar to the behavior in Ultrafast Fall Back Mode.

After the level observation time the receiver checks, if the RSSI level is within a valid range. If RSSI is within a valid range, the state machine will go on to check the Data criterion. If the RSSI is within a forbidden range, a new level observation time is started (Note that no parts of the Wake-Up pattern are lost in this case, when the RSSI criterion succeeds within the following observation time).

This will be done as long as the RSSI value is within a forbidden range and the On time is not elapsed.

If the receiver loses synchronization within the search for the Data criterion (e.g. pattern detection), the WU unit will be initialized and checks again for the RSSI criterion.

Instead of the additional RSSI criterion also Signal Recognition criterion can be applied.

When the Signal Recognition threshold (x_WURSSIBHy) is not exceeded at Observation Time, the Wake-Up on Level FSM (finite state machine) and Wake-Up on Data FSM are initialized.

If the threshold is exceeded, then the Wake-Up on Level FSM enters the READY state and has no further impact on Wake-up search until the Wake-up unit is initialized again.

When afterwards a Data Criterion is found to be OK (e.g. pattern matches, number of equal bits or random bits is reached), the Wake-up search is completed positively.

When a Data Criterion is found to be not OK, the Wake-up search is terminated independent of the state of the Wake-Up on Level FSM. Therefore both FSMs are initialized.

2.6.2.3 Fast Fall Back to SLEEP (FFB)

This mode is used to switch off the receiver, if there is no RF signal, as quickly as possible to reduce power consumption.

During the search for wake-up data, there is a check for a bit stream, to which the system can be synchronized. If there is no synchronization to a bit stream within the so-called Sync Search Time Out (SYSRCTO), the wake-up search for this channel is stopped. If synchronization to a bit stream is possible (and not lost again), the TDA5240 waits if the wake-up criterion is fulfilled. If the wake-up criterion is not fulfilled (in worst case, if the last bit of an expected wake-up data pattern is wrong), the wake-up procedure for this channel is stopped, and the TDA5240 tries to synchronize on the next channel, or falls back to sleep. That means that the effective search time and, consequently, the receiver active time is significantly shorter, and power consumption is reduced, when no input signal is present. Calculation of Sync Search Time Out can be found in **Chapter 2.4.8.8 RUNIN, Synchronization Search Time and Inter-Frame Time**.

The needed time for detecting that no relevant transmission took place can be further reduced by using Ultrafast Fall Back to SLEEP (UFFB). When there was no Wake-up on Level criterion fulfilled in UFFB Mode during the Observation Time (T_{WULOT}, see **Chapter 2.4.8.5**), then the system goes back to SLEEP (or to next config/channel). This can further reduce the receiver active time, when no data is available. When Wake-up on Level criterion was fulfilled, then the system proceeds with normal FFB functionality (SYSRCTO, optional Wake-up data criterion).

Note: UFFB and FFB start working at the same time!

Ultrafast Fall Back to SLEEP is working, when a Wake-up on Data criterion is selected, the UFFBLCOO bit is enabled and FFB or PWUS mode is selected. The UFFB level criterion can be selected in the x_WUC register.

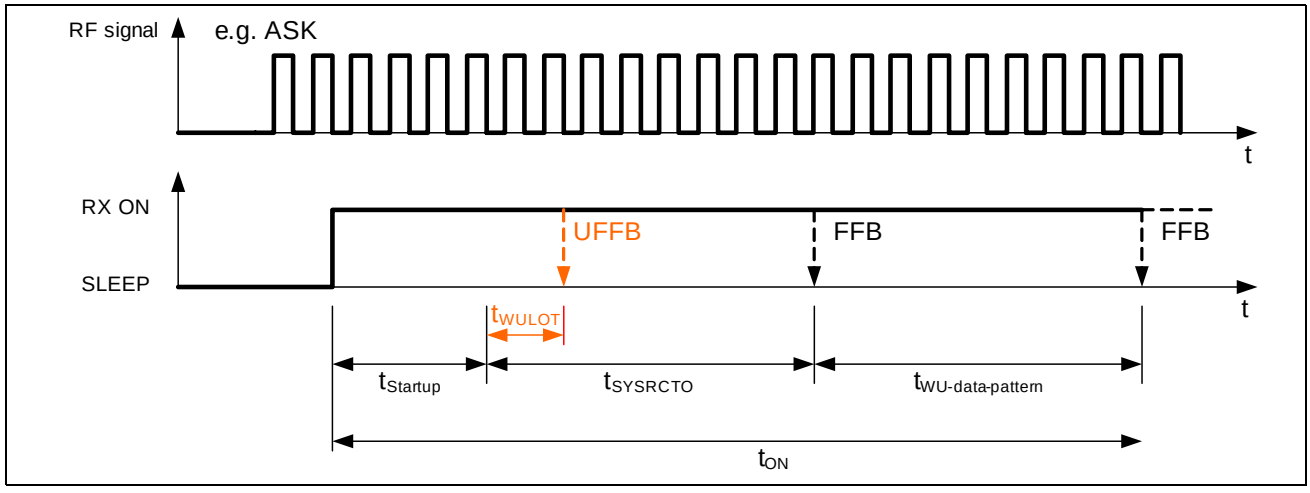


Figure 82 Ultrafast Fall Back to SLEEP

At the end of the observation time the RSSI peak tracking value of RSSIPWU signal is compared to the 3 thresholds. Then the decision is made. The algorithmic description is as follows (see also **Figure 10**, **Chapter 2.4.7 RSSI Peak Detector** and **Chapter 2.4.8.5 Wake-Up Generator**):

if (RSSIPWU_value > x_WURSSITHy) and (RSSIPWU_value < x_WURSSIBLy or RSSIPWU_value > x_WURSSIBHy)

then WU

else NOT

Instead of the RSSI criterion also Signal Recognition criterion can be applied. When the Signal Recognition threshold (x_WURSSIBHy) is not exceeded at Observation Time, then the system goes back to SLEEP or the Wake-Up on Level FSM (finite state machine) is initialized and a Wake-up search is performed on the next specified channel/configuration.

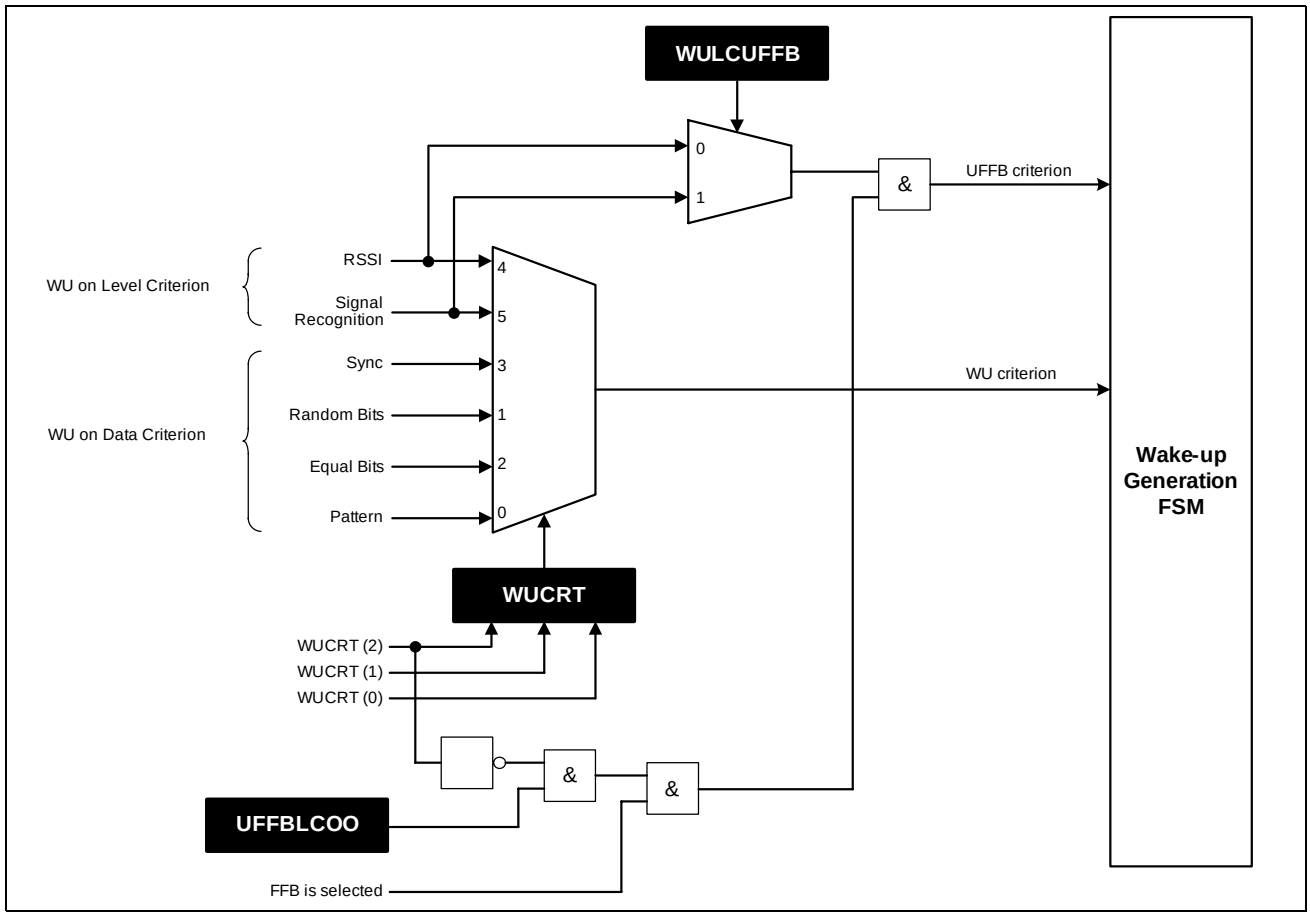


Figure 83 UFFB activation

The On and Off time setting is different from the Constant On-Off Time Mode. The entire On time is defined in the SPMONTA0 and SPMONTA1 registers. Regardless of the

numbers of RF channels and whether or not Multi- or Single-Configuration is used, the On time is defined with the Configuration A On-Timer. The deactivation of the receiver can happen at different times, but this event does not influence the timer stage, because the On time is still the same. So the master period is constant. The following scenarios are the same as before, but with Fast Fall Back to SLEEP.

Only the following receive modes (see **Chapter 2.5.1.2 Data Interface**) can be used:

- Packet Oriented FIFO Mode (POF)
- Packet Oriented Transparent Payload Mode (POTP)
- Transparent Mode - Chip Data and Strobe (TMCDS)

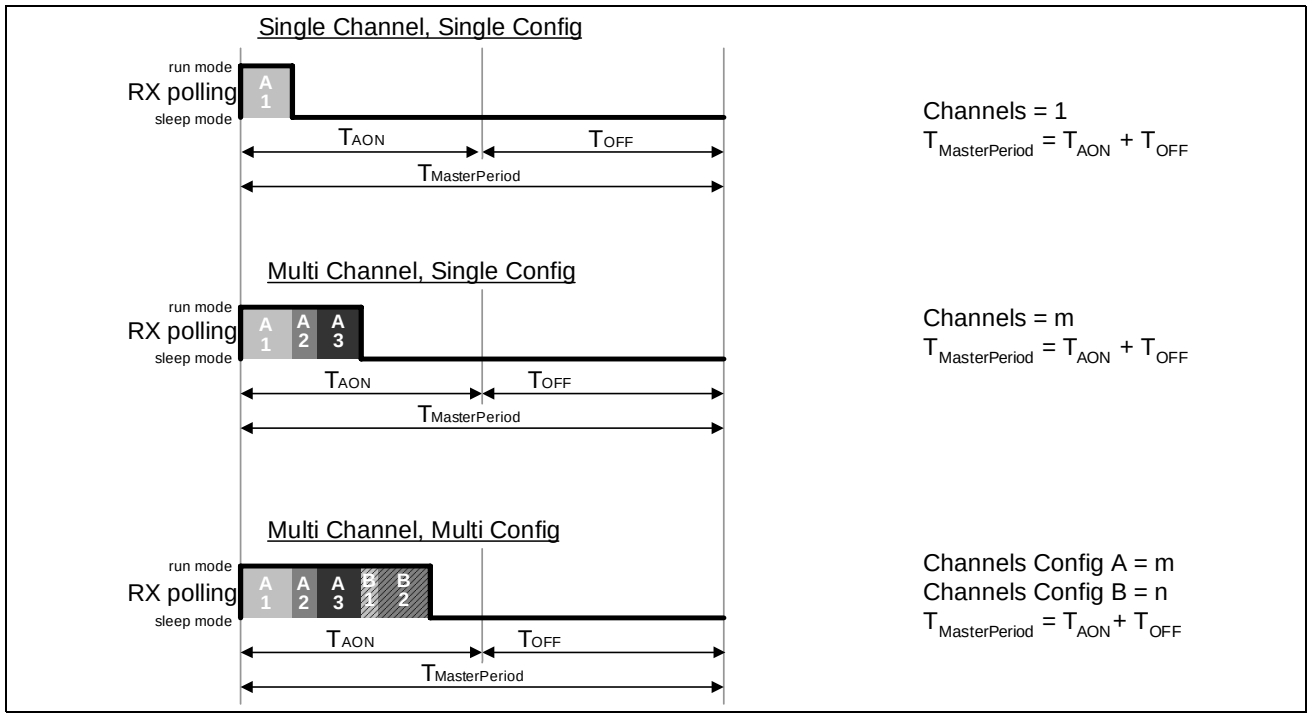


Figure 84 Fast Fall Back to SLEEP

Calculation of the On time:

The On time, which is now a sum for all of the channels and configurations used, must include enough time to ensure proper detection of the specified wake-up pattern on all channels. To cover the worst case scenario, the maximum time is required on all channels as in Constant On-Off.

T_{ON} must also include the relevant start-up times. In case of the first channel after T_{OFF}, this is the Receiver Start-Up Time. In case of following channels (RF Receiver is already on, there is only a change of the channel or the configuration), e.g. if Configuration B is used, this is the Channel Hop Latency Time.

In addition, it has to be considered that some data bits are required for synchronization and internal latency (see **Chapter 2.4.8.8 RUNIN, Synchronization Search Time and Inter-Frame Time**).

Calculation of the Off time:

The same general rules apply as for Constant On-Off Time. The Off time has to be short enough that no wake-up pattern reception is missed.

2.6.2.4 Mixed Mode (MM, Const On-Off & Fast Fall Back to SLEEP)

This mode combines Constant-On Time and Fast Fall Back to SLEEP within different configuration sets: Cfg.A: COO; Cfg.B: FFB; Cfg.C: FFB; Cfg.D: FFB

T_{ON} for Configuration A is always calculated according to Const On-Off rules.

T_{ON} for Configuration B, C and D is always calculated according to Fast Fall Back to SLEEP rules.

In Mixed Mode the On time of the first configuration within the FFB group is used. Below there are shown the same scenarios as before, but now for Mixed Mode. Note that Single-Configuration can be set, but is not recommended in Mixed Mode.

Only the following receive modes (see **Chapter 2.5.1.2 Data Interface**) can be used:

- Packet Oriented FIFO Mode (POF)
- Packet Oriented Transparent Payload Mode (POTP)
- Transparent Mode - Chip Data and Strobe (TMCDS)

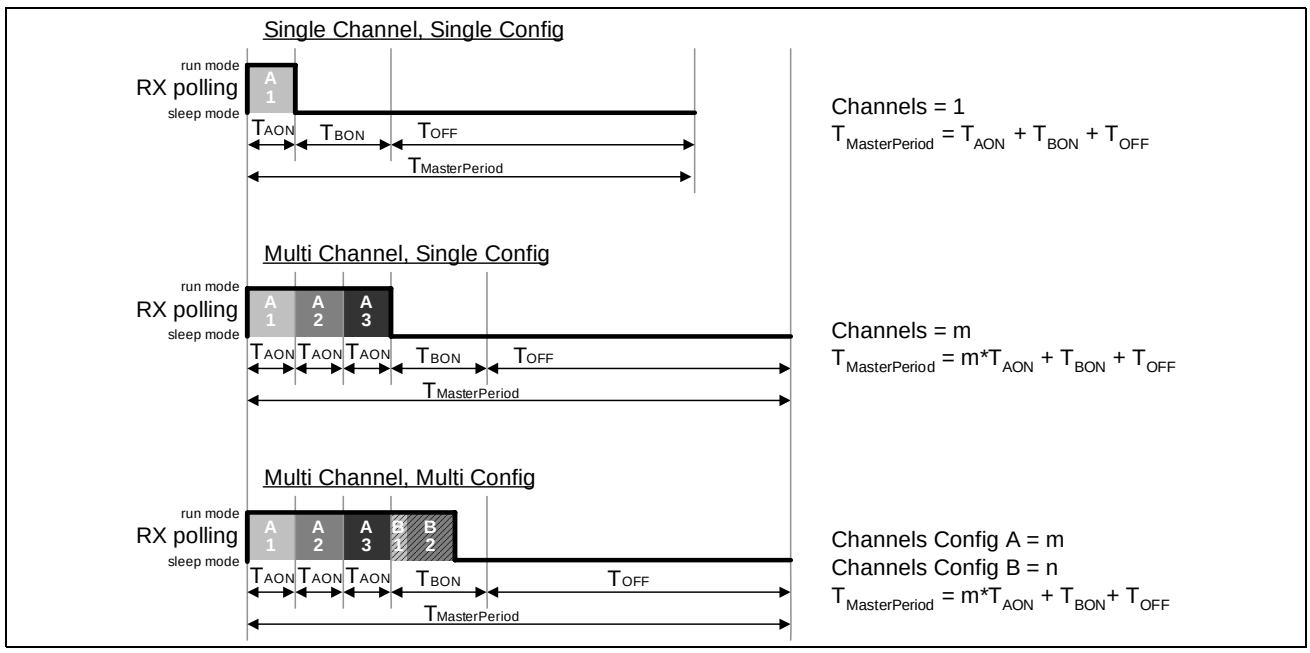


Figure 85 Mixed Mode

2.6.2.5 Permanent Wake-Up Search (PWUS)

In this mode the receiver will work in Fast Fall Back Mode, but it will not go back to the SLEEP state after the last channel has been searched. Instead, it will start again from the beginning (Configuration A, RF Channel 1) until the On time has elapsed. The timing calculation can be seen in **Figure 86**. Ultrafast Fall Back to SLEEP functionality can be used as well.

Only the following receive modes (see **Chapter 2.5.1.2 Data Interface**) can be used:

- Packet Oriented FIFO Mode (POF)
- Packet Oriented Transparent Payload Mode (POTP)
- Transparent Mode - Chip Data and Strobe (TMCDS)

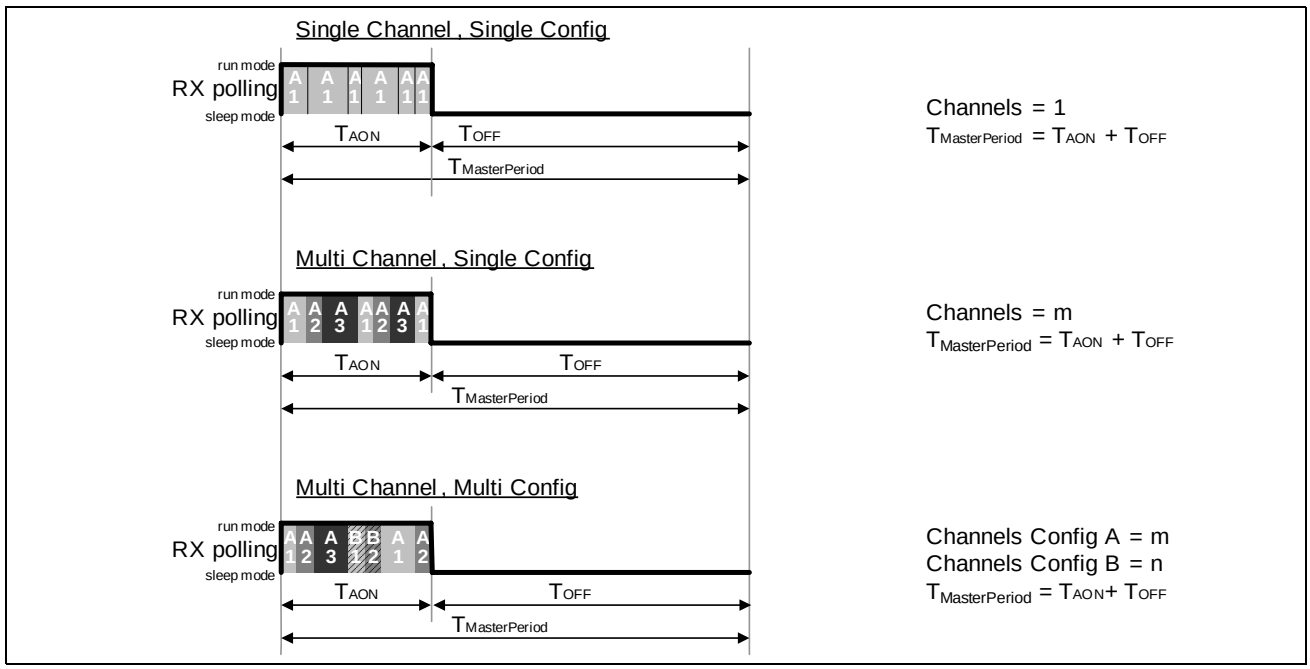


Figure 86 Permanent Wake-Up Search

2.6.2.6 Active Idle Period Selection

This mode is used to deactivate some polling periods and can additionally be applied to each of the above mentioned Polling Modes.

Normally, polling starts again after the $T_{MasterPeriod}$. With this Active Idle Period selection some of the polling periods can be deactivated, independent from the Polling Mode. The active and the idle sequence is set with the SPMAP and the SPMIP registers. The values of these registers determine the factor M and N.

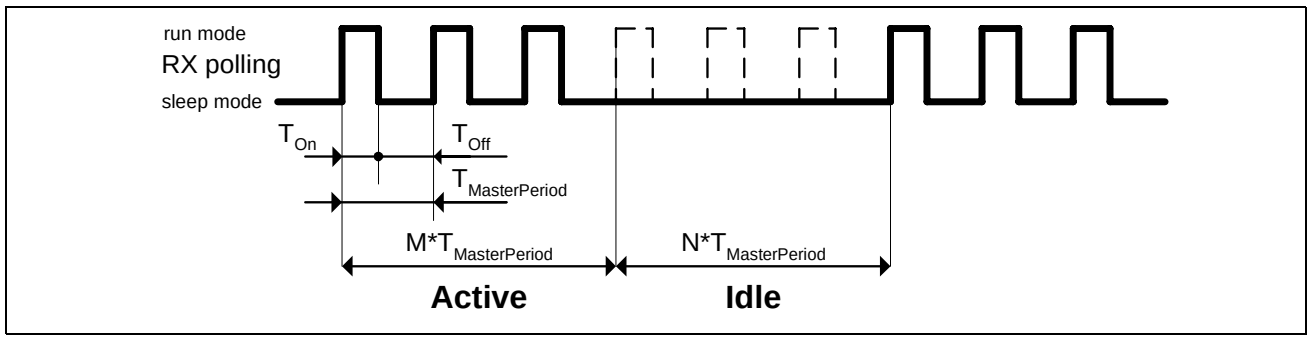


Figure 87 Active Idle Period

2.7 Definitions

2.7.1 Definition of Bit Rate

The definition for the bit rate in the following description is:

$$\text{bitrate} = \frac{\text{symbols}}{\text{s}}$$

If a symbol contains n chips (for Manchester n=2; for NRZ n=1) the chip rate is n times the bit rate:

$$\text{chiprate} = \text{n} \times \text{bitrate}$$

2.7.2 Definition of Manchester Duty Cycle

Several different definitions for the Manchester duty cycle *(MDC)* are in place. To avoid wrong interpretation some of the definitions are given below.

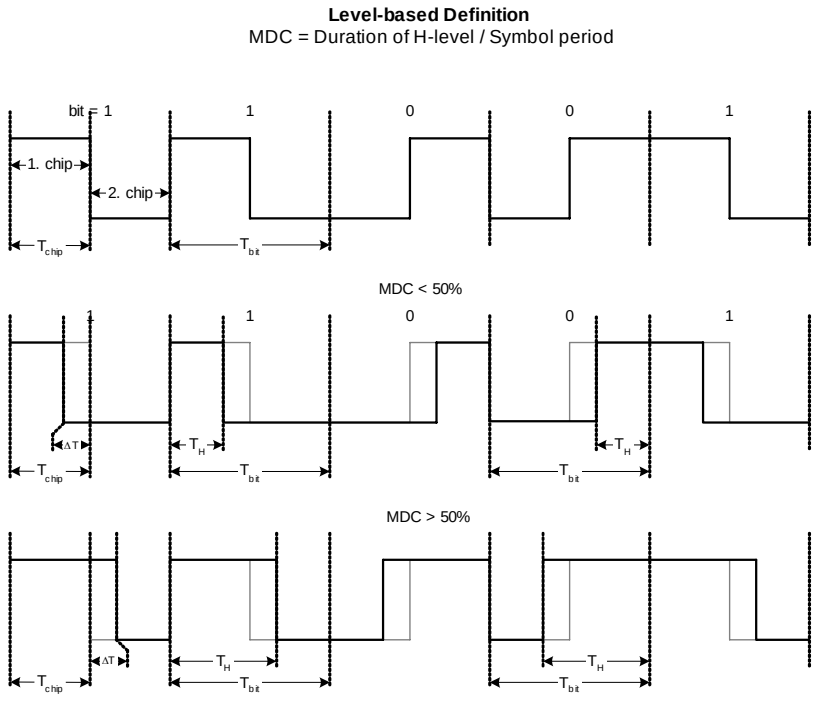


Figure 88 Definition A: Level-based definition

This definition determinates the duty cycle to be the ratio of the high pulse width and the ideal symbol period. The DC content is constant and directly proportional to the specified duty cycle.
For $\Delta T > 0$ the high period is longer than the chip-period and for $\Delta T < 0$ the high period is shorter than the chip-period.

Depending on the bit content, the same type of edge (e.g. rising edge) is sometimes shifted and sometimes not.

With this definition the Manchester duty cycle is calculated to

$$MDC_A = \frac{T_H}{T_{bit}} = \frac{T_{chip} + \Delta T}{T_{bit}}$$

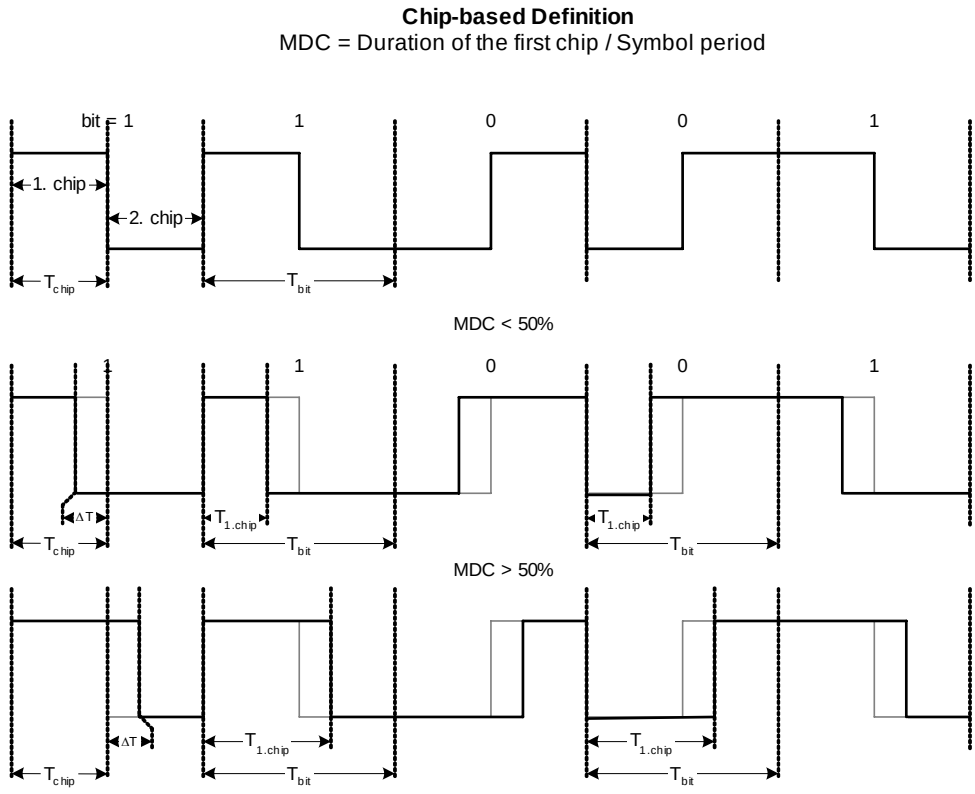


Figure 89 Definition B: Chip-based definition

This definition determinates the duty cycle to be the ratio of the first symbol chip and the ideal symbol period independently of the information bit content. The DC content depends on the information bit and it is balanced only if the message itself is balanced. For $\Delta T > 0$ the first chip-period is longer than the ideal chip-period and for $\Delta T < 0$ the first chip-period is shorter than the ideal chip-period.

Depending on the bit content, the same type of edge (e.g. rising edge) is sometimes shifted and sometimes not.

With this definition the Manchester duty cycle is calculated to

$$MDC_B = \frac{T_{1.chip}}{T_{bit}} = \frac{T_{chip} + \Delta T}{T_{bit}}$$

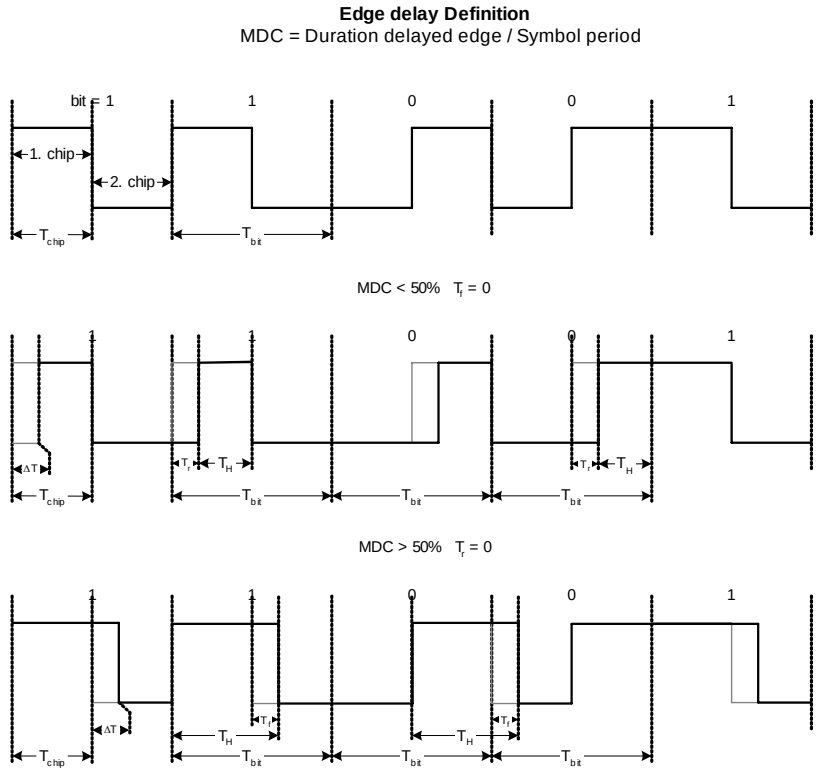


Figure 90 Definition C: Edge delay definition

This definition determinates the duty cycle to be the ratio of the duration of the delayed high-chip and the ideal symbol period independently of the information bit content. The position of the high-chip is determined by the delayed rising edge and/or the delayed falling edge. For $\Delta T = T_{fall} - T_{rise}$ the Manchester duty cycle is calculated to

$$MDC_C = \frac{T_{delayedHighchip}}{T_{bit}} = \frac{T_{chip} + \Delta T}{T_{bit}} = \frac{T_{chip} + T_{fall} - T_{rise}}{T_{bit}}$$

Independent on the bit content, the same type of edge (rising edge and/or falling edge) is shifted.

2.7.3 Definition of Power Level

The reference plane for the power level is the input of the receiver board. This means, the power level at this point (P_r) is corrected for all offsets in the signal path (e.g. attenuation of cables, power combiners etc.).

The specification value of power levels in terms of sensitivity is related to the peak power of P_r in case of On-Off Keying (OOK). This is noted by the unit dBm peak.

Specification value of power levels is related to a Manchester encoded signal with a Manchester duty cycle of 50% in case of ASK modulation.

An RF signal generator usually displays the level of the unmodulated carrier ($P_{carrier}$). This has following consequences for the different modulation types:

Table 6 Power Level

Modulation scheme	Realization with RF signal generator	Power level specification value
ASK	AM 100%	$P_r = P_{carrier} + 6dB$
ASK	Pulse modulation (=OOK)	$P_r = P_{carrier}$
FSK	FM with deviation Δf: $f_1 = f_{carrier} - \Delta f$ $f_2 = f_{carrier} + \Delta f$	$P_r = P_{carrier}$

For power levels in sensitivity parameters given as average power, this is noted by the unit dBm. Peak power can be calculated by adding 3 dB to the average power level in case of ASK modulation and a Manchester duty cycle of 50%.

2.7.4 Symbols of SFR Registers and Control Bits

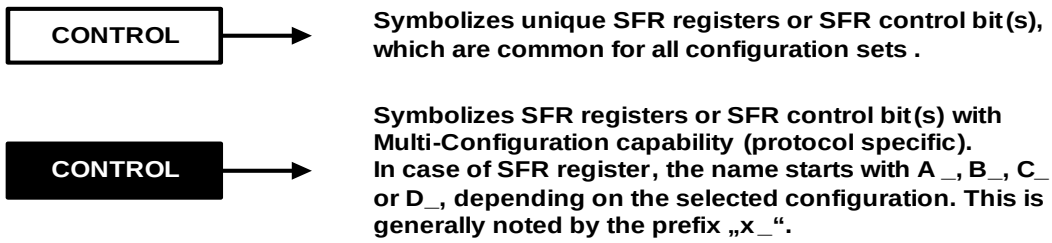


Figure 91 SFR Symbols

2.8 Digital Control (SFR Registers)

2.8.1 SFR Address Paging

An SPI instruction allows a maximum address space of 8 bit. The address space for supporting more than one configuration set is exceeding this 8 bit address room. Therefore a page switch is introduced, which can be applied via register SFRPAGE (see **Figure 92**).

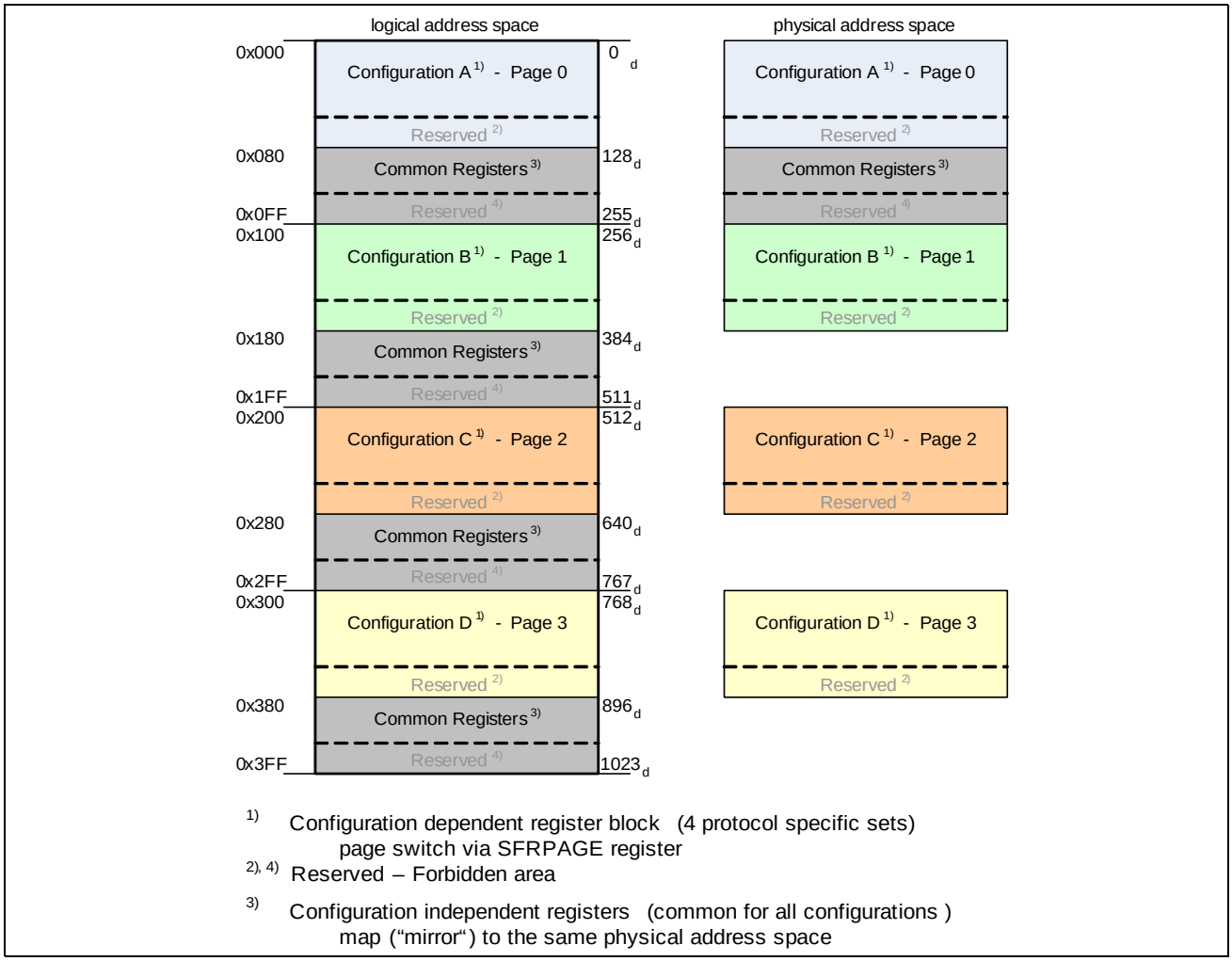


Figure 92 SFR Address Paging

2.8.2 SFR Register List and Detailed SFR Description

The register list is attached in the Appendix at the end of the document.

Registers for Configurations B, C and D are equivalent and not shown in detail.

All registers with prefix “A_” are related to Configuration A. All these registers are also available for Configuration B, C and D having the prefix “B_”, “C_” and “D_”.

3 Applications

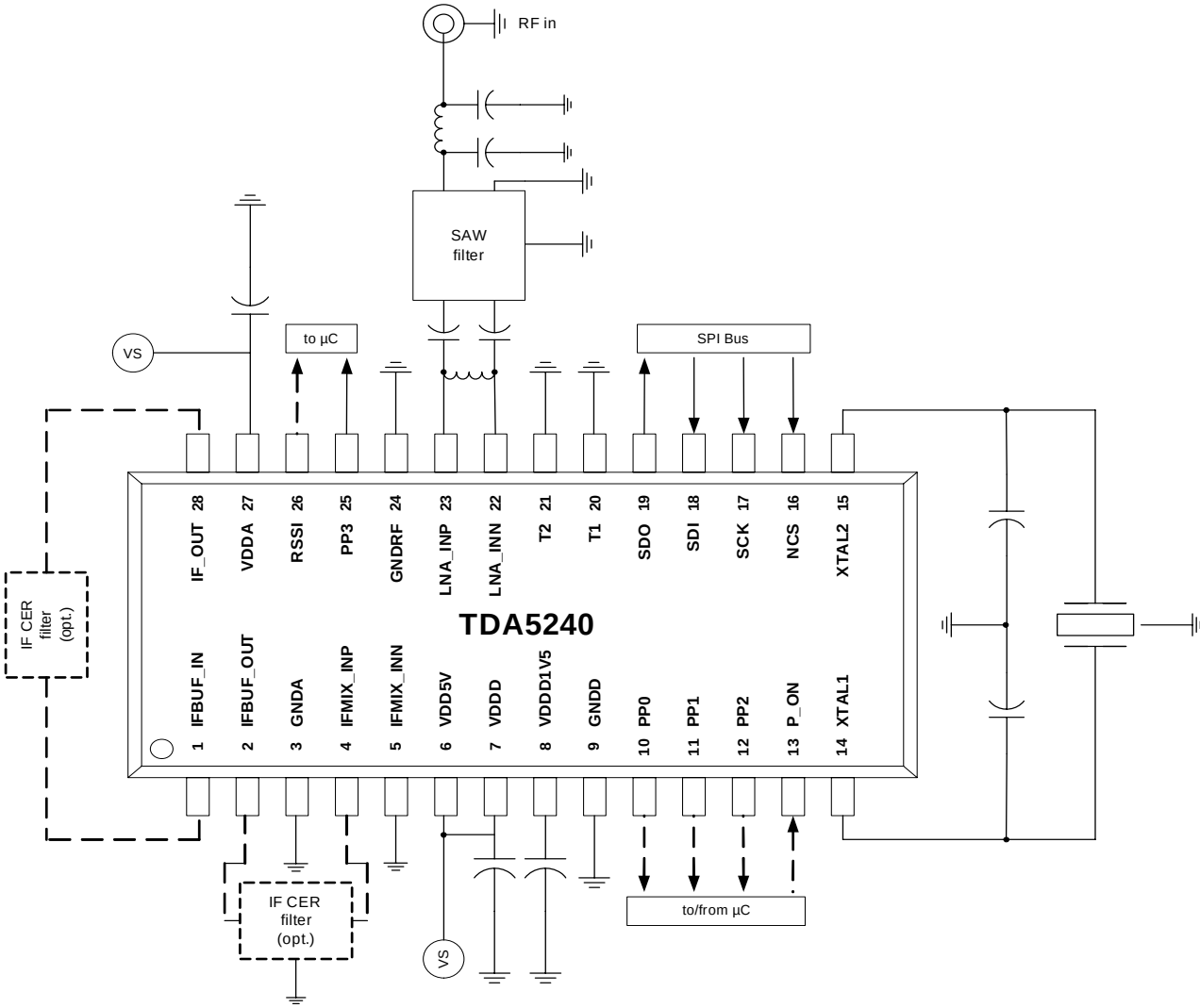


Figure 93 Typical Application Schematic

Note: As a good practice in any RF design, shielding around sensitive nodes can improve the EMC performance of the application.

For achieving the best sensitivity results the following has to be kept in mind. Every digital system generates certain frequencies (f_{SRC}, e.g. the crystal frequency or a microcontroller clock) and harmonics (N * f_{SRC}) of it, which can act as interferer (EMI source) and therefore sensitivity can be reduced.

There are two different cases, which need to be checked for the desired receive channel(s):

Elimination of in-band EMI mixing with (2*M + 1) * f_{LO}, where M > 0:

A square wave is used as LO (Local Oscillator) for the switching-type mixer, which also has odd harmonics. When the harmonics of the EMI source are exactly the IF frequency away from the harmonics of the LO, these spurs will be down-converted to the IF frequency and act as a co-channel interferer within the receiver's channel bandwidth mainly in the 315 MHz band.

In this case a change of the LO injection side (high side or low side injection) can be applied.

Example (Low Side LO-injection):

Wanted channel f_{RF} = 314.233MHz ==> f_{LO} = 303.533MHz ==> 3*f_{LO} = 910.599MHz

f_{XOSC} = 21.948717 MHz ==> 41 * f_{XOSC} = 899.8974 MHz

Resulting IF = 910.599 - 899.8974 MHz = 10.702 MHz ==> co-channel interferer within the receiver's channel bandwidth ==> change LO injection side

Example (High Side LO-injection):

Wanted channel f_{RF} = 314.233 MHz ==> f_{LO} = 324.933 MHz ==> 3*f_{LO} = 974.799 MHz

f_{XOSC} = 21.948717 MHz ==> 44 * f_{XOSC} = 965.744 MHz; 45 * f_{XOSC} = 987.692 MHz

==> both XOSC harmonics are not generating a co-channel interferer at 10.7 MHz

A final sensitivity measurement on the application hardware is recommended.

Elimination of in-band EMI mixing with 1 * f_{LO}:

Assuming a harmonic (N * f_{SRC}) is falling within the BW of the wanted channel and has an impact on the sensitivity there. In this case another XTAL frequency shall be selected, e.g. 10 kHz away

$| N * f_{SRC} - f_{LocalOscillator} | < BW_{Channel}$

Example (e.g. EMI source TDA5240 XOSC):

f_{XOSC} = 21.948717 MHz ==> 42 * f_{XOSC} = 921.846114 MHz

For further details please refer to the corresponding application note or to the latest configuration software.

3.1 Configuration Example

Please see configuration files supplied with the Explorer tool.

4 Reference

4.1 Electrical Data

4.1.1 Absolute Maximum Ratings

Attention: The maximum ratings must not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC may result.

Table 7 Absolute Maximum Ratings

#	Parameter	Symbol	Limit Values		Unit	Remarks
			min.	max.		
A1	Supply Voltage at VDD5V pin	V_{smax}	-0.3	+6	V	
A2	Supply Voltage at VDDD, VDDA pin	V_{smax}	-0.3	+4	V	
A3	Voltage between VDD5V vs VDDD and VDD5V vs VDDA	V_{smax}	-0.3	+4	V	
A4	Junction Temperature	T_j	-40	+125	°C	
A5	Storage Temperature	T_s	-40	+150	°C	
A6	Thermal resistance junction to air	$R_{th(ja)}$		140	K/W	
A7	Total power dissipation at T_{amb} = 105°C	P_{tot}		100	mW	
A8	ESD HBM integrity	V_{HBMRF}	-2	2	KV	According to ESD Standard JEDEC EIA / JESD22-A114-B
A9	ESD SDM integrity (All pins except corner pins)	V_{SDM}	-500	500	V	
A10	ESD SDM integrity (All corner pins)	V_{SDM}	-750	750	V	
A11	Latch up	I_{LU}	100		mA	AEC-Q100 (transient current)
A12	Maximum input voltage at digital input pins	V_{inmax}	-0.3	V_{DD5V}+0.5 or 6.0	V	whichever is lower
A13	Maximum current into digital input and output pins	I_{IOmax}		4	mA	

4.1.2 Operating Range

Table 8 Supply Operating Range and Ambient Temperature

#	Parameter	Symbol	Limit Values		Unit	Remarks
			min.	max.		
B1	Supply voltage at pin VDD5V	V_{DD5V}	4.5	5.5	V	Supply voltage range 1
B2	Supply voltage at pin VDD5V=VDDD=VDDA	V_{DD3V3}	3.0	3.6	V	Supply voltage range 2
B3	Ambient temperature	T_{amb}	-40	105	°C	

4.1.3 AC/DC Characteristics

Supply voltage VDD5V = 4.5 to 5.5 Volt or VDD5V = VDDA = VDDD = 3.0 to 3.6 Volt
Ambient temperature T_{amb} = -40...105°C; T_{amb} = +25°C and VDD5V = 5.0V or VDD5V = VDDA = VDDD = 3.3V for typical parameters, unless otherwise specified.

■ not subject to production test - verified by characterization/design

Table 9 AC/DC Characteristics

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks	
			min.	typ.	max.			
General DC Characteristics								
C1.1	Supply Current in Run Mode and Double Down Conversion Mode	$I_{Run, Double}$		12	15	mA	ASK or FSK mode P_{in} < -50dBm	
C1.2	Supply Current in Run Mode and Single Down Conversion Mode	$I_{Run, Single}$		10.5	14	mA	ASK or FSK mode P_{in} < -50dBm	
C2	Supply current in Sleep Mode	I_{sleep_low}					crystal oscillator in Low Power Mode; clock generator off; valid for SLEEP Mode and during SPM Off time	
	T_{amb} = 25 °C			40	50	µA		
	T_{amb} = 85 °C			60	110	µA		■
	T_{amb} = 105 °C			90	160	µA		■
C3	Supply current in Sleep Mode	I_{sleep_high}		115	350	µA	crystal oscillator in High Precision Mode C_{load} = 25 pF; clock generator off; valid for SLEEP Mode and during SPM Off time	
C4	Supply current in Power Down Mode	I_{PDN}						
	T_{amb} = 25 °C			0.8	1.5	µA		
	T_{amb} = 85 °C			3.7	13	µA		■
	T_{amb} = 105 °C			9.0	27	µA		■
C5	Supply current clock generator	I_{clock}		23	27	µA	$f_{clockout}$ = 1 kHz C_{load} = 10 pF	■
C6	Supply current IF-Buffer	I_{Buffer}		0.5	0.7	mA	f_{IF_1} = 10.7 MHz R_{load} = 330 Ω no AC signal	■

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks	
			min.	typ.	max.			
C7	Supply current during RF-FE startup / BPF calibration	$I_{RF\text{-}FE\text{-}startup,BPFcal}$		2.2	2.9	mA		■
C8	Brownout detector threshold	V_{BOR}	2.3	2.45	2.6	V		
C9	Receiver reset time	t_{Reset}	1.0		3.0	ms	Note: No SPI communication is allowed before XOSC start-up is finished and chip reset is already finished	
C10	Receiver startup time	$t_{RXstartup}$	455	455	455	µs	Time to startup RF frontend (comprises time required to switch crystal oscillator from Low Power Mode to High Precision Mode	■
C11	RF Channel Hop Latency Time and Configuration (Hop) Change Latency Time (e.g. Cfg A to Cfg B)	t_{C_Hop}	111	111	111	µs	Time to switch RF PLL between different RF Channels (does not include settling of Data Clock Recovery) and time to change Configuration	■
C12	RF Frontend startup delay	$t_{RFstartdelay}$	350	350	350	µs	Delay of startup of RF frontend	■
C13	P_ON pulse width	t_{P_ON}	15			µs	Minimal pulse width to reset the chip	■
C14	NINT pulse length	t_{NINT_Pulse}		12		µs	Pulse width of interrupt	■
C15	Accuracy of Temperature Sensor						Valid for temperature range -40°C .. +105°C; using upper 8 ADC bits (ADCRESH)	
C15.1	uncalibrated	$T_{Error, uncal}$			+/- 23	°C	uncalibrated (3 sigma) value	■
C15.2	calibrated	$T_{Error, cal}$			+/- 4.5	°C	after 1-point calibration at room temperature (3 sigma)	■
C16	Accuracy of VDDD readout						Valid for temperature range -40°C .. +105°C; using upper 8 ADC bits (ADCRESH)	
C16.1	uncalibrated	$V_{DDD, Error, uncal}$			+/- 200	mV	uncalibrated (3 sigma) value	■
C16.2	calibrated	$V_{DDD, Error, cal}$			+/- 25	mV	after 1-point calibration at room temperature (3 sigma)	■

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks	
			min.	typ.	max.			
General RF Characteristics (overall)								
D1	Frequency							
	Range 1	f_{band_1}	300		320	MHz	1st Local Oscillator Low Side LO-injection and High Side LO-injection allowed; See also **Chapter 3**	
	Range 2	f_{band_2}	425		450	MHz		
	Range 3	f_{band_3}	863		870	MHz		
	Range 4	f_{band_4}	902		928	MHz		
D2	Frequency step of Sigma-Delta PLL	f_{step}	10.5			Hz	$f_{step} = f_{XTAL} / 2^{21}$	■
D3	ASK Demodulation							
	Data Rate	R_{data}	0.5		40	kchip/s		■
	Data rate tol.	R_{data_tol}	-10		+10	%		■
	Modulation index	m_{ASK}	50		100	%	ASK	■
		m_{OOK}	99		100	%	ON-OFF keying	■
D4	FSK Demodulation							
	Data Rate	R_{data}	0.5		112	kchip/s	including tolerance	■
	Data rate tol.	R_{data_tol}	-10		+10	%		■
	Frequency deviation	Δf	1		64	kHz	frequency deviation zero-peak	■
	Modulation index	m_{FSK}	1.0				m = frequency_deviation$_{zero\text{-}peak}$ / maximum_occuring_data_frequency; m >= 1.25 is recommended at small frequency deviation	■
D5	Decoding schemes							
			Manchester, differential Manchester, Bi-phase Mark / Bi-phase Space					
	Duty cycle ASK	T_{chip}/T_{data}	35		55	%	see **Chapter 2.7.2** Definition C	■
	Duty cycle FSK	T_{chip}/T_{data}	45		55	%	see **Chapter 2.7.2** Definition B	■
D6	Overall noise figure						RF input matched to 50 Ω @ T_{amb} = 25 °C	
	Noise figure	NF		6	8	dB		■

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks	
			min.	typ.	max.			
D7	BER Sensitivity (FSK)						BER = $2*10^{-3}$	
		Manchester coding; for additional test conditions see right after this table					RF input matched to 50 Ω @ T_{amb} = 25 °C; Single-Ended Matching without SAW; Insertion loss of input matching network = 1dB; Receive Mode = TMMF (sampled with ideal data clock); Double Down Conversion	
D7.1	Data Rate 2 kBit/s; Δf = 10 kHz	$SFSK1_{BER}$		-119	-116	dBm	2nd IF BW = 50 kHz PDF = 33 kHz, AFC off, IFATT=0	■
D7.2	Data Rate 10 kBit/s; Δf = 14 kHz	$SFSK2_{BER}$		-114	-111	dBm	2nd IF BW = 50 kHz PDF = 65 kHz, AFC off, IFATT=0	■
D7.3	Data Rate 10 kBit/s; Δf = 50 kHz	$SFSK3_{BER}$		-112	-109	dBm	2nd IF BW = 125 kHz PDF = 132 kHz, AFC off, IFATT=0	■
D7.4	Data Rate 50 kBit/s; Δf = 50 kHz	$SFSK4_{BER}$		-105	-102	dBm	2nd IF BW = 300 kHz PDF = 239 kHz, AFC off, IFATT=0	■
D7.5	Data Rate 2 kBit/s; Δf = 10 kHz	$SFSK5_{BER}$		-110	-107	dBm	2nd IF BW = 300 kHz PDF = 282 kHz, IFATT=7 Note: 3dB sensitivity loss @ f_{offset}=+/-90kHz @ AFC on	■
D7.6	Data Rate 10 kBit/s; Δf = 14 kHz	$SFSK6_{BER}$		-106	-103	dBm	2nd IF BW = 300 kHz PDF = 282 kHz, IFATT=7 Note: 3dB sensitivity loss @ f_{offset}=+/-90kHz @ AFC on	■
D7.7	Data Rate 10 kBit/s; Δf = 50 kHz	$SFSK7_{BER}$		-110	-107	dBm	2nd IF BW = 300 kHz PDF = 282 kHz, IFATT=7 Note: 3dB sensitivity loss @ f_{offset}=+/-90kHz @ AFC on	■

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks	
			min.	typ.	max.			
D8	BER Sensitivity (OOK)						BER = $2*10^{-3}$ RF input matched to 50 Ω @ T_{amb} = 25 °C, peak power level (see **Chapter 2.7.3**); Single-Ended Matching without SAW; Insertion loss of input matching network = 1dB; Receive Mode = TMMF (sampled with ideal data clock); Double Down Conversion	
		Manchester coding; for additional test conditions see right after this table						
D8.1	Data Rate 0.5 kBit/s	$SASK1_{BER}$		-120	-117	dBm peak	m = 100%, IFATT=0 2nd IF BW = 50 kHz	■
D8.2	Data Rate 2 kBit/s	$SASK2_{BER}$		-116	-113	dBm peak	m = 100%, IFATT=0 2nd IF BW = 50 kHz	■
D8.3	Data Rate 10 kBit/s	$SASK3_{BER}$		-111	-108	dBm peak	m = 100%, IFATT=0 2nd IF BW = 50 kHz	■
D8.4	Data Rate 16 kBit/s	$SASK4_{BER}$		-109	-106	dBm peak	m = 100%, IFATT=0 2nd IF BW = 80 kHz	■
D8.5	Data Rate 0.5 kBit/s	$SASK5_{BER}$		-115	-112	dBm peak	m = 100%, IFATT=7 2nd IF BW = 300 kHz; Note: 3dB sensitivity loss @ f_{offset} = +/-100 kHz	■
D8.6	Data Rate 2 kBit/s	$SASK6_{BER}$		-112	-109	dBm peak	m = 100%, IFATT=7 2nd IF BW = 300 kHz; Note: 3dB sensitivity loss @ f_{offset} = +/-100 kHz	■
D8.7	Data Rate 10 kBit/s	$SASK7_{BER}$		-106	-103	dBm peak	m = 100%, IFATT=7 2nd IF BW = 300 kHz; Note: 3dB sensitivity loss @ f_{offset} = +/-100 kHz	■
D8.8	Data Rate 16 kBit/s	$SASK8_{BER}$		-104	-101	dBm peak	m = 100%, IFATT=7 2nd IF BW = 300 kHz; Note: 3dB sensitivity loss @ f_{offset} = +/-100 kHz	■
D9.1	Sensitivity increase for Single Down Conversion mode	ΔS_{SDC}	0	0.5	1	dB		■
D9.2	Double Down Conversion sensitivity decrease for higher blocking performance (IFATT=0 => IFATT=7)	$\Delta S_{DDC, IFATT7}$		1	2	dB		■

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks	
			min.	typ.	max.			
D9.3	Single Down Conversion sensitivity decrease for higher blocking performance (IFATT=4 => IFATT=7)	$\Delta S_{SDC, IFATT7}$		0.5	1	dB		■
D10.1	Sensitivity variation due to temperature (-40...+105°C)	ΔP_{in}			2	dB	relative to T_{amb} = 25 °C; temperature drift of crystal not considered	■
D10.2	Sensitivity variation due to frequency offset [1)]	ΔP_{in}			3	dB	AFC inactive; For Sensitivity Bandwidth see **Table 11**	■
D10.3	Sensitivity variation due to frequency offset	ΔP_{in}			3	dB	AFC active, slow AFC; For Sensitivity Bandwidth see **Table 11** and applied AFCLIMIT	■
D10.4	Sensitivity loss when AFC active at center frequency	ΔP_{in}			1	dB	AFC active; center frequency - no AFC wander (see **Chapter 2.4.6.3**)	■
D11	3rd order intercept IIP3	P_{IIP3}	-16	-14		dBm	input matched to 50 Ω; Insertion loss of input matching network = 1dB; IFATT = 7; valid for Single and Double Down Conversion Mode	■
D12	1 dB compression point CP1dB	P_{CP1dB}	-27	-25		dBm	input matched to 50 Ω; Insertion loss of input matching network = 1dB; IFATT = 7; valid for Single and Double Down Conversion Mode	■
D13	1st IF image rejection	d_{image1}	30	40		dB	1st IF = 10.7 MHz without front end SAW filter; valid for Double Down Conversion Mode	
D14	2nd IF image rejection	d_{image2}	30	34		dB	2nd IF = 274 kHz without 1st IF CER filter; valid for Single and Double Down Conversion Mode	

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks	
			min.	typ.	max.			
RF Front End Characteristics (Unless otherwise noted, all values apply for the specified frequency ranges)								
E1	LNA input impedance							
E1.1	f_{RF} = 315 MHz	$R_{in\_p,diff}$		680		Ω	differential parallel equivalent input between LNA_INP and LNA_INN	■
		$C_{in\_p,diff}$		1.05		pF		■
E1.2	f_{RF} = 434MHz	$R_{in\_p,diff}$		570		Ω		■
		$C_{in\_p,diff}$		0.87		pF		■
E1.3	f_{RF} = 868MHz	$R_{in\_p,diff}$		550		Ω		■
		$C_{in\_p,diff}$		0.63		pF		■
E1.4	f_{RF} = 915MHz	$R_{in\_p,diff}$		540		Ω		■
		$C_{in\_p,diff}$		0.63		pF		■
E1.5	f_{RF} = 315 MHz	$R_{in\_p,\ SE}$		500		Ω	single-ended parallel equivalent input between LNA_INP and GNDRF / LNA_INN and GNDRF	■
		$C_{in\_p,\ SE}$		1.87		pF		■
E1.6	f_{RF} = 434MHz	$R_{in\_p,\ SE}$		400		Ω		■
		$C_{in\_p,\ SE}$		1.63		pF		■
E1.7	f_{RF} = 868MHz	$R_{in\_p,\ SE}$		322		Ω		■
		$C_{in\_p,\ SE}$		1.59		pF		■
E1.8	f_{RF} = 915MHz	$R_{in\_p,\ SE}$		312		Ω		■
		$C_{in\_p,\ SE}$		1.56		pF		■
E2	FE output impedance	R_{out_IF}	290	330	380	Ω	f_{IF} = 10.7 MHz	■
E3	FE voltage conversion gain	$AV_{FE,\ max}$	34	36	38	dB	min. IF attenuation (IFATT = 0); input matched to 50 Ω; Insertion loss of input matching network = 1dB R_{load_IF} = 330 Ω; tested at 434 MHz	
E4	FE voltage conversion gain	AV_{FE_7}	29	31	33	dB	IF attenuation (IFATT = 7); input matched to 50 Ω; Insertion loss of input matching network = 1dB R_{load_IF} = 330 Ω; tested at 434 MHz	

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks	
			min.	typ.	max.			
E5	FE voltage conversion gain	$AV_{FE, min}$	22	24	26	dB	max. IF attenuation (IFATT = 15); input matched to 50 Ω; Insertion loss of input matching network = 1dB R_{load_IF} = 330 Ω; tested at 434 MHz	
E6	FE voltage conversion gain step			0.8		dB	12dB / 15 = 0.8dB/step Double Down Conversion: 16 gain settings (4 bit) Single Down Conversion: 7 gain settings	■
E7	1^{st} Local Oscillator SSB Noise						closed loop	
E7.1	PLL loop Bandwidth	BW	100	150	200	kHz	BW and its tolerances	■
E7.2	f_{in_R1} = 315MHz	d_{SSB_LO}		-81	-76	dBc/Hz	@ f_{offset} = 1 kHz	■
				-85	-80		@ f_{offset} = 10 kHz	■
				-82	-77		@ f_{offset} = 100 kHz	■
				-120	-115		@ f_{offset} = 1 MHz	■
				-130	-125		@ f_{offset} => 10 MHz	■
E7.3	f_{in_R2} = 434MHz	d_{SSB_LO}		-78	-73	dBc/Hz	@ f_{offset} = 1 kHz	■
				-83	-78		@ f_{offset} = 10 kHz	■
				-82	-77		@ f_{offset} = 100 kHz	■
				-117	-112		@ f_{offset} = 1 MHz	■
				-130	-125		@ f_{offset} => 10 MHz	■
E7.4	f_{in_R3} = 868MHz	d_{SSB_LO}		-75	-70	dBc/Hz	@ f_{offset} = 1 kHz	■
				-79	-74		@ f_{offset} = 10 kHz	■
				-77	-72		@ f_{offset} = 100 kHz	■
				-114	-109		@ f_{offset} = 1 MHz	■
				-130	-125		@ f_{offset} => 10 MHz	■
E7.5	f_{in_R4} = 915MHz	d_{SSB_LO}		-71	-66	dBc/Hz	@ f_{offset} = 1 kHz	■
				-79	-74		@ f_{offset} = 10 kHz	■
				-77	-72		@ f_{offset} = 100 kHz	■
				-116	-111		@ f_{offset} = 1 MHz	■
				-130	-125		@ f_{offset} => 10 MHz	■
E8.1	Spurious emission < 1 GHz				-57	dBm		■
E8.2	Spurious emission > 1 GHz				-47	dBm		■

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks	
			min.	typ.	max.			
E9	Inband fractional spur		-40			dBc		■
E10	3dB Overall Analog Frontend Bandwidth	BW_{ANA}		230		kHz	LNA input to Limiter output, excluding external CER filter	■
1st IF Buffer Characteristics								
F1	Input impedance	R_{in_IF}	290	330	370	Ω	f_{IF} = 10...12 MHz	■
F2	Output impedance	R_{out_IF}	290	330	370	Ω	f_{IF} = 10...12 MHz	■
F3	Voltage gain	AV_{Buffer}	3	4	5	dB	f_{IF} = 10...12 MHz Z_{source} = 330 Ω Z_{load} = 330 Ω	
F4	Buffer switch isolation (CERFSEL)	$d_{isolation}$	60			dB	f_{IF} = 10...12 MHz see **Figure 6**	■
2nd IF Mixer, RSSI and Filter Characteristics								
G1	Mixer input impedance	R_{in_IF}	290	330	390	Ω	f_{IF} = 10...12 MHz	■
G2	RSSI						Related to RF input matched to 50 Ω	
G2.1	Dynamic range (Linearity +/- 2 dB)	DR_{RSSI}	-110		-30	dBm	applies for digital RSSI; AGC on	■
			-115		-60	dBm	applies for analog RSSI @ 50kHz BPF, AGC off	■
			-110		-50	dBm	applies for analog RSSI @ 300kHz BPF, AGC off	■
G2.2	Linearity	DR_{LIN}	-1		+1	dB	-95 dBm...-35 dBm; applies for digital RSSI	■
G2.3	Temperature drift within linear dynamic range	DR_{TEMP}	-2.5		+1.5	dB	-95 dBm...-35 dBm; applies for digital RSSI	■
G2.4	Output dynamic range	V_{RSSI+}	0.8		2.0	V		
G2.5	analog RSSI error, untrimmed	$DRSSI_{ana}$	-4		+2	dB	at RSSI pin	
G2.6	analog RSSI slope, untrimmed	dV_{RSSI}/ dV_{mix_in}	8	10	12	mV/dB	at RSSI pin; typical 600 mV/60 dB = 10 mV/dB	
G2.7	digital RSSI error, untrimmed	$DRSSI_{dig\_u}$	-4		+2	dB	RSSI register readout	

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks	
			min.	typ.	max.			
G2.8	digital RSSI error, user trimmed via SFRs RSSISLOPE and RSSIOFFS	$DRSSI_{dig\_t}$	-1		+1	dB	RSSI register readout	■
G2.9	digital RSSI slope, untrimmed	dV_{RSSI}/dV_{mix_in}	2	2.5	3	LSB /dB	RSSI register readout; typical 600 mV/60 dB = 10 mV/dB, 1mV = 1 LSB (10-bit ADC) 8-bit readout: 4mV=1LSB	
G2.10	digital RSSI slope, user trimmed via SFRs RSSISLOPE and RSSIOFFS	dV_{RSSI}/dV_{mix_in}	2.35	2.5	2.65	LSB /dB	RSSI register readout; typical 600 mV/60 dB = 10 mV/dB, 1mV = 1 LSB (10-bit ADC) 8-bit readout: 4mV=1LSB	■
G2.11	Resistive load at RSSI pin	$R_{L,RSSImax}$	100			kΩ		■
G2.12	Capacitive load at RSSI pin	$C_{L,RSSI}$			20	pF		■
G3	2nd IF Filter (3rd order Bandpass Filter)							
G3.1	Center frequency	f_{center}	262	274	288	kHz	Asymmetric BPF corners: f_center=sqrt(f_{low} * f_{high}); Use AFC for more symmetry	
G3.2	-3 dB BW	BW_{-3dB}		50 80 125 200 300		kHz		■
G3.3	-3 dB BW tolerance	tol_BW_{-3dB}	-5		+5	%	For BW = 125, 200, 300 kHz	■
G3.4	-3 dB BW tolerance	tol_BW_{-3dB}	-6		+6	%	For BW = 50, 80 kHz	■

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks	
			min.	typ.	max.			
Crystal Oscillator Characteristics								
H1	Frequency range	f_{XTAL}		21.948 717		MHz		
H2	Crystal parameters							
H2.1	Motional capacitance	C_1	3	6	10	fF		■
H2.2	Motional resistance	R_1		18	80	Ω		■
H2.3	Shunt capacitance	C_0		2	4	pF		■
H2.4	Load capacitance	C_{Load}		12		pF	nominal value	■
H2.5	Initial frequency tolerance	f_{XTAL_Tol}	-30		+30	ppm	oscillator untrimmed (trim capacitor default settings, usage of recommended crystal); not including crystal tolerances	■
H2.6	Frequency trimming range	Δf_{XTAL}	-50		+50	ppm	larger trimming range possible via SD PLL	
H2.7	Trimming step	Δf_{X_step}		1	4	ppm	see also step size of SD PLL	■
H3	Clock output frequency at PPx pin	f_{clock_out}	11		5.5M	Hz	10pF load	
H4	Crystal oscillator settling time (switching from Low Power to High Precision Mode)	$t_{COSCsettle}$	292	292	292	µs		■
H5	Start up time	t_{start_up}		0.45	1	ms	crystal type: NDK NX5032SD; See also BOM for ext. load caps; Note: No SPI communication is allowed before XOSC start-up is finished and chip reset is already finished	

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks	
			min.	typ.	max.			
Digital Inputs/Outputs Characteristics								
I1	High level input voltage	V_{In_High}	0.7* VDDD		VDD5V +0.1	V		
I2	High level input leakage current	I_{In_High}			5	µA		
I3	Low level input voltage (except P_ON pin)	V_{In_Low}	0		0.8	V		
I4	Low level input voltage (at P_ON pin)	$V_{In\_Low\_PON}$	0		0.5	V		
I5	Low level input leakage current	I_{In_Low}	-5			µA		
I6	High level output voltage 1	V_{Out_High1}	VDD5V -0.4		VDD5V	V	IOH=-500 µA, static driver capability; Normal Pad Mode (see register PPCFG2 and CMC0)	
I7	Low level output voltage 1	V_{Out_Low1}	0		0.4	V	IOL=500 µA, static driver capability; Normal Pad Mode (see register PPCFG2 and CMC0)	
I8	High level output voltage 2	V_{Out_High2}	VDD5V -0.8		VDD5V	V	IOH=-4 mA, static driver capability; High Power Pad Mode (see register PPCFG2 and CMC0)	
I9	Low level output voltage 2	V_{Out_Low2}	0		0.8	V	IOL=4 mA, static driver capability; High Power Pad Mode (see register PPCFG2 and CMC0)	

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks	
			min.	typ.	max.			
Timing SPI-Bus Characteristics								
J1	Clock frequency	f_{clock}			2.2	MHz	Note: A high SPI clock rate during data reception can reduce sensitivity	
J2	Clock High time	t_{CLK_H}	200			ns		■
J3	Clock Low time	t_{CLK_L}	200			ns		■
J4	Active setup time	t_{setup}	200			ns		■
J5	Not active setup time	t_{not_setup}	200			ns		■
J6	Active hold time	t_{hold}	200			ns		■
J7	Not active hold time	t_{not_hold}	200			ns		■
J8	Deselect time	$t_{Deselect}$	200			ns		■
J9	SDI setup time	t_{SDI_setup}	100			ns		■
J10	SDI hold time	t_{SDI_hold}	100			ns		■
J11	Clock low to SDO valid	t_{CLK_SDO}			145	ns	@ C_{load} = 80 pF High Power Pad not enabled (Normal Mode) (see register PPCFG2 and CMC0)	■
J12	Clock low to SDO valid	t_{CLK_SDO}			40	ns	@ C_{load} = 10 pF High Power Pad not enabled (Normal Mode) (see register PPCFG2 and CMC0)	
J13	SDO rise time	t_{SDO_r}			90	ns	@ C_{load} = 80 pF	■
J14	SDO fall time	t_{SDO_f}			90	ns	@ C_{load} = 80 pF	■
J15	SDO rise time	t_{SDO_r}			15	ns	@ C_{load} = 10 pF	■
J16	SDO fall time	t_{SDO_f}			15	ns	@ C_{load} = 10 pF	■
J17	SDO disable time	$t_{SDO\_disable}$			25	ns		■

1) Please note that the system bandwidth is smaller than the smallest bandwidth in the signal path.

Unless explicitly otherwise noted, the following test conditions apply to the given specification values in Table 10 and items D7 and D8:

* Hardware: TDA5240 Platform Testboard V1.0
* Single-Ended Matching for 315.0 MHz / 433.92 MHz / 868.3 MHz / 915.0 MHz
* RF input matched to 50 Ω; Insertion loss of input matching network = 1dB
* Receive Frequency 315.0 MHz / 433.92 MHz / 868.3 MHz / 915.0 MHz; Lo-Side LO-Injection
* Reference Clock: XTAL=21.948717 MHz

* IF-Gain: Attenuation set to default value (IFATT = 7)
* Double Down Conversion
* 1 IF-Filter: Center=10.7MHz; BW=330kHz; Connected between IF_OUT and IFBUF_IN
* 2nd IF Filter BW: Depending on Data Rate and FSK Deviation
* Received Signal at zero Offset to IF Center Frequency
* RSSI trimmed
* FSK Pre-Demodulation Filter (PDF) BW: Depending on Data Rate and FSK Deviation
* No SPI-traffic during telegram reception, CLK_OUT disabled
* AFC and AGC are OFF, unless otherwise noted
* Specification values are in respect to Manchester-coded Infineon-Reference Pattern 1
  (7 Bits '0', 1 Bit '1', 1 Bits '0', 1 Bit '1', 1 Bits '0', 1 Bit '1', PRBS5 (31 Bit), 1 Bit 'M') according to **Figure 18**
  However a Code Violation is not used as EOM criterion

BER sensitivity measurements use Receive Mode TMMF (sampled with ideal data clock)
MER sensitivity measurements use Receive Mode POF

* DRE ... Data Date Error of received telegram vs. adjusted Data Rate
* DC ... Duty Cycle
* MER ... Message Error Rate
  [MER = 1 - (number_of_correctly_received_messages / number_of_transmitted messages)]
* FAR ... False Alarm Rate
  [FAR = number_of_mistakenly_wake_ups / number_of_periods_searching_for_data_on_channel]
* MMR ... Missed Message Rate
  [MMR = number_of_mistakenly_missed_wake_up_patterns /
  number_of_periods_with_wake_up_pattern_transmitted_and_searching_for_wake_up_pattern]
* BER ... Bit Error Rate (using a PRBS9 Pseudo-Random Binary Sequence)
  [BER = 1 - (number_of_correctly_received_bits / number_of_transmitted bits)]

Table 10 MER Characteristics (Receive Mode = POF)

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks	
			min.	typ.	max.			
Characteristics of Digital Data Filter and Data Clock Recovery Acceptance Criterion is: MER <= 10%. For additional test conditions see right before this table. Double Down Conversion Mode								
K1	Data Rate Error of received Telegram Sensitivity loss < 1dB	Db	-10		10	%	at DC = 50%	■
K2	Duty Cycle Error of Manchester coding of received Telegram							
K2.1	Sensitivity loss < 1dB	tolManch_DefB	45		55	%	According to Definition B in **Chapter 2.7.2**; including DRE of -10% to +10%; Data Rate < 50 kBit/s	■
K2.2	Sensitivity loss < 3.5dB	tolManch_DefC	35		55	%	According to Definition C in **Chapter 2.7.2** including DRE of -10% to +10%; Data Rate < 10 kBit/s	■
K2.3	Sensitivity loss < 1.5dB	tolManch_DefB	45		55	%	According to Definition B in **Chapter 2.7.2**; including DRE of -10% to +10%; Data Rate >= 50 kBit/s	■
K2.4	Sensitivity loss < 4dB	tolManch_DefC	35		55	%	According to Definition C in **Chapter 2.7.2** including DRE of -10% to +10%; Data Rate >= 10 kBit/s; Note: If BPF_BW / Bitrate < 12, the selected data rate in the configuration tool needs to be set 5% higher.	■

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks	
			min.	typ.	max.			
Sensitivity of Receiver Acceptance Criterion is: MER <= 10%. For additional test conditions see right before this table. Double Down Conversion Mode								
L1	Sensitivity Limit in ASK (OOK) Mode; Manchester coding						At DC = 50% and DRE = 0%. T_{amb} = 25 °C, peak power level (see **Chapter 2.7.3**)	
L1.1	Data Rate 0.5 kBit/s	SASK1		-120	-117	dBm peak	m = 100% 2nd IF BW = 50 kHz; IFATT = 0, CDR = normal; Data Slicer Bit Mode; 868/915MHz: <=1dB loss	■
L1.2	Data Rate 2 kBit/s	SASK2		-116	-113	dBm peak	m = 100% 2nd IF BW = 50 kHz; IFATT = 0, CDR = normal; Data Slicer Bit Mode	■
L1.3	Data Rate 10 kBit/s	SASK3		-111	-108	dBm peak	m = 100% 2nd IF BW = 50 kHz; IFATT = 0, CDR = normal; Data Slicer Bit Mode	■
L1.4	Data Rate 16 kBit/s	SASK4		-109	-106	dBm peak	m = 100% 2nd IF BW = 80 kHz; IFATT = 0, CDR = normal; Data Slicer Bit Mode; 868/915MHz: <=1dB loss	■
L1.5	Data Rate 0.5 kBit/s	SASK5		-115	-112	dBm peak	m = 100% 2nd IF BW = 300 kHz; IFATT = 7, CDR = fast; Data Slicer Bit Mode; Note: 3dB sensitivity loss @ f_{offset} = +/-100 kHz	■
L1.6	Data Rate 2 kBit/s	SASK6		-112	-109	dBm peak	m = 100% 2nd IF BW = 300 kHz; IFATT = 7, CDR = fast; Data Slicer Bit Mode; 868/915MHz: <=1dB loss; Note: 3dB sensitivity loss @ f_{offset} = +/-100 kHz	■
L1.7	Data Rate 10 kBit/s	SASK7		-106	-103	dBm peak	m = 100% 2nd IF BW = 300 kHz; IFATT = 7, CDR = fast; Data Slicer Bit Mode; Note: 3dB sensitivity loss @ f_{offset} = +/-100 kHz	■

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks	
			min.	typ.	max.			
L1.8	Data Rate 16 kBit/s	SASK8		-104	-101	dBm peak	m = 100% 2nd IF BW = 300 kHz; IFATT = 7, CDR = fast; Data Slicer Bit Mode; Note: 3dB sensitivity loss @ f_{offset} = +/-100 kHz	■
L2	Sensitivity Limit in FSK Mode; Manchester coding						At DC = 50% and DRE = 0%. T_{amb} = 25 °C	
L2.1	Data Rate 2 kBit/s; Δf = 10 kHz	SFSK1		-118	-115	dBm	2nd IF BW = 50 kHz; PDF = 33 kHz, AFC off; IFATT = 0, CDR = normal; Data Slicer Bit Mode	■
L2.2	Data Rate 10 kBit/s; Δf = 14 kHz	SFSK2		-113	-110	dBm	2nd IF BW = 50 kHz; PDF = 65 kHz, AFC off; IFATT = 0, CDR = normal; Data Slicer Bit Mode	■
L2.3	Data Rate 10 kBit/s; Δf = 50 kHz	SFSK3		-112	-109	dBm	2nd IF BW = 125 kHz; PDF = 132 kHz, AFC off; IFATT = 0, CDR = normal; Data Slicer Bit Mode; 868/915MHz: <=1dB loss	■
L2.4	Data Rate 50 kBit/s; Δf = 50 kHz	SFSK4		-106	-103	dBm	2nd IF BW = 300 kHz; PDF = 239 kHz, AFC off; IFATT = 0, CDR = normal; Data Slicer Bit Mode	■
L2.5	Data Rate 2 kBit/s; Δf = 10 kHz	SFSK5		-108	-105	dBm	2nd IF BW = 300 kHz; PDF = 282 kHz; IFATT = 7, CDR = fast; Data Slicer Bit Mode; 868/915MHz: <=1dB loss; Note: 3dB sensitivity loss @ f_{offset}=+/-90kHz @ AFC on	■
L2.6	Data Rate 10 kBit/s; Δf = 14 kHz	SFSK6		-107	-104	dBm	2nd IF BW = 300 kHz; PDF = 282 kHz; IFATT = 7, CDR = fast; Data Slicer Bit Mode; Note: 3dB sensitivity loss @ f_{offset}=+/-90kHz @ AFC on	■
L2.7	Data Rate 10 kBit/s; Δf = 50 kHz	SFSK7		-109	-106	dBm	2nd IF BW = 300 kHz; PDF = 282 kHz; IFATT = 7, CDR = fast; Data Slicer Bit Mode; Note: 3dB sensitivity loss @ f_{offset}=+/-90kHz @ AFC on	■

#	Parameter	Symbol	Limit Values			Unit	Test Conditions Remarks	
			min.	typ.	max.			
Dynamic Range of Receiver Acceptance Criteria are: MER <= 1E-3, FAR < 1E-5, MMR < 1E-4 (Criterion: 8 Equal Bits), Manchester coding. For additional test conditions see right before this table. Double Down Conversion Mode								
M1	Dynamic Range in ASK (OOK) Mode, AGC on						At DC = 50% and DRE = 0%. T_{amb} = 25 °C, peak power level (see Chapter 2.7.3)	
M1.1	Data Rate 2 kBit/s	DR2,OOK	-10		-109	dBm peak	m = 100% 2nd IF BW = 50 kHz; IFATT = 0, CDR = normal; Data Slicer Bit Mode	■
M1.2	Data Rate 10 kBit/s	DR10,OOK	-10		-105	dBm peak	m = 100% 2nd IF BW = 50 kHz; IFATT = 0, CDR = normal; Data Slicer Bit Mode	■
M1.3	Data Rate 2 kBit/s	DR2,ASK50	-45		-103	dBm peak	m = 50% 2nd IF BW = 50 kHz; IFATT = 0, CDR = normal; Data Slicer Bit Mode	■
M1.4	Data Rate 10 kBit/s	DR10,ASK50	-60		-99	dBm peak	m = 50% 2nd IF BW = 50 kHz; IFATT = 0, CDR = normal; Data Slicer Bit Mode	■
M2	Dynamic Range in FSK Mode, AGC on Data Rate 10 kBit/s & Δf = 50 kHz						At DC = 50% and DRE = 0%. T_{amb} = 25 °C	
M2.1	0% AM Modulation	DR10,AM0	-10		-106	dBm	2nd IF BW = 125 kHz PDF = 132 kHz; IFATT = 0, CDR = normal; Data Slicer Bit Mode	■
M2.2	90% AM Modulation, 100 Hz	DR10,AM90	-10		-90	dBm	2nd IF BW = 125 kHz PDF = 132 kHz; IFATT = 0, CDR = normal; Data Slicer Bit Mode	■

Table 11 Typical Achievable Sensitivity Bandwidth [kHz]

Ceramic Filter BW = 330 kHz

Table is valid for DDC (Double Down Conversion) and SDC (Single Down Conversion)

Valid for AFC=off; For FSK & AFC=on the BW can be increased by 2*AFCLIMIT, where AFCLIMIT < 43 kHz

BPF/PDF Filter [Hz]	Modulation	FSK Deviation [+/- Hz]	Sensitivity Loss	Data Rate [bit/s], Manchester					
				0.5 k	1 k	5	10 k	20 k	50 k
BPF = 300 k PDF = 282 k	ASK	-	3 dB	230	230	230	230	230	-
			6 dB	280	280	280	280	280	-
	FSK	0.5 k	3 dB	160	150	-	-	-	-
			6 dB	230	220	-	-	-	-
		1 k	3 dB	140	160	-	-	-	-
			6 dB	220	230	-	-	-	-
		5 k	3 dB	120	130	150	140	-	-
			6 dB	200	210	220	220	-	-
		10 k	3 dB	120	120	140	140	150	-
			6 dB	180	190	210	210	210	-
		15 k	3 dB	-	-	130	140	150	-
			6 dB	-	-	200	200	210	-
		20 k	3 dB	110	-	130	130	140	-
			6 dB	160	-	190	190	190	-
		40 k	3 dB	-	-	-	120	-	-
			6 dB	-	-	-	160	-	-
		50 k	3 dB	110	110	110	110	100	100
			6 dB	140	140	140	140	140	140

Table 11 Typical Achievable Sensitivity Bandwidth [kHz]

Ceramic Filter BW = 330 kHz

Table is valid for DDC (Double Down Conversion) and SDC (Single Down Conversion)

Valid for AFC=off; For FSK & AFC=on the BW can be increased by 2*AFCLIMIT, where AFCLIMIT < 43 kHz

BPF/PDF Filter [Hz]	Modulation	FSK Deviation [+/- Hz]	Sensitivity Loss	Data Rate [bit/s], Manchester					
				0.5 k	1 k	5	10 k	20 k	50 k
BPF = 200 k PDF = 239 k	ASK	-	3 dB	180	180	180	180	180	-
			6 dB	220	220	220	220	220	-
	FSK	0.5 k	3 dB	140	140	-	-	-	-
			6 dB	190	190	-	-	-	-
		1 k	3 dB	130	130	-	-	-	-
			6 dB	180	190	-	-	-	-
		5 k	3 dB	100	120	130	130	-	-
			6 dB	160	170	180	180	-	-
		10 k	3 dB	100	100	120	120	140	-
			6 dB	140	150	170	170	170	-
		15 k	3 dB	-	-	110	110	120	-
			6 dB	-	-	150	150	160	-
		20 k	3 dB	90	-	100	100	110	-
			6 dB	130	-	140	150	150	-
		40 k	3 dB	-	-	-	90	-	-
			6 dB	-	-	-	120	-	-
		50 k	3 dB	-	-	-	-	-	-
			6 dB	-	-	-	-	-	-

Table 11 Typical Achievable Sensitivity Bandwidth [kHz]

Ceramic Filter BW = 330 kHz

Table is valid for DDC (Double Down Conversion) and SDC (Single Down Conversion)

Valid for AFC=off; For FSK & AFC=on the BW can be increased by 2*AFCLIMIT, where AFCLIMIT < 43 kHz

BPF/PDF Filter [Hz]	Modulation	FSK Deviation [+/- Hz]	Sensitivity Loss	Data Rate [bit/s], Manchester					
				0.5 k	1 k	5	10 k	20 k	50 k
BPF = 125 k PDF = 132 k	ASK	-	3 dB	120	120	120	120	120	-
			6 dB	150	150	150	150	150	-
	FSK	0.5 k	3 dB	100	100	-	-	-	-
			6 dB	120	120	-	-	-	-
		1 k	3 dB	90	100	-	-	-	-
			6 dB	120	120	-	-	-	-
		5 k	3 dB	70	80	80	90	-	-
			6 dB	100	110	110	110	-	-
		10 k	3 dB	70	70	80	80	80	-
			6 dB	90	100	100	100	100	-
		15 k	3 dB	-	-	70	80	80	-
			6 dB	-	-	90	90	100	-
		20 k	3 dB	60	-	70	70	70	-
			6 dB	80	-	90	90	90	-
		40 k	3 dB	-	-	-	-	-	-
			6 dB	-	-	-	-	-	-
		50 k	3 dB	-	-	-	-	-	-
			6 dB	-	-	-	-	-	-

4.2 Test Circuit - Evaluation Board v1.0

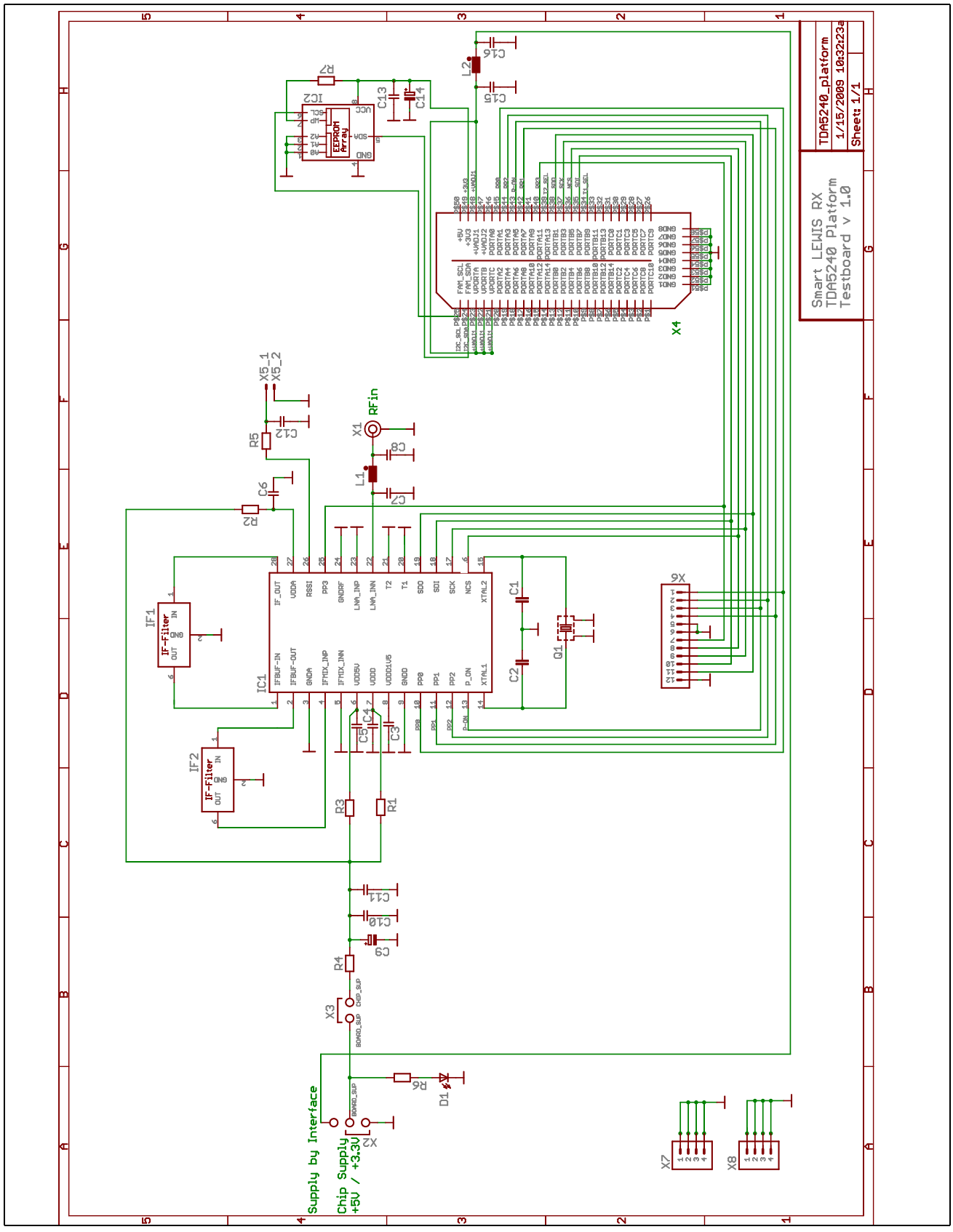


Figure 94 Test Circuit Schematic

4.3 Test Board Layout, Evaluation Board v1.0

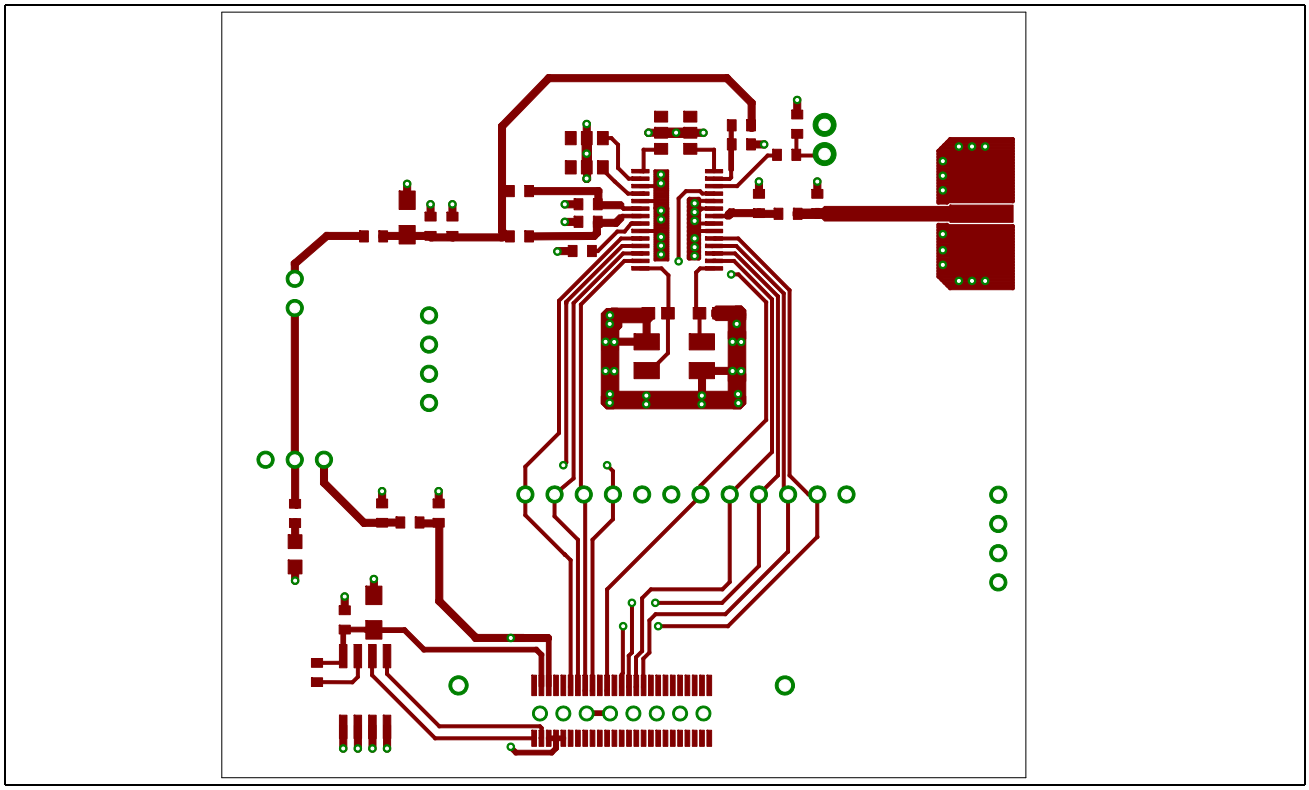


Figure 95 Test Board Layout, Top View

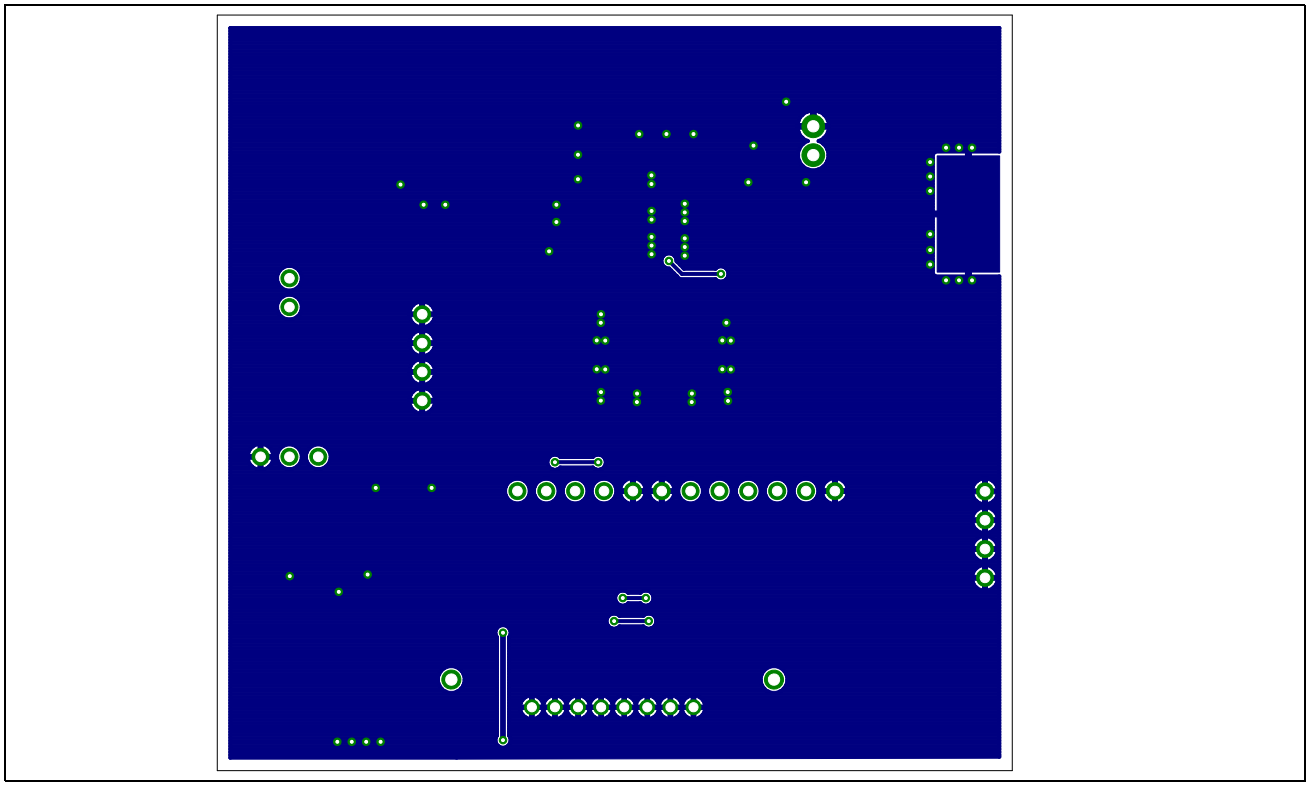


Figure 96 Test Board Layout, Bottom View

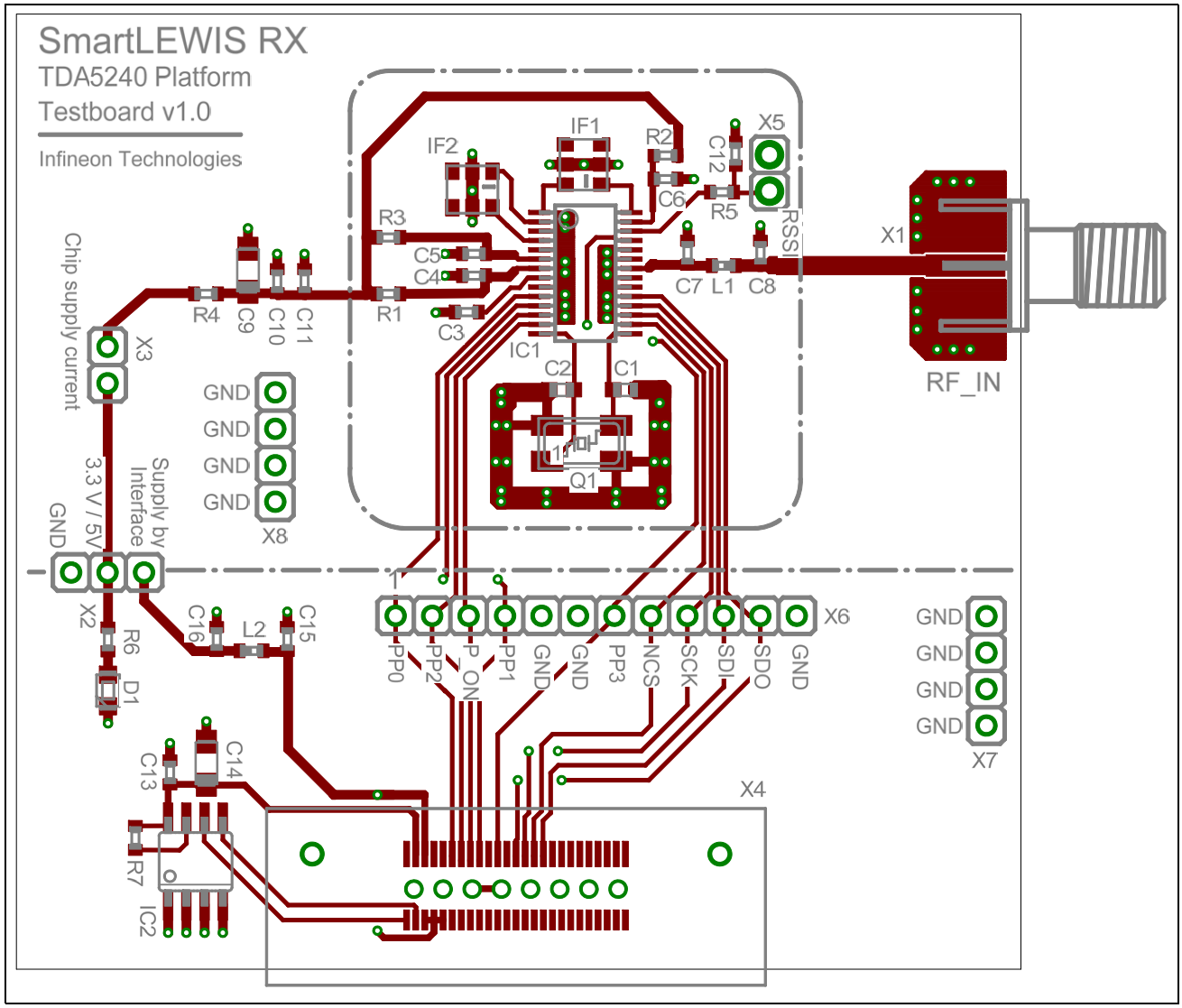


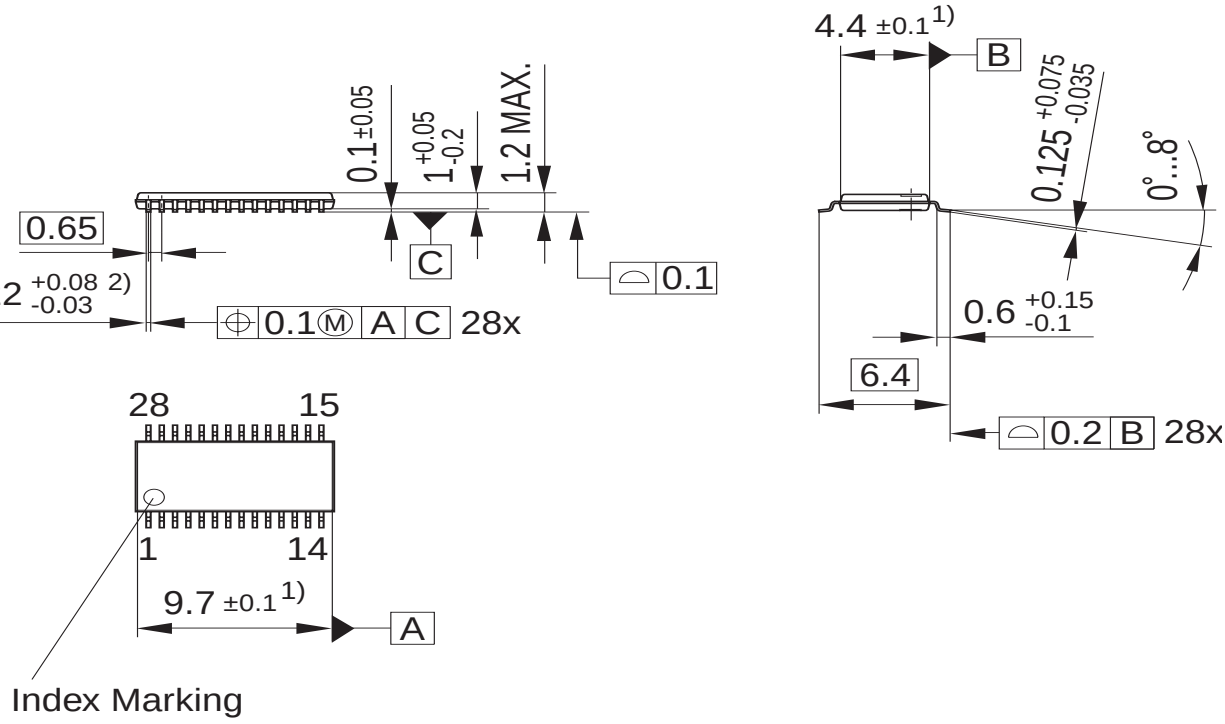
Figure 97 Test Board Layout, Component View

4.4 Bill of Materials

Pos	Part	Value	Package	Device / Type	Tolerance	Manufacturer	Remark/Options (RF+supply variant)
1	IC1	TDA5240	PG-TSSOP-28			Infineon	
2	C1	3.9 pF	0603	C0G	+/- 0.1 pF		crystal oscillator load
3	C2	3.9 pF	0603	C0G	+/- 0.1 pF		crystal oscillator load
4	C3	100 nF	0603	X7R	+/- 10 %		
5	C4	100 nF	0603	X7R	+/- 10 %		
6	C5	100 nF / (1 µF)	0603	X7R / X5R	+/- 10 %		3.3V / (5 V environment)
7	C6	100 nF	0603	X7R	+/- 10 %		
8	C7	1 pF	0603	C0G	+/- 0.1 pF		matching for 315MHz
		0.5 pF	0603	C0G	+/- 0.1 pF		matching for 434MHz
		open	0603	C0G			matching for 868MHz
		1 pF	0603	C0G	+/- 0.1 pF		matching for 915MHz
9	C8	open	0603	C0G			matching for 315MHz
		open	0603	C0G			matching for 434MHz
		2.7 pF	0603	C0G	+/- 0.1 pF		matching for 868MHz
		5.1 pF	0603	C0G	+/- 0.1 pF		matching for 915MHz
10	C9	1 µF	SMC-A	Tantal	+/- 10%		polarized capacitor
11	C10	100 nF	0603	X7R	+/- 10%		
12	C11	10 nF	0603	X7R	+/- 10%		
13	L1	68 nH	0603		+/- 2%		matching for 315MHz
		39 nH	0603		+/- 2%		matching for 434MHz
		22 nH	0603		+/- 2%		matching for 868MHz
		15 nH	0603		+/- 2%		matching for 915MHz
14	R1	10 Ohm / (open)	0603		+/- 5%		3.3 V / (5 V environment)
15	R2	4.7 Ohm / (open)	0603		+/- 5%		3.3 V / (5 V environment)
16	R3	4.7 Ohm / (22 Ohm)	0603		+/- 5%		3.3 V / (5 V environment)
17	R4	0 Ohm	0603				
18	IF1	SFECF10 M7EA00				Murata	BW = 330 kHz
19	Q1	21.948717 MHz	NX5032SD	C0=1.7 pF C1=7 fF CL=12 pF		NDK (Frischer Electronic), EXS00A-CS01580	SMD crystal

Pos	Part	Value	Package	Device / Type	Tolerance	Manufacturer	Remark/Options (RF+supply variant)
Interface / optional							
20	IC2	AT24C32 C-SH-B or AT24C512	SOIC8				EEPROM for board detection
21	C12	open	0603	X7R	+/- 10%		RSSI measurement low pass
22	C13	100 nF	0603	X7R	+/- 10%		
23	C14	1 µF	SMC-A	Tantal	+/- 10%		polarized capacitor
24	C15	10 nF	0603	X7R	+/- 10%		filter network on supply line
25	C16	10 nF	0603	X7R	+/- 10%		filter network on supply line
26	L2	0 Ohm	0603				no filter network on supply line
27	R5	open	0603				RSSI measurement low pass
28	R6	1 kOhm	0603				
29	R7	0 Ohm	0603				write protection for EEPROM
30	D1	LED		LS M676-P251-1			status indication LED
31	IF2	open				Murata	2nd IF filter is optional
32	X1	SMA socket					RF input
33	X2	3 pins					Board supply
34	X3	2 pins					Chip supply current (jumper closed)
35	X4	50 pins	SIB-QTS-025-01-X-D-RA			Samtec	Connector to PC/µC/Interface
36	X5	2 pins					RSSI measuring point
37	X6	12 pins					Interface line measuring point
38	X7	4 pins					GND
39	X8	4 pins					GND
40	Jumper 1	2 pins					Jumper for X3
41	Jumper 2	2 pins					Jumper for X2 - Supply by interface
Board material 1.5mm FR4 with 35µm copper on both sides							

5 Package Outlines



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion

Figure 98 PG-TSSOP-28 Package Outline (green package)

Table 12 Order Information

Type	Ordering Code	Package
TDA5240	SP000550860	PG-TSSOP-28

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”:**http://www.infineon.com/products**

SMD = Surface Mounted Device

Dimensions in mm

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Appendix - Registers Chapter

Appendix - Registers Chapter

Register Overview

Table 1 Register Overview

Register Short Name	Register Long Name	Offset Address	Page Number
Appendix - Registers Chapter, Register Description			
A_MID0	Message ID Register 0	000_H	193
A_MID1	Message ID Register 1	001_H	193
A_MID2	Message ID Register 2	002_H	193
A_MID3	Message ID Register 3	003_H	194
A_MID4	Message ID Register 4	004_H	194
A_MID5	Message ID Register 5	005_H	194
A_MID6	Message ID Register 6	006_H	195
A_MID7	Message ID Register 7	007_H	195
A_MID8	Message ID Register 8	008_H	196
A_MID9	Message ID Register 9	009_H	196
A_MID10	Message ID Register 10	$00A_H$	196
A_MID11	Message ID Register 11	$00B_H$	197
A_MID12	Message ID Register 12	$00C_H$	197
A_MID13	Message ID Register 13	$00D_H$	197
A_MID14	Message ID Register 14	$00E_H$	198
A_MID15	Message ID Register 15	$00F_H$	198
A_MID16	Message ID Register 16	010_H	198
A_MID17	Message ID Register 17	011_H	199
A_MID18	Message ID Register 18	012_H	199
A_MID19	Message ID Register 19	013_H	200
A_MIDC0	Message ID Control Register 0	014_H	200
A_MIDC1	Message ID Control Register 1	015_H	200
A_IF1	IF1 Register	016_H	201
A_WUC	Wake-Up Control Register	017_H	202
A_WUPAT0	Wake-Up Pattern Register 0	018_H	203
A_WUPAT1	Wake-Up Pattern Register 1	019_H	204
A_WUBCNT	Wake-Up Bit or Chip Count Register	$01A_H$	204
A_WURSSITH1	RSSI Wake-Up Threshold for Channel 1 Register	$01B_H$	205
A_WURSSIBL1	RSSI Wake-Up Blocking Level Low Channel 1 Register	$01C_H$	205
A_WURSSIBH1	RSSI Wake-Up Blocking Level High Channel 1 Register	$01D_H$	206
A_WURSSITH2	RSSI Wake-Up Threshold for Channel 2 Register	$01E_H$	206

Table 1 Register Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
A_WURSSIBL2	RSSI Wake-Up Blocking Level Low Channel 2 Register	$01F_H$	207
A_WURSSIBH2	RSSI Wake-Up Blocking Level High Channel 2 Register	020_H	207
A_WURSSITH3	RSSI Wake-Up Threshold for Channel 3 Register	021_H	208
A_WURSSIBL3	RSSI Wake-Up Blocking Level Low Channel 3 Register	022_H	208
A_WURSSIBH3	RSSI Wake-Up Blocking Level High Channel 3 Register	023_H	208
A_SIGDETSAT	Signal Detector Saturation Threshold Register	024_H	209
A_WULOT	Wake-up on Level Observation Time Register	025_H	209
A_SYSRCTO	Synchronization Search Time-Out Register	026_H	210
A_TOTIM_SYNC	SYNC Timeout Timer Register	027_H	210
A_TOTIM_TSI	TSI Timeout Timer Register	028_H	211
A_TOTIM_EOM	EOM Timeout Timer Register	029_H	211
A_AFCLIMIT	AFC Limit Configuration Register	$02A_H$	212
A_AFCAGCD	AFC/AGC Freeze Delay Register	$02B_H$	212
A_AFCSFCFG	AFC Start/Freeze Configuration Register	$02C_H$	213
A_AFCK1CFG0	AFC Integrator 1 Gain Register 0	$02D_H$	214
A_AFCK1CFG1	AFC Integrator 1 Gain Register 1	$02E_H$	214
A_AFCK2CFG0	AFC Integrator 2 Gain Register 0	$02F_H$	215
A_AFCK2CFG1	AFC Integrator 2 Gain Register 1	030_H	215
A_PMFUDSF	Peak Memory Filter Up-Down Factor Register	031_H	215
A_AGCSFCFG	AGC Start/Freeze Configuration Register	032_H	216
A_AGCCFG0	AGC Configuration Register 0	033_H	217
A_AGCCFG1	AGC Configuration Register 1	034_H	218
A_AGCTHR	AGC Threshold Register	035_H	219
A_DIGRXC	Digital Receiver Configuration Register	036_H	219
A_PKBITPOS	RSSI Peak Detector Bit Position Register	037_H	220
A_ISUPFCSEL	Image Supression Fc Selection Register	038_H	221
A_PDECF	Pre Decimation Factor Register	039_H	221
A_PDECSCFSK	Pre Decimation Scaling Register FSK Mode	$03A_H$	222
A_PDECSCASK	Pre Decimation Scaling Register ASK Mode	$03B_H$	222
A_MFC	Matched Filter Control Register	$03C_H$	223
A_SRC	Sampe Rate Converter NCO Tune	$03D_H$	223
A_EXTSLC	Externel Data Slicer Configuration	$03E_H$	223
A_SIGDET0	Signal Detector Threshold Level Register - Run Mode	$03F_H$	224
A_SIGDET1	Signal Detector Threshold Level Register - Wakeup	040_H	224

Table 1 Register Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
A_SIGDETLO	Signal Detector Threshold Low Level Register	041_H	225
A_SIGDETSEL	Signal Detector Range Selection Register	042_H	225
A_SIGDETCFG	Signal Detector Configuration Register	043_H	226
A_NDTHRES	FSK Noise Detector Threshold Register	044_H	227
A_NDCONFIG	FSK Noise Detector Configuration Register	045_H	227
A_CDRP	Clock and Data Recovery P Configuration Register	046_H	228
A_CDRI	Clock and Data Recovery Configuration Register	047_H	229
A_CDRRI	Clock and Data Recovery RUNIN Configuration Register	048_H	230
A_CDRTOLC	CDR DC Chip Tolerance Register	049_H	231
A_CDRTOLB	CDR DC Bit Tolerance Register	$04A_H$	232
A_TVWIN	Timing Violation Window Register	$04B_H$	232
A_SLCCFG	Slicer Configuration Register	$04C_H$	233
A_TSIMODE	TSI Detection Mode Register	$04D_H$	233
A_TSILENA	TSI Length Register A	$04E_H$	234
A_TSILENB	TSI Length Register B	$04F_H$	235
A_TSIGAP	TSI Gap Length Register	050_H	235
A_TSIPTA0	TSI Pattern Data Reference A Register 0	051_H	236
A_TSIPTA1	TSI Pattern Data Reference A Register 1	052_H	236
A_TSIPTB0	TSI Pattern Data Reference B Register 0	053_H	237
A_TSIPTB1	TSI Pattern Data Reference B Register 1	054_H	237
A_EOMC	End Of Message Control Register	055_H	237
A_EOMDLEN	EOM Data Length Limit Register	056_H	238
A_EOMDLENP	EOM Data Length Limit Parallel Mode Register	057_H	238
A_CHCFG	Channel Configuration Register	058_H	239
A_PLLINTC1	PLL MMD Integer Value Register Channel 1	059_H	240
A_PLLFRAC0C1	PLL Fractional Division Ratio Register 0 Channel 1	$05A_H$	241
A_PLLFRAC1C1	PLL Fractional Division Ratio Register 1 Channel 1	$05B_H$	241
A_PLLFRAC2C1	PLL Fractional Division Ratio Register 2 Channel 1	$05C_H$	242
A_PLLINTC2	PLL MMD Integer Value Register Channel 2	$05D_H$	242
A_PLLFRAC0C2	PLL Fractional Division Ratio Register 0 Channel 2	$05E_H$	243
A_PLLFRAC1C2	PLL Fractional Division Ratio Register 1 Channel 2	$05F_H$	243
A_PLLFRAC2C2	PLL Fractional Division Ratio Register 2 Channel 2	060_H	244
A_PLLINTC3	PLL MMD Integer Value Register Channel 3	061_H	244
A_PLLFRAC0C3	PLL Fractional Division Ratio Register 0 Channel 3	062_H	244
A_PLLFRAC1C3	PLL Fractional Division Ratio Register 1 Channel 3	063_H	245
A_PLLFRAC2C3	PLL Fractional Division Ratio Register 2 Channel 3	064_H	245
SFRPAGE	Special Function Register Page Register	080_H	246

Table 1 Register Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
PPCFG0	PP0 and PP1 Configuration Register	081_H	246
PPCFG1	PP2 and PP3 Configuration Register	082_H	247
PPCFG2	PPx Port Configuration Register	083_H	249
RXRUNCFG0	RX RUN Configuration Register 0	084_H	250
RXRUNCFG1	RX RUN Configuration Register 1	085_H	251
CLKOUT0	Clock Divider Register 0	086_H	252
CLKOUT1	Clock Divider Register 1	087_H	252
CLKOUT2	Clock Divider Register 2	088_H	252
RFC	RF Control Register	089_H	253
BPFCALCFG0	BPF Calibration Configuration Register 0	$08A_H$	254
BPFCALCFG1	BPF Calibration Configuration Register 1	$08B_H$	254
XTALCAL0	XTAL Coarse Calibration Register	$08C_H$	255
XTALCAL1	XTAL Fine Calibration Register	$08D_H$	255
RSSIMONC	RSSI Monitor Configuration Register	$08E_H$	256
ADCINSEL	ADC Input Selection Register	$08F_H$	257
RSSIOFFS	RSSI Offset Register	090_H	257
RSSISLOPE	RSSI Slope Register	091_H	257
CDRDRTHRP	CDR Data Rate Acceptance Positive Threshold Register	092_H	258
CDRDRTHRN	CDR Data Rate Acceptance Negative Threshold Register	093_H	258
IM0	Interrupt Mask Register 0	094_H	259
IM1	Interrupt Mask Register 1	095_H	260
SPMAP	Self Polling Mode Active Periods Register	096_H	261
SPMIP	Self Polling Mode Idle Periods Register	097_H	261
SPMC	Self Polling Mode Control Register	098_H	262
SPMRT	Self Polling Mode Reference Timer Register	099_H	262
SPMOFFT0	Self Polling Mode Off Time Register 0	$09A_H$	263
SPMOFFT1	Self Polling Mode Off Time Register 1	$09B_H$	263
SPMONTA0	Self Polling Mode On Time Config A Register 0	$09C_H$	264
SPMONTA1	Self Polling Mode On Time Config A Register 1	$09D_H$	264
SPMONTB0	Self Polling Mode On Time Config B Register 0	$09E_H$	265
SPMONTB1	Self Polling Mode On Time Config B Register 1	$09F_H$	265
SPMONTC0	Self Polling Mode On Time Config C Register 0	$0A0_H$	266
SPMONTC1	Self Polling Mode On Time Config C Register 1	$0A1_H$	266
SPMONTD0	Self Polling Mode On Time Config D Register 0	$0A2_H$	267
SPMONTD1	Self Polling Mode On Time Config D Register 1	$0A3_H$	267
EXTPCMD	External Processing Command Register	$0A4_H$	268
CMC1	Chip Mode Control Register 1	$0A5_H$	269

Table 1 Register Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
CMC0	Chip Mode Control Register 0	$0A6_H$	270
RSSIPWU	Wakeup Peak Detector Readout Register	$0A7_H$	271
IS0	Interrupt Status Register 0	$0A8_H$	271
IS1	Interrupt Status Register 1	$0A9_H$	272
RFPLLACC	RF PLL Actual Channel and Configuration Register	$0AA_H$	274
RSSIPRX	RSSI Peak Detector Readout Register	$0AB_H$	275
RSSIPPL	RSSI Payload Peak Detector Readout Register	$0AC_H$	275
PLDLEN	Payload Data Length Register	$0AD_H$	275
ADCRESH	ADC Result High Byte Register	$0AE_H$	276
ADCRESL	ADC Result Low Byte Register	$0AF_H$	276
VACRES	VCO Autocalibration Result Readout Register	$0B0_H$	277
AFCOFFSET	AFC Offset Read Register	$0B1_H$	277
AGCGAINR	AGC Gain Readout Register	$0B2_H$	278
SPIAT	SPI Address Tracer Register	$0B3_H$	278
SPIDT	SPI Data Tracer Register	$0B4_H$	279
SPICHKSUM	SPI Checksum Register	$0B5_H$	279
SN0	Serial Number Register 0	$0B6_H$	280
SN1	Serial Number Register 1	$0B7_H$	280
SN2	Serial Number Register 2	$0B8_H$	280
SN3	Serial Number Register 3	$0B9_H$	281
RSSIRX	RSSI Readout Register	$0BA_H$	281
RSSIPMF	RSSI Peak Memory Filter Readout Register	$0BB_H$	281
SPWR	Signal Power Readout Register	$0BC_H$	282
NPWR	Noise Power Readout Register	$0BD_H$	282
B_MID0	Message ID Register 0	100_H	
B_MID1	Message ID Register 1	101_H	
B_MID2	Message ID Register 2	102_H	
B_MID3	Message ID Register 3	103_H	
B_MID4	Message ID Register 4	104_H	
B_MID5	Message ID Register 5	105_H	
B_MID6	Message ID Register 6	106_H	
B_MID7	Message ID Register 7	107_H	
B_MID8	Message ID Register 8	108_H	
B_MID9	Message ID Register 9	109_H	
B_MID10	Message ID Register 10	$10A_H$	
B_MID11	Message ID Register 11	$10B_H$	
B_MID12	Message ID Register 12	$10C_H$	
B_MID13	Message ID Register 13	$10D_H$	

Table 1 Register Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
B_MID14	Message ID Register 14	$10E_H$	
B_MID15	Message ID Register 15	$10F_H$	
B_MID16	Message ID Register 16	110_H	
B_MID17	Message ID Register 17	111_H	
B_MID18	Message ID Register 18	112_H	
B_MID19	Message ID Register 19	113_H	
B_MIDC0	Message ID Control Register 0	114_H	
B_MIDC1	Message ID Control Register 1	115_H	
B_IF1	IF1 Register	116_H	
B_WUC	Wake-Up Control Register	117_H	
B_WUPAT0	Wake-Up Pattern Register 0	118_H	
B_WUPAT1	Wake-Up Pattern Register 1	119_H	
B_WUBCNT	Wake-Up Bit or Chip Count Register	$11A_H$	
B_WURSSITH1	RSSI Wake-Up Threshold for Channel 1 Register	$11B_H$	
B_WURSSIBL1	RSSI Wake-Up Blocking Level Low Channel 1 Register	$11C_H$	
B_WURSSIBH1	RSSI Wake-Up Blocking Level High Channel 1 Register	$11D_H$	
B_WURSSITH2	RSSI Wake-Up Threshold for Channel 2 Register	$11E_H$	
B_WURSSIBL2	RSSI Wake-Up Blocking Level Low Channel 2 Register	$11F_H$	
B_WURSSIBH2	RSSI Wake-Up Blocking Level High Channel 2 Register	120_H	
B_WURSSITH3	RSSI Wake-Up Threshold for Channel 3 Register	121_H	
B_WURSSIBL3	RSSI Wake-Up Blocking Level Low Channel 3 Register	122_H	
B_WURSSIBH3	RSSI Wake-Up Blocking Level High Channel 3 Register	123_H	
B_SIGDETSAT	Signal Detector Saturation Threshold Register	124_H	
B_WULOT	Wake-Up on Level Observation Time Register	125_H	
B_SYSRCTO	Synchronization Search Time-Out Register	126_H	
B_TOTIM_SYNC	SYNC Timeout Timer Register	127_H	
B_TOTIM_TSI	TSI Timeout Timer Register	128_H	
B_TOTIM_EOM	EOM Timeout Timer Register	129_H	
B_AFCLIMIT	AFC Limit Configuration Register	$12A_H$	
B_AFCAGCD	AFC/AGC Freeze Delay Register	$12B_H$	
B_AFCSFCFG	AFC Start/Freeze Configuration Register	$12C_H$	
B_AFCK1CFG0	AFC Integrator 1 Gain Register 0	$12D_H$	
B_AFCK1CFG1	AFC Integrator 1 Gain Register 1	$12E_H$	
B_AFCK2CFG0	AFC Integrator 2 Gain Register 0	$12F_H$	

Table 1 Register Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
B_AFCK2CFG1	AFC Integrator 2 Gain Register 1	130_H	
B_PMFUDSF	Peak Memory Filter Up-Down Factor Register	131_H	
B_AGCSFCFG	AGC Start/Freeze Configuration Register	132_H	
B_AGCCFG0	AGC Configuration Register 0	133_H	
B_AGCCFG1	AGC Configuration Register 1	134_H	
B_AGCTHR	AGC Threshold Register	135_H	
B_DIGRXC	Digital Receiver Configuration Register	136_H	
B_PKBITPOS	RSSI Peak Detector Bit Position Register	137_H	
B_ISUPFCSEL	Image Supression Fc Selection Register	138_H	
B_PDECF	Pre Decimation Factor Register	139_H	
B_PDECSCFSK	Pre Decimation Scaling Register FSK Mode	$13A_H$	
B_PDECSCASK	Pre Decimation Scaling Register ASK Mode	$13B_H$	
B_MFC	Matched Filter Control Register	$13C_H$	
B_SRC	Sampe Rate Converter NCO Tune	$13D_H$	
B_EXTSLC	Externel Data Slicer Configuration	$13E_H$	
B_SIGDET0	Signal Detector Threshold Level Register - Run Mode	$13F_H$	
B_SIGDET1	Signal Detector Threshold Level Register - Wakeup	140_H	
B_SIGDETLO	Signal Detector Threshold Low Level Register	141_H	
B_SIGDETSEL	Signal Detector Range Selection Register	142_H	
B_SIGDETCFG	Signal Detector Configuration Register	143_H	
B_NDTHRES	FSK Noise Detector Threshold Register	144_H	
B_NDCONFIG	FSK Noise Detector Configuration Register	145_H	
B_CDRP	Clock and Data Recovery P Configuration Register	146_H	
B_CDRI	Clock and Data Recovery Configuration Register	147_H	
B_CDRRI	Clock and Data Recovery RUNIN Configuration Register	148_H	
B_CDRTOLC	CDR DC Chip Tolerance Register	149_H	
B_CDRTOLB	CDR DC Bit Tolerance Register	$14A_H$	
B_TVWIN	Timing Violation Window Register	$14B_H$	
B_SLCCFG	Slicer Configuration Register	$14C_H$	
B_TSIMODE	TSI Detection Mode Register	$14D_H$	
B_TSILENA	TSI Length Register A	$14E_H$	
B_TSILENB	TSI Length Register B	$14F_H$	
B_TSIGAP	TSI Gap Length Register	150_H	
B_TSIPTA0	TSI Pattern Data Reference A Register 0	151_H	
B_TSIPTA1	TSI Pattern Data Reference A Register 1	152_H	

Table 1 Register Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
B_TSIPTB0	TSI Pattern Data Reference B Register 0	153_H	
B_TSIPTB1	TSI Pattern Data Reference B Register 1	154_H	
B_EOMC	End Of Message Control Register	155_H	
B_EOMDLEN	EOM Data Length Limit Register	156_H	
B_EOMDLENP	EOM Data Length Limit Parallel Mode Register	157_H	
B_CHCFG	Channel Configuration Register	158_H	
B_PLLINTC1	PLL MMD Integer Value Register Channel 1	159_H	
B_PLLFRAC0C1	PLL Fractional Division Ratio Register 0 Channel 1	$15A_H$	
B_PLLFRAC1C1	PLL Fractional Division Ratio Register 1 Channel 1	$15B_H$	
B_PLLFRAC2C1	PLL Fractional Division Ratio Register 2 Channel 1	$15C_H$	
B_PLLINTC2	PLL MMD Integer Value Register Channel 2	$15D_H$	
B_PLLFRAC0C2	PLL Fractional Division Ratio Register 0 Channel 2	$15E_H$	
B_PLLFRAC1C2	PLL Fractional Division Ratio Register 1 Channel 2	$15F_H$	
B_PLLFRAC2C2	PLL Fractional Division Ratio Register 2 Channel 2	160_H	
B_PLLINTC3	PLL MMD Integer Value Register Channel 3	161_H	
B_PLLFRAC0C3	PLL Fractional Division Ratio Register 0 Channel 3	162_H	
B_PLLFRAC1C3	PLL Fractional Division Ratio Register 1 Channel 3	163_H	
B_PLLFRAC2C3	PLL Fractional Division Ratio Register 2 Channel 3	164_H	
C_MID0	Message ID Register 0	200_H	
C_MID1	Message ID Register 1	201_H	
C_MID2	Message ID Register 2	202_H	
C_MID3	Message ID Register 3	203_H	
C_MID4	Message ID Register 4	204_H	
C_MID5	Message ID Register 5	205_H	
C_MID6	Message ID Register 6	206_H	
C_MID7	Message ID Register 7	207_H	
C_MID8	Message ID Register 8	208_H	
C_MID9	Message ID Register 9	209_H	
C_MID10	Message ID Register 10	$20A_H$	
C_MID11	Message ID Register 11	$20B_H$	
C_MID12	Message ID Register 12	$20C_H$	
C_MID13	Message ID Register 13	$20D_H$	
C_MID14	Message ID Register 14	$20E_H$	
C_MID15	Message ID Register 15	$20F_H$	
C_MID16	Message ID Register 16	210_H	
C_MID17	Message ID Register 17	211_H	
C_MID18	Message ID Register 18	212_H	
C_MID19	Message ID Register 19	213_H	

Table 1 Register Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
C_MIDC0	Message ID Control Register 0	214_H	
C_MIDC1	Message ID Control Register 1	215_H	
C_IF1	IF1 Register	216_H	
C_WUC	Wake-Up Control Register	217_H	
C_WUPAT0	Wake-Up Pattern Register 0	218_H	
C_WUPAT1	Wake-Up Pattern Register 1	219_H	
C_WUBCNT	Wake-Up Bit or Chip Count Register	$21A_H$	
C_WURSSITH1	RSSI Wake-Up Threshold for Channel 1 Register	$21B_H$	
C_WURSSIBL1	RSSI Wake-Up Blocking Level Low Channel 1 Register	$21C_H$	
C_WURSSIBH1	RSSI Wake-Up Blocking Level High Channel 1 Register	$21D_H$	
C_WURSSITH2	RSSI Wake-Up Threshold for Channel 2 Register	$21E_H$	
C_WURSSIBL2	RSSI Wake-Up Blocking Level Low Channel 2 Register	$21F_H$	
C_WURSSIBH2	RSSI Wake-Up Blocking Level High Channel 2 Register	220_H	
C_WURSSITH3	RSSI Wake-Up Threshold for Channel 3 Register	221_H	
C_WURSSIBL3	RSSI Wake-Up Blocking Level Low Channel 3 Register	222_H	
C_WURSSIBH3	RSSI Wake-Up Blocking Level High Channel 3 Register	223_H	
C_SIGDETSAT	Signal Detector Saturation Threshold Register	224_H	
C_WULOT	Wake-Up on Level Observation Time Register	225_H	
C_SYSRCTO	Synchronization Search Time-Out Register	226_H	
C_TOTIM_SYNC	SYNC Timeout Timer Register	227_H	
C_TOTIM_TSI	TSI Timeout Timer Register	228_H	
C_TOTIM_EOM	EOM Timeout Timer Register	229_H	
C_AFCLIMIT	AFC Limit Configuration Register	$22A_H$	
C_AFCAGCD	AFC/AGC Freeze Delay Register	$22B_H$	
C_AFCSFCFG	AFC Start/Freeze Configuration Register	$22C_H$	
C_AFCK1CFG0	AFC Integrator 1 Gain Register 0	$22D_H$	
C_AFCK1CFG1	AFC Integrator 1 Gain Register 1	$22E_H$	
C_AFCK2CFG0	AFC Integrator 2 Gain Register 0	$22F_H$	
C_AFCK2CFG1	AFC Integrator 2 Gain Register 1	230_H	
C_PMFUDSF	Peak Memory Filter Up-Down Factor Register	231_H	
C_AGCSFCFG	AGC Start/Freeze Configuration Register	232_H	
C_AGCCFG0	AGC Configuration Register 0	233_H	
C_AGCCFG1	AGC Configuration Register 1	234_H	
C_AGCTHR	AGC Threshold Register	235_H	

Table 1 Register Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
C_DIGRXC	Digital Receiver Configuration Register	236_H	
C_PKBITPOS	RSSI Peak Detector Bit Position Register	237_H	
C_ISUPFCSEL	Image Supression Fc Selection Register	238_H	
C_PDECF	Pre Decimation Factor Register	239_H	
C_PDECSCFSK	Pre Decimation Scaling Register FSK Mode	$23A_H$	
C_PDECSCASK	Pre Decimation Scaling Register ASK Mode	$23B_H$	
C_MFC	Matched Filter Control Register	$23C_H$	
C_SRC	Sampe Rate Converter NCO Tune	$23D_H$	
C_EXTSLC	Externel Data Slicer Configuration	$23E_H$	
C_SIGDET0	Signal Detector Threshold Level Register - Run Mode	$23F_H$	
C_SIGDET1	Signal Detector Threshold Level Register - Wakeup	240_H	
C_SIGDETLO	Signal Detector Threshold Low Level Register	241_H	
C_SIGDETSEL	Signal Detector Range Selection Register	242_H	
C_SIGDETCFG	Signal Detector Configuration Register	243_H	
C_NDTHRES	FSK Noise Detector Threshold Register	244_H	
C_NDCONFIG	FSK Noise Detector Configuration Register	245_H	
C_CDRP	Clock and Data Recovery P Configuration Register	246_H	
C_CDRI	Clock and Data Recovery Configuration Register	247_H	
C_CDRRI	Clock and Data Recovery RUNIN Configuration Register	248_H	
C_CDRTOLC	CDR DC Chip Tolerance Register	249_H	
C_CDRTOLB	CDR DC Bit Tolerance Register	$24A_H$	
C_TVWIN	Timing Violation Window Register	$24B_H$	
C_SLCCFG	Slicer Configuration Register	$24C_H$	
C_TSIMODE	TSI Detection Mode Register	$24D_H$	
C_TSILENA	TSI Length Register A	$24E_H$	
C_TSILENB	TSI Length Register B	$24F_H$	
C_TSIGAP	TSI Gap Length Register	250_H	
C_TSIPTA0	TSI Pattern Data Reference A Register 0	251_H	
C_TSIPTA1	TSI Pattern Data Reference A Register 1	252_H	
C_TSIPTB0	TSI Pattern Data Reference B Register 0	253_H	
C_TSIPTB1	TSI Pattern Data Reference B Register 1	254_H	
C_EOMC	End Of Message Control Register	255_H	
C_EOMDLEN	EOM Data Length Limit Register	256_H	
C_EOMDLENP	EOM Data Length Limit Parallel Mode Register	257_H	
C_CHCFG	Channel Configuration Register	258_H	

Table 1 Register Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
C_PLLINTC1	PLL MMD Integer Value Register Channel 1	259_H	
C_PLLFRAC0C1	PLL Fractional Division Ratio Register 0 Channel 1	$25A_H$	
C_PLLFRAC1C1	PLL Fractional Division Ratio Register 1 Channel 1	$25B_H$	
C_PLLFRAC2C1	PLL Fractional Division Ratio Register 2 Channel 1	$25C_H$	
C_PLLINTC2	PLL MMD Integer Value Register Channel 2	$25D_H$	
C_PLLFRAC0C2	PLL Fractional Division Ratio Register 0 Channel 2	$25E_H$	
C_PLLFRAC1C2	PLL Fractional Division Ratio Register 1 Channel 2	$25F_H$	
C_PLLFRAC2C2	PLL Fractional Division Ratio Register 2 Channel 2	260_H	
C_PLLINTC3	PLL MMD Integer Value Register Channel 3	261_H	
C_PLLFRAC0C3	PLL Fractional Division Ratio Register 0 Channel 3	262_H	
C_PLLFRAC1C3	PLL Fractional Division Ratio Register 1 Channel 3	263_H	
C_PLLFRAC2C3	PLL Fractional Division Ratio Register 2 Channel 3	264_H	
D_MID0	Message ID Register 0	300_H	
D_MID1	Message ID Register 1	301_H	
D_MID2	Message ID Register 2	302_H	
D_MID3	Message ID Register 3	303_H	
D_MID4	Message ID Register 4	304_H	
D_MID5	Message ID Register 5	305_H	
D_MID6	Message ID Register 6	306_H	
D_MID7	Message ID Register 7	307_H	
D_MID8	Message ID Register 8	308_H	
D_MID9	Message ID Register 9	309_H	
D_MID10	Message ID Register 10	$30A_H$	
D_MID11	Message ID Register 11	$30B_H$	
D_MID12	Message ID Register 12	$30C_H$	
D_MID13	Message ID Register 13	$30D_H$	
D_MID14	Message ID Register 14	$30E_H$	
D_MID15	Message ID Register 15	$30F_H$	
D_MID16	Message ID Register 16	310_H	
D_MID17	Message ID Register 17	311_H	
D_MID18	Message ID Register 18	312_H	
D_MID19	Message ID Register 19	313_H	
D_MIDC0	Message ID Control Register 0	314_H	
D_MIDC1	Message ID Control Register 1	315_H	
D_IF1	IF1 Register	316_H	
D_WUC	Wake-Up Control Register	317_H	
D_WUPAT0	Wake-Up Pattern Register 0	318_H	
D_WUPAT1	Wake-Up Pattern Register 1	319_H	

Table 1 Register Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
D_WUBCNT	Wake-Up Bit or Chip Count Register	$31A_H$	
D_WURSSITH1	RSSI Wake-Up Threshold for Channel 1 Register	$31B_H$	
D_WURSSIBL1	RSSI Wake-Up Blocking Level Low Channel 1 Register	$31C_H$	
D_WURSSIBH1	RSSI Wake-Up Blocking Level High Channel 1 Register	$31D_H$	
D_WURSSITH2	RSSI Wake-Up Threshold for Channel 2 Register	$31E_H$	
D_WURSSIBL2	RSSI Wake-Up Blocking Level Low Channel 2 Register	$31F_H$	
D_WURSSIBH2	RSSI Wake-Up Blocking Level High Channel 2 Register	320_H	
D_WURSSITH3	RSSI Wake-Up Threshold for Channel 3 Register	321_H	
D_WURSSIBL3	RSSI Wake-Up Blocking Level Low Channel 3 Register	322_H	
D_WURSSIBH3	RSSI Wake-Up Blocking Level High Channel 3 Register	323_H	
D_SIGDETSAT	Signal Detector Saturation Threshold Register	324_H	
D_WULOT	Wake-Up on Level Observation Time Register	325_H	
D_SYSRCTO	Synchronization Search Time-Out Register	326_H	
D_TOTIM_SYNC	SYNC Timeout Timer Register	327_H	
D_TOTIM_TSI	TSI Timeout Timer Register	328_H	
D_TOTIM_EOM	EOM Timeout Timer Register	329_H	
D_AFCLIMIT	AFC Limit Configuration Register	$32A_H$	
D_AFCAGCD	AFC/AGC Freeze Delay Register	$32B_H$	
D_AFCSFCFG	AFC Start/Freeze Configuration Register	$32C_H$	
D_AFCK1CFG0	AFC Integrator 1 Gain Register 0	$32D_H$	
D_AFCK1CFG1	AFC Integrator 1 Gain Register 1	$32E_H$	
D_AFCK2CFG0	AFC Integrator 2 Gain Register 0	$32F_H$	
D_AFCK2CFG1	AFC Integrator 2 Gain Register 1	330_H	
D_PMFUDSF	Peak Memory Filter Up-Down Factor Register	331_H	
D_AGCSFCFG	AGC Start/Freeze Configuration Register	332_H	
D_AGCCFG0	AGC Configuration Register 0	333_H	
D_AGCCFG1	AGC Configuration Register 1	334_H	
D_AGCTHR	AGC Threshold Register	335_H	
D_DIGRXC	Digital Receiver Configuration Register	336_H	
D_PKBITPOS	RSSI Peak Detector Bit Position Register	337_H	
D_ISUPFCSEL	Image Supression Fc Selection Register	338_H	
D_PDECF	Pre Decimation Factor Register	339_H	
D_PDECSCFSK	Pre Decimation Scaling Register FSK Mode	$33A_H$	
D_PDECSCASK	Pre Decimation Scaling Register ASK Mode	$33B_H$	

Table 1 Register Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
D_MFC	Matched Filter Control Register	$33C_H$	
D_SRC	Sampe Rate Converter NCO Tune	$33D_H$	
D_EXTSLC	Externel Data Slicer Configuration	$33E_H$	
D_SIGDET0	Signal Detector Threshold Level Register - Run Mode	$33F_H$	
D_SIGDET1	Signal Detector Threshold Level Register - Wakeup	340_H	
D_SIGDETLO	Signal Detector Threshold Low Level Register	341_H	
D_SIGDETSEL	Signal Detector Range Selection Register	342_H	
D_SIGDETCFG	Signal Detector Configuration Register	343_H	
D_NDTHRES	FSK Noise Detector Threshold Register	344_H	
D_NDCONFIG	FSK Noise Detector Configuration Register	345_H	
D_CDRP	Clock and Data Recovery P Configuration Register	346_H	
D_CDRI	Clock and Data Recovery Configuration Register	347_H	
D_CDRRI	Clock and Data Recovery RUNIN Configuration Register	348_H	
D_CDRTOLC	CDR DC Chip Tolerance Register	349_H	
D_CDRTOLB	CDR DC Bit Tolerance Register	$34A_H$	
D_TVWIN	Timing Violation Window Register	$34B_H$	
D_SLCCFG	Slicer Configuration Register	$34C_H$	
D_TSIMODE	TSI Detection Mode Register	$34D_H$	
D_TSILENA	TSI Length Register A	$34E_H$	
D_TSILENB	TSI Length Register B	$34F_H$	
D_TSIGAP	TSI Gap Length Register	350_H	
D_TSIPTA0	TSI Pattern Data Reference A Register 0	351_H	
D_TSIPTA1	TSI Pattern Data Reference A Register 1	352_H	
D_TSIPTB0	TSI Pattern Data Reference B Register 0	353_H	
D_TSIPTB1	TSI Pattern Data Reference B Register 1	354_H	
D_EOMC	End Of Message Control Register	355_H	
D_EOMDLEN	EOM Data Length Limit Register	356_H	
D_EOMDLENP	EOM Data Length Limit Parallel Mode Register	357_H	
D_CHCFG	Channel Configuration Register	358_H	
D_PLLINTC1	PLL MMD Integer Value Register Channel 1	359_H	
D_PLLFRAC0C1	PLL Fractional Division Ratio Register 0 Channel 1	$35A_H$	
D_PLLFRAC1C1	PLL Fractional Division Ratio Register 1 Channel 1	$35B_H$	
D_PLLFRAC2C1	PLL Fractional Division Ratio Register 2 Channel 1	$35C_H$	
D_PLLINTC2	PLL MMD Integer Value Register Channel 2	$35D_H$	
D_PLLFRAC0C2	PLL Fractional Division Ratio Register 0 Channel 2	$35E_H$	

Table 1 Register Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
D_PLLFRAC1C2	PLL Fractional Division Ratio Register 1 Channel 2	$35F_H$	
D_PLLFRAC2C2	PLL Fractional Division Ratio Register 2 Channel 2	360_H	
D_PLLINTC3	PLL MMD Integer Value Register Channel 3	361_H	
D_PLLFRAC0C3	PLL Fractional Division Ratio Register 0 Channel 3	362_H	
D_PLLFRAC1C3	PLL Fractional Division Ratio Register 1 Channel 3	363_H	
D_PLLFRAC2C3	PLL Fractional Division Ratio Register 2 Channel 3	364_H	

Table 2 Register Overview and Reset Value

Register Short Name	Register Long Name	Offset Address	Reset Value
Appendix - Registers Chapter, Register Description			
A_MID0	Message ID Register 0	000_H	00_H
A_MID1	Message ID Register 1	001_H	00_H
A_MID2	Message ID Register 2	002_H	00_H
A_MID3	Message ID Register 3	003_H	00_H
A_MID4	Message ID Register 4	004_H	00_H
A_MID5	Message ID Register 5	005_H	00_H
A_MID6	Message ID Register 6	006_H	00_H
A_MID7	Message ID Register 7	007_H	00_H
A_MID8	Message ID Register 8	008_H	00_H
A_MID9	Message ID Register 9	009_H	00_H
A_MID10	Message ID Register 10	$00A_H$	00_H
A_MID11	Message ID Register 11	$00B_H$	00_H
A_MID12	Message ID Register 12	$00C_H$	00_H
A_MID13	Message ID Register 13	$00D_H$	00_H
A_MID14	Message ID Register 14	$00E_H$	00_H
A_MID15	Message ID Register 15	$00F_H$	00_H
A_MID16	Message ID Register 16	010_H	00_H
A_MID17	Message ID Register 17	011_H	00_H
A_MID18	Message ID Register 18	012_H	00_H
A_MID19	Message ID Register 19	013_H	00_H
A_MIDC0	Message ID Control Register 0	014_H	00_H
A_MIDC1	Message ID Control Register 1	015_H	00_H
A_IF1	IF1 Register	016_H	20_H
A_WUC	Wake-Up Control Register	017_H	04_H
A_WUPAT0	Wake-Up Pattern Register 0	018_H	00_H
A_WUPAT1	Wake-Up Pattern Register 1	019_H	00_H
A_WUBCNT	Wake-Up Bit or Chip Count Register	$01A_H$	00_H
A_WURSSITH1	RSSI Wake-Up Threshold for Channel 1 Register	$01B_H$	00_H

Table 2 Register Overview and Reset Value (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
A_WURSSIBL1	RSSI Wake-Up Blocking Level Low Channel 1 Register	$01C_H$	FF_H
A_WURSSIBH1	RSSI Wake-Up Blocking Level High Channel 1 Register	$01D_H$	00_H
A_WURSSITH2	RSSI Wake-Up Threshold for Channel 2 Register	$01E_H$	00_H
A_WURSSIBL2	RSSI Wake-Up Blocking Level Low Channel 2 Register	$01F_H$	FF_H
A_WURSSIBH2	RSSI Wake-Up Blocking Level High Channel 2 Register	020_H	00_H
A_WURSSITH3	RSSI Wake-Up Threshold for Channel 3 Register	021_H	00_H
A_WURSSIBL3	RSSI Wake-Up Blocking Level Low Channel 3 Register	022_H	FF_H
A_WURSSIBH3	RSSI Wake-Up Blocking Level High Channel 3 Register	023_H	00_H
A_SIGDETSAT	Signal Detector Saturation Threshold Register	024_H	10_H
A_WULOT	Wake-up on Level Observation Time Register	025_H	00_H
A_SYSRCTO	Synchronization Search Time-Out Register	026_H	87_H
A_TOTIM_SYNC	SYNC Timeout Timer Register	027_H	FF_H
A_TOTIM_TSI	TSI Timeout Timer Register	028_H	00_H
A_TOTIM_EOM	EOM Timeout Timer Register	029_H	00_H
A_AFCLIMIT	AFC Limit Configuration Register	$02A_H$	02_H
A_AFCAGCD	AFC/AGC Freeze Delay Register	$02B_H$	00_H
A_AFCSFCFG	AFC Start/Freeze Configuration Register	$02C_H$	00_H
A_AFCK1CFG0	AFC Integrator 1 Gain Register 0	$02D_H$	00_H
A_AFCK1CFG1	AFC Integrator 1 Gain Register 1	$02E_H$	00_H
A_AFCK2CFG0	AFC Integrator 2 Gain Register 0	$02F_H$	00_H
A_AFCK2CFG1	AFC Integrator 2 Gain Register 1	030_H	00_H
A_PMFUDSF	Peak Memory Filter Up-Down Factor Register	031_H	42_H
A_AGCSFCFG	AGC Start/Freeze Configuration Register	032_H	00_H
A_AGCCFG0	AGC Configuration Register 0	033_H	$2B_H$
A_AGCCFG1	AGC Configuration Register 1	034_H	03_H
A_AGCTHR	AGC Threshold Register	035_H	08_H
A_DIGRXC	Digital Receiver Configuration Register	036_H	40_H
A_PKBITPOS	RSSI Peak Detector Bit Position Register	037_H	00_H
A_ISUPFCSEL	Image Supression Fc Selection Register	038_H	07_H
A_PDECF	Pre Decimation Factor Register	039_H	00_H
A_PDECSCFSK	Pre Decimation Scaling Register FSK Mode	$03A_H$	00_H
A_PDECSCASK	Pre Decimation Scaling Register ASK Mode	$03B_H$	20_H
A_MFC	Matched Filter Control Register	$03C_H$	07_H
A_SRC	Sampe Rate Converter NCO Tune	$03D_H$	00_H

Table 2 Register Overview and Reset Value (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
A_EXTSLC	Externel Data Slicer Configuration	$03E_H$	02_H
A_SIGDET0	Signal Detector Threshold Level Register - Run Mode	$03F_H$	00_H
A_SIGDET1	Signal Detector Threshold Level Register - Wakeup	040_H	00_H
A_SIGDETLO	Signal Detector Threshold Low Level Register	041_H	00_H
A_SIGDETSEL	Signal Detector Range Selection Register	042_H	$7F_H$
A_SIGDETCFG	Signal Detector Configuration Register	043_H	00_H
A_NDTHRES	FSK Noise Detector Threshold Register	044_H	00_H
A_NDCONFIG	FSK Noise Detector Configuration Register	045_H	07_H
A_CDRP	Clock and Data Recovery P Configuration Register	046_H	$E6_H$
A_CDRI	Clock and Data Recovery Configuration Register	047_H	65_H
A_CDRRI	Clock and Data Recovery RUNIN Configuration Register	048_H	01_H
A_CDRTOLC	CDR DC Chip Tolerance Register	049_H	$0C_H$
A_CDRTOLB	CDR DC Bit Tolerance Register	$04A_H$	$1E_H$
A_TVWIN	Timing Violation Window Register	$04B_H$	28_H
A_SLCCFG	Slicer Configuration Register	$04C_H$	90_H
A_TSIMODE	TSI Detection Mode Register	$04D_H$	80_H
A_TSILENA	TSI Length Register A	$04E_H$	00_H
A_TSILENB	TSI Length Register B	$04F_H$	00_H
A_TSIGAP	TSI Gap Length Register	050_H	00_H
A_TSIPTA0	TSI Pattern Data Reference A Register 0	051_H	00_H
A_TSIPTA1	TSI Pattern Data Reference A Register 1	052_H	00_H
A_TSIPTB0	TSI Pattern Data Reference B Register 0	053_H	00_H
A_TSIPTB1	TSI Pattern Data Reference B Register 1	054_H	00_H
A_EOMC	End Of Message Control Register	055_H	05_H
A_EOMDLEN	EOM Data Length Limit Register	056_H	00_H
A_EOMDLENP	EOM Data Length Limit Parallel Mode Register	057_H	00_H
A_CHCFG	Channel Configuration Register	058_H	04_H
A_PLLINTC1	PLL MMD Integer Value Register Channel 1	059_H	93_H
A_PLLFRAC0C1	PLL Fractional Division Ratio Register 0 Channel 1	$05A_H$	$F3_H$
A_PLLFRAC1C1	PLL Fractional Division Ratio Register 1 Channel 1	$05B_H$	07_H
A_PLLFRAC2C1	PLL Fractional Division Ratio Register 2 Channel 1	$05C_H$	09_H
A_PLLINTC2	PLL MMD Integer Value Register Channel 2	$05D_H$	13_H
A_PLLFRAC0C2	PLL Fractional Division Ratio Register 0 Channel 2	$05E_H$	$F3_H$
A_PLLFRAC1C2	PLL Fractional Division Ratio Register 1 Channel 2	$05F_H$	07_H
A_PLLFRAC2C2	PLL Fractional Division Ratio Register 2 Channel 2	060_H	09_H

Table 2 Register Overview and Reset Value (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
A_PLLINTC3	PLL MMD Integer Value Register Channel 3	061_H	13_H
A_PLLFRAC0C3	PLL Fractional Division Ratio Register 0 Channel 3	062_H	$F3_H$
A_PLLFRAC1C3	PLL Fractional Division Ratio Register 1 Channel 3	063_H	07_H
A_PLLFRAC2C3	PLL Fractional Division Ratio Register 2 Channel 3	064_H	09_H
SFRPAGE	Special Function Register Page Register	080_H	00_H
PPCFG0	PP0 and PP1 Configuration Register	081_H	50_H
PPCFG1	PP2 and PP3 Configuration Register	082_H	12_H
PPCFG2	PPx Port Configuration Register	083_H	00_H
RXRUNCFG0	RX RUN Configuration Register 0	084_H	FF_H
RXRUNCFG1	RX RUN Configuration Register 1	085_H	FF_H
CLKOUT0	Clock Divider Register 0	086_H	$0B_H$
CLKOUT1	Clock Divider Register 1	087_H	00_H
CLKOUT2	Clock Divider Register 2	088_H	00_H
RFC	RF Control Register	089_H	07_H
BPFCALCFG0	BPF Calibration Configuration Register 0	$08A_H$	07_H
BPFCALCFG1	BPF Calibration Configuration Register 1	$08B_H$	04_H
XTALCAL0	XTAL Coarse Calibration Register	$08C_H$	10_H
XTALCAL1	XTAL Fine Calibration Register	$08D_H$	00_H
RSSIMONC	RSSI Monitor Configuration Register	$08E_H$	01_H
ADCINSEL	ADC Input Selection Register	$08F_H$	00_H
RSSIOFFS	RSSI Offset Register	090_H	80_H
RSSISLOPE	RSSI Slope Register	091_H	80_H
CDRDRTHRP	CDR Data Rate Acceptance Positive Threshold Register	092_H	$1E_H$
CDRDRTHRN	CDR Data Rate Acceptance Negative Threshold Register	093_H	23_H
IM0	Interrupt Mask Register 0	094_H	00_H
IM1	Interrupt Mask Register 1	095_H	00_H
SPMAP	Self Polling Mode Active Periods Register	096_H	01_H
SPMIP	Self Polling Mode Idle Periods Register	097_H	01_H
SPMC	Self Polling Mode Control Register	098_H	00_H
SPMRT	Self Polling Mode Reference Timer Register	099_H	01_H
SPMOFFT0	Self Polling Mode Off Time Register 0	$09A_H$	01_H
SPMOFFT1	Self Polling Mode Off Time Register 1	$09B_H$	00_H
SPMONTA0	Self Polling Mode On Time Config A Register 0	$09C_H$	01_H
SPMONTA1	Self Polling Mode On Time Config A Register 1	$09D_H$	00_H
SPMONTB0	Self Polling Mode On Time Config B Register 0	$09E_H$	01_H
SPMONTB1	Self Polling Mode On Time Config B Register 1	$09F_H$	00_H
SPMONTC0	Self Polling Mode On Time Config C Register 0	$0A0_H$	01_H

Table 2 Register Overview and Reset Value (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
SPMONTC1	Self Polling Mode On Time Config C Register 1	$0A1_H$	00_H
SPMONTD0	Self Polling Mode On Time Config D Register 0	$0A2_H$	01_H
SPMONTD1	Self Polling Mode On Time Config D Register 1	$0A3_H$	00_H
EXTPCMD	External Processing Command Register	$0A4_H$	00_H
CMC1	Chip Mode Control Register 1	$0A5_H$	04_H
CMC0	Chip Mode Control Register 0	$0A6_H$	10_H
RSSIPWU	Wakeup Peak Detector Readout Register	$0A7_H$	00_H
IS0	Interrupt Status Register 0	$0A8_H$	FF_H
IS1	Interrupt Status Register 1	$0A9_H$	FF_H
RFPLLACC	RF PLL Actual Channel and Configuration Register	$0AA_H$	00_H
RSSIPRX	RSSI Peak Detector Readout Register	$0AB_H$	00_H
RSSIPPL	RSSI Payload Peak Detector Readout Register	$0AC_H$	00_H
PLDLEN	Payload Data Length Register	$0AD_H$	00_H
ADCRESH	ADC Result High Byte Register	$0AE_H$	00_H
ADCRESL	ADC Result Low Byte Register	$0AF_H$	00_H
VACRES	VCO Autocalibration Result Readout Register	$0B0_H$	00_H
AFCOFFSET	AFC Offset Read Register	$0B1_H$	00_H
AGCGAINR	AGC Gain Readout Register	$0B2_H$	00_H
SPIAT	SPI Address Tracer Register	$0B3_H$	00_H
SPIDT	SPI Data Tracer Register	$0B4_H$	00_H
SPICHKSUM	SPI Checksum Register	$0B5_H$	00_H
SN0	Serial Number Register 0	$0B6_H$	00_H
SN1	Serial Number Register 1	$0B7_H$	00_H
SN2	Serial Number Register 2	$0B8_H$	00_H
SN3	Serial Number Register 3	$0B9_H$	00_H
RSSIRX	RSSI Readout Register	$0BA_H$	00_H
RSSIPMF	RSSI Peak Memory Filter Readout Register	$0BB_H$	00_H
SPWR	Signal Power Readout Register	$0BC_H$	00_H
NPWR	Noise Power Readout Register	$0BD_H$	00_H
B_MID0	Message ID Register 0	100_H	00_H
B_MID1	Message ID Register 1	101_H	00_H
B_MID2	Message ID Register 2	102_H	00_H
B_MID3	Message ID Register 3	103_H	00_H
B_MID4	Message ID Register 4	104_H	00_H
B_MID5	Message ID Register 5	105_H	00_H
B_MID6	Message ID Register 6	106_H	00_H
B_MID7	Message ID Register 7	107_H	00_H
B_MID8	Message ID Register 8	108_H	00_H

Table 2 Register Overview and Reset Value (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
B_MID9	Message ID Register 9	109_H	00_H
B_MID10	Message ID Register 10	$10A_H$	00_H
B_MID11	Message ID Register 11	$10B_H$	00_H
B_MID12	Message ID Register 12	$10C_H$	00_H
B_MID13	Message ID Register 13	$10D_H$	00_H
B_MID14	Message ID Register 14	$10E_H$	00_H
B_MID15	Message ID Register 15	$10F_H$	00_H
B_MID16	Message ID Register 16	110_H	00_H
B_MID17	Message ID Register 17	111_H	00_H
B_MID18	Message ID Register 18	112_H	00_H
B_MID19	Message ID Register 19	113_H	00_H
B_MIDC0	Message ID Control Register 0	114_H	00_H
B_MIDC1	Message ID Control Register 1	115_H	00_H
B_IF1	IF1 Register	116_H	20_H
B_WUC	Wake-Up Control Register	117_H	04_H
B_WUPAT0	Wake-Up Pattern Register 0	118_H	00_H
B_WUPAT1	Wake-Up Pattern Register 1	119_H	00_H
B_WUBCNT	Wake-Up Bit or Chip Count Register	$11A_H$	00_H
B_WURSSITH1	RSSI Wake-Up Threshold for Channel 1 Register	$11B_H$	00_H
B_WURSSIBL1	RSSI Wake-Up Blocking Level Low Channel 1 Register	$11C_H$	FF_H
B_WURSSIBH1	RSSI Wake-Up Blocking Level High Channel 1 Register	$11D_H$	00_H
B_WURSSITH2	RSSI Wake-Up Threshold for Channel 2 Register	$11E_H$	00_H
B_WURSSIBL2	RSSI Wake-Up Blocking Level Low Channel 2 Register	$11F_H$	FF_H
B_WURSSIBH2	RSSI Wake-Up Blocking Level High Channel 2 Register	120_H	00_H
B_WURSSITH3	RSSI Wake-Up Threshold for Channel 3 Register	121_H	00_H
B_WURSSIBL3	RSSI Wake-Up Blocking Level Low Channel 3 Register	122_H	FF_H
B_WURSSIBH3	RSSI Wake-Up Blocking Level High Channel 3 Register	123_H	00_H
B_SIGDETSAT	Signal Detector Saturation Threshold Register	124_H	10_H
B_WULOT	Wake-Up on Level Observation Time Register	125_H	00_H
B_SYSRCTO	Synchronization Search Time-Out Register	126_H	87_H
B_TOTIM_SYNC	SYNC Timeout Timer Register	127_H	FF_H
B_TOTIM_TSI	TSI Timeout Timer Register	128_H	00_H
B_TOTIM_EOM	EOM Timeout Timer Register	129_H	00_H
B_AFCLIMIT	AFC Limit Configuration Register	$12A_H$	02_H

Table 2 Register Overview and Reset Value (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
B_AFCAGCD	AFC/AGC Freeze Delay Register	$12B_H$	00_H
B_AFCSFCFG	AFC Start/Freeze Configuration Register	$12C_H$	00_H
B_AFCK1CFG0	AFC Integrator 1 Gain Register 0	$12D_H$	00_H
B_AFCK1CFG1	AFC Integrator 1 Gain Register 1	$12E_H$	00_H
B_AFCK2CFG0	AFC Integrator 2 Gain Register 0	$12F_H$	00_H
B_AFCK2CFG1	AFC Integrator 2 Gain Register 1	130_H	00_H
B_PMFUDSF	Peak Memory Filter Up-Down Factor Register	131_H	42_H
B_AGCSFCFG	AGC Start/Freeze Configuration Register	132_H	00_H
B_AGCCFG0	AGC Configuration Register 0	133_H	$2B_H$
B_AGCCFG1	AGC Configuration Register 1	134_H	03_H
B_AGCTHR	AGC Threshold Register	135_H	08_H
B_DIGRXC	Digital Receiver Configuration Register	136_H	40_H
B_PKBITPOS	RSSI Peak Detector Bit Position Register	137_H	00_H
B_ISUPFCSEL	Image Supression Fc Selection Register	138_H	07_H
B_PDECF	Pre Decimation Factor Register	139_H	00_H
B_PDECSCFSK	Pre Decimation Scaling Register FSK Mode	$13A_H$	00_H
B_PDECSCASK	Pre Decimation Scaling Register ASK Mode	$13B_H$	20_H
B_MFC	Matched Filter Control Register	$13C_H$	07_H
B_SRC	Sampe Rate Converter NCO Tune	$13D_H$	00_H
B_EXTSLC	Externel Data Slicer Configuration	$13E_H$	02_H
B_SIGDET0	Signal Detector Threshold Level Register - Run Mode	$13F_H$	00_H
B_SIGDET1	Signal Detector Threshold Level Register - Wakeup	140_H	00_H
B_SIGDETLO	Signal Detector Threshold Low Level Register	141_H	00_H
B_SIGDETSEL	Signal Detector Range Selection Register	142_H	$7F_H$
B_SIGDETCFG	Signal Detector Configuration Register	143_H	00_H
B_NDTHRES	FSK Noise Detector Threshold Register	144_H	00_H
B_NDCONFIG	FSK Noise Detector Configuration Register	145_H	07_H
B_CDRP	Clock and Data Recovery P Configuration Register	146_H	$E6_H$
B_CDRI	Clock and Data Recovery Configuration Register	147_H	65_H
B_CDRRI	Clock and Data Recovery RUNIN Configuration Register	148_H	01_H
B_CDRTOLC	CDR DC Chip Tolerance Register	149_H	$0C_H$
B_CDRTOLB	CDR DC Bit Tolerance Register	$14A_H$	$1E_H$
B_TVWIN	Timing Violation Window Register	$14B_H$	28_H
B_SLCCFG	Slicer Configuration Register	$14C_H$	90_H
B_TSIMODE	TSI Detection Mode Register	$14D_H$	80_H

Table 2 Register Overview and Reset Value (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
B_TSILENA	TSI Length Register A	$14E_H$	00_H
B_TSILENB	TSI Length Register B	$14F_H$	00_H
B_TSIGAP	TSI Gap Length Register	150_H	00_H
B_TSIPTA0	TSI Pattern Data Reference A Register 0	151_H	00_H
B_TSIPTA1	TSI Pattern Data Reference A Register 1	152_H	00_H
B_TSIPTB0	TSI Pattern Data Reference B Register 0	153_H	00_H
B_TSIPTB1	TSI Pattern Data Reference B Register 1	154_H	00_H
B_EOMC	End Of Message Control Register	155_H	05_H
B_EOMDLEN	EOM Data Length Limit Register	156_H	00_H
B_EOMDLENP	EOM Data Length Limit Parallel Mode Register	157_H	00_H
B_CHCFG	Channel Configuration Register	158_H	04_H
B_PLLINTC1	PLL MMD Integer Value Register Channel 1	159_H	93_H
B_PLLFRAC0C1	PLL Fractional Division Ratio Register 0 Channel 1	$15A_H$	$F3_H$
B_PLLFRAC1C1	PLL Fractional Division Ratio Register 1 Channel 1	$15B_H$	07_H
B_PLLFRAC2C1	PLL Fractional Division Ratio Register 2 Channel 1	$15C_H$	09_H
B_PLLINTC2	PLL MMD Integer Value Register Channel 2	$15D_H$	13_H
B_PLLFRAC0C2	PLL Fractional Division Ratio Register 0 Channel 2	$15E_H$	$F3_H$
B_PLLFRAC1C2	PLL Fractional Division Ratio Register 1 Channel 2	$15F_H$	07_H
B_PLLFRAC2C2	PLL Fractional Division Ratio Register 2 Channel 2	160_H	09_H
B_PLLINTC3	PLL MMD Integer Value Register Channel 3	161_H	13_H
B_PLLFRAC0C3	PLL Fractional Division Ratio Register 0 Channel 3	162_H	$F3_H$
B_PLLFRAC1C3	PLL Fractional Division Ratio Register 1 Channel 3	163_H	07_H
B_PLLFRAC2C3	PLL Fractional Division Ratio Register 2 Channel 3	164_H	09_H
C_MID0	Message ID Register 0	200_H	00_H
C_MID1	Message ID Register 1	201_H	00_H
C_MID2	Message ID Register 2	202_H	00_H
C_MID3	Message ID Register 3	203_H	00_H
C_MID4	Message ID Register 4	204_H	00_H
C_MID5	Message ID Register 5	205_H	00_H
C_MID6	Message ID Register 6	206_H	00_H
C_MID7	Message ID Register 7	207_H	00_H
C_MID8	Message ID Register 8	208_H	00_H
C_MID9	Message ID Register 9	209_H	00_H
C_MID10	Message ID Register 10	$20A_H$	00_H
C_MID11	Message ID Register 11	$20B_H$	00_H
C_MID12	Message ID Register 12	$20C_H$	00_H
C_MID13	Message ID Register 13	$20D_H$	00_H
C_MID14	Message ID Register 14	$20E_H$	00_H

Table 2 Register Overview and Reset Value (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
C_MID15	Message ID Register 15	$20F_H$	00_H
C_MID16	Message ID Register 16	210_H	00_H
C_MID17	Message ID Register 17	211_H	00_H
C_MID18	Message ID Register 18	212_H	00_H
C_MID19	Message ID Register 19	213_H	00_H
C_MIDC0	Message ID Control Register 0	214_H	00_H
C_MIDC1	Message ID Control Register 1	215_H	00_H
C_IF1	IF1 Register	216_H	20_H
C_WUC	Wake-Up Control Register	217_H	04_H
C_WUPAT0	Wake-Up Pattern Register 0	218_H	00_H
C_WUPAT1	Wake-Up Pattern Register 1	219_H	00_H
C_WUBCNT	Wake-Up Bit or Chip Count Register	$21A_H$	00_H
C_WURSSITH1	RSSI Wake-Up Threshold for Channel 1 Register	$21B_H$	00_H
C_WURSSIBL1	RSSI Wake-Up Blocking Level Low Channel 1 Register	$21C_H$	FF_H
C_WURSSIBH1	RSSI Wake-Up Blocking Level High Channel 1 Register	$21D_H$	00_H
C_WURSSITH2	RSSI Wake-Up Threshold for Channel 2 Register	$21E_H$	00_H
C_WURSSIBL2	RSSI Wake-Up Blocking Level Low Channel 2 Register	$21F_H$	FF_H
C_WURSSIBH2	RSSI Wake-Up Blocking Level High Channel 2 Register	220_H	00_H
C_WURSSITH3	RSSI Wake-Up Threshold for Channel 3 Register	221_H	00_H
C_WURSSIBL3	RSSI Wake-Up Blocking Level Low Channel 3 Register	222_H	FF_H
C_WURSSIBH3	RSSI Wake-Up Blocking Level High Channel 3 Register	223_H	00_H
C_SIGDETSAT	Signal Detector Saturation Threshold Register	224_H	10_H
C_WULOT	Wake-Up on Level Observation Time Register	225_H	00_H
C_SYSRCTO	Synchronization Search Time-Out Register	226_H	87_H
C_TOTIM_SYNC	SYNC Timeout Timer Register	227_H	FF_H
C_TOTIM_TSI	TSI Timeout Timer Register	228_H	00_H
C_TOTIM_EOM	EOM Timeout Timer Register	229_H	00_H
C_AFCLIMIT	AFC Limit Configuration Register	$22A_H$	02_H
C_AFCAGCD	AFC/AGC Freeze Delay Register	$22B_H$	00_H
C_AFCSFCFG	AFC Start/Freeze Configuration Register	$22C_H$	00_H
C_AFCK1CFG0	AFC Integrator 1 Gain Register 0	$22D_H$	00_H
C_AFCK1CFG1	AFC Integrator 1 Gain Register 1	$22E_H$	00_H
C_AFCK2CFG0	AFC Integrator 2 Gain Register 0	$22F_H$	00_H
C_AFCK2CFG1	AFC Integrator 2 Gain Register 1	230_H	00_H

Table 2 Register Overview and Reset Value (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
C_PMFUDSF	Peak Memory Filter Up-Down Factor Register	231_H	42_H
C_AGCSFCFG	AGC Start/Freeze Configuration Register	232_H	00_H
C_AGCCFG0	AGC Configuration Register 0	233_H	$2B_H$
C_AGCCFG1	AGC Configuration Register 1	234_H	03_H
C_AGCTHR	AGC Threshold Register	235_H	08_H
C_DIGRXC	Digital Receiver Configuration Register	236_H	40_H
C_PKBITPOS	RSSI Peak Detector Bit Position Register	237_H	00_H
C_ISUPFCSEL	Image Supression Fc Selection Register	238_H	07_H
C_PDECF	Pre Decimation Factor Register	239_H	00_H
C_PDECSCFSK	Pre Decimation Scaling Register FSK Mode	$23A_H$	00_H
C_PDECSCASK	Pre Decimation Scaling Register ASK Mode	$23B_H$	20_H
C_MFC	Matched Filter Control Register	$23C_H$	07_H
C_SRC	Sampe Rate Converter NCO Tune	$23D_H$	00_H
C_EXTSLC	Externel Data Slicer Configuration	$23E_H$	02_H
C_SIGDET0	Signal Detector Threshold Level Register - Run Mode	$23F_H$	00_H
C_SIGDET1	Signal Detector Threshold Level Register - Wakeup	240_H	00_H
C_SIGDETLO	Signal Detector Threshold Low Level Register	241_H	00_H
C_SIGDETSEL	Signal Detector Range Selection Register	242_H	$7F_H$
C_SIGDETCFG	Signal Detector Configuration Register	243_H	00_H
C_NDTHRES	FSK Noise Detector Threshold Register	244_H	00_H
C_NDCONFIG	FSK Noise Detector Configuration Register	245_H	07_H
C_CDRP	Clock and Data Recovery P Configuration Register	246_H	$E6_H$
C_CDRI	Clock and Data Recovery Configuration Register	247_H	65_H
C_CDRRI	Clock and Data Recovery RUNIN Configuration Register	248_H	01_H
C_CDRTOLC	CDR DC Chip Tolerance Register	249_H	$0C_H$
C_CDRTOLB	CDR DC Bit Tolerance Register	$24A_H$	$1E_H$
C_TVWIN	Timing Violation Window Register	$24B_H$	28_H
C_SLCCFG	Slicer Configuration Register	$24C_H$	90_H
C_TSIMODE	TSI Detection Mode Register	$24D_H$	80_H
C_TSILENA	TSI Length Register A	$24E_H$	00_H
C_TSILENB	TSI Length Register B	$24F_H$	00_H
C_TSIGAP	TSI Gap Length Register	250_H	00_H
C_TSIPTA0	TSI Pattern Data Reference A Register 0	251_H	00_H
C_TSIPTA1	TSI Pattern Data Reference A Register 1	252_H	00_H
C_TSIPTB0	TSI Pattern Data Reference B Register 0	253_H	00_H

Table 2 Register Overview and Reset Value (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
C_TSIPTB1	TSI Pattern Data Reference B Register 1	254_H	00_H
C_EOMC	End Of Message Control Register	255_H	05_H
C_EOMDLEN	EOM Data Length Limit Register	256_H	00_H
C_EOMDLENP	EOM Data Length Limit Parallel Mode Register	257_H	00_H
C_CHCFG	Channel Configuration Register	258_H	04_H
C_PLLINTC1	PLL MMD Integer Value Register Channel 1	259_H	93_H
C_PLLFRAC0C1	PLL Fractional Division Ratio Register 0 Channel 1	$25A_H$	$F3_H$
C_PLLFRAC1C1	PLL Fractional Division Ratio Register 1 Channel 1	$25B_H$	07_H
C_PLLFRAC2C1	PLL Fractional Division Ratio Register 2 Channel 1	$25C_H$	09_H
C_PLLINTC2	PLL MMD Integer Value Register Channel 2	$25D_H$	13_H
C_PLLFRAC0C2	PLL Fractional Division Ratio Register 0 Channel 2	$25E_H$	$F3_H$
C_PLLFRAC1C2	PLL Fractional Division Ratio Register 1 Channel 2	$25F_H$	07_H
C_PLLFRAC2C2	PLL Fractional Division Ratio Register 2 Channel 2	260_H	09_H
C_PLLINTC3	PLL MMD Integer Value Register Channel 3	261_H	13_H
C_PLLFRAC0C3	PLL Fractional Division Ratio Register 0 Channel 3	262_H	$F3_H$
C_PLLFRAC1C3	PLL Fractional Division Ratio Register 1 Channel 3	263_H	07_H
C_PLLFRAC2C3	PLL Fractional Division Ratio Register 2 Channel 3	264_H	09_H
D_MID0	Message ID Register 0	300_H	00_H
D_MID1	Message ID Register 1	301_H	00_H
D_MID2	Message ID Register 2	302_H	00_H
D_MID3	Message ID Register 3	303_H	00_H
D_MID4	Message ID Register 4	304_H	00_H
D_MID5	Message ID Register 5	305_H	00_H
D_MID6	Message ID Register 6	306_H	00_H
D_MID7	Message ID Register 7	307_H	00_H
D_MID8	Message ID Register 8	308_H	00_H
D_MID9	Message ID Register 9	309_H	00_H
D_MID10	Message ID Register 10	$30A_H$	00_H
D_MID11	Message ID Register 11	$30B_H$	00_H
D_MID12	Message ID Register 12	$30C_H$	00_H
D_MID13	Message ID Register 13	$30D_H$	00_H
D_MID14	Message ID Register 14	$30E_H$	00_H
D_MID15	Message ID Register 15	$30F_H$	00_H
D_MID16	Message ID Register 16	310_H	00_H
D_MID17	Message ID Register 17	311_H	00_H
D_MID18	Message ID Register 18	312_H	00_H
D_MID19	Message ID Register 19	313_H	00_H
D_MIDC0	Message ID Control Register 0	314_H	00_H

Table 2 Register Overview and Reset Value (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
D_MIDC1	Message ID Control Register 1	315_H	00_H
D_IF1	IF1 Register	316_H	20_H
D_WUC	Wake-Up Control Register	317_H	04_H
D_WUPAT0	Wake-Up Pattern Register 0	318_H	00_H
D_WUPAT1	Wake-Up Pattern Register 1	319_H	00_H
D_WUBCNT	Wake-Up Bit or Chip Count Register	$31A_H$	00_H
D_WURSSITH1	RSSI Wake-Up Threshold for Channel 1 Register	$31B_H$	00_H
D_WURSSIBL1	RSSI Wake-Up Blocking Level Low Channel 1 Register	$31C_H$	FF_H
D_WURSSIBH1	RSSI Wake-Up Blocking Level High Channel 1 Register	$31D_H$	00_H
D_WURSSITH2	RSSI Wake-Up Threshold for Channel 2 Register	$31E_H$	00_H
D_WURSSIBL2	RSSI Wake-Up Blocking Level Low Channel 2 Register	$31F_H$	FF_H
D_WURSSIBH2	RSSI Wake-Up Blocking Level High Channel 2 Register	320_H	00_H
D_WURSSITH3	RSSI Wake-Up Threshold for Channel 3 Register	321_H	00_H
D_WURSSIBL3	RSSI Wake-Up Blocking Level Low Channel 3 Register	322_H	FF_H
D_WURSSIBH3	RSSI Wake-Up Blocking Level High Channel 3 Register	323_H	00_H
D_SIGDETSAT	Signal Detector Saturation Threshold Register	324_H	10_H
D_WULOT	Wake-Up on Level Observation Time Register	325_H	00_H
D_SYSRCTO	Synchronization Search Time-Out Register	326_H	87_H
D_TOTIM_SYNC	SYNC Timeout Timer Register	327_H	FF_H
D_TOTIM_TSI	TSI Timeout Timer Register	328_H	00_H
D_TOTIM_EOM	EOM Timeout Timer Register	329_H	00_H
D_AFCLIMIT	AFC Limit Configuration Register	$32A_H$	02_H
D_AFCAGCD	AFC/AGC Freeze Delay Register	$32B_H$	00_H
D_AFCSFCFG	AFC Start/Freeze Configuration Register	$32C_H$	00_H
D_AFCK1CFG0	AFC Integrator 1 Gain Register 0	$32D_H$	00_H
D_AFCK1CFG1	AFC Integrator 1 Gain Register 1	$32E_H$	00_H
D_AFCK2CFG0	AFC Integrator 2 Gain Register 0	$32F_H$	00_H
D_AFCK2CFG1	AFC Integrator 2 Gain Register 1	330_H	00_H
D_PMFUDSF	Peak Memory Filter Up-Down Factor Register	331_H	42_H
D_AGCSFCFG	AGC Start/Freeze Configuration Register	332_H	00_H
D_AGCCFG0	AGC Configuration Register 0	333_H	$2B_H$
D_AGCCFG1	AGC Configuration Register 1	334_H	03_H
D_AGCTHR	AGC Threshold Register	335_H	08_H
D_DIGRXC	Digital Receiver Configuration Register	336_H	40_H

Table 2 Register Overview and Reset Value (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
D_PKBITPOS	RSSI Peak Detector Bit Position Register	337_H	00_H
D_ISUPFCSEL	Image Supression Fc Selection Register	338_H	07_H
D_PDECF	Pre Decimation Factor Register	339_H	00_H
D_PDECSCFSK	Pre Decimation Scaling Register FSK Mode	$33A_H$	00_H
D_PDECSCASK	Pre Decimation Scaling Register ASK Mode	$33B_H$	20_H
D_MFC	Matched Filter Control Register	$33C_H$	07_H
D_SRC	Sampe Rate Converter NCO Tune	$33D_H$	00_H
D_EXTSLC	Externel Data Slicer Configuration	$33E_H$	02_H
D_SIGDET0	Signal Detector Threshold Level Register - Run Mode	$33F_H$	00_H
D_SIGDET1	Signal Detector Threshold Level Register - Wakeup	340_H	00_H
D_SIGDETLO	Signal Detector Threshold Low Level Register	341_H	00_H
D_SIGDETSEL	Signal Detector Range Selection Register	342_H	$7F_H$
D_SIGDETCFG	Signal Detector Configuration Register	343_H	00_H
D_NDTHRES	FSK Noise Detector Threshold Register	344_H	00_H
D_NDCONFIG	FSK Noise Detector Configuration Register	345_H	07_H
D_CDRP	Clock and Data Recovery P Configuration Register	346_H	$E6_H$
D_CDRI	Clock and Data Recovery Configuration Register	347_H	65_H
D_CDRRI	Clock and Data Recovery RUNIN Configuration Register	348_H	01_H
D_CDRTOLC	CDR DC Chip Tolerance Register	349_H	$0C_H$
D_CDRTOLB	CDR DC Bit Tolerance Register	$34A_H$	$1E_H$
D_TVWIN	Timing Violation Window Register	$34B_H$	28_H
D_SLCCFG	Slicer Configuration Register	$34C_H$	90_H
D_TSIMODE	TSI Detection Mode Register	$34D_H$	80_H
D_TSILENA	TSI Length Register A	$34E_H$	00_H
D_TSILENB	TSI Length Register B	$34F_H$	00_H
D_TSIGAP	TSI Gap Length Register	350_H	00_H
D_TSIPTA0	TSI Pattern Data Reference A Register 0	351_H	00_H
D_TSIPTA1	TSI Pattern Data Reference A Register 1	352_H	00_H
D_TSIPTB0	TSI Pattern Data Reference B Register 0	353_H	00_H
D_TSIPTB1	TSI Pattern Data Reference B Register 1	354_H	00_H
D_EOMC	End Of Message Control Register	355_H	05_H
D_EOMDLEN	EOM Data Length Limit Register	356_H	00_H
D_EOMDLENP	EOM Data Length Limit Parallel Mode Register	357_H	00_H
D_CHCFG	Channel Configuration Register	358_H	04_H
D_PLLINTC1	PLL MMD Integer Value Register Channel 1	359_H	93_H

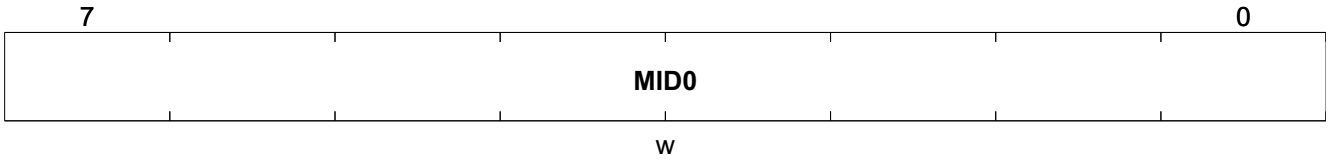
Table 2 Register Overview and Reset Value (cont'd)

Register Short Name	Register Long Name	Offset Address	Reset Value
D_PLLFRAC0C1	PLL Fractional Division Ratio Register 0 Channel 1	$35A_H$	$F3_H$
D_PLLFRAC1C1	PLL Fractional Division Ratio Register 1 Channel 1	$35B_H$	07_H
D_PLLFRAC2C1	PLL Fractional Division Ratio Register 2 Channel 1	$35C_H$	09_H
D_PLLINTC2	PLL MMD Integer Value Register Channel 2	$35D_H$	13_H
D_PLLFRAC0C2	PLL Fractional Division Ratio Register 0 Channel 2	$35E_H$	$F3_H$
D_PLLFRAC1C2	PLL Fractional Division Ratio Register 1 Channel 2	$35F_H$	07_H
D_PLLFRAC2C2	PLL Fractional Division Ratio Register 2 Channel 2	360_H	09_H
D_PLLINTC3	PLL MMD Integer Value Register Channel 3	361_H	13_H
D_PLLFRAC0C3	PLL Fractional Division Ratio Register 0 Channel 3	362_H	$F3_H$
D_PLLFRAC1C3	PLL Fractional Division Ratio Register 1 Channel 3	363_H	07_H
D_PLLFRAC2C3	PLL Fractional Division Ratio Register 2 Channel 3	364_H	09_H

Register Description

Message ID Register 0

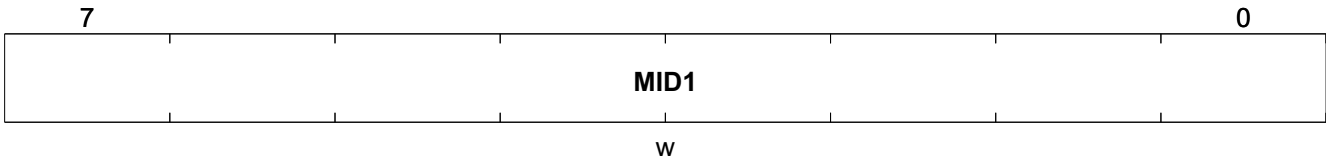
A_MID0 | **Offset** | **Reset Value**
Message ID Register 0 | **000_H** | **00_H**



Field	Bits	Type	Description
MID0	7:0	w	**Message ID Register 0** Reset: 00_H

Message ID Register 1

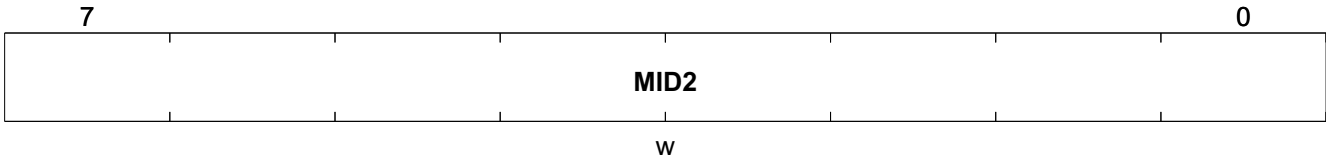
A_MID1 | **Offset** | **Reset Value**
Message ID Register 1 | **001_H** | **00_H**



Field	Bits	Type	Description
MID1	7:0	w	**Message ID Register 1** Reset: 00_H

Message ID Register 2

A_MID2 | **Offset** | **Reset Value**
Message ID Register 2 | **002_H** | **00_H**

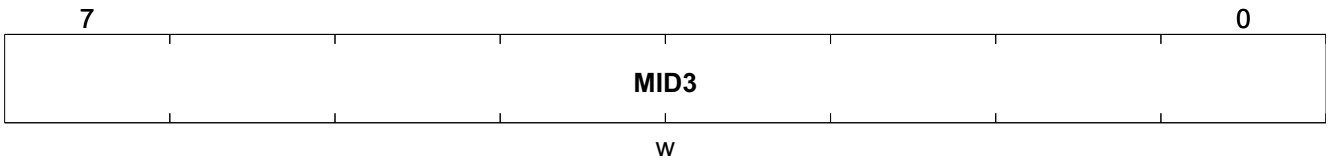


Field	Bits	Type	Description
MID2	7:0	w	**Message ID Register 2** Reset: 00_H

Message ID Register 3

A_MID3 **Offset** **Reset Value**

Message ID Register 3 **003_H** **00_H**

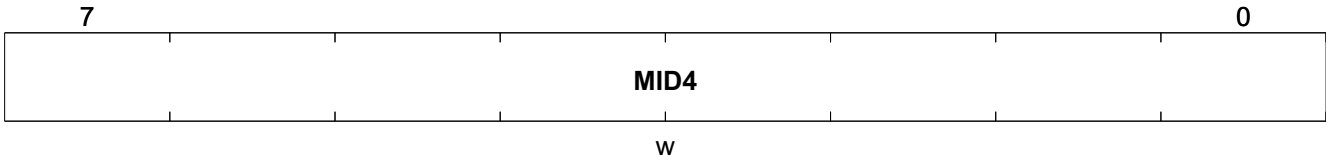


Field	Bits	Type	Description
MID3	7:0	w	**Message ID Register 3** Reset: 00_H

Message ID Register 4

A_MID4 **Offset** **Reset Value**

Message ID Register 4 **004_H** **00_H**

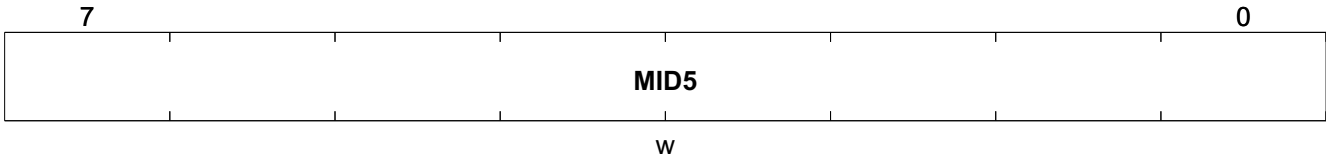


Field	Bits	Type	Description
MID4	7:0	w	**Message ID Register 4** Reset: 00_H

Message ID Register 5

A_MID5 **Offset** **Reset Value**

Message ID Register 5 **005_H** **00_H**

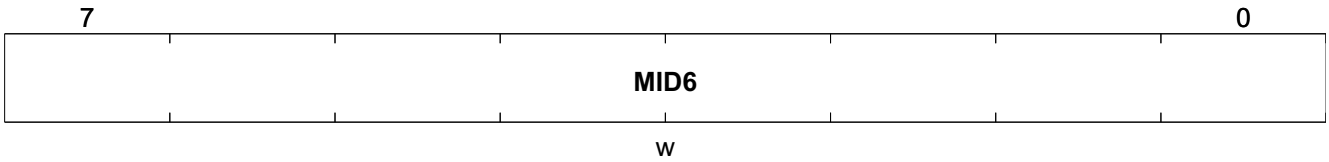


Field	Bits	Type	Description
MID5	7:0	w	**Message ID Register 5** Reset: 00_H

Message ID Register 6

A_MID6 **Offset** **Reset Value**

Message ID Register 6 **006_H** **00_H**

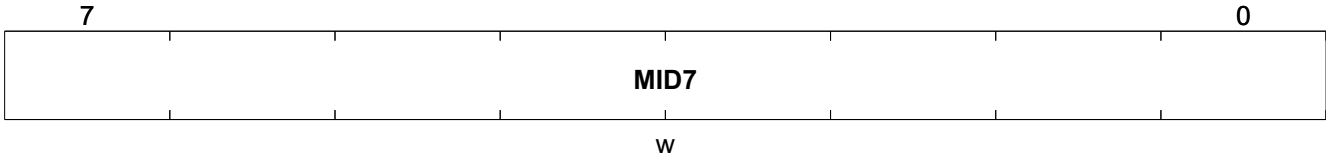


Field	Bits	Type	Description
MID6	7:0	w	**Message ID Register 6** Reset: 00_H

Message ID Register 7

A_MID7 **Offset** **Reset Value**

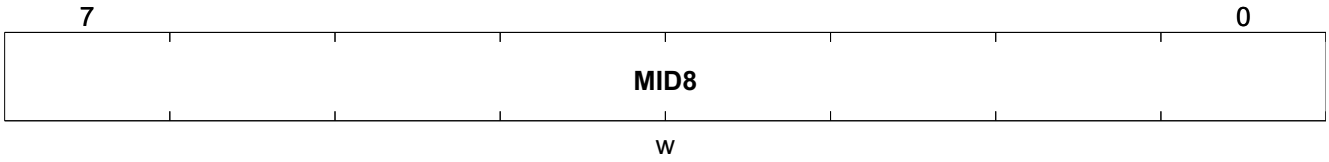
Message ID Register 7 **007_H** **00_H**



Field	Bits	Type	Description
MID7	7:0	w	**Message ID Register 7** Reset: 00_H

Message ID Register 8

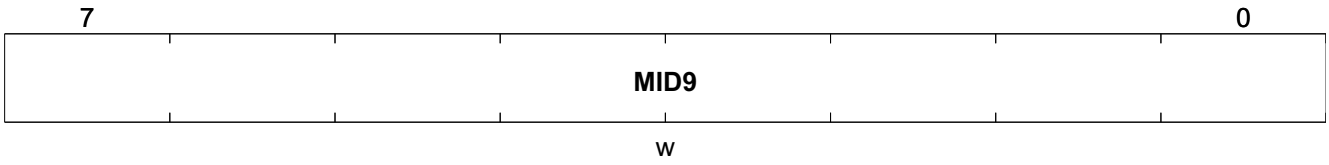
A_MID8	Offset	Reset Value
Message ID Register 8	008_H	00_H



Field	Bits	Type	Description
MID8	7:0	w	**Message ID Register 8** Reset: 00_H

Message ID Register 9

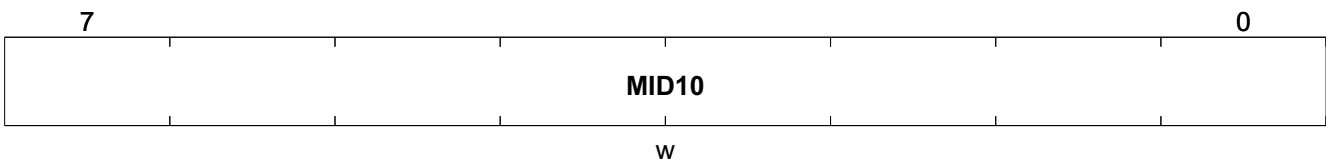
A_MID9	Offset	Reset Value
Message ID Register 9	009_H	00_H



Field	Bits	Type	Description
MID9	7:0	w	**Message ID Register 9** Reset: 00_H

Message ID Register 10

A_MID10	Offset	Reset Value
Message ID Register 10	$00A_H$	00_H

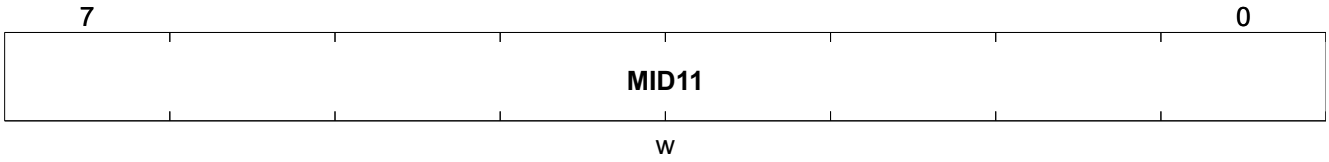


Field	Bits	Type	Description
MID10	7:0	w	**Message ID Register 10** Reset: 00_H

Message ID Register 11

A_MID11 **Offset** **Reset Value**

Message ID Register 11 **$00B_H$** **00_H**

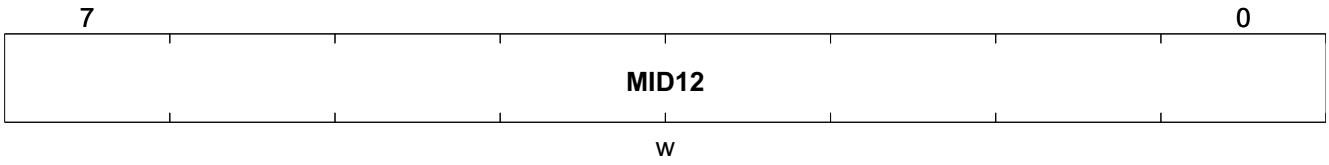


Field	Bits	Type	Description
MID11	7:0	w	**Message ID Register 11** Reset: 00_H

Message ID Register 12

A_MID12 **Offset** **Reset Value**

Message ID Register 12 **$00C_H$** **00_H**

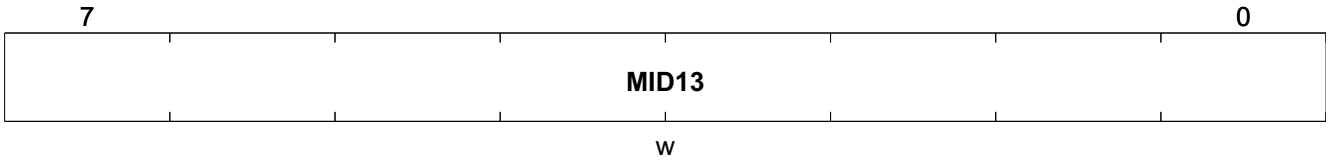


Field	Bits	Type	Description
MID12	7:0	w	**Message ID Register 12** Reset: 00_H

Message ID Register 13

A_MID13 **Offset** **Reset Value**

Message ID Register 13 **$00D_H$** **00_H**

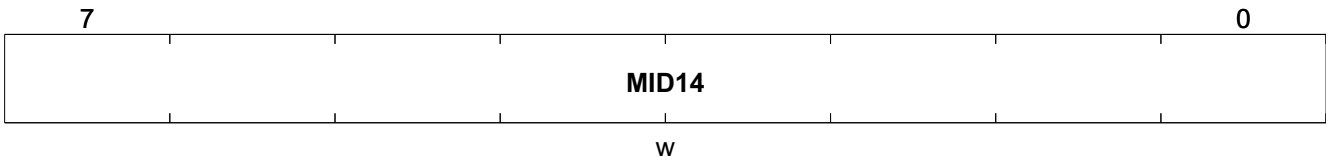


Field	Bits	Type	Description
MID13	7:0	w	**Message ID Register 13** Reset: 00_H

Message ID Register 14

A_MID14 **Offset** **Reset Value**

Message ID Register 14 **$00E_H$** **00_H**

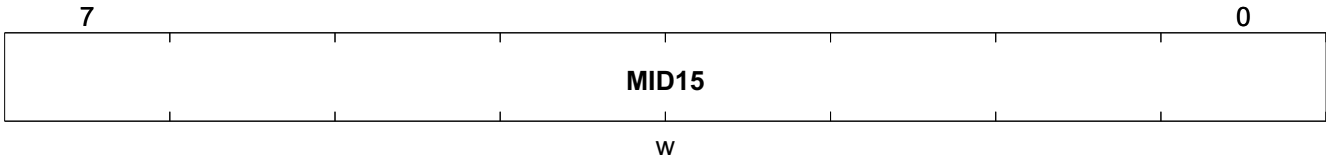


Field	Bits	Type	Description
MID14	7:0	w	**Message ID Register 14** Reset: 00_H

Message ID Register 15

A_MID15 **Offset** **Reset Value**

Message ID Register 15 **$00F_H$** **00_H**

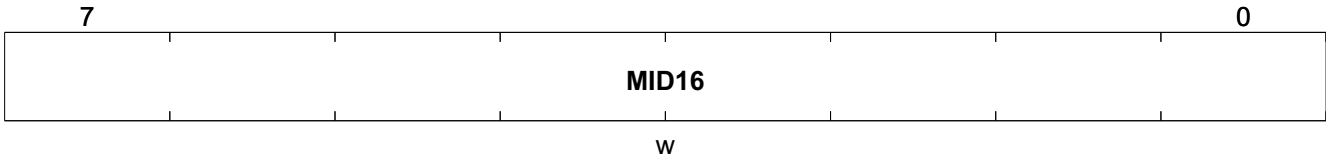


Field	Bits	Type	Description
MID15	7:0	w	**Message ID Register 15** Reset: 00_H

Message ID Register 16

A_MID16 | **Offset** | **Reset Value**

Message ID Register 16 | **010_H** | **00_H**

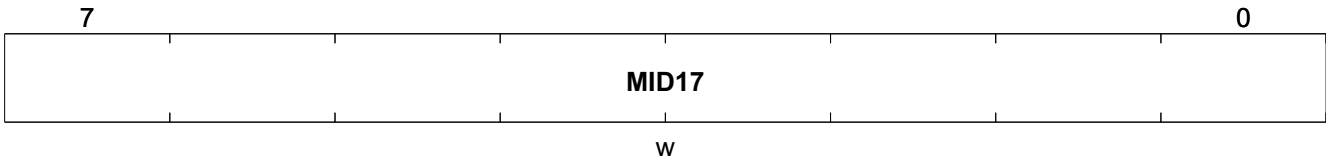


Field	Bits	Type	Description
MID16	7:0	w	**Message ID Register 16** Reset: 00_H

Message ID Register 17

A_MID17 | **Offset** | **Reset Value**

Message ID Register 17 | **011_H** | **00_H**

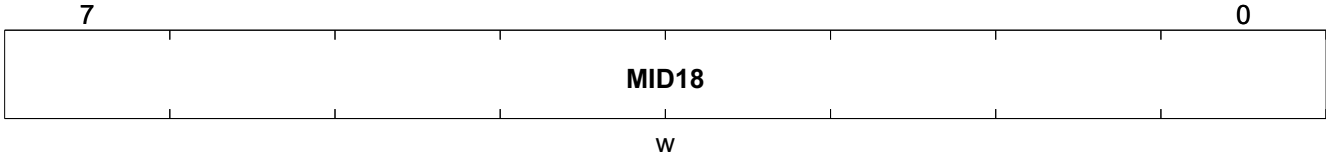


Field	Bits	Type	Description
MID17	7:0	w	**Message ID Register 17** Reset: 00_H

Message ID Register 18

A_MID18 | **Offset** | **Reset Value**

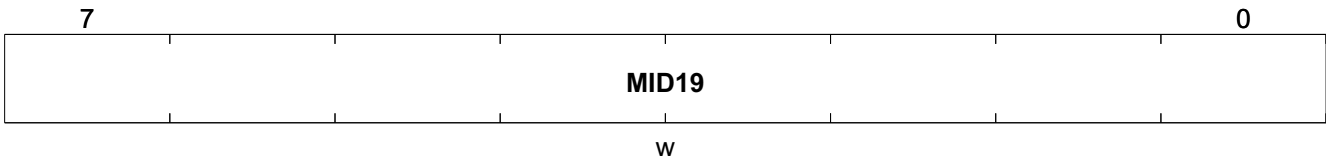
Message ID Register 18 | **012_H** | **00_H**



Field	Bits	Type	Description
MID18	7:0	w	**Message ID Register 18** Reset: 00_H

Message ID Register 19

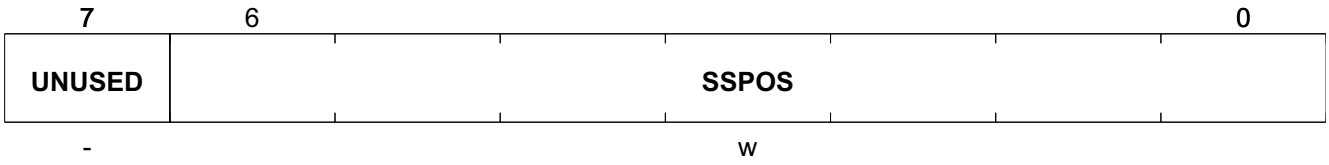
A_MID19	Offset	Reset Value
Message ID Register 19	013_H	00_H



Field	Bits	Type	Description
MID19	7:0	w	**Message ID Register 19** Reset: 00_H

Message ID Control Register 0

A_MIDC0	Offset	Reset Value
Message ID Control Register 0	014_H	00_H



Field	Bits	Type	Description
UNUSED	7	-	**UNUSED** Reset: 0_H
SSPOS	6:0	w	**Message ID Scan Start Position** Min: 00h = Comparision starts one Bit after FSYNC Max: 7F = Comparision starts 128 Bits after FSYNC Reset: 00_H

Message ID Control Register 1

A_MIDC1	Offset	Reset Value
Message ID Control Register 1	015_H	00_H

7	6	5	4	3	2	1	0
UNUSED				MIDSEN	MIDBO	MIDNTS	
-				w	w	w	

Field	Bits	Type	Description
UNUSED	7:4	-	**UNUSED** Reset: 0_H
MIDSEN	3	w	**Enable Message ID Screening** 0_B Disabled 1_B Enabled Reset: 0_H
MIDBO	2	w	**Message ID Byte Organisation** 0_B 2 Byte Mode 1_B 4 Byte Mode Reset: 0_H
MIDNTS	1:0	w	**Message ID Number of Bytes To Scan (4 Byte Mode / 2 Byte Mode)** 00_B 1 Byte to scan / 1 Byte to scan 01_B 2 Bytes to scan / 2 Bytes to scan 10_B 3 Bytes to scan / 2 Bytes to scan 11_B 4 Bytes to scan / 2 Bytes to scan Reset: 0_H

IF1 Register

A_IF1	Offset	Reset Value
IF1 Register	**016_H**	**20_H**

7	6	5	4	3	2	1	0
UNUSED	SSBSEL	BPFBWSEL			SDCSEL	IFBUFEN	CERFSEL
-	w	w			w	w	w

Field	Bits	Type	Description
UNUSED	7	-	**UNUSED** Reset: 0_H
SSBSEL	6	w	**RXRF Receive Side Band Select** 0_B RF = LO + IF1 (Lo-side LO-injection) 1_B RF = LO - IF1 (Hi-side LO-injection) Reset: 0_H

Field	Bits	Type	Description
BPFBWSEL	5:3	w	**Band Pass Filter Bandwidth Selection** 000_B 50 kHz 001_B 80 kHz 010_B 125 kHz 011_B 200 kHz 100_B 300 kHz 101_B not used 110_B not used 111_B not used Reset: 4_H
SDCSEL	2	w	**Single / Double Conversion Selection** 0_B Double Conversion (10.7 MHz/274 kHz) 1_B Single Conversion (274 kHz) Reset: 0_H
IFBUFEN	1	w	**IF Buffer Enable** 0_B Disabled 1_B Enabled Reset: 0_H
CERFSEL	0	w	**Number of external Ceramic Filters** 0_B 1 Ceramic Filter 1_B 2 Ceramic Filters Reset: 0_H

Wake-Up Control Register

A_WUC	Offset	Reset Value
Wake-Up Control Register	**017_H**	**04_H**

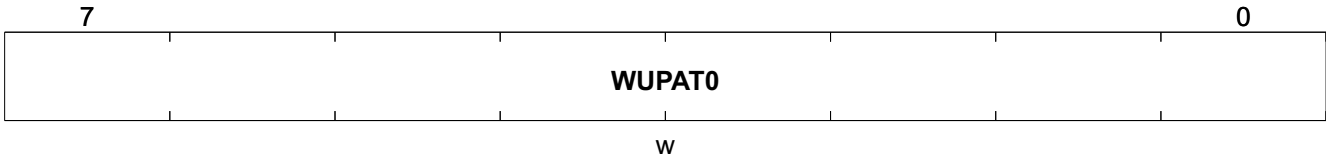
7	6	5	4	3	2	1	0
UNUSED	**PWUEN**	**WUPMSEL**	**WULCUFFB**	**UFFBLCOO**	**WUCRT**		
-	w	w	w	w	w		

Field	Bits	Type	Description
UNUSED	7	-	**UNUSED** Reset: 0_H
PWUEN	6	w	**Parallel Wake Up Mode Enable** This feature can only be used, when modulation type is the same for SPM and RMSP 0_B Disabled 1_B Enabled Reset: 0_H

Field	Bits	Type	Description
WUPMSEL	5	w	**Wake Up Pattern Mode Selection** 0_B Chip mode 1_B Bit mode Reset: 0_H
WULCUFFB	4	w	**Select a "Wake Up on Level Criterion", when UFFBLCOO is enabled.** 0_B RSSI automatically selected, when A_CHCFG.EXTPROC = "10" 1_B Signal Recognition Reset: 0_H
UFFBLCOO	3	w	**Ultrafast Fall Back to SLEEP or additional Level criterion in Constant On Off.** Enables additional parallel processing of "Level Criterion", when a "Data Criterion" is selected in WUCRT. In case of Fast Fall Back to SLEEP or Permanent Wake-Up Search, this mode is called UFFB (Ultrafast Fall Back). Same Mode can be used in Constant On-Off. 0_B Disabled 1_B Enabled Reset: 0_H
WUCRT	2:0	w	**Select a "Wake Up Criterion"** 000_B Pattern Detection (Data Criterion) When A_CHCFG.EXTROC = "01" this setting is mapped to 0x3 001_B Random Bits (Data Criterion) When A_CHCFG.EXTROC = "01" this setting is mapped to 0x3 010_B Equal Bits (Data Criterion) When A_CHCFG.EXTROC = "01" this setting is mapped to 0x3 011_B Wake Up on Symbol Sync, Valid Data Rate (Data Criterion); The A_WUBCNT Register is not used in this mode 100_B RSSI (Level Criterion) automatically selected, when A_CHCFG.EXTPROC = "10" 101_B Signal Recognition (Level Criterion) 110_B n.u. 111_B n.u. Reset: 4_H

Wake-Up Pattern Register 0

A_WUPAT0	Offset	Reset Value
Wake-Up Pattern Register 0	**018_H**	**00_H**

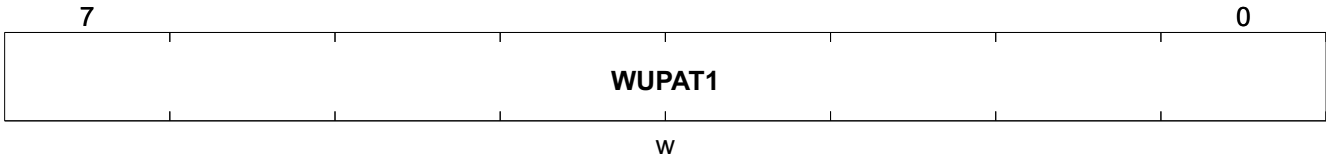


Field	Bits	Type	Description
WUPAT0	7:0	w	**Wake Up Detection Pattern: Bit 7...Bit 0(LSB) (in Bits/Chips)** Reset: 00_H

Wake-Up Pattern Register 1

A_WUPAT1 **Offset** **Reset Value**

Wake-Up Pattern Register 1 **019_H** **00_H**

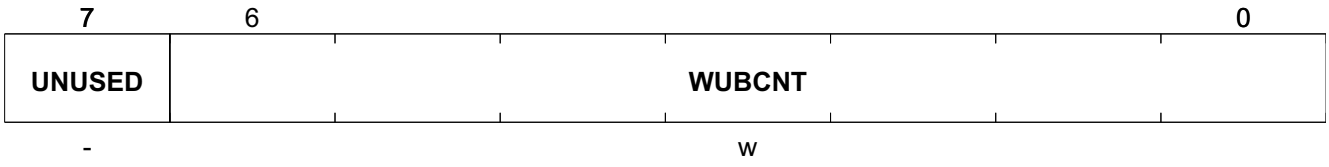


Field	Bits	Type	Description
WUPAT1	7:0	w	**Wake Up Detection Pattern: (MSB) Bit 15...Bit 8 (in Bits/Chips)** Reset: 00_H

Wake-Up Bit or Chip Count Register

A_WUBCNT **Offset** **Reset Value**

Wake-Up Bit or Chip Count Register **$01A_H$** **00_H**

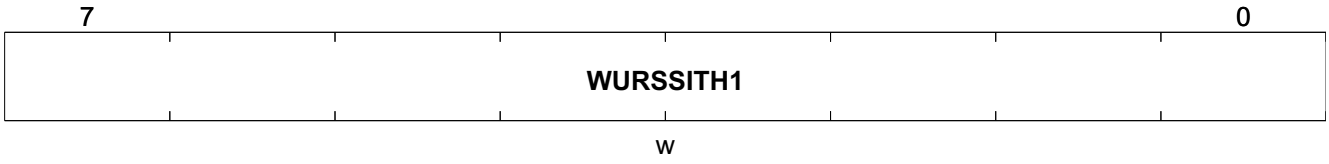


Field	Bits	Type	Description
UNUSED	7	-	**UNUSED** Reset: 0_H

Field	Bits	Type	Description
WUBCNT	6:0	w	**Wake Up Bit/Chip Count Register (unit is bits; only exception is WU Pattern Chip Mode, where unit is chips, see A_WUC.WUPMSEL)** Counter Register to define the maximum counts of bits/chips for Wake Up detection. Min: 00h = 0 Bits/Chips to count In Random Bits or Equal Bits Mode this will cause a Wake Up on Data Criterion immediately after Symbol Synchronization is found. In Pattern Detection Mode this will cause no Wake Up on Data Criterion. In this Mode there is needed minimum 11h = 17 Bits/Chips to shift one Pattern through the whole Pattern Detector. Because comparision can only be started when at least the comparision register is completely filled. Max: 7Fh: 127 Bits/Chips to count after Symbol Sync found Reset: 00_H

RSSI Wake-Up Threshold for Channel 1 Register

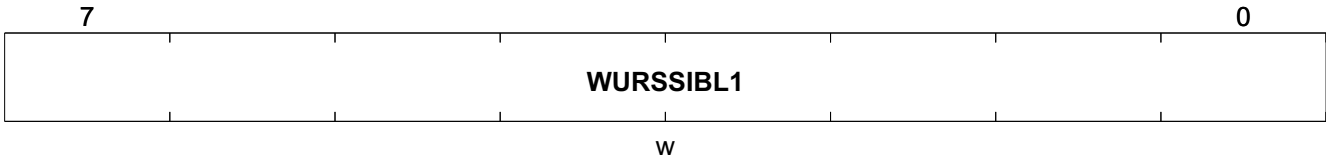
A_WURSSITH1	Offset	Reset Value
RSSI Wake-Up Threshold for Channel 1 Register	**$01B_H$**	**00_H**



Field	Bits	Type	Description
WURSSITH1	7:0	w	**Wake Up on RSSI Threshold level for Channel 1** Wake Up Request generated when actual RSSI level is above this threshold Reset: 00_H

RSSI Wake-Up Blocking Level Low Channel 1 Register

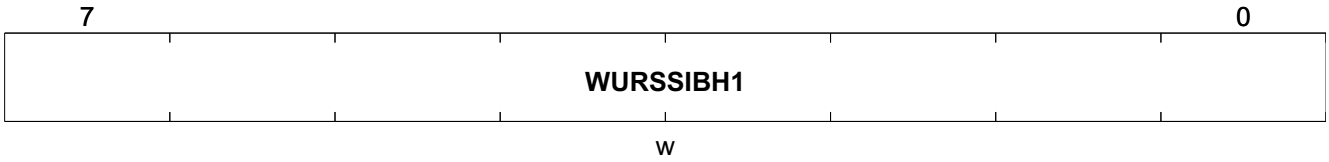
A_WURSSIBL1	Offset	Reset Value
RSSI Wake-Up Blocking Level Low Channel 1 Register	**$01C_H$**	**FF_H**



Field	Bits	Type	Description
WURSSIBL1	7:0	w	**Wake Up on RSSI Blocking Level LOW for Channel 1** Reset: FF_H

RSSI Wake-Up Blocking Level High Channel 1 Register

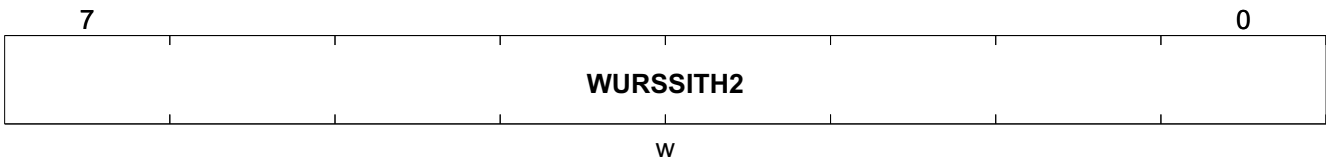
A_WURSSIBH1	Offset	Reset Value
RSSI Wake-Up Blocking Level High Channel 1 Register	**$01D_H$**	**00_H**



Field	Bits	Type	Description
WURSSIBH1	7:0	w	**Wake Up on RSSI Blocking Level HIGH for Channel 1, when RSSI is selected as WU criterion or FFB criterion.** In case of Signal Recognition as WU criterion or FFB criterion, the register defines the minimum consecutive T/16 samples of the Signal Recognition output to be at high level for a positive wake up event generation or FFB generation Reset: 00_H

RSSI Wake-Up Threshold for Channel 2 Register

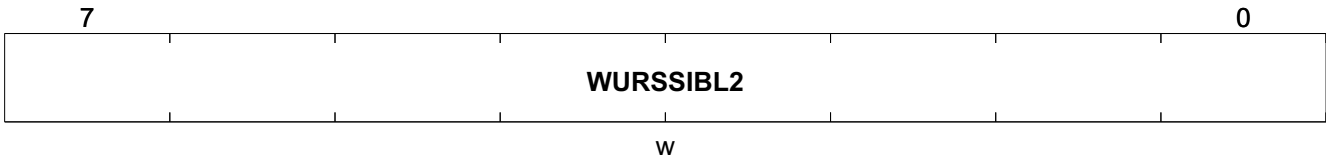
A_WURSSITH2	Offset	Reset Value
RSSI Wake-Up Threshold for Channel 2 Register	**$01E_H$**	**00_H**



Field	Bits	Type	Description
WURSSITH2	7:0	w	**Wake Up on RSSI Threshold level for Channel 2** Wake Up Request generated when actual RSSI level is above this threshold Reset: 00_H

RSSI Wake-Up Blocking Level Low Channel 2 Register

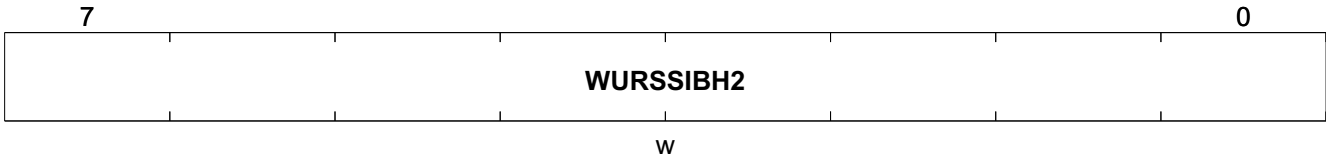
A_WURSSIBL2	Offset	Reset Value
RSSI Wake-Up Blocking Level Low Channel 2 Register	**$01F_H$**	**FF_H**



Field	Bits	Type	Description
WURSSIBL2	7:0	w	**Wake Up on RSSI Blocking Level LOW for Channel 2** Reset: FF_H

RSSI Wake-Up Blocking Level High Channel 2 Register

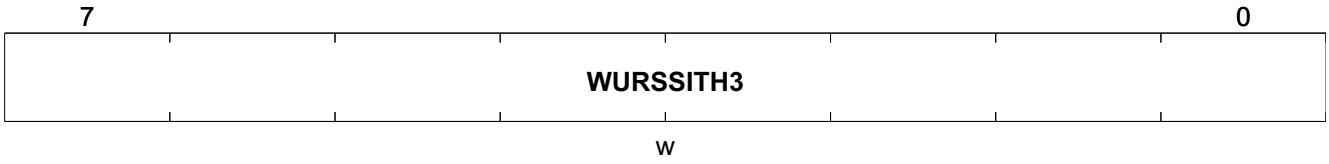
A_WURSSIBH2	Offset	Reset Value
RSSI Wake-Up Blocking Level High Channel 2 Register	**020_H**	**00_H**



Field	Bits	Type	Description
WURSSIBH2	7:0	w	**Wake Up on RSSI Blocking Level HIGH for Channel 2, when RSSI is selected as WU criterion or FFB criterion.** In case of Signal Recognition as WU criterion or FFB criterion, the register defines the minimum consecutive T/16 samples of the Signal Recognition output to be at high level for a positive wake up event generation or FFB generation Reset: 00_H

RSSI Wake-Up Threshold for Channel 3 Register

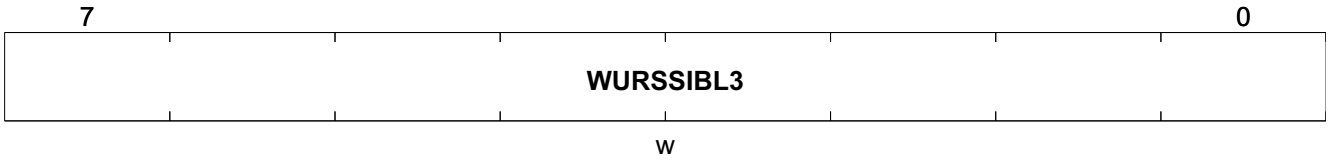
A_WURSSITH3	Offset	Reset Value
RSSI Wake-Up Threshold for Channel 3 Register	021_H	00_H



Field	Bits	Type	Description
WURSSITH3	7:0	w	**Wake Up on RSSI Threshold level for Channel 3** Wake Up Request generated when actual RSSI level is above this threshold Reset: 00_H

RSSI Wake-Up Blocking Level Low Channel 3 Register

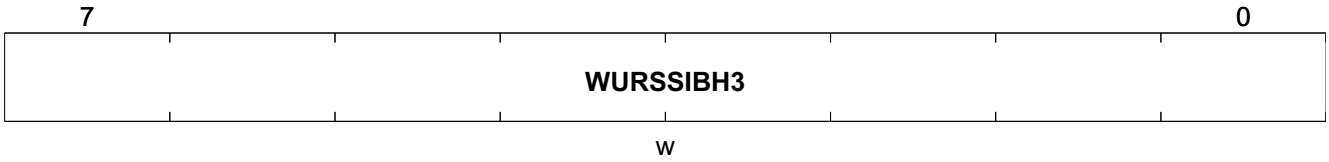
A_WURSSIBL3	Offset	Reset Value
RSSI Wake-Up Blocking Level Low Channel 3 Register	022_H	FF_H



Field	Bits	Type	Description
WURSSIBL3	7:0	w	**Wake Up on RSSI Blocking Level LOW for Channel 3** Reset: FF_H

RSSI Wake-Up Blocking Level High Channel 3 Register

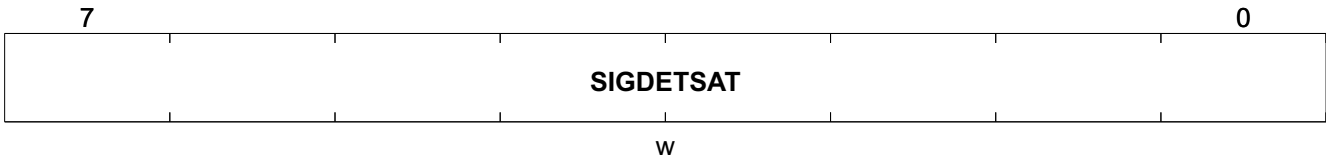
A_WURSSIBH3	Offset	Reset Value
RSSI Wake-Up Blocking Level High Channel 3 Register	023_H	00_H



Field	Bits	Type	Description
WURSSIBH3	7:0	w	**Wake Up on RSSI Blocking Level HIGH for Channel 3, when RSSI is selected as WU criterion or FFB criterion.** In case of Signal Recognition as WU criterion or FFB criterion, the register defines the minimum consecutive T/16 samples of the Signal Recognition output to be at high level for a positive wake up event generation or FFB generation Reset: 00_H

Signal Detector Saturation Threshold Register

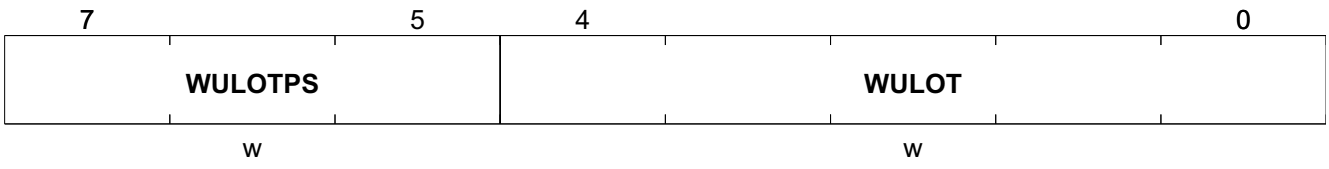
A_SIGDETSAT	Offset	Reset Value
Signal Detector Saturation Threshold Register	**024_H**	**10_H**



Field	Bits	Type	Description
SIGDETSAT	7:0	w	**Saturation threshold of the Sigdet peak detector used for zero-tube threshold calculation.** Reset: 10_H

Wake-up on Level Observation Time Register

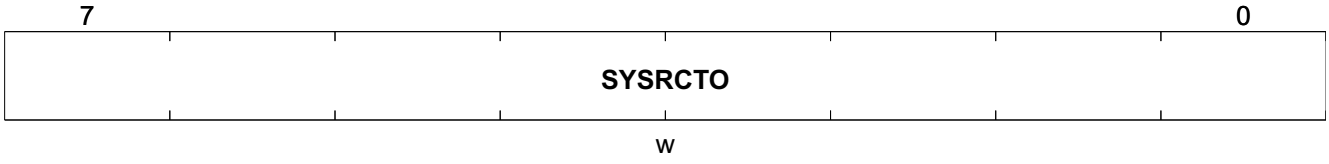
A_WULOT	Offset	Reset Value
Wake-up on Level Observation Time Register	**025_H**	**00_H**



Field	Bits	Type	Description
WULOTPS	7:5	w	**Wake-Up Level Observation Time PreScaler** 000_B 4 001_B 8 010_B 16 011_B 32 100_B 64 101_B 128 110_B 256 111_B 512 Reset: 0_H
WULOT	4:0	w	**Wake-Up Level Observation Time** Min. 01h : Twulot = 1 * WULOTPS * 64 / Fsys Max 1Fh : Twulot = 31 * WULOTPS * 64 / Fsys Value 00h : Twulot = 32 * WULOTPS * 64 / Fsys Reset: 00_H

Synchronization Search Time-Out Register

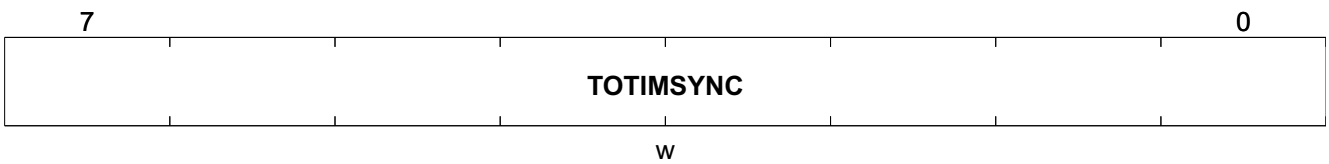
A_SYSRCTO	Offset	Reset Value
Synchronization Search Time-Out Register	**026_H**	**87_H**



Field	Bits	Type	Description
SYSRCTO	7:0	w	**Synchronization search time out** FFh: 15 15/16 bit 00h: 0 bit Reset: 87_H

SYNC Timeout Timer Register

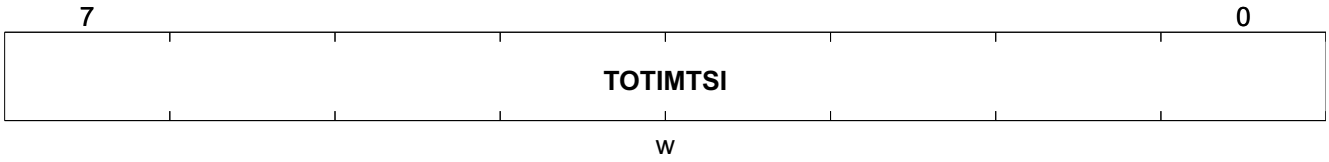
A_TOTIM_SYNC	Offset	Reset Value
SYNC Timeout Timer Register	**027_H**	**FF_H**



Field	Bits	Type	Description
TOTIMSYNC	7:0	w	**Set value of Time-Out Timer (Symbol Synchronization)** Timer is used to get back from Run Mode Self Polling to the Self Polling Mode whenever there is no Symbol Synchronization. Timer is set back at new cycle start of Run Mode Self Polling. TimeOut= (TOTIMSYNC * 64 * 512) / fsys Min: 01h = (1 * 64 * 512)/ fsys Max: FFh= (255 * 64 * 512) / fsys 00h: disabled Reset: FF_H

TSI Timeout Timer Register

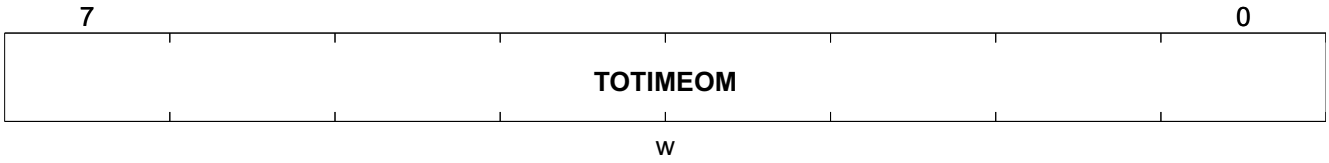
A_TOTIM_TSI	Offset	Reset Value
TSI Timeout Timer Register	**028_H**	**00_H**



Field	Bits	Type	Description
TOTIMTSI	7:0	w	**Set value of Time-Out Timer (Telegram Start Identifier)** Timer is used to get back from Run Mode Self Polling to the Self Polling Mode whenever a Symbol Synchronisation is available but there is no TSI detected. Timer is set back at new cycle start of Run Mode Self Polling. TimeOut= (TOTIMTSI * 64 * 512) / fsys Min: 01h = (1 * 64 * 512)/ fsys Max: FFh= (255 * 64 * 512) / fsys 00h: disabled Reset: 00_H

EOM Timeout Timer Register

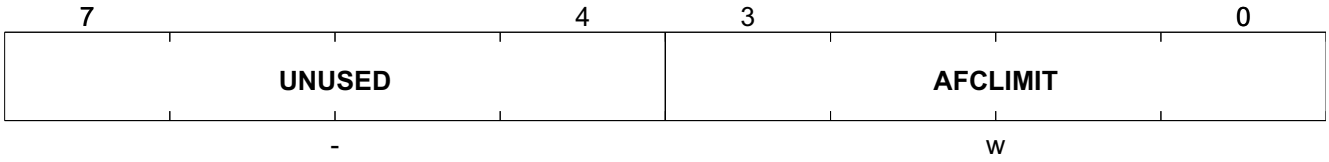
A_TOTIM_EOM	Offset	Reset Value
EOM Timeout Timer Register	**029_H**	**00_H**



Field	Bits	Type	Description
TOTIMEOM	7:0	w	**Set value of Time-Out Timer (End of Message)** Timer is used to get back from Run Mode Self Polling to the Self Polling Mode whenever a TSI has been detected but there is no EOM detected. Timer is set back at new cycle start of Run Mode Self Polling. TimeOut= (TOTIMEOM * 64 * 512 * 2) / fsys Min: 01h = (1 * 64 * 512 * 2)/ fsys Max: FFh= (255 * 64 * 512 * 2) / fsys 00h: disabled Reset: 00_H

AFC Limit Configuration Register

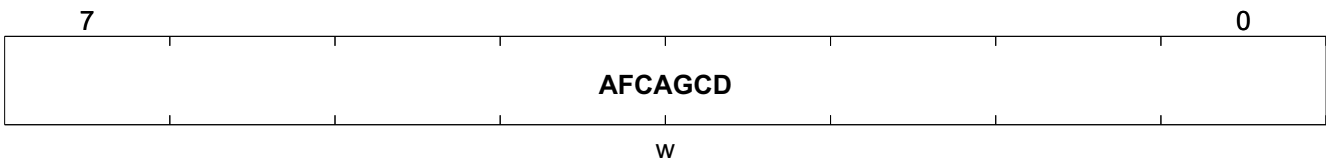
A_AFCLIMIT	Offset	Reset Value
AFC Limit Configuration Register	**$02A_H$**	**02_H**



Field	Bits	Type	Description
UNUSED	7:4	-	**UNUSED** Reset: 0_H
AFCLIMIT	3:0	w	**AFC Frequency Offset Saturation Limit ==> 1...15 x 21.4 kHz** Min: 1h = +/- Fsys / 2^(22-12) Hz Max: Fh = +/- 15 * Fsys / 2^(22-12) Hz Reg. value 0h = 0 Hz - no AFC correction Reset: 2_H

AFC/AGC Freeze Delay Register

A_AFCAGCD	Offset	Reset Value
AFC/AGC Freeze Delay Register	**$02B_H$**	**00_H**



Field	Bits	Type	Description
AFCAGCD	7:0	w	**AFC/AGC Freeze Delay Counter Division Ratio** The base period for the delay counter is the 8-16 samples/chip (predecimation strobe) divided by 4 Reset: 00_H

AFC Start/Freeze Configuration Register

A_AFCSFCFG	Offset	Reset Value
AFC Start/Freeze Configuration Register	**$02C_H$**	**00_H**

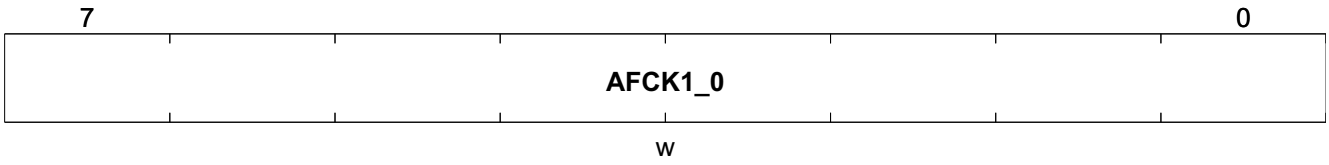
7	6	5	4	2	1	0
UNUSED	**AFCBLASK**	**AFCRESATCC**	**AFCFREEZE**		**AFCSTART**	
-	w	w	w		w	

Field	Bits	Type	Description
UNUSED	7	-	**UNUSED** Reset: 0_H
AFCBLASK	6	w	**AFC blocking during a low phase in the ASK signal** 0_B Disabled 1_B Enabled Reset: 0_H
AFCRESATCC	5	w	**Enable AFC Restart at Channel Change and at the beginning of the current configuration in Self Polling Mode** and at leaving the HOLD state (when bit CMC0.INITPLLHOLD is set) in Run Mode Slave 0_B Disabled 1_B Enabled Reset: 0_H
AFCFREEZE	4:2	w	**AFC Freeze Configuration** When selecting a Level criterion here, please note to use the same Level criterion as for Wake-Up 000_B Stay ON 001_B Freeze on RSSI Event + Delay (AFCAGCDEL) 010_B Freeze on Signal Recognition Event + Delay (AFCAGCDEL) 011_B Freeze on Symbol Synchronization + Delay (AFCAGCDEL) 100_B SPI Command - write to EXTPCMD.AFCMANF bit 101_B n.u. 110_B n.u. 111_B n.u. Reset: 0_H

Field	Bits	Type	Description
AFCSTART	1:0	w	**AFC Start Configuration** When selecting a Level criterion here, please note to use the same Level criterion as for Wake-Up 00_B OFF 01_B Direct ON 10_B Start on RSSI event 11_B Start on Signal Recognition event Reset: 0_H

AFC Integrator 1 Gain Register 0

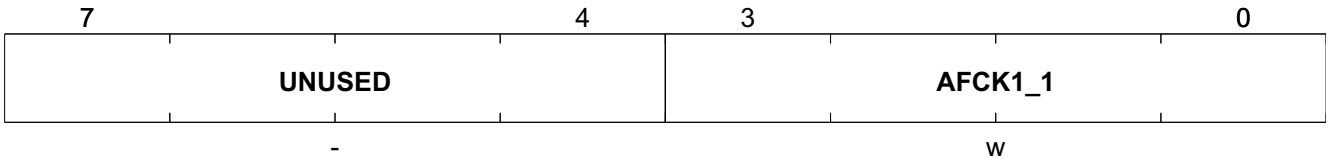
A_AFCK1CFG0	Offset	Reset Value
AFC Integrator 1 Gain Register 0	**$02D_H$**	**00_H**



Field	Bits	Type	Description
AFCK1_0	7:0	w	**AFC Filter coefficient K1, AFCK1(11:0) = AFCK1_1(MSB) & AFCK1_0(LSB)** Reset: 00_H

AFC Integrator 1 Gain Register 1

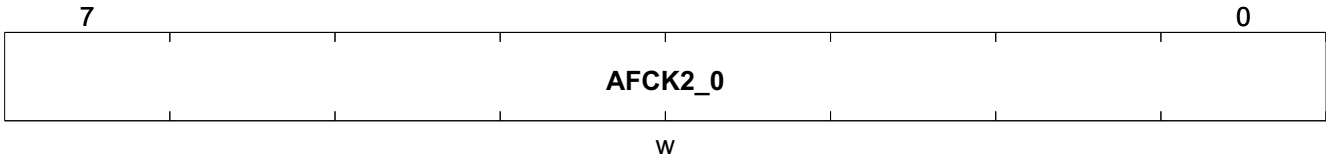
A_AFCK1CFG1	Offset	Reset Value
AFC Integrator 1 Gain Register 1	**$02E_H$**	**00_H**



Field	Bits	Type	Description
UNUSED	7:4	-	**UNUSED** Reset: 0_H
AFCK1_1	3:0	w	**AFC Filter coefficient K1, AFCK1(11:0) = AFCK1_1(MSB) & AFCK1_0(LSB)** Reset: 0_H

AFC Integrator 2 Gain Register 0

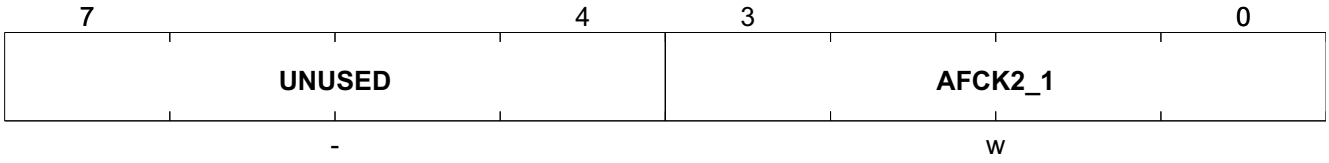
A_AFCK2CFG0	Offset	Reset Value
AFC Integrator 2 Gain Register 0	$02F_H$	00_H



Field	Bits	Type	Description
AFCK2_0	7:0	w	**AFC Filter coefficient K2, AFCK2(11:0) = AFCK2_1(MSB) & AFCK2_0(LSB)** Reset: 00_H

AFC Integrator 2 Gain Register 1

A_AFCK2CFG1	Offset	Reset Value
AFC Integrator 2 Gain Register 1	030_H	00_H



Field	Bits	Type	Description
UNUSED	7:4	-	**UNUSED** Reset: 0_H
AFCK2_1	3:0	w	**AFC Filter coefficient K2, AFCK2(11:0) = AFCK2_1(MSB) & AFCK2_0(LSB)** Reset: 0_H

Peak Memory Filter Up-Down Factor Register

A_PMFUDSF	Offset	Reset Value
Peak Memory Filter Up-Down Factor Register	031_H	42_H

7	6	4	3	2	0
UNUSED	PMFUP		UNUSED	PMFDN	
-	w		-	w	

Field	Bits	Type	Description
UNUSED	7	-	**UNUSED** Reset: 0_H
PMFUP	6:4	w	**Peak Memory Filter Attack (Up) Factor** 000_B 2^-1 001_B 2^-2 010_B 2^-3 011_B 2^-4 100_B 2^-5 101_B 2^-6 110_B 2^-7 111_B 2^-8 Reset: 4_H
UNUSED	3	-	**UNUSED** Reset: 0_H
PMFDN	2:0	w	**Peak Memory Filter Decay (Down) Factor (additional to Attack Factor)** 000_B 2^-2 001_B 2^-3 010_B 2^-4 011_B 2^-5 100_B 2^-6 101_B 2^-7 110_B 2^-8 111_B 2^-9 Reset: 2_H

AGC Start/Freeze Configuration Register

A_AGCSFCFG	Offset	Reset Value
AGC Start/Freeze Configuration Register	**032_H**	**00_H**

7	6	5	4	2	1	0
UNUSED		AGCRESATCC	AGCFREEZE		AGCSTART	
-		w	w		w	

Field	Bits	Type	Description
UNUSED	7:6	-	**UNUSED** Reset: 0_H
AGCRESATCC	5	w	**Enable AGC Restart at Channel Change and at the beginning of the current configuration in Self Polling Mode** and at leaving the HOLD state (when bit CMC0.INITPLLHOLD is set) in Run Mode Slave 0_B Disabled 1_B Enabled Reset: 0_H
AGCFREEZE	4:2	w	**AGC Freeze Configuration** When selecting a Level criterion here, please note to use the same Level criterion as for Wake-Up 000_B Stay ON 001_B Freeze on RSSI Event + Delay (AFCAGCDEL) 010_B Freeze on Signal Recognition Event + Delay (AFCAGCDEL) 011_B Freeze on Symbol Synchronization + Delay (AFCAGCDEL) 100_B SPI Command - write to EXTPCMD.AGCMANF bit 101_B n.u. 110_B n.u. 111_B n.u. Reset: 0_H
AGCSTART	1:0	w	**AGC Start Configuration** When selecting a Level criterion here, please note to use the same Level criterion as for Wake-Up 00_B OFF 01_B Direct ON 10_B Start on RSSI event 11_B Start on Signal Recognition event Reset: 0_H

AGC Configuration Register 0

A_AGCCFG0	Offset	Reset Value
AGC Configuration Register 0	**033_H**	**$2B_H$**

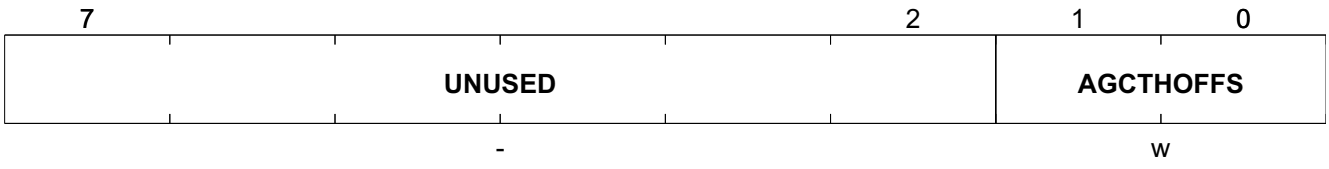
7	6	4	3	2	1	0
UNUSED	**AGCDGC**		**AGCHYS**		**AGCGAIN**	
-	w		w		w	

Field	Bits	Type	Description
UNUSED	7	-	**UNUSED** Reset: 0_H

Field	Bits	Type	Description
AGCDGC	6:4	w	**AGC Digital RSSI Gain Correction Tuning** 000_B 14.5 dB 001_B 15.0 dB 010_B 15.5 dB 011_B 16.0 dB 100_B 16.5 dB 101_B 17.0 dB 110_B 17.5 dB 111_B 18.0 dB Reset: 2_H
AGCHYS	3:2	w	**AGC Threshold Hysteresis** 00_B 12.8 dB 01_B 17.1 dB 10_B 21.3 dB 11_B 25.6 dB Reset: 2_H
AGCGAIN	1:0	w	**AGC Gain Control** 00_B 0 dB 01_B -15 dB 10_B -30 dB 11_B Automatic Reset: 3_H

AGC Configuration Register 1

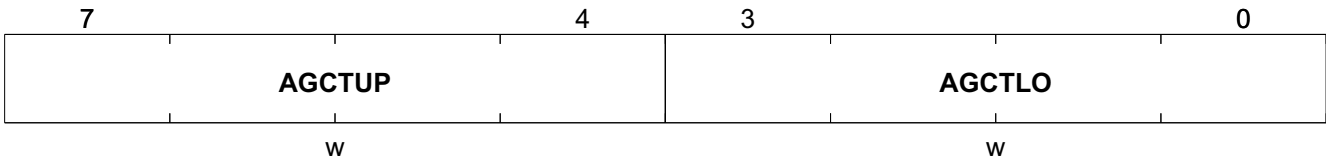
A_AGCCFG1	Offset	Reset Value
AGC Configuration Register 1	**034_H**	**03_H**



Field	Bits	Type	Description
UNUSED	7:2	-	**UNUSED** Reset: 00_H
AGCTHOFFS	1:0	w	**AGC Threshold Offset** 00_B 25.5 dB 01_B 38.3 dB 10_B 51.1 dB 11_B 63.9 dB Reset: 3_H

AGC Threshold Register

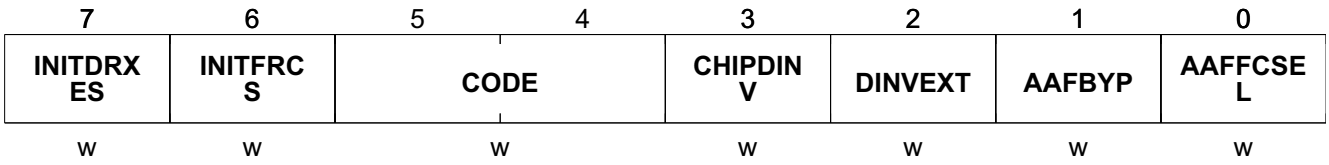
A_AGCTHR	Offset	Reset Value
AGC Threshold Register	035_H	08_H



Field	Bits	Type	Description
AGCTUP	7:4	w	**AGC Upper Attack Threshold [dB]** AGC Upper Threshold = A_AGCCFG1.AGCTHOFFS + 25.6 + AGCTUP*1.6 Reset: 0_H
AGCTLO	3:0	w	**AGC Lower Attack Threshold [dB]** AGC Lower Threshold = A_AGCCFG1.AGCTHOFFS + AGCTLO*1.6 Reset: 8_H

Digital Receiver Configuration Register

A_DIGRXC	Offset	Reset Value
Digital Receiver Configuration Register	036_H	40_H

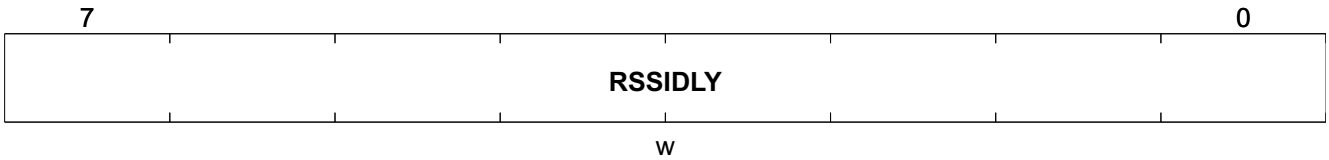


Field	Bits	Type	Description
INITDRXES	7	w	**Init the Digital Receiver at EOM or Loss of Symbol Sync (e.g. for initialization of the Peak Memory Filter)** 0_B Disabled 1_B Enabled Reset: 0_H
INITFRCS	6	w	**Init the Framer at Cycle Start in RMSP.** If disabled, the WUP Data can be used as part of TSI as well in case the modulation type is the same for SPM and RMSP 0_B Disabled 1_B Enabled Reset: 1_H

Field	Bits	Type	Description
CODE	5:4	w	**Encoding Mode Selection** 00_B Manchester Code 01_B Differential Manchester Code 10_B Biphase Space 11_B Biphase Mark Reset: 0_H
CHIPDINV	3	w	**Baseband Chip Data Inversion for CH_DATA and Decoder/Framer input. Therefore Inverted Manchester and Inverted Differential Manchester can be decoded internally.** 0_B Not inverted 1_B Inverted Reset: 0_H
DINVEXT	2	w	**Data Inversion of signal DATA and DATA_MATCHFIL for External Processing** 0_B Not inverted 1_B Inverted Reset: 0_H
AAFBYP	1	w	**Anti-Alliasing Filter Bypass for RSSI pin** 0_B Not bypassed 1_B Bypassed Reset: 0_H
AAFFCSEL	0	w	**Anti-Alliasing Filter Corner Frequency Select** 0_B 40 kHz 1_B 80 kHz Reset: 0_H

RSSI Peak Detector Bit Position Register

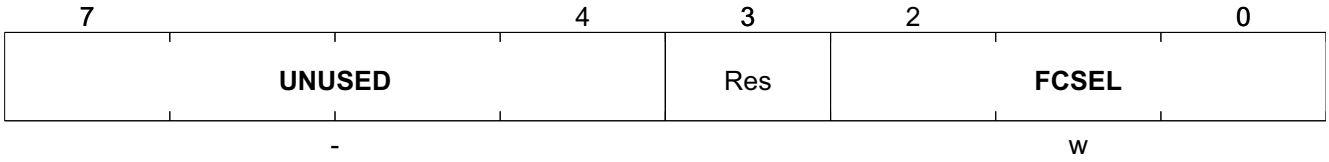
A_PKBITPOS	Offset	Reset Value
RSSI Peak Detector Bit Position Register	**037_H**	**00_H**



Field	Bits	Type	Description
RSSIDLY	7:0	w	**RSSI Detector Start-up Delay for RSSIPPL register** Min: 00h: 0 bit delay (Start with first bit after FSYNC) Max: FFh: 255 bit delay Note: Due to filtering and signal computation, the latency T1 and T2 have to be added Reset: 00_H

Image Supression Fc Selection Register

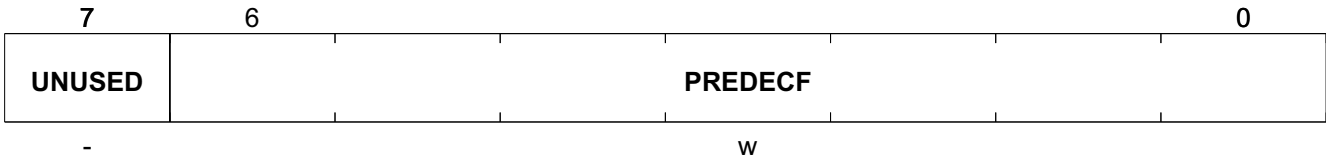
A_ISUPFCSEL	Offset	Reset Value
Image Supression Fc Selection Register	**038_H**	**07_H**



Field	Bits	Type	Description
UNUSED	7:4	-	**UNUSED** Reset: 0_H
FCSEL	2:0	w	**Image Supression Filter Corner Frequency Selection for FSK signal path** 000_B 33 kHz 001_B 46 kHz 010_B 65 kHz 011_B 93 kHz 100_B 132 kHz 101_B 190 kHz 110_B 239 kHz 111_B 282 kHz Reset: 7_H

Pre Decimation Factor Register

A_PDECF	Offset	Reset Value
Pre Decimation Factor Register	**039_H**	**00_H**



Field	Bits	Type	Description
UNUSED	7	-	**UNUSED** Reset: 0_H
PREDECF	6:0	w	**Predecimation Filter Decimation Factor** Predecimation Factor = PREDECF + 1 Reset: 00_H

Pre Decimation Scaling Register FSK Mode

A_PDECSCFSK	Offset	Reset Value
Pre Decimation Scaling Register FSK Mode	$03A_H$	00_H

7	6	5	4	0
Res		INTPOLENF	PDSCALEF	
		w	w	

Field	Bits	Type	Description
INTPOLENF	5	w	**FSK Data Interpolation Enable** 0_B Disabled 1_B Enabled Reset: 0_H
PDSCALEF	4:0	w	**Predecimation Block Scaling Factor for FSK** Min 00h : 2^-10 Max 17h : 2^13 Reset: 00_H

Pre Decimation Scaling Register ASK Mode

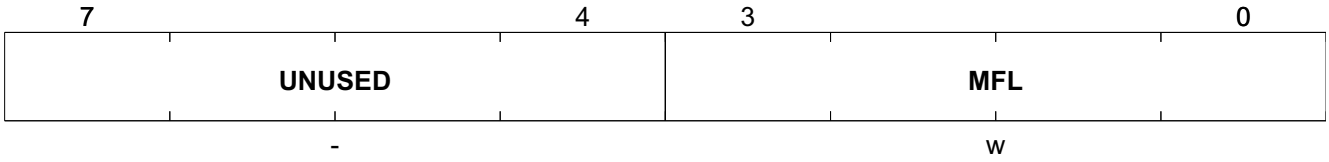
A_PDECSCASK	Offset	Reset Value
Pre Decimation Scaling Register ASK Mode	$03B_H$	20_H

7	6	5	4	0
UNUSED	Res	INTPOLENA	PDSCALEA	
-		w	w	

Field	Bits	Type	Description
UNUSED	7	-	**UNUSED** Reset: 0_H
INTPOLENA	5	w	**ASK Data Interpolation Enable** 0_B Disabled 1_B Enabled Reset: 1_H
PDSCALEA	4:0	w	**Predecimation Block Scaling Factor for ASK** Min 00h : 2^-10 Max 17h : 2^13 Reset: 00_H

Matched Filter Control Register

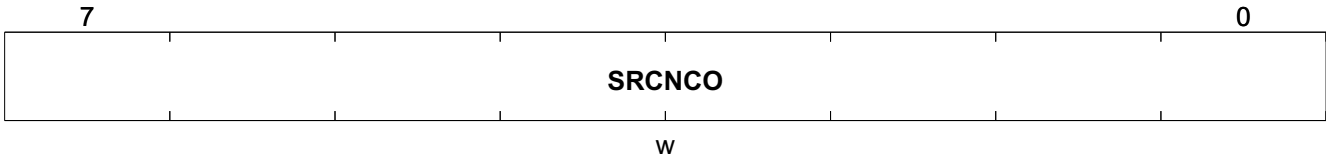
A_MFC	Offset	Reset Value
Matched Filter Control Register	**$03C_H$**	**07_H**



Field	Bits	Type	Description
UNUSED	7:4	-	**UNUSED** Reset: 0_H
MFL	3:0	w	**Matched Filter Length** MF Length = MFL + 1 Reset: 7_H

Sampe Rate Converter NCO Tune

A_SRC	Offset	Reset Value
Sampe Rate Converter NCO Tune	**$03D_H$**	**00_H**



Field	Bits	Type	Description
SRCNCO	7:0	w	**Sample Rate Converter NCO Tune** Min 00h : Fout = Fin Max FFh : Fout = Fin / 2 Reset: 00_H

Externel Data Slicer Configuration

A_EXTSLC	Offset	Reset Value
Externel Data Slicer Configuration	**$03E_H$**	**02_H**

7	6	5	4	3	2	0
UNUSED	Res		**ESLCSCA**		**ESLCBW**	
-			w		w	

Field	Bits	Type	Description
UNUSED	7	-	**UNUSED** Reset: 0_H
ESLCSCA	4:3	w	**External Slicer BW Selection Scaling** 00_B 1/2 01_B 1/4 10_B 1/8 11_B 1/16 Reset: 0_H
ESLCBW	2:0	w	**External Slicer Manual BW Selection** 000_B 1/8 001_B 1/16 010_B 1/24 011_B 1/32 100_B 1/40 101_B 1/48 110_B n.u. 111_B n.u. Reset: 2_H

Signal Detector Threshold Level Register - Run Mode

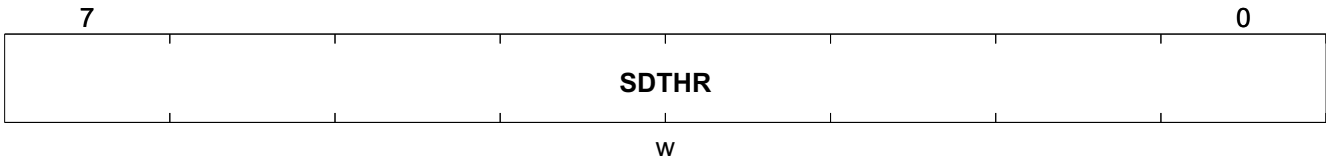
A_SIGDET0	Offset	Reset Value
Signal Detector Threshold Level Register - Run Mode	**$03F_H$**	**00_H**

7						0
SDTHR						
w						

Field	Bits	Type	Description
SDTHR	7:0	w	**Signal Detector Threshold Level for Run Mode** Reset: 00_H

Signal Detector Threshold Level Register - Wakeup

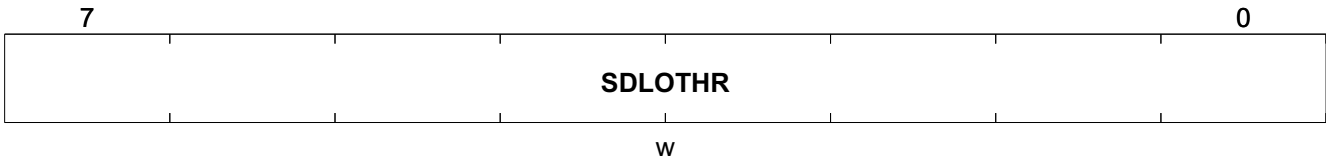
A_SIGDET1	Offset	Reset Value
Signal Detector Threshold Level Register - Wakeup	040_H	00_H



Field	Bits	Type	Description
SDTHR	7:0	w	**Signal Detector Threshold Level for Wakeup** Reset: 00_H

Signal Detector Threshold Low Level Register

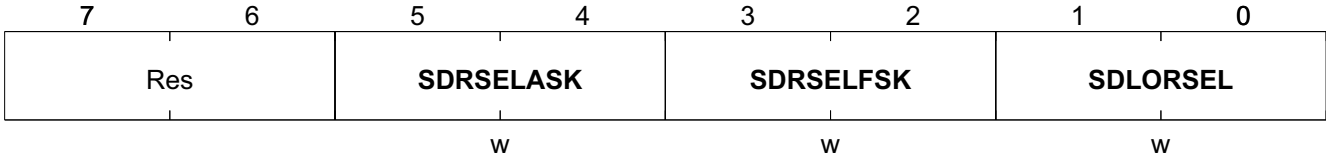
A_SIGDETLO	Offset	Reset Value
Signal Detector Threshold Low Level Register	041_H	00_H



Field	Bits	Type	Description
SDLOTHR	7:0	w	**Signal Detector Threshold Low Level. This threshold level is** only valid, if the FSK Noise detector selection in the A_NDCONFIG register is set to 11b Reset: 00_H

Signal Detector Range Selection Register

A_SIGDETSEL	Offset	Reset Value
Signal Detector Range Selection Register	042_H	$7F_H$



Field	Bits	Type	Description
SDRSELASK	5:4	w	**A_SIGDET0/1 range selection factor for ASK. The selected signal detector value is multiplied by the 2^range selection factor. Use the right setting to fit the measured SPWR value.** 00_B 6 01_B 7 10_B 7+6 11_B 8 Reset: 3_H
SDRSELFSK	3:2	w	**A_SIGDET0/1 range selection factor for FSK. The selected signal detector value is multiplied by the 2^range selection factor. Use the right setting to fit the measured SPWR value.** 00_B 2 01_B 4 10_B 6 11_B 8 Reset: 3_H
SDLORSEL	1:0	w	**SIGDETLO range selection factor. The selected signal detector value is multiplied by the 2^range selection factor. Use the right setting to fit the measured SPWR value.** 00_B 2 01_B 4 10_B 6 11_B 8 Reset: 3_H

Signal Detector Configuration Register

A_SIGDETCFG	Offset	Reset Value
Signal Detector Configuration Register	**043_H**	**00_H**

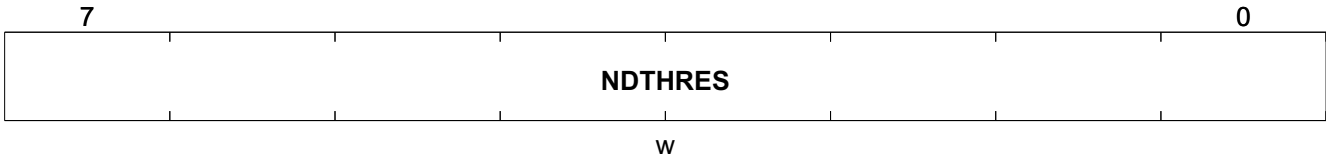
7	4	3	2	1	0
UNUSED		Res	**SDLORE**	**SDCNT1**	**SDCNT0**
-			w	w	w

Field	Bits	Type	Description
UNUSED	7:4	-	**UNUSED** Reset: 0_H
SDLORE	2	w	**Source selection of Signal Power Readout Register** 0_B Signal Power for A_SIGDET0/1 1_B Signal for minimal usable FSK deviation, the sigdet low level can be read out with SPWR register Reset: 0_H

Field	Bits	Type	Description
SDCNT1	1	w	**Signal Detector Threshold Counter for Wakeup** 0_B Disabled 1_B 1/2 bit Reset: 0_H
SDCNT0	0	w	**Signal Detector Threshold Counter for Run Mode** 0_B Disabled 1_B 1/2 bit Reset: 0_H

FSK Noise Detector Threshold Register

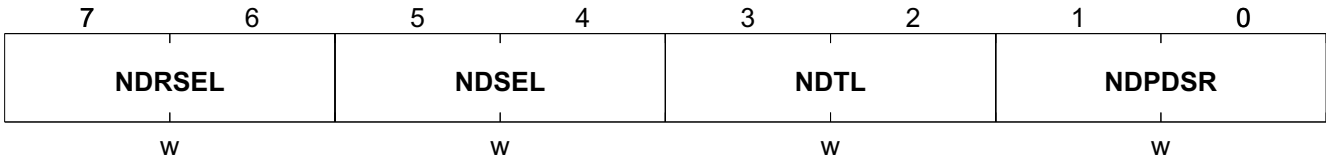
A_NDTHRES	Offset	Reset Value
FSK Noise Detector Threshold Register	**044_H**	**00_H**



Field	Bits	Type	Description
NDTHRES	7:0	w	**FSK Noise Detector Threshold** Reset: 00_H

FSK Noise Detector Configuration Register

A_NDCONFIG	Offset	Reset Value
FSK Noise Detector Configuration Register	**045_H**	**07_H**



Field	Bits	Type	Description
NDRSEL	7:6	w	**FSK Noise Detector Range Selection** 00_B 2^7 01_B 2^6 10_B 2^5 11_B 2^4 Reset: 0_H

Field	Bits	Type	Description
NDSEL	5:4	w	**Signal and Noise Detector Selection** 00_B Signal detection (=Squelch) only. This mode is recommended for ASK. 01_B Noise detection only 10_B Signal and noise detection simultaneously 11_B Signal and noise detection simultaneously, but the FSK noise detect signal is valid only if the SIGDETLO threshold is exceeded. This is the recommended mode for FSK. Reset: 0_H
NDTL	3:2	w	**FSK Noise Detector Threshold Level** 00_B 1/2 01_B 3/8 10_B 1/4 11_B 1/8 Reset: 1_H
NDPDSR	1:0	w	**FSK Noise Detector - Peak Detector Slew Rate** 00_B 1/256 01_B 1/128 10_B 1/64 11_B 1/32 Reset: 3_H

Clock and Data Recovery P Configuration Register

A_CDRP	Offset	Reset Value
Clock and Data Recovery P Configuration Register	**046_H**	**$E6_H$**

7	6	5	4	3	2	1	0
PDSR		PHDEN1	PHDEN0	PVAL		PSAT	
w		w	w	w		w	

Field	Bits	Type	Description
PDSR	7:6	w	**Peak-Detector slew rate. The slew rate of the Peak-Detector in the clock-recovery path will be set with** PDSR. Actually, Peak-Detector part of Signal Detector Block 00_B up/down = 1/64 01_B up = 1/64; down = 1/128 10_B up = 1/32; down = 1/128 11_B up = 1/32; down = 1/256 Reset: 3_H

Field	Bits	Type	Description
PHDEN1	5	w	**Phase detector error (PDE) outer tolerance range** 0_B Disabled: PDEout = PDEin. 1_B Enabled: If PDEin > abs(7/16) bit then PDEout = 0 else PDEout = PDEin. Reset: 1_H
PHDEN0	4	w	**Phase detector error (PDE) inner tolerance range** 0_B Disabled: PDEout = PDEin. 1_B Enabled: If PDEin < abs(1/16) bit then PDEout = 0 else PDEout = PDEin. Reset: 0_H
PVAL	3:2	w	**P Value. The PVAL is the P value of the Clock-Recovery PI Loop-Filter. The Phase-** Detector output error will be multiplied with the set value. 00_B 1/1 phase detector error 01_B 1/2 phase detector error 10_B 1/4 phase detector error 11_B 1/8 phase detector error Reset: 1_H
PSAT	1:0	w	**P Value Saturation. The saturation of the P-Loop-Filter path will be set according to the PSAT** value. Remark that the internal phase resolution of the phase detector is 1/16 bit. 00_B saturation to 1/16 bit 01_B saturation to 2/16 bit 10_B saturation to 4/16 bit 11_B saturation to 8/16 bit Reset: 2_H

Clock and Data Recovery Configuration Register

A_CDRI	Offset	Reset Value
Clock and Data Recovery Configuration Register	**047_H**	**65_H**

7	6	5	4	3	2	1	0
CORSAT		**LFSAT**		**IVAL**		**ISAT**	
w		w		w		w	

Field	Bits	Type	Description
CORSAT	7:6	w	**Correlator output value (Timing extrapolation unit). The timing extrapolation unit output value will be multiplied with the LFSAT** value. The timing extrapolation unit measures the data rate error during the RUNIN sequence and sets the I-Loop-Filter path when the RUNIN length is reached. 00_B 1/4 calculated value 01_B 1/8 calculated value 10_B 1/16 calculated value 11_B 1/32 calculated value Reset: 1_H
LFSAT	5:4	w	**Loop Filter Saturation. The saturation of the I-Loop-Filter path will be set according to the LFSAT** value.Remark that the internal phase resolution of the phase detector is 1/16 bit. 00_B saturation to 1/32 bit 01_B saturation to 1/16 bit 10_B saturation to 2/16 bit 11_B saturation to 4/16 bit Reset: 2_H
IVAL	3:2	w	**I Value. The IVAL is the I value of the Clock-Recovery PI Loop-Filter. The Phase-** Detector output error will be multiplied with this set value. 00_B 1/32 phase detector error 01_B 1/64 phase detector error 10_B 1/128 phase detector error 11_B 1/256 phase detector error Reset: 1_H
ISAT	1:0	w	**I Value Saturation. The saturation of the I-Loop-Filter accumulator will be set according to the** ISAT value. Remark that the internal phase resolution of the phase detector is 1/16 bit. 00_B saturation to 1/16 bit 01_B saturation to 2/16 bit 10_B saturation to 4/16 bit 11_B saturation to 8/16 bit Reset: 1_H

Clock and Data Recovery RUNIN Configuration Register

A_CDRRI	Offset	Reset Value
Clock and Data Recovery RUNIN Configuration Register	**048_H**	**01_H**

7				3	2	1		0
UNUSED					DRLIMEN	RUNLEN		
-					w	w		

Field	Bits	Type	Description
UNUSED	7:3	-	**UNUSED** Reset: 00_H
DRLIMEN	2	w	**Enable data rate error acceptance limitation.** The limits are defined in CDRDRTHRP and CDRDRTHRN registers. 0_B Disabled 1_B Enabled Reset: 0_H
RUNLEN	1:0	w	**RUNIN Length. The RUNIN length is equal to PLL-start-value calculation time. This means** that the shorter RUNIN length decreases the data rate offset calculation accuracy and symbol synchronization found signal generation stability. Note that the RUNLEN have to be changed together with the TSI configuration registers. 00_B 8 chips 01_B 7 chips 10_B 6 chips 11_B 5 chips Reset: 1_H

CDR DC Chip Tolerance Register

A_CDRTOLC	Offset	Reset Value
CDR DC Chip Tolerance Register	**049_H**	**$0C_H$**

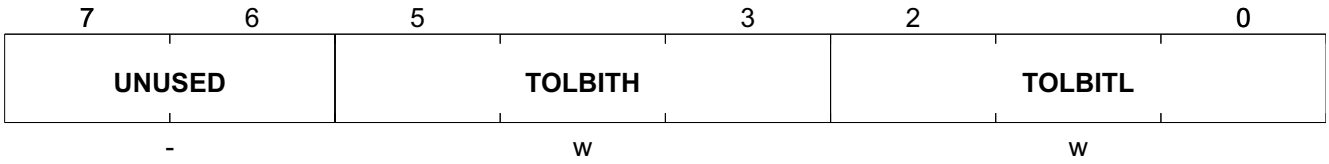
7	6	5		3	2		0
UNUSED		TOLCHIPH			TOLCHIPL		
-		w			w		

Field	Bits	Type	Description
UNUSED	7:6	-	**UNUSED** Reset: 0_H
TOLCHIPH	5:3	w	**Duty Cycle Tolerance for Chip Border High Level. Represents the number of 1/16 bit sample deviation from the ideal chip border where an edge can occur in direction to the following chip border.** Reset: 1_H

Field	Bits	Type	Description
TOLCHIPL	2:0	w	**Duty Cycle Tolerance for Chip Border Low Level. Represents the number of 1/16 bit sample deviation from the ideal chip border where an edge can occur in direction to the previous chip border.** Reset: 4_H

CDR DC Bit Tolerance Register

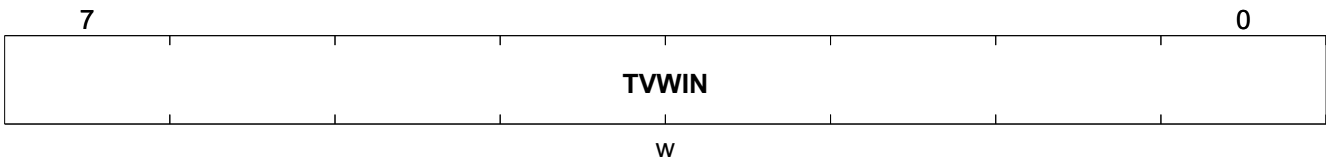
A_CDRTOLB	Offset	Reset Value
CDR DC Bit Tolerance Register	**$04A_H$**	**$1E_H$**



Field	Bits	Type	Description
UNUSED	7:6	-	**UNUSED** Reset: 0_H
TOLBITH	5:3	w	**Duty Cycle Tolerance for Bit Border High Level. Represents the number of 1/16 bit sample deviation from the ideal bit border where an edge can occur in direction to the following bit border.** Reset: 3_H
TOLBITL	2:0	w	**Duty Cycle Tolerance for Bit Border Low Level. Represents the number of 1/16 bit sample deviation from the ideal bit border where an edge can occur in direction to the previous bit border.** Reset: 6_H

Timing Violation Window Register

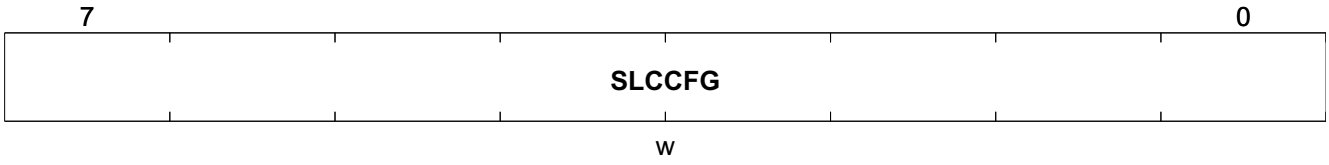
A_TVWIN	Offset	Reset Value
Timing Violation Window Register	**$04B_H$**	**28_H**



Field	Bits	Type	Description
TVWIN	7:0	w	**Timing Violation Window Length.** Defines the maximal number of 1/16 data samples without detected edge which will be tolerated by CDR with no Loss of Symbol Synchronization 28h: 40/16 bit ((8 + 16 *CV + 8)*1.25) FFh: 255/16 bit Note: in TSIGAP mode the value must be higher. Reset: 28_H

Slicer Configuration Register

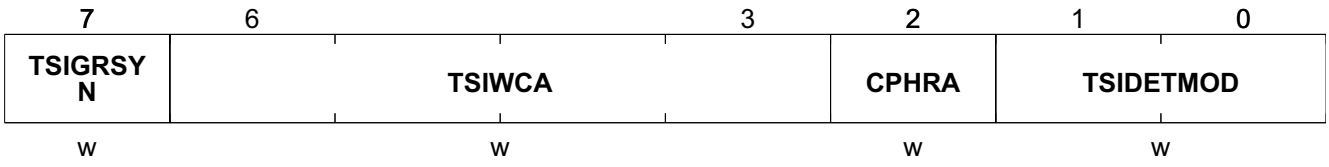
A_SLCCFG	Offset	Reset Value
Slicer Configuration Register	**$04C_H$**	**90_H**



Field	Bits	Type	Description
SLCCFG	7:0	w	**Data Slicer Configuration** Value 90_H : Chip Mode EOM-CV: For patterns with code violations in data packet and optimized for activated EOM code violation criterion (and optional EOM data length criterion) Value 94_H : Chip Mode EOM-Datalength: For patterns with code violations in data packet and optimized for activated EOM data length criterion only (EOMDATLEN) Value 95_H : Chip Mode Transparent: When Framer is not used, but CH_DATA / CH_STR are used for data processing Value 75_H : Bit Mode: Only for patterns without Code Violations Reset: 90_H

TSI Detection Mode Register

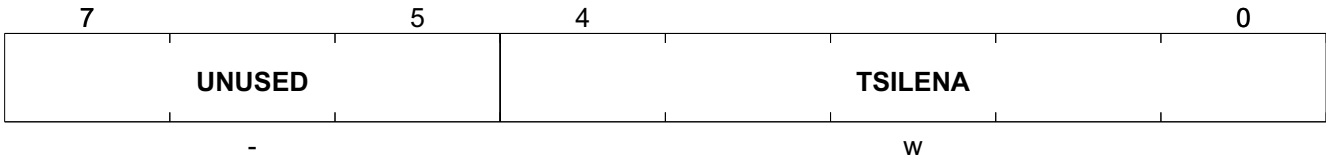
A_TSIMODE	Offset	Reset Value
TSI Detection Mode Register	**$04D_H$**	**80_H**



Field	Bits	Type	Description
TSIGRSYN	7	w	**TSI Gap Resync Mode (only for TSIDETMODE=2_H)** 0_B Disabled - In this mode the GAPVAL and TSIGAP values are used, so the overall GAP time can be defined in T/16 steps. 1_B Enabled - PLL resync after TSI Gap In this mode the T/2 GAP resolution can be set in the 5 MSB TSIGAP register bits. GAPVAL value is not used. Prefered in TSI Gap Mode. Reset: 1_H
TSIWCA	6:3	w	**Wild Cards for 4 LSB chips of Correlator A** If all 4 chips are 0, the whole TSI pattern for Correlator A is valid if a chip is 1, the corresponding chip from the TSI pattern is ignored Reset: 0_H
CPHRA	2	w	**Code Phase Readjustment in Payload** 0_B disabled - code polarity is defined by the TSI pattern 1_B enabled - code phase readjustment in payload Reset: 0_H
TSIDETMOD	1:0	w	**TSI Detection Mode** 00_B 16 Bit TSI Mode - TSI configuration B AND A valid (sequentially), B is valid if A_TSILENA=16 (=10_H) and the A_TSILENB > 0 01_B 8 Bit Parallel TSI Mode - TSI configurations A OR B (parallel) 10_B 8 Bit TSI Gap Mode - TSI configurations A AND B with Gap (sequentially with Gap between TSIA & TSIB) 11_B 8 Bit Extended TSI Mode - TSI configurations A OR B (parallel with matching information), dependent on found TSI A or B, 0 resp. 1 will be sent as 1st received bit. Reset: 0_H

TSI Length Register A

A_TSILENA	Offset	Reset Value
TSI Length Register A	**$04E_H$**	**00_H**

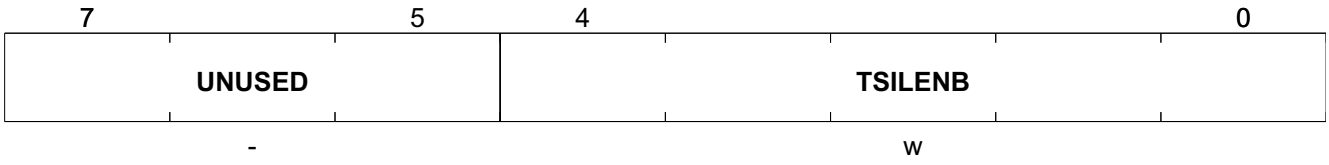


Field	Bits	Type	Description
UNUSED	7:5	-	**UNUSED** Reset: 0_H

Field	Bits	Type	Description
TSILENA	4:0	w	**TSI A Length (in chips):** (11_H up to $1F_H$ not used) Min: 01 = 1 Chip; Be aware that such small values makes it impossible to find the right phase of the pattern in the data stream and therefore wrong data and code violations can be generated. Max: 10h = 16 Chips = 8 Bit Reset: 00_H

TSI Length Register B

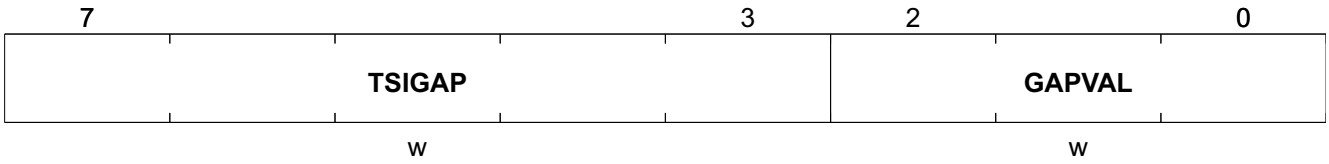
A_TSILENB	Offset	Reset Value
TSI Length Register B	**$04F_H$**	**00_H**



Field	Bits	Type	Description
UNUSED	7:5	-	**UNUSED** Reset: 0_H
TSILENB	4:0	w	**TSI B Length (in chips):** (11_H up to $1F_H$ not used) Min: For 16 Bit TSI Mode: Min: 00h = 0 Chip (see also A_TSILENA) For all other TSI Modes: Min: 01h = 1 Chip (see also A_TSILENA) Max: 10h = 16 Chips = 8 Bit Reset: 00_H

TSI Gap Length Register

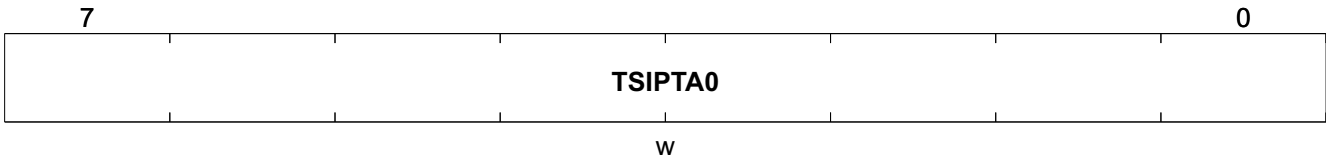
A_TSIGAP	Offset	Reset Value
TSI Gap Length Register	**050_H**	**00_H**



Field	Bits	Type	Description
TSIGAP	7:3	w	**TSI Gap (T/2 bit resolution)** 1Fh: 15 1/2 bit gap 00h: 0 bit gap TSIGAP is used to lock the PLL after TSI A is found, if the TSI detection mode 10b is selected. Reset: 00_H
GAPVAL	2:0	w	**TSI Gap (T/16 bit resolution)** 111b: 7/16 bit gap 000b: 0 bit gap GAPVAL is used to correct the DCO phase after TSIGAP time, if A_TSIMODE.TSIGRSYN is disabled Reset: 0_H

TSI Pattern Data Reference A Register 0

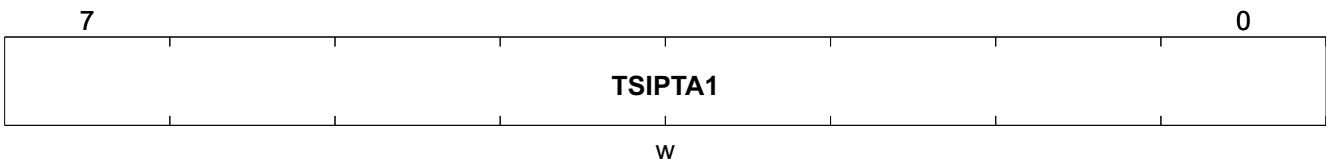
A_TSIPTA0	Offset	Reset Value
TSI Pattern Data Reference A Register 0	**051_H**	**00_H**



Field	Bits	Type	Description
TSIPTA0	7:0	w	**Data Pattern for TSI comparison: Bit 7...Bit 0(LSB) (in Chips)** Reset: 00_H

TSI Pattern Data Reference A Register 1

A_TSIPTA1	Offset	Reset Value
TSI Pattern Data Reference A Register 1	**052_H**	**00_H**



Field	Bits	Type	Description
TSIPTA1	7:0	w	**Data Pattern for TSI comparison: Bit 15(MSB)...Bit 8 (in Chips)** Reset: 00_H

TSI Pattern Data Reference B Register 0

A_TSIPTB0	Offset	Reset Value
TSI Pattern Data Reference B Register 0	053_H	00_H

7	6	5	4	3	2	1	0
TSIPTB0							
w							

Field	Bits	Type	Description
TSIPTB0	7:0	w	**Data Pattern for TSI comparison: Bit 7...Bit 0(LSB) (in Chips)** Reset: 00_H

TSI Pattern Data Reference B Register 1

A_TSIPTB1	Offset	Reset Value
TSI Pattern Data Reference B Register 1	054_H	00_H

7	6	5	4	3	2	1	0
TSIPTB1							
w							

Field	Bits	Type	Description
TSIPTB1	7:0	w	**Data Pattern for TSI comparison: Bit 15(MSB)...Bit 8 (in Chips)** Reset: 00_H

End Of Message Control Register

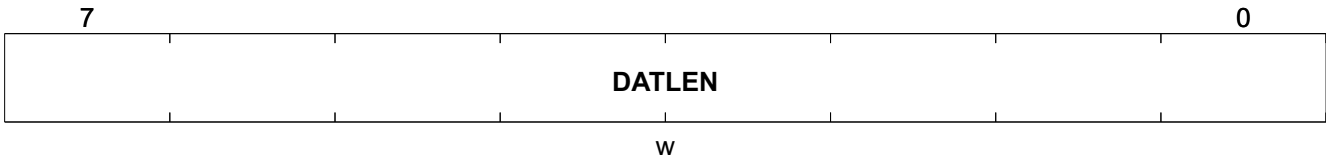
A_EOMC	Offset	Reset Value
End Of Message Control Register	055_H	05_H

7	6	5	4	3	2	1	0
UNUSED				Res	EOMSYLO	EOMCV	EOMDATLEN
-					w	w	w

Field	Bits	Type	Description
UNUSED	7:4	-	**UNUSED** Reset: 0_H
EOMSYLO	2	w	**EOM by Sync Loss** 0_B Disabled 1_B Enabled Reset: 1_H
EOMCV	1	w	**EOM by Code Violation** 0_B Disabled 1_B Enabled Reset: 0_H
EOMDATLEN	0	w	**EOM by Data Length** 0_B Disabled 1_B Enabled Reset: 1_H

EOM Data Length Limit Register

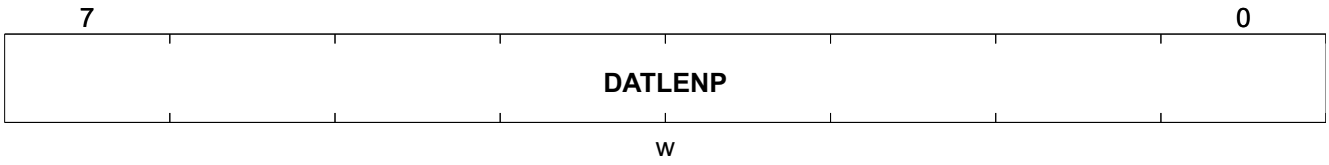
A_EOMDLEN	Offset	Reset Value
EOM Data Length Limit Register	**056_H**	**00_H**



Field	Bits	Type	Description
DATLEN	7:0	w	**Length of Data Field in Telegram, only valid when EOM criterion is EOMDATLEN** Counting of number of payload bits starts after the last TSI Bit. EOM will be generated after the last payload bit. In 8-bit extended TSI mode, the value must be the payload length + 1, because of the additional bit inserted (matching information). Min: 00h = 256 payload bits Reg. value 01h = 1 payload bit Max: FFh = 255 payload bits Reset: 00_H

EOM Data Length Limit Parallel Mode Register

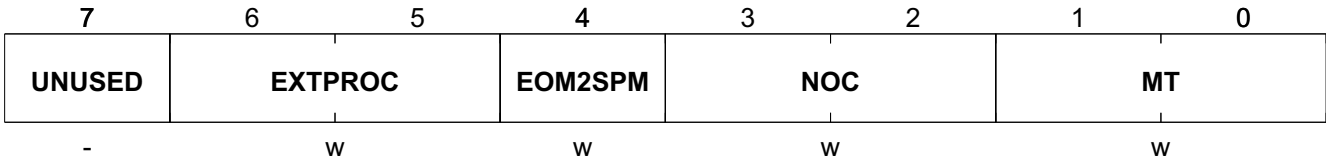
A_EOMDLENP	Offset	Reset Value
EOM Data Length Limit Parallel Mode Register	057_H	00_H



Field	Bits	Type	Description
DATLENP	7:0	w	**Length of Data Field in Telegram in Parallel Mode for TSI Pattern B, only valid when EOM criterion is EOMDATLEN** Counting of number of payload bits starts after the last TSI Bit. EOM will be generated after the last payload bit. In 8-bit extended TSI mode, the value must be the payload length + 1, because of the additional bit inserted (matching information). Min: 00h = 256 payload bits Reg. value 01h = 1 payload bit Max: FFh = 255 payload bits Reset: 00_H

Channel Configuration Register

A_CHCFG	Offset	Reset Value
Channel Configuration Register	058_H	04_H

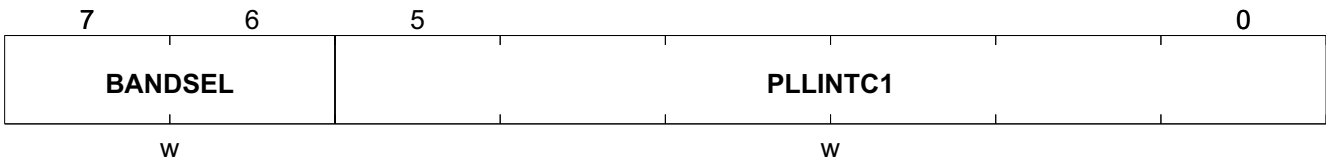


Field	Bits	Type	Description
UNUSED	7	-	**UNUSED** Reset: 0_H

Field	Bits	Type	Description
EXTPROC	6:5	w	**External Data Processing** 00_B No deactivation of functional blocks 01_B Chip Data (RX Mode: TMCDS) - no framing - FSYNC, MID and EOM interrupts disabled - only TOTIM_SYNC is active - random, equal and pattern WU are disabled (mapped to sync) 10_B Data + Data MF (RX Mode: TMMF, TMRDS) - no framing - FSYNC, MID and EOM interrupts disabled - all TOTIMs are inactive - only WU on RSSI (Level Criterion) possible 11_B not used Reset: 0_H
EOM2SPM	4	w	**Continue with Self Polling Mode after EOM detected in Run Mode Self Polling** 0_B Disabled - stay in Run Mode Self Polling (next Payload Frame is expected) 1_B Enabled - leave Run Mode Self Polling after EOM Reset: 0_H
NOC	3:2	w	**Number of Channels (Run Mode Slave / Self Polling Mode - Run Mode Self Polling)** 00_B Channel 1 / Channel 1 01_B Channel 1 / Channel 1 10_B Channel 2 / Channel 1 + 2 11_B Channel 3 / Channel 1 + 2 + 3 Reset: 1_H
MT	1:0	w	**Modulation Type (Run Mode Slave / Self Polling Mode - Run Mode Self Polling)** 00_B ASK / ASK - ASK 01_B FSK / FSK - FSK 10_B ASK / FSK - ASK 11_B FSK / ASK - FSK Reset: 0_H

PLL MMD Integer Value Register Channel 1

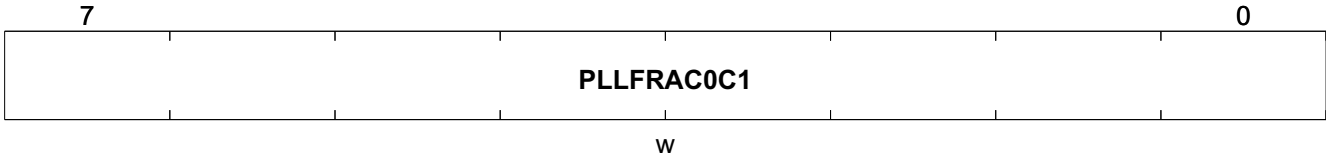
A_PLLINTC1	Offset	Reset Value
PLL MMD Integer Value Register Channel 1	**059_H**	**93_H**



Field	Bits	Type	Description
BANDSEL	7:6	w	**Frequency Band Selection** 00_B not used 01_B 915MHz/868MHz 10_B 434MHz 11_B 315MHz Reset: 2_H
PLLINTC1	5:0	w	**SDPLL Multi Modulus Divider Integer Offset value for Channel 1** PLLINT(5:0) = dec2hex(INT(f_LO / f_XTAL)) Reset: 13_H

PLL Fractional Division Ratio Register 0 Channel 1

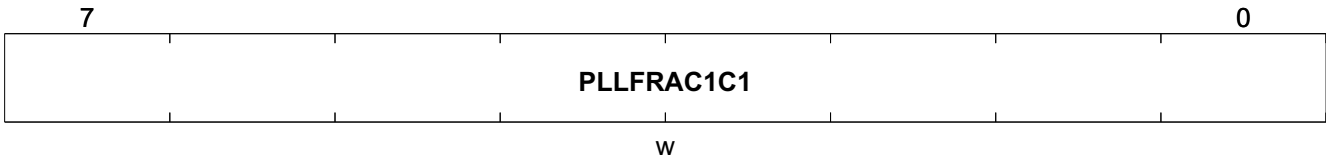
A_PLLFRAC0C1	Offset	Reset Value
PLL Fractional Division Ratio Register 0 Channel 1	**$05A_H$**	**$F3_H$**



Field	Bits	Type	Description
PLLFRAC0C1	7:0	w	**Synthesizer channel frequency value (21 bits, bits 7:0), fractional division ratio for Channel 1** PLLFRAC(20:0) = dec2hex(((f_LO / f_XTAL) - PLLINT) * 2^21) Reset: $F3_H$

PLL Fractional Division Ratio Register 1 Channel 1

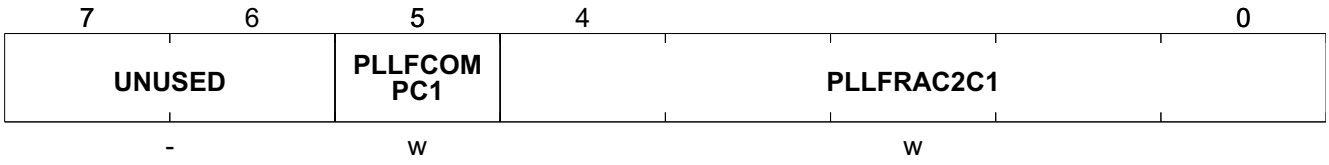
A_PLLFRAC1C1	Offset	Reset Value
PLL Fractional Division Ratio Register 1 Channel 1	**$05B_H$**	**07_H**



Field	Bits	Type	Description
PLLFRAC1C1	7:0	w	**Synthesizer channel frequency value (21 bits, bits 15:8), fractional division ratio for Channel 1** PLLFRAC(20:0) = dec2hex(((f_LO / f_XTAL) - PLLINT) * 2^21) Reset: 07_H

PLL Fractional Division Ratio Register 2 Channel 1

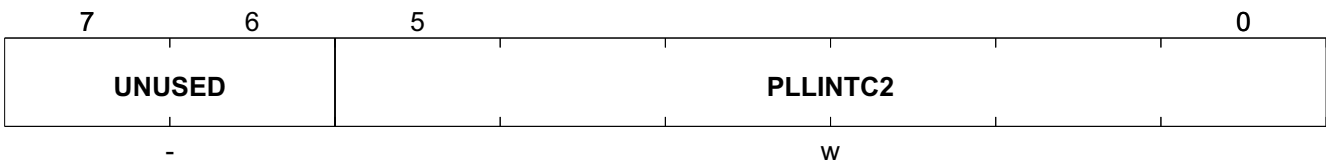
A_PLLFRAC2C1	Offset	Reset Value
PLL Fractional Division Ratio Register 2 Channel 1	**$05C_H$**	**09_H**



Field	Bits	Type	Description
UNUSED	7:6	-	**UNUSED** Reset: 0_H
PLLFCOMPC1	5	w	**Fractional Spurii Compensation enable for Channel 1** 0_B Disabled 1_B Enabled Reset: 0_H
PLLFRAC2C1	4:0	w	**Synthesizer channel frequency value (21 bits, bits 20:16), fractional division ratio for Channel 1** PLLFRAC(20:0) = dec2hex(((f_LO / f_XTAL) - PLLINT) * 2^21) Reset: 09_H

PLL MMD Integer Value Register Channel 2

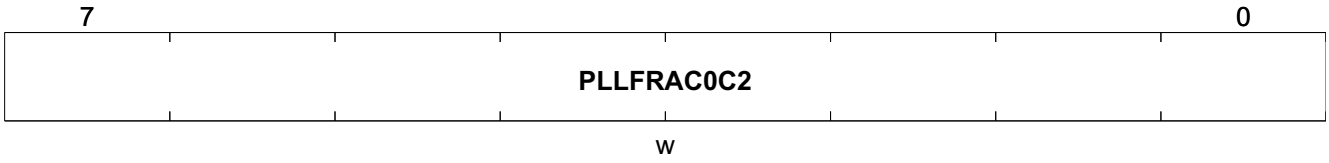
A_PLLINTC2	Offset	Reset Value
PLL MMD Integer Value Register Channel 2	**$05D_H$**	**13_H**



Field	Bits	Type	Description
UNUSED	7:6	-	**UNUSED** Reset: 0_H
PLLINTC2	5:0	w	**SDPLL Multi Modulus Divider Integer Offset value for Channel 2** PLLINT(5:0) = dec2hex(INT(f_LO / f_XTAL)) Reset: 13_H

PLL Fractional Division Ratio Register 0 Channel 2

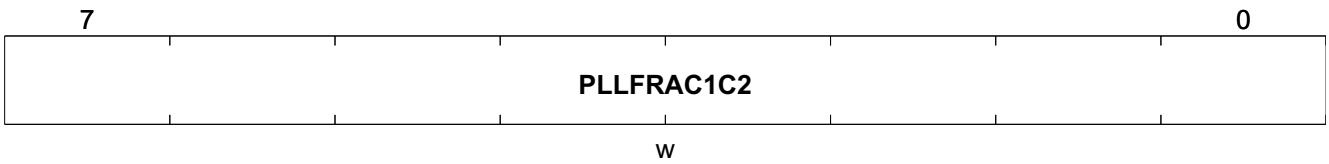
A_PLLFRAC0C2	Offset	Reset Value
PLL Fractional Division Ratio Register 0 Channel 2	**$05E_H$**	**$F3_H$**



Field	Bits	Type	Description
PLLFRAC0C2	7:0	w	**Synthesizer channel frequency value (21 bits, bits 7:0), fractional division ratio for Channel 2** PLLFRAC(20:0) = dec2hex(((f_LO / f_XTAL) - PLLINT) * 2^21) Reset: $F3_H$

PLL Fractional Division Ratio Register 1 Channel 2

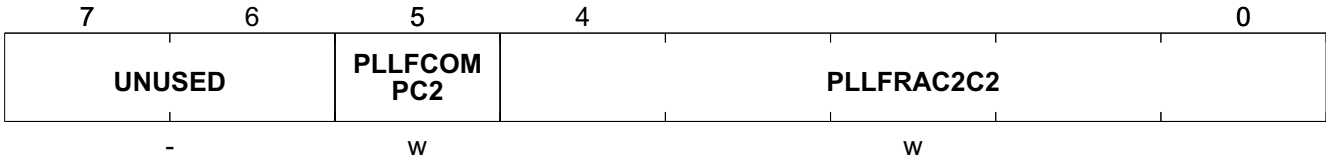
A_PLLFRAC1C2	Offset	Reset Value
PLL Fractional Division Ratio Register 1 Channel 2	**$05F_H$**	**07_H**



Field	Bits	Type	Description
PLLFRAC1C2	7:0	w	**Synthesizer channel frequency value (21 bits, bits 15:8), fractional division ratio for Channel 2** PLLFRAC(20:0) = dec2hex(((f_LO / f_XTAL) - PLLINT) * 2^21) Reset: 07_H

PLL Fractional Division Ratio Register 2 Channel 2

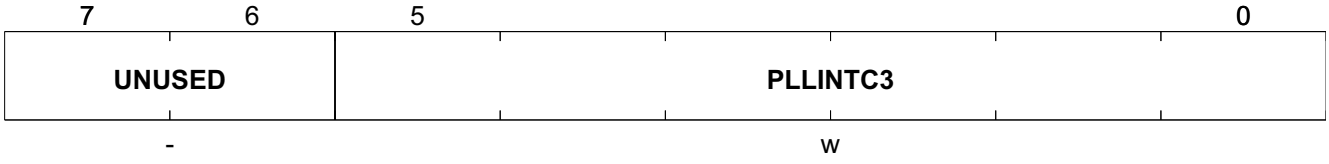
A_PLLFRAC2C2	Offset	Reset Value
PLL Fractional Division Ratio Register 2 Channel 2	060_H	09_H



Field	Bits	Type	Description
UNUSED	7:6	-	**UNUSED** Reset: 0_H
PLLFCOMPC2	5	w	**Fractional Spurii Compensation enable for Channel 2** 0_B Disabled 1_B Enabled Reset: 0_H
PLLFRAC2C2	4:0	w	**Synthesizer channel frequency value (21 bits, bits 20:16), fractional division ratio for Channel 2** PLLFRAC(20:0) = dec2hex(((f_LO / f_XTAL) - PLLINT) * 2^21) Reset: 09_H

PLL MMD Integer Value Register Channel 3

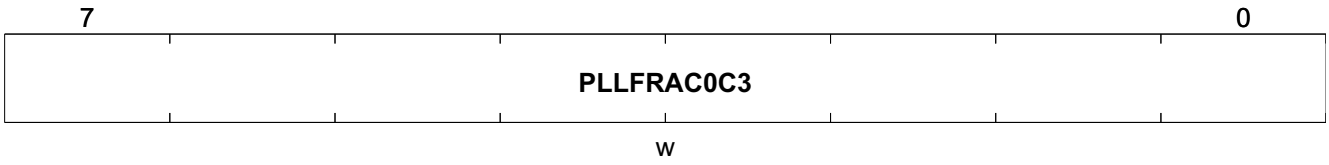
A_PLLINTC3	Offset	Reset Value
PLL MMD Integer Value Register Channel 3	061_H	13_H



Field	Bits	Type	Description
UNUSED	7:6	-	**UNUSED** Reset: 0_H
PLLINTC3	5:0	w	**SDPLL Multi Modulus Divider Integer Offset value for Channel 3** PLLINT(5:0) = dec2hex(INT(f_LO / f_XTAL)) Reset: 13_H

PLL Fractional Division Ratio Register 0 Channel 3

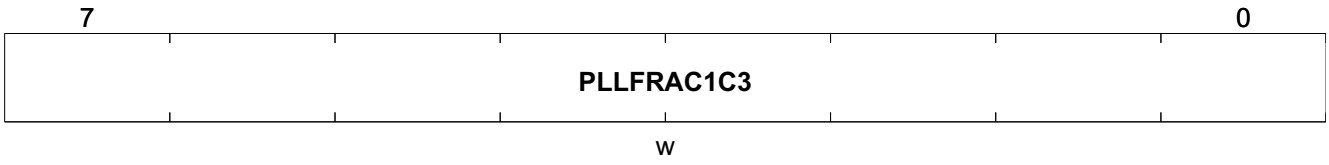
A_PLLFRAC0C3	Offset	Reset Value
PLL Fractional Division Ratio Register 0 Channel 3	062_H	$F3_H$



Field	Bits	Type	Description
PLLFRAC0C3	7:0	w	**Synthesizer channel frequency value (21 bits, bits 7:0), fractional division ratio for Channel 3** PLLFRAC(20:0) = dec2hex(((f_LO / f_XTAL) - PLLINT) * 2^21) Reset: $F3_H$

PLL Fractional Division Ratio Register 1 Channel 3

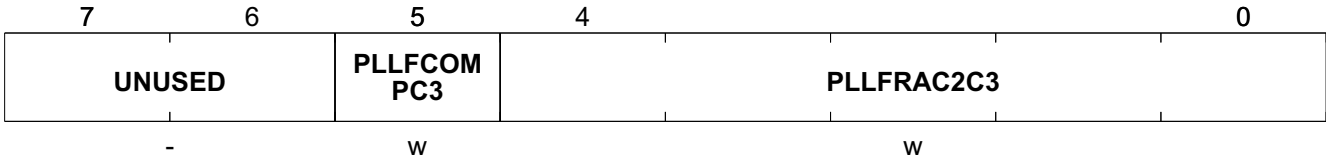
A_PLLFRAC1C3	Offset	Reset Value
PLL Fractional Division Ratio Register 1 Channel 3	063_H	07_H



Field	Bits	Type	Description
PLLFRAC1C3	7:0	w	**Synthesizer channel frequency value (21 bits, bits 15:8), fractional division ratio for Channel 3** PLLFRAC(20:0) = dec2hex(((f_LO / f_XTAL) - PLLINT) * 2^21) Reset: 07_H

PLL Fractional Division Ratio Register 2 Channel 3

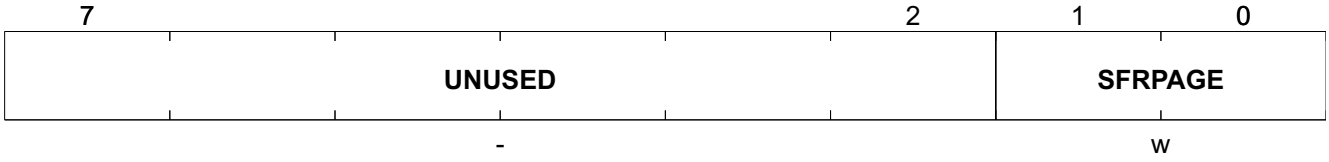
A_PLLFRAC2C3	Offset	Reset Value
PLL Fractional Division Ratio Register 2 Channel 3	064_H	09_H



Field	Bits	Type	Description
UNUSED	7:6	-	**UNUSED** Reset: 0_H
PLLFCOMPC3	5	w	**Fractional Spurii Compensation enable for Channel 3** 0_B Disabled 1_B Enabled Reset: 0_H
PLLFRAC2C3	4:0	w	**Synthesizer channel frequency value (21 bits, bits 20:16), fractional division ratio for Channel 3** PLLFRAC(20:0) = dec2hex(((f_LO / f_XTAL) - PLLINT) * 2^21) Reset: 09_H

Special Function Register Page Register

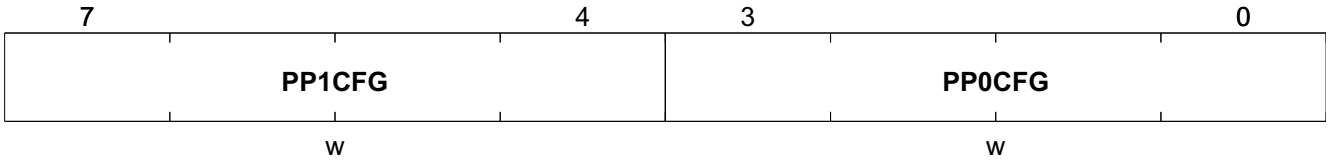
SFRPAGE	Offset	Reset Value
Special Function Register Page Register	**080_H**	**00_H**



Field	Bits	Type	Description
UNUSED	7:2	-	**UNUSED** Reset: 00_H
SFRPAGE	1:0	w	**Selection of Register Page File (Configuration A..D) for SPI communication** 00_B Page 0 (Config. A, start address: 000_H) 01_B Page 1 (Config. B, start address: 100_H) 10_B Page 2 (Config. C, start address: 200_H) 11_B Page 3 (Config. D, start address: 300_H) Reset: 0_H

PP0 and PP1 Configuration Register

PPCFG0	Offset	Reset Value
PP0 and PP1 Configuration Register	**081_H**	**50_H**

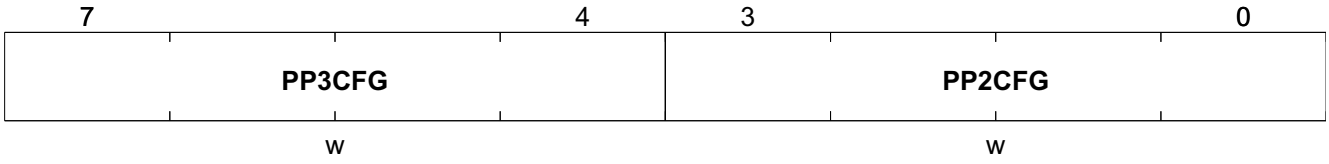


Field	Bits	Type	Description
PP1CFG	7:4	w	**Port Pin 1 Output Signal Selection** 0000_B CLK_OUT 0001_B RX_RUN 0010_B NINT 0011_B LOW 0100_B HIGH 0101_B DATA 0110_B DATA_MATCHFIL 0111_B n.u. 1000_B CH_DATA 1001_B CH_STR 1010_B RXD 1011_B RXSTR 1100_B n.u. 1101_B n.u. 1110_B n.u. 1111_B n.u. Reset: 5_H
PP0CFG	3:0	w	**Port Pin 0 Output Signal Selection** 0000_B CLK_OUT 0001_B RX_RUN 0010_B NINT 0011_B LOW 0100_B HIGH 0101_B DATA 0110_B DATA_MATCHFIL 0111_B n.u. 1000_B CH_DATA 1001_B CH_STR 1010_B RXD 1011_B RXSTR 1100_B n.u. 1101_B n.u. 1110_B n.u. 1111_B n.u. Reset: 0_H

PP2 and PP3 Configuration Register

PPCFG1 **Offset** **Reset Value**

PP2 and PP3 Configuration Register **082_H** **12_H**



Field	Bits	Type	Description
PP3CFG	7:4	w	**Port Pin 3 Output Signal Selection** 0000_B n.u. 0001_B RX_RUN 0010_B NINT 0011_B LOW 0100_B HIGH 0101_B DATA 0110_B DATA_MATCHFIL 0111_B n.u. 1000_B CH_DATA 1001_B CH_STR 1010_B RXD 1011_B RXSTR 1100_B n.u. 1101_B n.u. 1110_B n.u. 1111_B n.u. Reset: 1_H
PP2CFG	3:0	w	**Port Pin 2 Output Signal Selection** 0000_B CLK_OUT 0001_B RX_RUN 0010_B NINT 0011_B LOW 0100_B HIGH 0101_B DATA 0110_B DATA_MATCHFIL 0111_B n.u. 1000_B CH_DATA 1001_B CH_STR 1010_B RXD 1011_B RXSTR 1100_B n.u. 1101_B n.u. 1110_B n.u. 1111_B n.u. Reset: 2_H

PPx Port Configuration Register

PPCFG2	Offset	Reset Value
PPx Port Configuration Register	083_H	00_H

7	6	5	4	3	2	1	0
PP3HPPEN	PP2HPPEN	PP1HPPEN	PP0HPPEN	PP3INV	PP2INV	PP1INV	PP0INV
w	w	w	w	w	w	w	w

Field	Bits	Type	Description
PP3HPPEN	7	w	**PP3 High Power Pad Enable** 0_B Normal 1_B High Power Reset: 0_H
PP2HPPEN	6	w	**PP2 High Power Pad Enable** 0_B Normal 1_B High Power Reset: 0_H
PP1HPPEN	5	w	**PP1 High Power Pad Enable** 0_B Normal 1_B High Power Reset: 0_H
PP0HPPEN	4	w	**PP0 High Power Pad Enable** 0_B Normal 1_B High Power Reset: 0_H
PP3INV	3	w	**PP3 Inversion Enable** 0_B Not Inverted 1_B Inverted Reset: 0_H
PP2INV	2	w	**PP2 Inversion Enable** 0_B Not Inverted 1_B Inverted Reset: 0_H
PP1INV	1	w	**PP1 Inversion Enable** 0_B Not Inverted 1_B Inverted Reset: 0_H
PP0INV	0	w	**PP0 Inversion Enable** 0_B Not Inverted 1_B Inverted Reset: 0_H

RX RUN Configuration Register 0

RXRUNCFG0	Offset	Reset Value
RX RUN Configuration Register 0	084_H	FF_H

7	6	5	4	3	2	1	0
RXRUNPP 1D	RXRUNPP 1C	RXRUNPP 1B	RXRUNPP 1A	RXRUNPP 0D	RXRUNPP 0C	RXRUNPP 0B	RXRUNPP 0A
w	w	w	w	w	w	w	w

Field	Bits	Type	Description
RXRUNPP1D	7	w	**RXRUN Active Level on PP1 for Configuration D** 0_B Active Low 1_B Active High Reset: 1_H
RXRUNPP1C	6	w	**RXRUN Active Level on PP1 for Configuration C** 0_B Active Low 1_B Active High Reset: 1_H
RXRUNPP1B	5	w	**RXRUN Active Level on PP1 for Configuration B** 0_B Active Low 1_B Active High Reset: 1_H
RXRUNPP1A	4	w	**RXRUN Active Level on PP1 for Configuration A** 0_B Active Low 1_B Active High Reset: 1_H
RXRUNPP0D	3	w	**RXRUN Active Level on PP0 for Configuration D** 0_B Active Low 1_B Active High Reset: 1_H
RXRUNPP0C	2	w	**RXRUN Active Level on PP0 for Configuration C** 0_B Active Low 1_B Active High Reset: 1_H
RXRUNPP0B	1	w	**RXRUN Active Level on PP0 for Configuration B** 0_B Active Low 1_B Active High Reset: 1_H
RXRUNPP0A	0	w	**RXRUN Active Level on PP0 for Configuration A** 0_B Active Low 1_B Active High Reset: 1_H

RX RUN Configuration Register 1

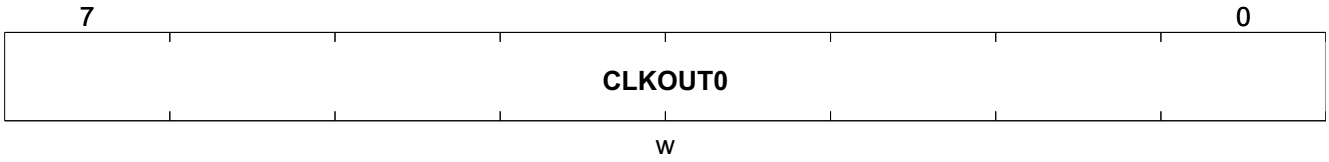
RXRUNCFG1	Offset	Reset Value
RX RUN Configuration Register 1	085_H	FF_H

7	6	5	4	3	2	1	0
RXRUNPP 3D	RXRUNPP 3C	RXRUNPP 3B	RXRUNPP 3A	RXRUNPP 2D	RXRUNPP 2C	RXRUNPP 2B	RXRUNPP 2A
w	w	w	w	w	w	w	w

Field	Bits	Type	Description
RXRUNPP3D	7	w	**RXRUN Active Level on PP3 for Configuration D** 0_B Active Low 1_B Active High Reset: 1_H
RXRUNPP3C	6	w	**RXRUN Active Level on PP3 for Configuration C** 0_B Active Low 1_B Active High Reset: 1_H
RXRUNPP3B	5	w	**RXRUN Active Level on PP3 for Configuration B** 0_B Active Low 1_B Active High Reset: 1_H
RXRUNPP3A	4	w	**RXRUN Active Level on PP3 for Configuration A** 0_B Active Low 1_B Active High Reset: 1_H
RXRUNPP2D	3	w	**RXRUN Active Level on PP2 for Configuration D** 0_B Active Low 1_B Active High Reset: 1_H
RXRUNPP2C	2	w	**RXRUN Active Level on PP2 for Configuration C** 0_B Active Low 1_B Active High Reset: 1_H
RXRUNPP2B	1	w	**RXRUN Active Level on PP2 for Configuration B** 0_B Active Low 1_B Active High Reset: 1_H
RXRUNPP2A	0	w	**RXRUN Active Level on PP2 for Configuration A** 0_B Active Low 1_B Active High Reset: 1_H

Clock Divider Register 0

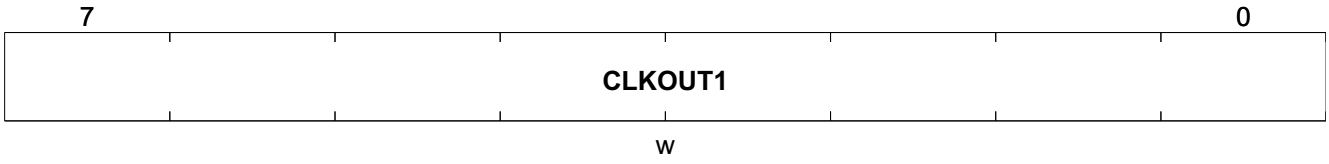
CLKOUT0	Offset	Reset Value
Clock Divider Register 0	086_H	$0B_H$



Field	Bits	Type	Description
CLKOUT0	7:0	w	**Clock Out Divider: CLKOUT(19:0) = CLKOUT2(MSB) & CLKOUT1 & CLKOUT0(LSB)** Min: 00002h = Clock divided by 2*2 Max: FFFFFh = Clock divided by ((2^20)-1)*2 Reg. value 00000h = Clock divided by (2^20)*2 Reset: $0B_H$

Clock Divider Register 1

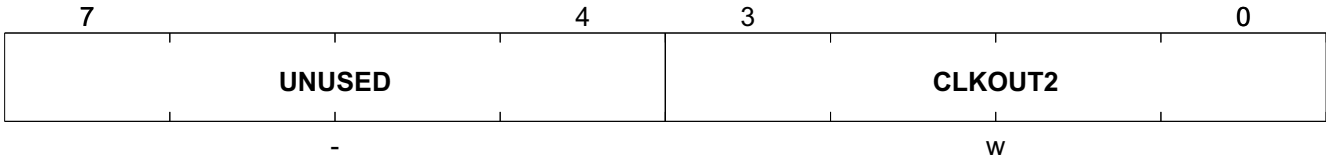
CLKOUT1	Offset	Reset Value
Clock Divider Register 1	087_H	00_H



Field	Bits	Type	Description
CLKOUT1	7:0	w	**Clock Out Divider: CLKOUT(19:0) = CLKOUT2(MSB) & CLKOUT1 & CLKOUT0(LSB)** Min: 00002h = Clock divided by 2*2 Max: FFFFFh = Clock divided by ((2^20)-1)*2 Reg. value 00000h = Clock divided by (2^20)*2 Reset: 00_H

Clock Divider Register 2

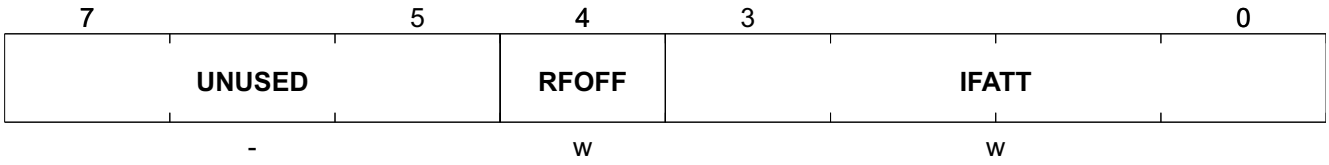
CLKOUT2	Offset	Reset Value
Clock Divider Register 2	088_H	00_H



Field	Bits	Type	Description
UNUSED	7:4	-	**UNUSED** Reset: 0_H
CLKOUT2	3:0	w	**Clock Out Divider: CLKOUT(19:0) = CLKOUT2(MSB) & CLKOUT1 & CLKOUT0(LSB)** Min: 00002h = Clock divided by 2*2 Max: FFFFFh = Clock divided by ((2^20)-1)*2 Reg. value 00000h = Clock divided by (2^20)*2 Reset: 0_H

RF Control Register

RFC	Offset	Reset Value
RF Control Register	**089_H**	**07_H**



Field	Bits	Type	Description
UNUSED	7:5	-	**UNUSED** Reset: 0_H
RFOFF	4	w	**Switch off RF-path (for RSSI trimming)** 0_B RF path enabled 1_B RF path disabled Reset: 0_H

Field	Bits	Type	Description
IFATT	3:0	w	**Adjust IF attenuation from LNA_IN to IF_OUT (Double-Down Conversion / Single-Down Conversion)** Used to trim out external component tolerances. 0000_B 0 dB / n.u. 0001_B 0.8 dB / n.u. 0010_B 1.6 dB / n.u. 0011_B 2.4 dB / n.u. 0100_B 3.2 dB / 0 dB 0101_B 4.0 dB / 0.8 dB 0110_B 4.8 dB / 1.6 dB 0111_B 5.6 dB / 2.4 dB 1000_B 6.4 dB / 3.2 dB 1001_B 7.2 dB / 4.0 dB 1010_B 8.0 dB / 4.8 dB 1011_B 8.8 dB / n.u. 1100_B 9.6 dB / n.u. 1101_B 10.4 dB / n.u. 1110_B 11.2 dB / n.u. 1111_B 12.0 dB / n.u. Reset: 7_H

BPF Calibration Configuration Register 0

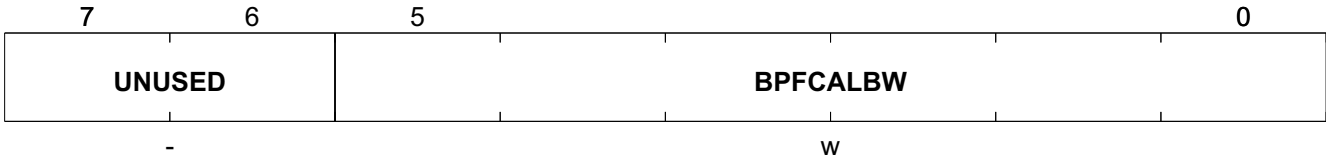
BPFCALCFG0	Offset	Reset Value
BPF Calibration Configuration Register 0	**$08A_H$**	**07_H**

7	5	4	3	0
UNUSED		Res	**BPFCALST**	
-			w	

Field	Bits	Type	Description
UNUSED	7:5	-	**UNUSED** Reset: 0_H
BPFCALST	3:0	w	**BPF Calibration Time (use default = 07_H)** Min: 0h= Txtal * 80 * 7 * (0 + 4) Max: Fh= Txtal * 80 * 7 * (15 + 4) Reset: 7_H

BPF Calibration Configuration Register 1

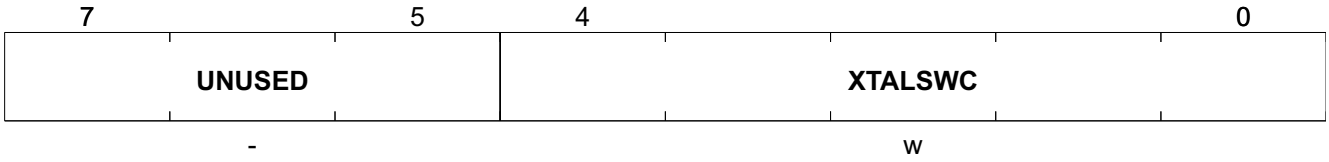
BPFCALCFG1	Offset	Reset Value
BPF Calibration Configuration Register 1	**$08B_H$**	**04_H**



Field	Bits	Type	Description
UNUSED	7:6	-	**UNUSED** Reset: 0_H
BPFCALBW	5:0	w	**Band Pass Filter Bandwidth Selection during Calibration** 04_H - 50 kHz (=default) $0D_H$ - 80 kHz 16_H - 125 kHz $1F_H$ - 200 kHz 27_H - 300 kHz Reset: 04_H

XTAL Coarse Calibration Register

XTALCAL0	Offset	Reset Value
XTAL Coarse Calibration Register	**$08C_H$**	**10_H**



Field	Bits	Type	Description
UNUSED	7:5	-	**UNUSED** Reset: 0_H
XTALSWC	4:0	w	**Xtal Trim Capacitor Value** Min 00h: 0pF Value 01h: 1pF Max 18h: 24pF higher values than 18h are automatically mapped to 24pF Reset: 10_H

XTAL Fine Calibration Register

XTALCAL1	Offset	Reset Value
XTAL Fine Calibration Register	**$08D_H$**	**00_H**

7	6	5	4	3	2	1	0
UNUSED				XTALSWF 3	XTALSWF 2	XTALSWF 1	XTALSWF 0
-				w	w	w	w

Field	Bits	Type	Description
UNUSED	7:4	-	**UNUSED** Reset: 0_H
XTALSWF3	3	w	**Connect 500 fF XTAL Trim capacitor** 0_B not connected 1_B connected Reset: 0_H
XTALSWF2	2	w	**Connect 250 fF XTAL Trim capacitor** 0_B not connected 1_B connected Reset: 0_H
XTALSWF1	1	w	**Connect 125 fF XTAL Trim capacitor** 0_B not connected 1_B connected Reset: 0_H
XTALSWF0	0	w	**Connect 62.5 fF XTAL Trim capacitor** 0_B not connected 1_B connected Reset: 0_H

RSSI Monitor Configuration Register

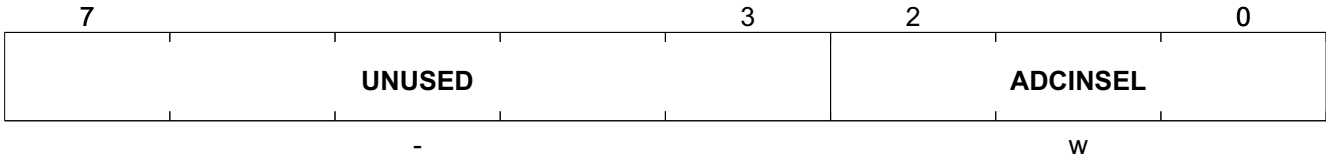
RSSIMONC	Offset	Reset Value
RSSI Monitor Configuration Register	**$08E_H$**	**01_H**

7	6	5	4	3	2	1	0
UNUSED					Res		RSSIMON EN
-							w

Field	Bits	Type	Description
UNUSED	7:3	-	**UNUSED** Reset: 00_H
RSSIMONEN	0	w	**Enable Buffer for RSSI pin** 0_B Disabled 1_B Enabled Reset: 1_H

ADC Input Selection Register

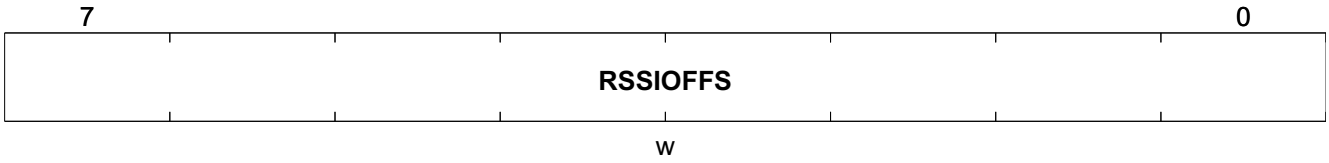
ADCINSEL	Offset	Reset Value
ADC Input Selection Register	$08F_H$	00_H



Field	Bits	Type	Description
UNUSED	7:3	-	**UNUSED** Reset: 00_H
ADCINSEL	2:0	w	**ADC Input Selection** 000_B RSSI 001_B Temperature 010_B VDDD / 2 011_B n.u. 100_B n.u. 101_B n.u. 110_B n.u. 111_B n.u. Reset: 0_H

RSSI Offset Register

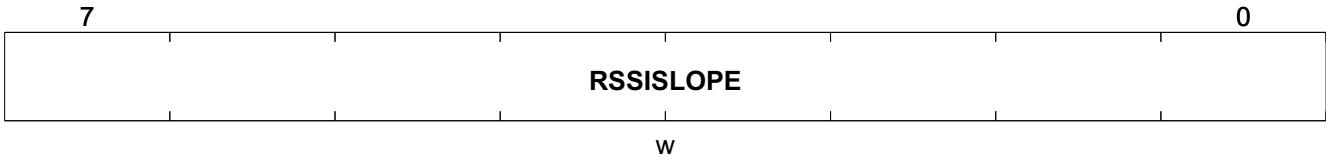
RSSIOFFS	Offset	Reset Value
RSSI Offset Register	090_H	80_H



Field	Bits	Type	Description
RSSIOFFS	7:0	w	**RSSI Offset Compensation Value** Min: 00h= -256 Max: FFh= 254 Reset: 80_H

RSSI Slope Register

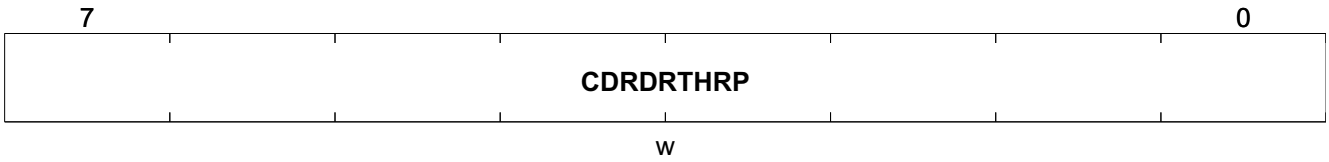
RSSISLOPE	Offset	Reset Value
RSSI Slope Register	091_H	80_H



Field	Bits	Type	Description
RSSISLOPE	7:0	w	**RSSI Slope Compensation Value (Multiplication Value)** Multiplication Factor = RSSISLOPE * 2^-7 Min: 00h= 0.0 Max: FFh= 1.992 Reset: 80_H

CDR Data Rate Acceptance Positive Threshold Register

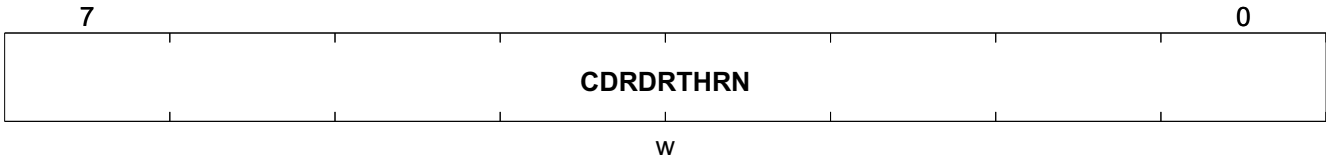
CDRDRTHRP	Offset	Reset Value
CDR Data Rate Acceptance Positive Threshold Register	092_H	$1E_H$



Field	Bits	Type	Description
CDRDRTHRP	7:0	w	**Data Rate Acceptance Positive Threshold Value** This feature can be turned on with *_CDRRI.DRLIMEN. Higher the value, more percent of the datarate is tolerated. Default => 10% Reset: $1E_H$

CDR Data Rate Acceptance Negative Threshold Register

CDRDRTHRN	Offset	Reset Value
CDR Data Rate Acceptance Negative Threshold Register	093_H	23_H



Field	Bits	Type	Description
CDRDRTHRN	7:0	w	**Data Rate Acceptance Negative Threshold Value** This feature can be turned on with *_CDRRI.DRLIMEN. Higher the value, more percent of the datarate is tolerated. Default => 10% Reset: 23_H

Interrupt Mask Register 0

IM0	Offset	Reset Value
Interrupt Mask Register 0	**094_H**	**00_H**

7	6	5	4	3	2	1	0
IMEOMB	**IMMIDFB**	**IMFSYNCB**	**IMWUB**	**IMEOMA**	**IMMIDFA**	**IMFSYNCA**	**IMWUA**
w	w	w	w	w	w	w	w

Field	Bits	Type	Description
IMEOMB	7	w	**Mask Interrupt on "End of Message" for Configuration B** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H
IMMIDFB	6	w	**Mask Interrupt on "Message ID Found" for Configuration B** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H
IMFSYNCB	5	w	**Mask Interrupt on "Frame Sync" for Configuration B** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H
IMWUB	4	w	**Mask Interrupt on "Wake-up" for Configuration B** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H
IMEOMA	3	w	**Mask Interrupt on "End of Message" for Configuration A** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H

Field	Bits	Type	Description
IMMIDFA	2	w	**Mask Interrupt on "Message ID Found" for Configuration A** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H
IMFSYNCA	1	w	**Mask Interrupt on "Frame Sync" for Configuration A** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H
IMWUA	0	w	**Mask Interrupt on "Wake-up" for Configuration A** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H

Interrupt Mask Register 1

IM1	Offset	Reset Value
Interrupt Mask Register 1	**095_H**	**00_H**

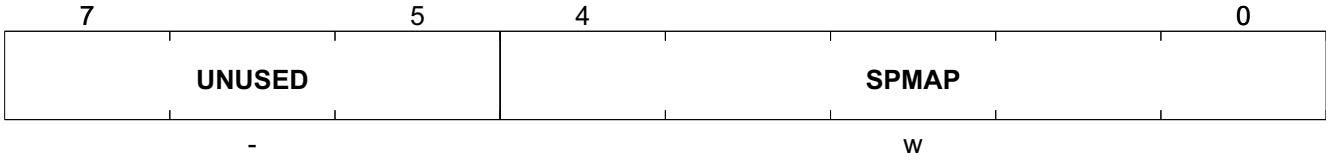
7	6	5	4	3	2	1	0
IMEOMD	**IMMIDFD**	**IMFSYNCD**	**IMWUD**	**IMEOMC**	**IMMIDFC**	**IMFSYNCC**	**IMWUC**
w	w	w	w	w	w	w	w

Field	Bits	Type	Description
IMEOMD	7	w	**Mask Interrupt on "End of Message" for Configuration D** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H
IMMIDFD	6	w	**Mask Interrupt on "Message ID Found" for Configuration D** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H
IMFSYNCD	5	w	**Mask Interrupt on "Frame Sync" for Configuration D** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H
IMWUD	4	w	**Mask Interrupt on "Wake-up" for Configuration D** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H
IMEOMC	3	w	**Mask Interrupt on "End of Message" for Configuration C** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H

Field	Bits	Type	Description
IMMIDFC	2	w	**Mask Interrupt on "Message ID Found" for Configuration C** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H
IMFSYNCC	1	w	**Mask Interrupt on "Frame Sync" for Configuration C** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H
IMWUC	0	w	**Mask Interrupt on "Wake-up" for Configuration C** 0_B Interrupt enabled 1_B Interrupt disabled Reset: 0_H

Self Polling Mode Active Periods Register

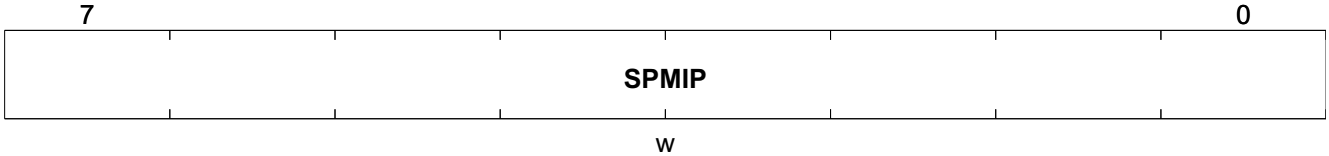
SPMAP	Offset	Reset Value
Self Polling Mode Active Periods Register	**096_H**	**01_H**



Field	Bits	Type	Description
UNUSED	7:5	-	**UNUSED** Reset: 0_H
SPMAP	4:0	w	**Self Polling Mode Active Periods value** Min: 01h = 1 (Master) Period Max: 1Fh = 31(Master) Periods Reg. value 00h = 32 (Master) Periods Reset: 01_H

Self Polling Mode Idle Periods Register

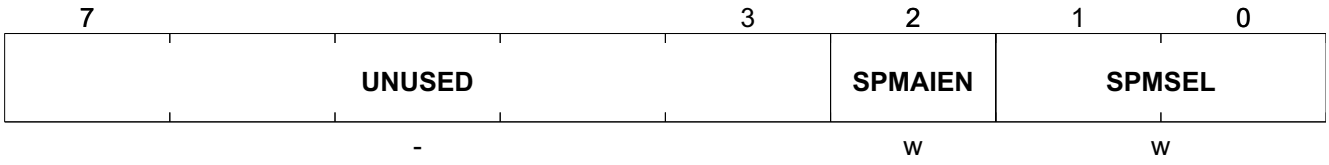
SPMIP	Offset	Reset Value
Self Polling Mode Idle Periods Register	**097_H**	**01_H**



Field	Bits	Type	Description
SPMIP	7:0	w	**Self Polling Mode Idle Periods value** Min: 01h = 1 (Master) Period Max: FFh = 255 (Master) Periods Reg. value 00h = 256 (Master) Periods Reset: 01_H

Self Polling Mode Control Register

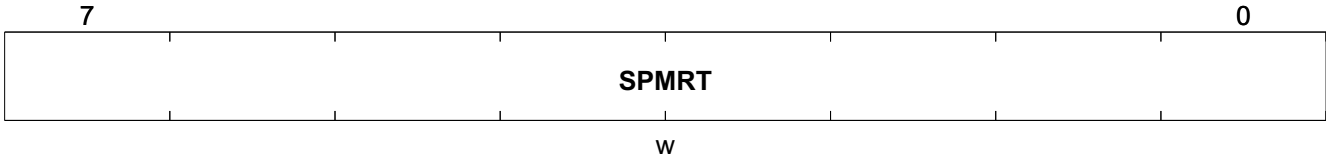
SPMC	Offset	Reset Value
Self Polling Mode Control Register	**098_H**	**00_H**



Field	Bits	Type	Description
UNUSED	7:3	-	**UNUSED** Reset: 00_H
SPMAIEN	2	w	**Self Polling Mode Active Idle Enable** 0_B Disabled 1_B Enabled Reset: 0_H
SPMSEL	1:0	w	**Self Polling Mode Selection** 00_B Constant On/Off (COO) 01_B Fast Fall Back to Sleep (FFB) 10_B Mixed Mode (MM, Combination of Const On/Off and Fast Fall Back to Sleep for different Configurations: COO, FFB, FFB, FFB) 11_B Permanent Wake Up Search (PWUS) Reset: 0_H

Self Polling Mode Reference Timer Register

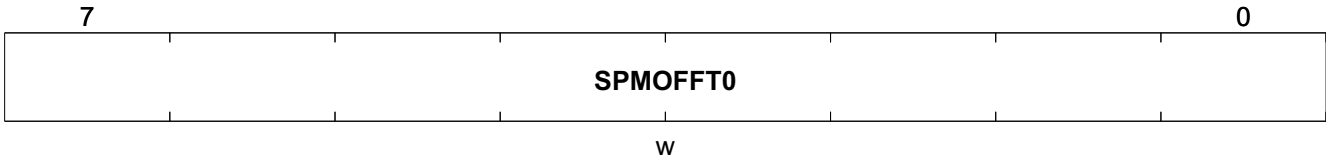
SPMRT	Offset	Reset Value
Self Polling Mode Reference Timer Register	**099_H**	**01_H**



Field	Bits	Type	Description
SPMRT	7:0	w	**Self Polling Mode Reference Timer value** The output of this timer is used as input for the On/Off Timer Incoming Periodic Time = 64 / fsys Output Periodic Time = TRT = (64 * SPMRT) / fsys Min: 01h = (64*1) / fsys Max: 00h = (64 * 256) / fsys Reset: 01_H

Self Polling Mode Off Time Register 0

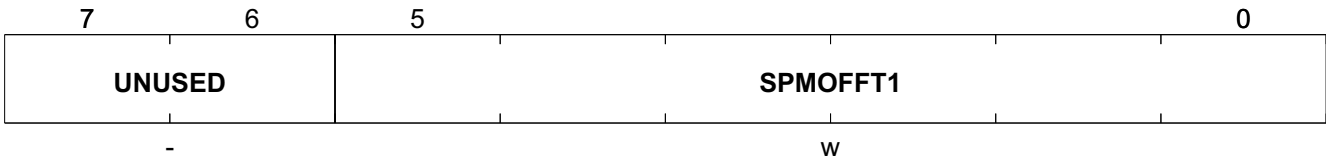
SPMOFFT0	Offset	Reset Value
Self Polling Mode Off Time Register 0	**$09A_H$**	**01_H**



Field	Bits	Type	Description
SPMOFFT0	7:0	w	**Self Polling Mode Off Time value: SPMOFFT(13:0) = SPMOFFT1(MSB) & SPMOFFT0(LSB)** Off -Time = TRT * SPMOFFT Min: 0001h = 1 * TRT Reg.Value 3FFFh = 16383 * TRT Max: 0000h = 16384 * TRT Reset: 01_H

Self Polling Mode Off Time Register 1

SPMOFFT1	Offset	Reset Value
Self Polling Mode Off Time Register 1	**$09B_H$**	**00_H**

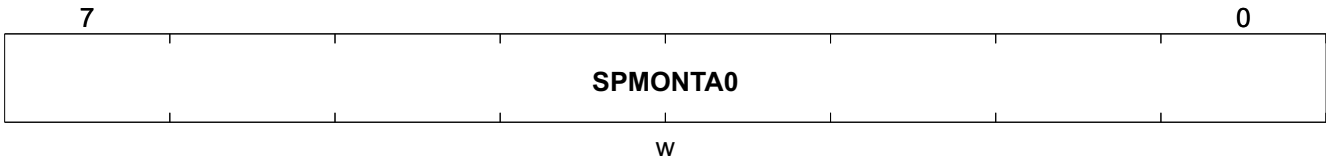


Field	Bits	Type	Description
UNUSED	7:6	-	**UNUSED** Reset: 0_H

Field	Bits	Type	Description
SPMOFFT1	5:0	w	**Self Polling Mode Off Time value: SPMOFFT(13:0) = SPMOFFT1(MSB) & SPMOFFT0(LSB)** Off -Time = TRT * SPMOFFT Min: 0001h = 1 * TRT Reg.Value 3FFFh = 16383 * TRT Max: 0000h = 16384 * TRT Reset: 00_H

Self Polling Mode On Time Config A Register 0

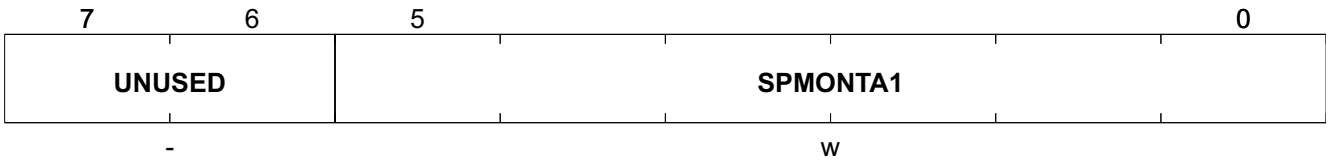
SPMONTA0	Offset	Reset Value
Self Polling Mode On Time Config A Register 0	**$09C_H$**	**01_H**



Field	Bits	Type	Description
SPMONTA0	7:0	w	**Set Value Self Polling Mode On Time: SPMONTA(13:0) = SPMONTA1(MSB) & SPMONTA0(LSB)** On-Time = TRT *SPMONTA Min: 0001h = 1*TRT Reg.Value: 3FFFh = 16383*TRT Max: 0000h = 16384*TRT Reset: 01_H

Self Polling Mode On Time Config A Register 1

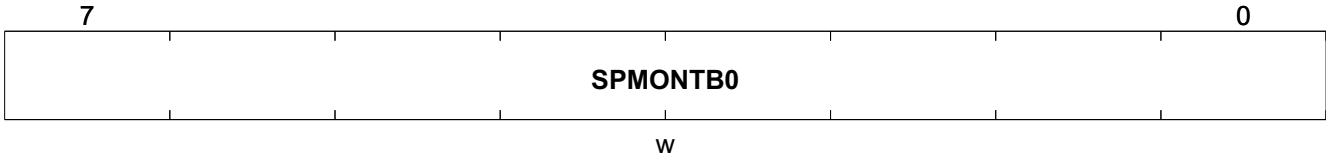
SPMONTA1	Offset	Reset Value
Self Polling Mode On Time Config A Register 1	**$09D_H$**	**00_H**



Field	Bits	Type	Description
UNUSED	7:6	-	**UNUSED** Reset: 0_H
SPMONTA1	5:0	w	**Set Value Self Polling Mode On Time: SPMONTA(13:0) = SPMONTA1(MSB) & SPMONTA0(LSB)** On-Time = TRT *SPMONTA Min: 0001h = 1*TRT Reg.Value: 3FFFh = 16383*TRT Max: 0000h = 16384*TRT Reset: 00_H

Self Polling Mode On Time Config B Register 0

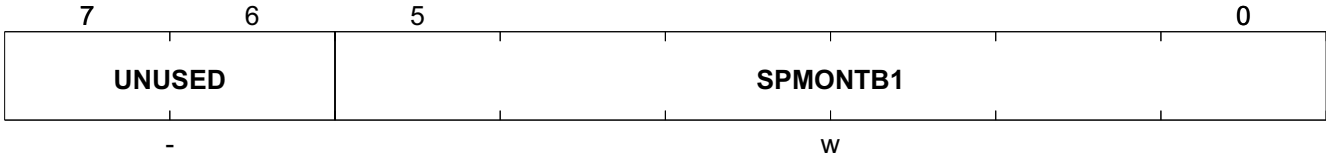
SPMONTB0	Offset	Reset Value
Self Polling Mode On Time Config B Register 0	**$09E_H$**	**01_H**



Field	Bits	Type	Description
SPMONTB0	7:0	w	**Set Value Self Polling Mode On Time: SPMONTB(13:0) = SPMONTB1(MSB) & SPMONTB0(LSB)** On-Time = TRT *SPMONTB Min: 0001h = 1*TRT Reg.Value: 3FFFh = 16383*TRT Max: 0000h = 16384*TRT Reset: 01_H

Self Polling Mode On Time Config B Register 1

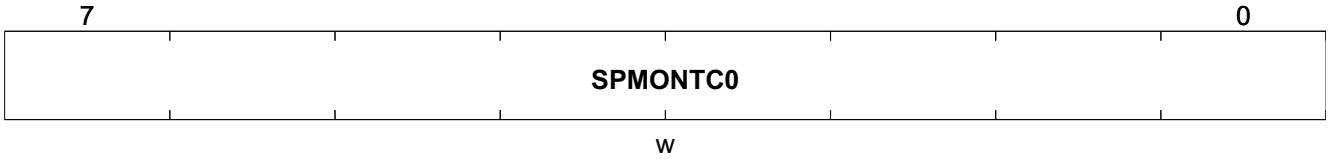
SPMONTB1	Offset	Reset Value
Self Polling Mode On Time Config B Register 1	**$09F_H$**	**00_H**



Field	Bits	Type	Description
UNUSED	7:6	-	**UNUSED** Reset: 0_H
SPMONTB1	5:0	w	**Set Value Self Polling Mode On Time: SPMONTB(13:0) = SPMONTB1(MSB) & SPMONTB0(LSB)** On-Time = TRT *SPMONTB Min: 0001h = 1*TRT Reg.Value: 3FFFh = 16383*TRT Max: 0000h = 16384*TRT Reset: 00_H

Self Polling Mode On Time Config C Register 0

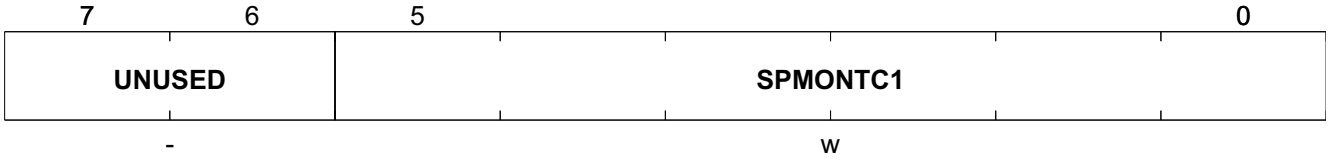
SPMONTC0	Offset	Reset Value
Self Polling Mode On Time Config C Register 0	**$0A0_H$**	**01_H**



Field	Bits	Type	Description
SPMONTC0	7:0	w	**Set Value Self Polling Mode On Time: SPMONTC(13:0) = SPMONTC1(MSB) & SPMONTC0(LSB)** On-Time = TRT *SPMONTC Min: 0001h = 1*TRT Reg.Value: 3FFFh = 16383*TRT Max: 0000h = 16384*TRT Reset: 01_H

Self Polling Mode On Time Config C Register 1

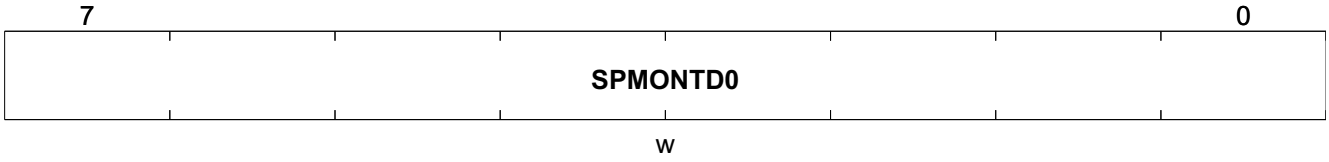
SPMONTC1	Offset	Reset Value
Self Polling Mode On Time Config C Register 1	**$0A1_H$**	**00_H**



Field	Bits	Type	Description
UNUSED	7:6	-	**UNUSED** Reset: 0_H
SPMONTC1	5:0	w	**Set Value Self Polling Mode On Time: SPMONTC(13:0) = SPMONTC1(MSB) & SPMONTC0(LSB)** On-Time = TRT *SPMONTC Min: 0001h = 1*TRT Reg.Value: 3FFFh = 16383*TRT Max: 0000h = 16384*TRT Reset: 00_H

Self Polling Mode On Time Config D Register 0

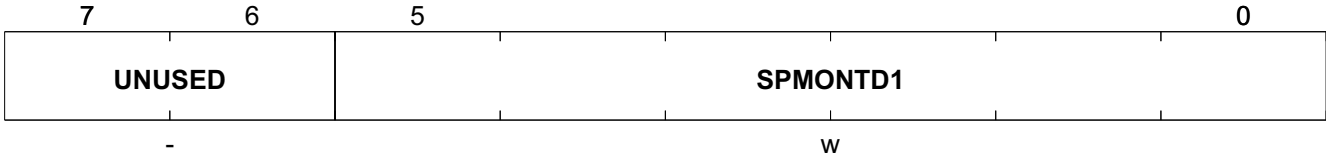
SPMONTD0	Offset	Reset Value
Self Polling Mode On Time Config D Register 0	**$0A2_H$**	**01_H**



Field	Bits	Type	Description
SPMONTD0	7:0	w	**Set Value Self Polling Mode On Time: SPMONTD(13:0) = SPMONTD1(MSB) & SPMONTD0(LSB)** On-Time = TRT *SPMONTD Min: 0001h = 1*TRT Reg.Value: 3FFFh = 16383*TRT Max: 0000h = 16384*TRT Reset: 01_H

Self Polling Mode On Time Config D Register 1

SPMONTD1	Offset	Reset Value
Self Polling Mode On Time Config D Register 1	**$0A3_H$**	**00_H**



Field	Bits	Type	Description
UNUSED	7:6	-	**UNUSED** Reset: 0_H
SPMONTD1	5:0	w	**Set Value Self Polling Mode On Time: SPMONTD(13:0) = SPMONTD1(MSB) & SPMONTD0(LSB)** On-Time = TRT *SPMONTD Min: 0001h = 1*TRT Reg.Value: 3FFFh = 16383*TRT Max: 0000h = 16384*TRT Reset: 00_H

External Processing Command Register

EXTPCMD	Offset	Reset Value
External Processing Command Register	**$0A4_H$**	**00_H**

7	6	4	3	2	1	0
Res	UNUSED		AGCMANF	AFCMANF	EXTTOTIM	EXTEOM
	-		wc	wc	wc	wc

Field	Bits	Type	Description
UNUSED	6:4	-	**UNUSED** Reset: 0_H
AGCMANF	3	wc	**AGC Manual Freeze** When *_AGCSFCFG.AGCFREEZE set to SPI Command, this bit sets the AGC to freeze mode 0_B Inactive 1_B Active Reset: 0_H
AFCMANF	2	wc	**AFC Manual Freeze** When *_AFCSFCFG.AFCFREEZE set to SPI Command, this bit sets the AFC to freeze mode 0_B Inactive 1_B Active Reset: 0_H
EXTTOTIM	1	wc	**Force TOTIM signal in external data processing mode (*_CHCFG.EXTROC = 1_H or 2_H)** 0_B no external TOTIM signal forced 1_B external TOTIM signal forced Reset: 0_H

Field	Bits	Type	Description
EXTEOM	0	wc	**Force EOM signal in external data processing mode (*_CHCFG.EXTROC = 1_H or 2_H)** 0_B no external EOM signal forced 1_B external EOM signal forced Reset: 0_H

Chip Mode Control Register 1

CMC1	Offset	Reset Value
Chip Mode Control Register 1	**$0A5_H$**	**04_H**

7	6	5	4	3	2	1	0
UNUSED		EOM2NCFG	TOTIM2NCH	INITFIFO	FSINITFIFO	FIFOLK	XTALHPMS
-		w	w	w	w	w	w

Field	Bits	Type	Description
UNUSED	7:6	-	**UNUSED** Reset: 0_H
EOM2NCFG	5	w	**Continue with next Configuration in Self Polling Mode after EOM detected in Run Mode Self Polling** 0_B Continue with Configuration A in Self Polling Mode 1_B Continue with next Configuration in Self Polling Mode Reset: 0_H
TOTIM2NCH	4	w	**Continue with next RF channel in Self Polling Mode after TOTIM detected in Run Mode Self Polling. In case of single RF channel application this means "continue with next Configuration" instead of "continue with next RF channel".** 0_B Continue with Configuration A in Self Polling Mode 1_B Continue with next RF channel in Self Polling Mode Reset: 0_H
INITFIFO	3	w	**Initialization of FIFO at Cycle Start** This Initialization of the FIFO can be configured in both Run Mode Slave and Self Polling Mode. In Run Mode Slave this happens at the beginning. In Self Polling Mode the initialization is done after Wake up found (switching from Self Polling Mode to Run Mode Self Polling). 0_B Initialization disabled 1_B Initialization enabled Reset: 0_H
FSINITFIFO	2	w	**Initialization of FIFO at Frame Start** 0_B Initialization disabled 1_B Initialization enabled Reset: 1_H

Field	Bits	Type	Description
FIFOLK	1	w	**Lock Data FIFO at EOM** 0_B FIFO lock is disabled 1_B FIFO lock is enabled at EOM. This also locks the digital receive chain at EOM until release from FIFO lock state. Reset: 0_H
XTALHPMS	0	w	**XTAL High Precision Mode in Sleep Mode** 0_B Disabled 1_B Enabled Reset: 0_H

Chip Mode Control Register 0

CMC0	Offset	Reset Value
Chip Mode Control Register 0	$0A6_H$	10_H

7	6	5	4	3	2	1	0
SDOHPPEN	INITPLLHOLD	HOLD	CLKOUTEN	MCS		SLRXEN	MSEL
w	w	w	w	w		w	w

Field	Bits	Type	Description
SDOHPPEN	7	w	**SDO High Power Pad Enable** 0_B Normal 1_B High Power Reset: 0_H
INITPLLHOLD	6	w	**Init PLL after coming from HOLD (when new channel programmed).** This requires an additional Channel Hop Time before initialization of the Digital Receiver. 0_B No init of PLL 1_B Init of PLL Reset: 0_H
HOLD	5	w	**Holds the chip in the Register Configuration state (only in Run Mode Slave)** 0_B Normal Operation 1_B Jump into the Register Config state Hold Reset: 0_H
CLKOUTEN	4	w	**CLK_OUT Enable** 0_B Disabled 1_B Enable programmable clock output Reset: 1_H

Field	Bits	Type	Description
MCS	3:2	w	**Multi Configuration Selection (Run Mode Slave / Self Polling Mode)** 00_B Config A / Config A 01_B Config B / Config A + B 10_B Config C / Config A + B + C 11_B Config D / Config A + B + C + D Reset: 0_H
SLRXEN	1	w	**Slave Receiver Enable** This Bit is only used in Operating Mode Run Mode Slave / Sleep Mode 0_B Receiver is in Sleep Mode 1_B Receiver is in Run Mode Slave Reset: 0_H
MSEL	0	w	**Operating Mode Selection** 0_B Run Mode Slave / Sleep Mode 1_B Self Polling Mode Reset: 0_H

Wakeup Peak Detector Readout Register

RSSIPWU	Offset	Reset Value
Wakeup Peak Detector Readout Register	**$0A7_H$**	**00_H**

7	6	5	4	3	2	1	0
RSSIPWU							
r							

Field	Bits	Type	Description
RSSIPWU	7:0	r	**Peak Detector Level at Wakeup** Set at every WU event and also set at the end of every configuration/channel cycle within a Self Polling period. Cleared at Reset only. Reset: 00_H

Interrupt Status Register 0

IS0	Offset	Reset Value
Interrupt Status Register 0	**$0A8_H$**	**FF_H**

7	6	5	4	3	2	1	0
EOMB	MIDFB	FSYNCB	WUB	EOMA	MIDFA	FSYNCA	WUA
rc	rc	rc	rc	rc	rc	rc	rc

Field	Bits	Type	Description
EOMB	7	rc	**Interrupt Request by "End of Message" from Configuration B (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H
MIDFB	6	rc	**Interrupt Request by "Message ID Found" from Configuration B (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H
FSYNCB	5	rc	**Interrupt Request by "Frame Sync" from Configuration B (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H
WUB	4	rc	**Interrupt Request by "Wake Up" from Configuration B (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H
EOMA	3	rc	**Interrupt Request by "End of Message" from Configuration A (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H
MIDFA	2	rc	**Interrupt Request by "Message ID Found" from Configuration A (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H
FSYNCA	1	rc	**Interrupt Request by "Frame Sync" from Configuration A (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H
WUA	0	rc	**Interrupt Request by "Wake Up" from Configuration A (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H

Interrupt Status Register 1

IS1	Offset	Reset Value
Interrupt Status Register 1	$0A9_H$	FF_H

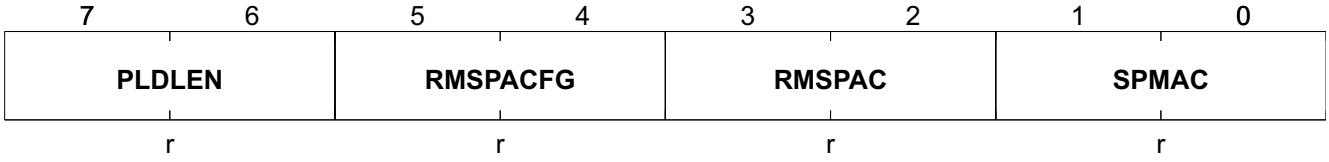
7	6	5	4	3	2	1	0
EOMD	MIDFD	FSYNCD	WUD	EOMC	MIDFC	FSYNCC	WUC
rc	rc	rc	rc	rc	rc	rc	rc

Field	Bits	Type	Description
EOMD	7	rc	**Interrupt Request by "End of Message" from Configuration D (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H
MIDFD	6	rc	**Interrupt Request by "Message ID Found" from Configuration D (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H
FSYNCD	5	rc	**Interrupt Request by "Frame Sync" from Configuration D (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H
WUD	4	rc	**Interrupt Request by "Wake Up" from Configuration D (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H
EOMC	3	rc	**Interrupt Request by "End of Message" from Configuration C (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H
MIDFC	2	rc	**Interrupt Request by "Message ID Found" from Configuration C (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H
FSYNCC	1	rc	**Interrupt Request by "Frame Sync" from Configuration C (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H

Field	Bits	Type	Description
WUC	0	rc	**Interrupt Request by "Wake Up" from Configuration C (Reset event sets all Bits to 1)** 0_B Not detected 1_B Detected Reset: 1_H

RF PLL Actual Channel and Configuration Register

RFPLLACC	Offset	Reset Value
RF PLL Actual Channel and Configuration Register	**$0AA_H$**	**00_H**



Field	Bits	Type	Description
PLDLEN	7:6	r	**Payload Data Length stored at TSI detection of the next message, PLDLEN(9:0) = RFPLLACC.PLDLEN(MSB) & PLDLEN(LSB).** Cleared with INIT FIFO Min. 000h = 0 bits received Max. 3FFh = 1023 bits received Reset: 0_H
RMSPACFG	5:4	r	**RF PLL Run Mode Self Polling Actual Configuration** 00_B Configuration A 01_B Configuration B 10_B Configuration C 11_B Configuration D Reset: 0_H
RMSPAC	3:2	r	**RF PLL Run Mode Self Polling Actual Channel** 00_B No valid data in FIFO from any channel and configuration 01_B Data in FIFO belong to Channel 1 10_B Data in FIFO belong to Channel 2 11_B Data in FIFO belong to Channel 3 Reset: 0_H
SPMAC	1:0	r	**RF PLL Self Polling Mode Actual Channel** 00_B No Wake Up from any Channel was actually found 01_B Wake Up was found from Channel 1 10_B Wake Up was found from Channel 2 11_B Wake Up was found from Channel 3 Reset: 0_H

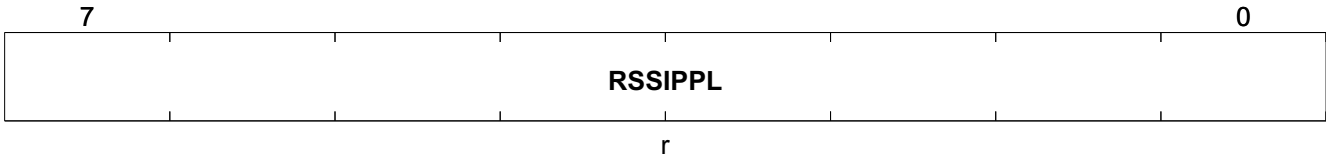
RSSI Peak Detector Readout Register

RSSIPRX	Offset	Reset Value
RSSI Peak Detector Readout Register	$0AB_H$	00_H

Field	Bits	Type	Description
RSSIPRX	7:0	rc	**RSSI Peak Level during Receiving** Tracking is active when Digital Receiver is enabled Set at higher peak levels than stored Cleared at Reset and SPI read out Reset: 00_H

RSSI Payload Peak Detector Readout Register

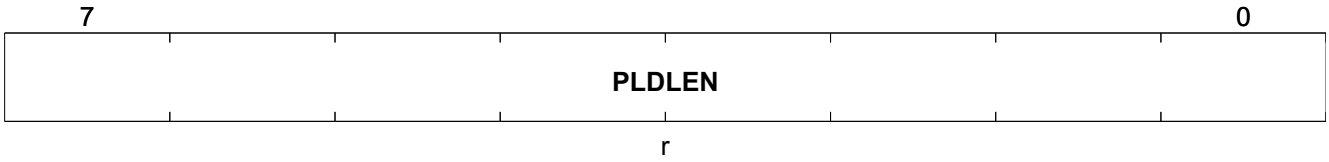
RSSIPPL	Offset	Reset Value
RSSI Payload Peak Detector Readout Register	$0AC_H$	00_H



Field	Bits	Type	Description
RSSIPPL	7:0	r	**RSSI Peak Level during Payload** Tracking starts after FSYNC + PKBITPOS Set at every EOM Cleared at the Reset only Reset: 00_H

Payload Data Length Register

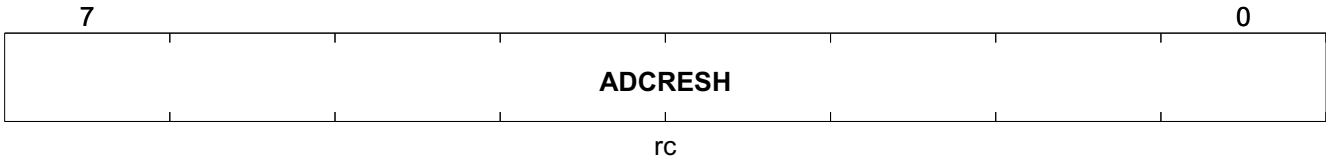
PLDLEN	Offset	Reset Value
Payload Data Length Register	$0AD_H$	00_H



Field	Bits	Type	Description
PLDLEN	7:0	r	**Payload Data Length stored at TSI detection of the next message, PLDLEN(9:0) = RFPLLACC.PLDLEN(MSB) & PLDLEN(LSB).** Cleared with INIT FIFO Min. 000h = 0 bits received Max. 3FFh = 1023 bits received Reset: 00_H

ADC Result High Byte Register

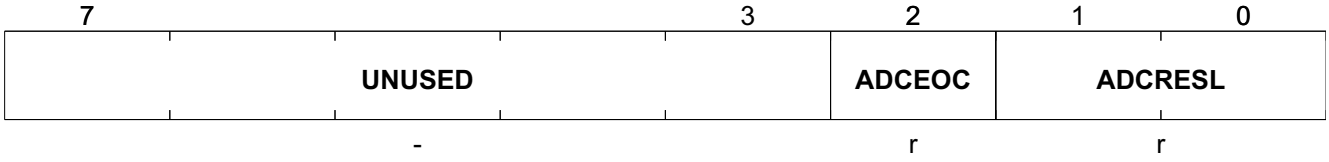
ADCRESH	Offset	Reset Value
ADC Result High Byte Register	**$0AE_H$**	**00_H**



Field	Bits	Type	Description
ADCRESH	7:0	rc	**ADC Result Value ADCRES(9:0) = ADCRESH(7:0) & ADCRESL(1:0)** Note: RC for control signal generation only, no clear Reset: 00_H

ADC Result Low Byte Register

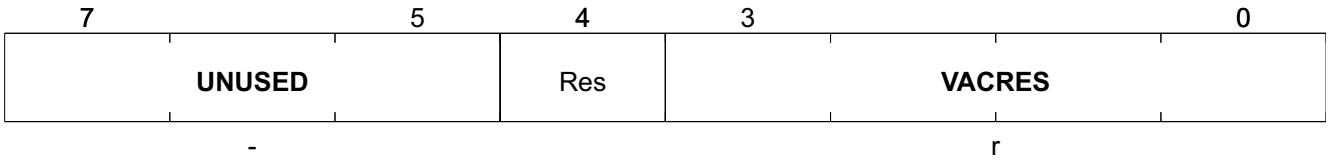
ADCRESL	Offset	Reset Value
ADC Result Low Byte Register	**$0AF_H$**	**00_H**



Field	Bits	Type	Description
UNUSED	7:3	-	**UNUSED** Reset: 00_H
ADCEOC	2	r	**ADC End of Conversion detected** 0_B not detected 1_B detected Reset: 0_H
ADCRESL	1:0	r	**ADC Result Value ADCRES(9:0) = ADCRESH(7:0) & ADCRESL(1:0)** The 2 LSBs of the ADC result are captured when the SFR register ADCRESH is readout. Reset: 0_H

VCO Autocalibration Result Readout Register

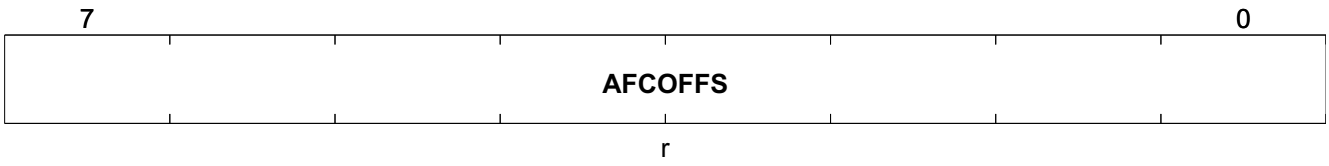
VACRES	Offset	Reset Value
VCO Autocalibration Result Readout Register	**$0B0_H$**	**00_H**



Field	Bits	Type	Description
UNUSED	7:5	-	**UNUSED** Reset: 0_H
VACRES	3:0	r	**VCO Autocalibration Result** Returns the VCO range selected by VCO Autocalibration Reset: 0_H

AFC Offset Read Register

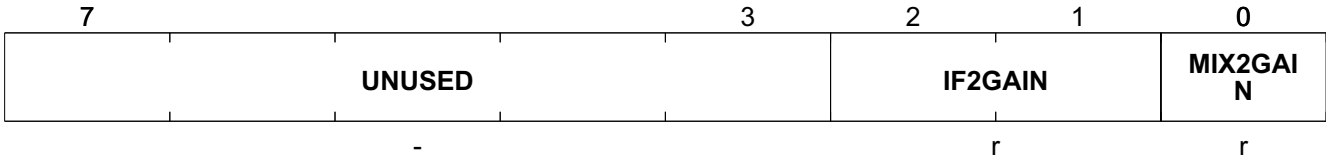
AFCOFFSET	Offset	Reset Value
AFC Offset Read Register	**$0B1_H$**	**00_H**



Field	Bits	Type	Description
AFCOFFS	7:0	r	**Readout of the Frequency Offset found by AFC (AFC loop filter output).** Value is in signed representation. Frequency resolution is 2.68 kHz/digit Output can be limited by x_AFCLIMIT register Update rate is 548 kHz Reset: 00_H

AGC Gain Readout Register

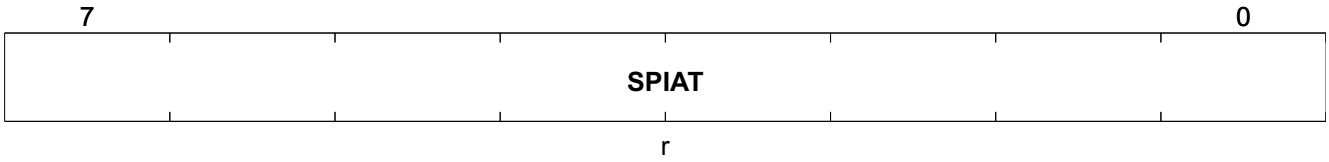
AGCGAINR	Offset	Reset Value
AGC Gain Readout Register	**$0B2_H$**	**00_H**



Field	Bits	Type	Description
UNUSED	7:3	-	**UNUSED** Reset: 00_H
IF2GAIN	2:1	r	**AGC IF2 Gain Readout** 00_B 0 dB 01_B -15 dB 10_B -30 dB 11_B n.u. Reset: 0_H
MIX2GAIN	0	r	**AGC MIX2 Gain Readout** 0_B 0 dB 1_B -15 dB Reset: 0_H

SPI Address Tracer Register

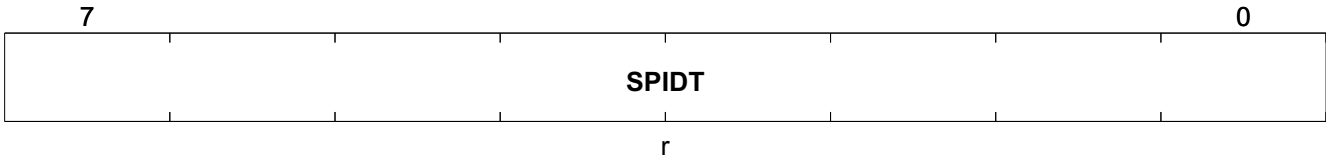
SPIAT	Offset	Reset Value
SPI Address Tracer Register	**$0B3_H$**	**00_H**



Field	Bits	Type	Description
SPIAT	7:0	r	**SPI Address Tracer, Readout of the last address of a SFR Register written by SPI** Reset: 00_H

SPI Data Tracer Register

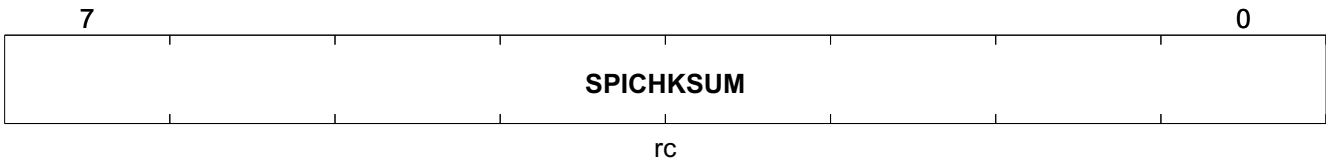
SPIDT	Offset	Reset Value
SPI Data Tracer Register	**$0B4_H$**	**00_H**



Field	Bits	Type	Description
SPIDT	7:0	r	**SPI Data Tracer, Readout of the last written data to a SFR Register by SPI** Reset: 00_H

SPI Checksum Register

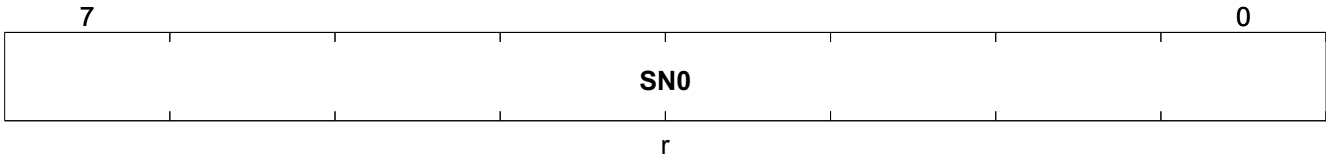
SPICHKSUM	Offset	Reset Value
SPI Checksum Register	**$0B5_H$**	**00_H**



Field	Bits	Type	Description
SPICHKSUM	7:0	rc	**SPI Checksum Readout** Reset: 00_H

Serial Number Register 0

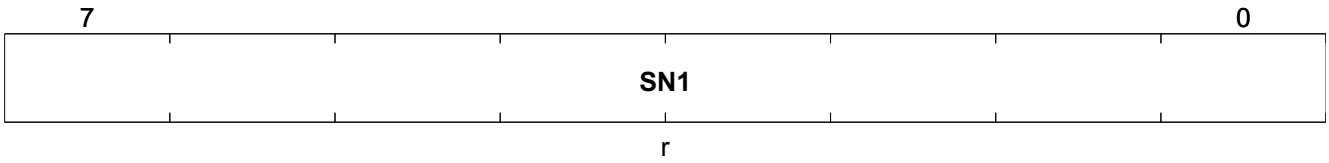
SN0	Offset	Reset Value
Serial Number Register 0	$0B6_H$	00_H



Field	Bits	Type	Description
SN0	7:0	r	**Serial Number: SN(31:0) = SN3(MSB) & SN2 & SN1 & SN0(LSB)** Reset: 00_H

Serial Number Register 1

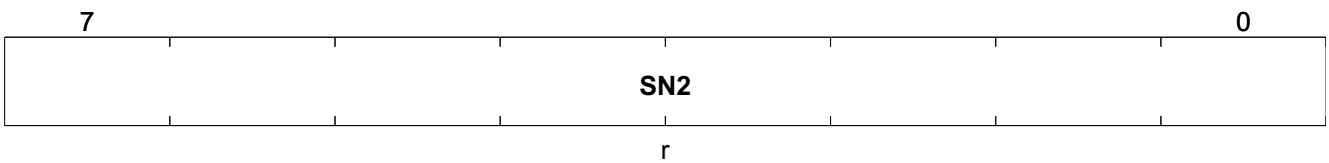
SN1	Offset	Reset Value
Serial Number Register 1	$0B7_H$	00_H



Field	Bits	Type	Description
SN1	7:0	r	**Serial Number: SN(31:0) = SN3(MSB) & SN2 & SN1 & SN0(LSB)** Reset: 00_H

Serial Number Register 2

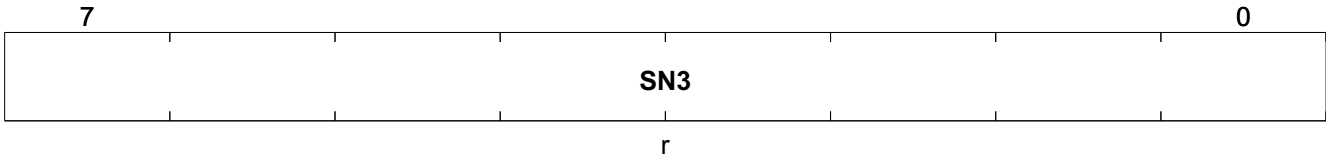
SN2	Offset	Reset Value
Serial Number Register 2	$0B8_H$	00_H



Field	Bits	Type	Description
SN2	7:0	r	**Serial Number: SN(31:0) = SN3(MSB) & SN2 & SN1 & SN0(LSB)** Reset: 00_H

Serial Number Register 3

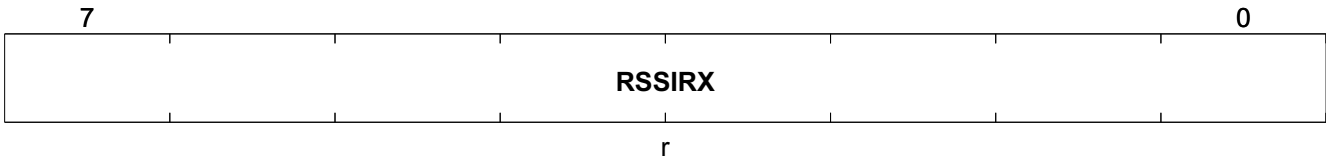
SN3	Offset	Reset Value
Serial Number Register 3	**$0B9_H$**	**00_H**



Field	Bits	Type	Description
SN3	7:0	r	**Serial Number: SN(31:0) = SN3(MSB) & SN2 & SN1 & SN0(LSB)** Reset: 00_H

RSSI Readout Register

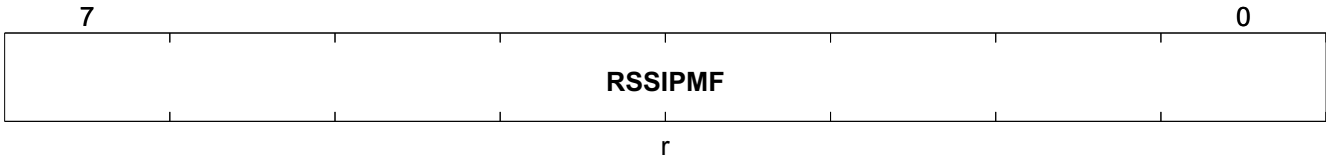
RSSIRX	Offset	Reset Value
RSSI Readout Register	**$0BA_H$**	**00_H**



Field	Bits	Type	Description
RSSIRX	7:0	r	**RSSI value after averaging over 4 samples** Reset: 00_H

RSSI Peak Memory Filter Readout Register

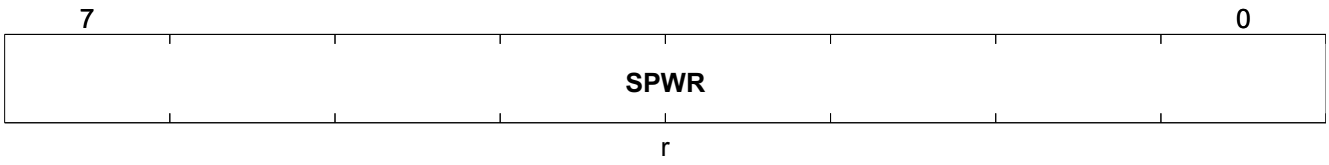
RSSIPMF	Offset	Reset Value
RSSI Peak Memory Filter Readout Register	**$0BB_H$**	**00_H**



Field	Bits	Type	Description
RSSIPMF	7:0	r	**RSSI Peak Memory Filter Level** Reset: 00_H

Signal Power Readout Register

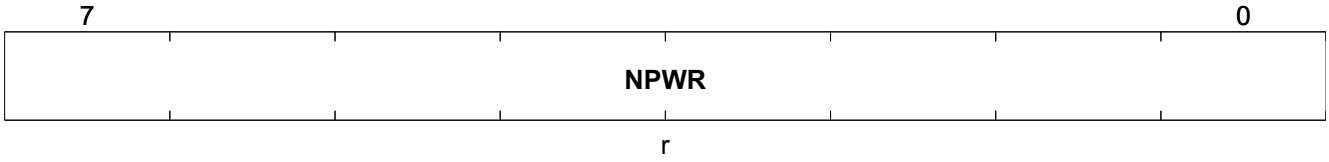
SPWR	Offset	Reset Value
Signal Power Readout Register	**$0BC_H$**	**00_H**



Field	Bits	Type	Description
SPWR	7:0	r	**Signal Power** The register contains the actual signal power which should be used to calculate the value of x_SIGDET0, x_SIGDET1 and x_SIGDETLO registers Reset: 00_H

Noise Power Readout Register

NPWR	Offset	Reset Value
Noise Power Readout Register	**$0BD_H$**	**00_H**



Field	Bits	Type	Description
NPWR	7:0	r	**FSK Noise Power** The register contains the actual noise power which should be used to calculate the value for the x_NDTHRES register Reset: 00_H