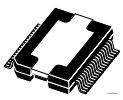
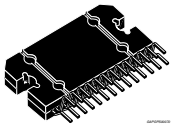
TDA7808

High efficiency digital input automotive quad power amplifier, ’start stop’ compatible

Datasheet - production data



PowerSO-36 (Slug up)



Flexiwatt27 (Vertical)

Features

- AEC-Q100 qualified
- 24-bit digital processing
- 115 dB dynamic range (A-weighted)
- SB-I (SB - improved) high efficiency operation the highest ’non - class D’ efficiency
- High output power capability:
  - 4 x 27 W 4 Ω @ 14.4 V, 1 kHz, THD = 10%
- Flexible mode control:
  - Full I^2C bus driving 1.8 V/3.3 V) with four addresses selectable (only for PowerSO36 package option)
  - Independent front/rear play/ mute
  - Selectable digital gains for very-low noise line-out function
- Start-stop compatibility (operation down to 6 V)
- Sample rates: 44.1 kHz, 48 kHz, 96 kHz, 192 kHz
- Flexible serial data port (1.8 V / 3.3 V):
  - I^2S standard, TDM 4Ch, TDM 8Ch, TDM 16ch (8+8ch)
- Offset detector
- Independent front/rear clipping detector
- CMOS compatible enable pin
- Thermal protection
- Pop free in mute to play transitions and viceversa

Description

TDA7808 is a single chip quad bridge amplifier in advanced BCD technology integrating: a full D/A converter, digital input for direct connection to I^2S (or TDM) and powerful MOSFET output stages.

The integrated D/A converter allows the performance to reach an outstanding 115 dB S/N ratio with more than 110 dB of dynamic range.

Moreover TDA7808 integrates an innovative high efficiency concept, optimized also for uncorrelated music signals. The device is designed to be compatible to battery modulation for class-G systems.

Thanks to this concept, the dissipated output power under average listening conditions can be reduced up to 50% when compared to the conventional class AB solutions.

TDA7808 integrates also a programmable PLL that is able to lock at the input frequencies of 64*Fs for all the input configurations.

TDA7808 is able to play music down to 6 V supply voltage - so it is compatible with the so called 'start stop' battery profile recently adopted by car makers (thus reducing the fuel consumption and the impact over the environment).

Table 1. Device summary

Order code	Package	Packing
TDA7808-ZSX	PowerSO36 (Slug up)	Tube
TDA7808-ZST		Tape & reel
TDA7808-48X	Flexiwatt27 (Vertical)	Tube

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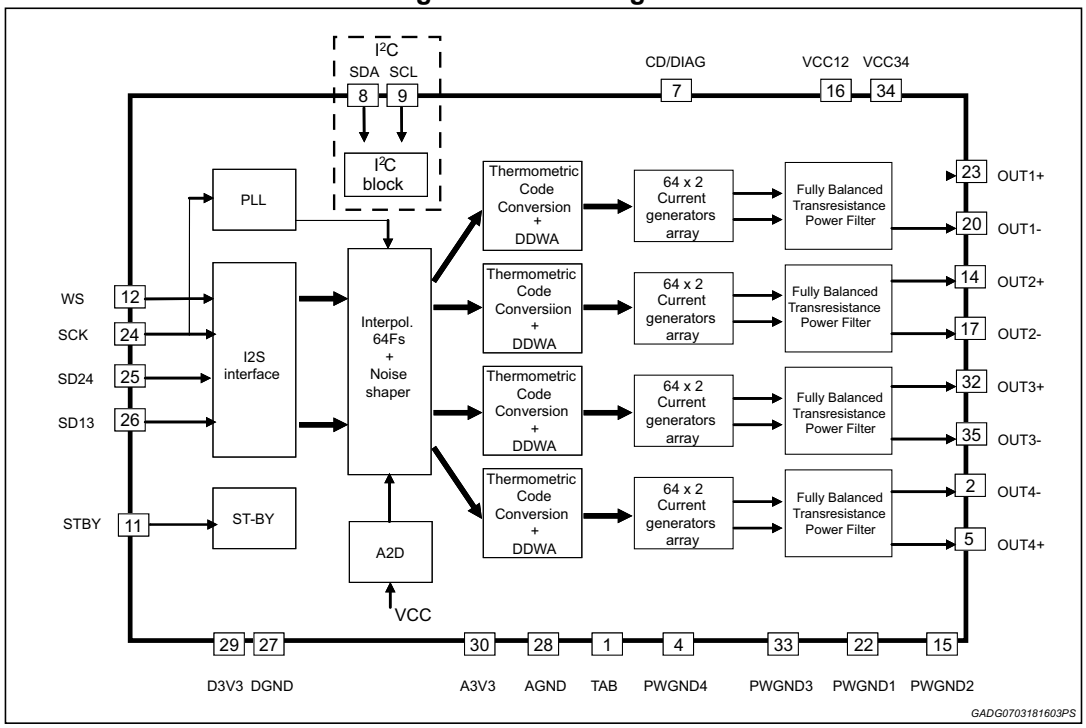
1.1 Block diagram

Figure 1. Block diagram



1.2 Pins description

Figure 2. Pins connection diagrams (top view)

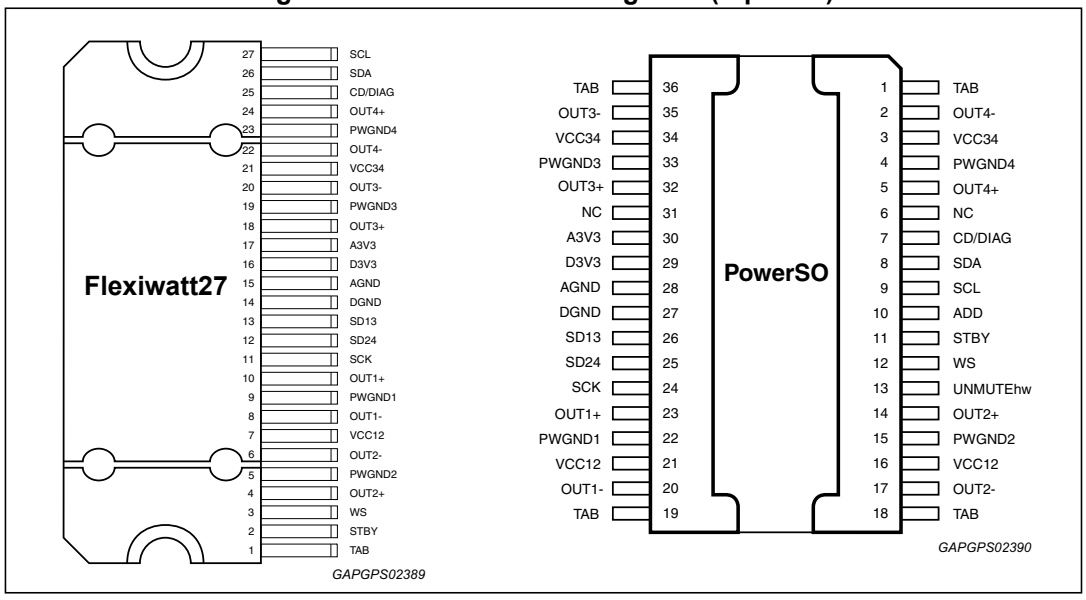


Table 2. Flexiwatt 27 pins description

N°	Pin	Function	
1	TAB	Device slug connection	Ground
2	STBY	STBY pin	Input
3	WS	Word select (I^2S bus)	Logic Input
4	OUT2+	Channel 2 (Left Rear) positive output	Power Output
5	PWGND2	Power ground channels 2	Power Ground
6	OUT2-	Channels 2 (Left Rear) negative output	Power Output
7	VCC12	Channel 1 and 2 positive supply	Battery
8	OUT1-	Channel 1 (Left Front) negative output	Power Output
9	PWGND1	Power ground channel 1	Power Ground
10	OUT1+	Channel 1 (Left Front) positive output	Power Output
11	SCK	Serial clock (I^2S bus)	Logic Input
12	SD24	Serial data channels 2 and 4 (I^2S bus)	Logic Input
13	SD13	Serial data channels 1 and 3 (I^2S bus)	Logic Input
14	DGND	Digital ground	Signal Ground
15	AGND	Analog ground	Signal Ground
16	D3V3	Digital 3.3V supply filter	Digital Regulator
17	A3V3	Analog 3.3V supply filter	Analog Regulator
18	OUT3+	Channels 3 (right front) positive output	Power Output
19	PWGND3	Power ground channel 3	Power Ground
20	OUT3-	Channels 3 (right front) negative output	Power Output
21	VCC34	Channels 3 and 4 positive supply	Battery
22	OUT4-	Channels 4 (right rear) negative output	Power Output
23	PWGND4	Power ground channel 4	Power Ground
24	OUT4+	Channels 4 (right rear) positive output	Power Output
25	CD/DIAG	Clip detector and diagnostic output	Open Drain Output
26	SDA	I^2C data	Signal Input
27	SCL	I^2C clock	Signal Input

Table 3. PowerSO-36 pins description

N°	Pin	Function	
1	TAB	Device slug connection	Ground
2	OUT4-	Channels 4 (right rear) negative output	Power Output
3	VCC34	Channels 3 and 4 positive supply	Battery
4	PWGND4	Power ground channel 4	Power Ground
5	OUT4+	Channels 4 (right rear) positive output	Power Output
6	NC	Not connected	-
7	CD/DIAG	Clip detector and diagnostic output	Open Drain Output
8	SDA	I^2C data	Signal Input
9	SCL	I^2C clock	Signal Input
10	ADD	I^2C Address	Logic Input
11	STBY	STBY pin	Input
12	WS	Word select (I^2S bus)	Logic Input
13	UNMUTEhw	Unmute Hardware	Logic Input
14	OUT2+	Channel 2 (Left Rear) positive output	Power Output
15	PWGND2	Power ground channels 2	Power Ground
16	VCC12	Channel 1 and 2 positive supply	Battery
17	OUT2-	Channels 2 (Left Rear) negative output	Power Output
18	TAB	TAB connection	Ground
19	TAB	TAB connection	Ground
20	OUT1-	Channel 1 (Left Front) negative output	Power Output
21	VCC12	Channel 1 and 2 positive supply	Battery
22	PWGND1	Power ground channel 1	Power Ground
23	OUT1+	Channel 1 (Left Front) positive output	Power Output
24	SCK	Serial clock (I^2S bus)	Logic Input
25	SD24	Serial data channels 2 and 4 (I^2S bus)	Logic Input
26	SD13	Serial data channels 1 and 3 (I^2S bus)	Logic Input
27	DGND	Digital ground	Signal Ground
28	AGND	Analog ground	Signal Ground
29	D3V3	Digital 3.3V supply filter	Digital Regulator
30	A3V3	Analog 3.3V supply filter	Analog Regulator
31	NC	Not connected	-
32	OUT3+	Channels 3 (right front) positive output	Power Output
33	PWGND3	Power ground channel 3	Power Ground
34	VCC34	Channels 3 and 4 positive supply	Battery
35	OUT3-	Channels 3 (right front) negative output	Power Output
36	TAB	TAB connection	Ground

2 Application diagrams

Figure 3. I²C bus mode application diagram (Flexiwatt)

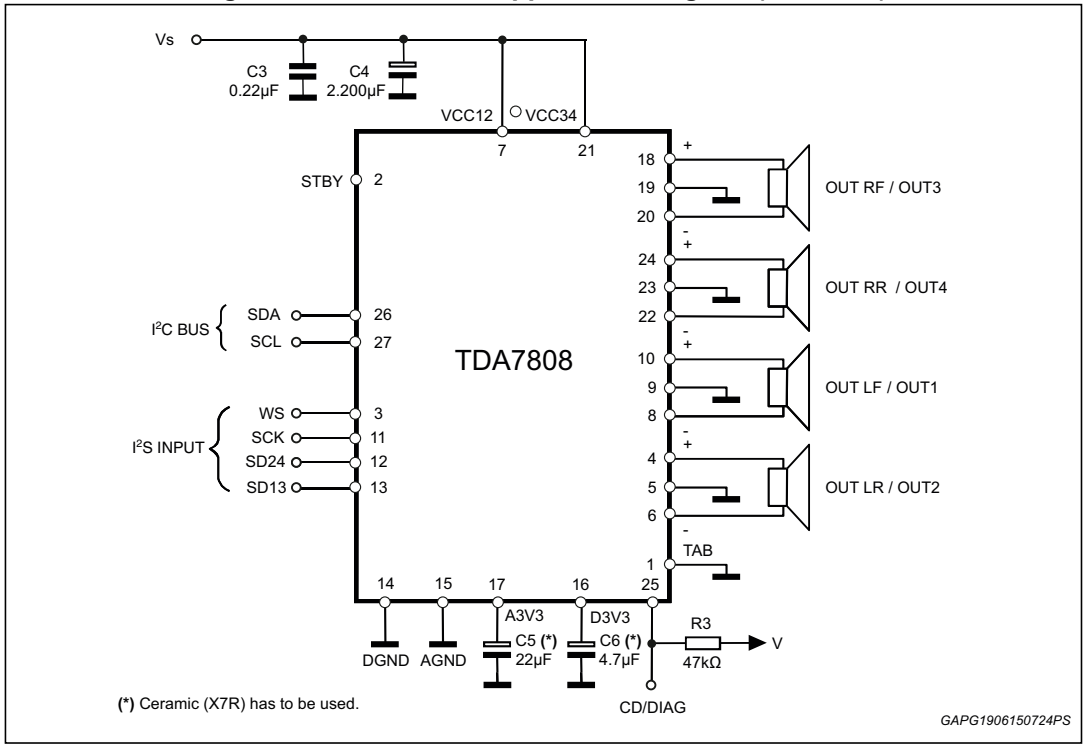
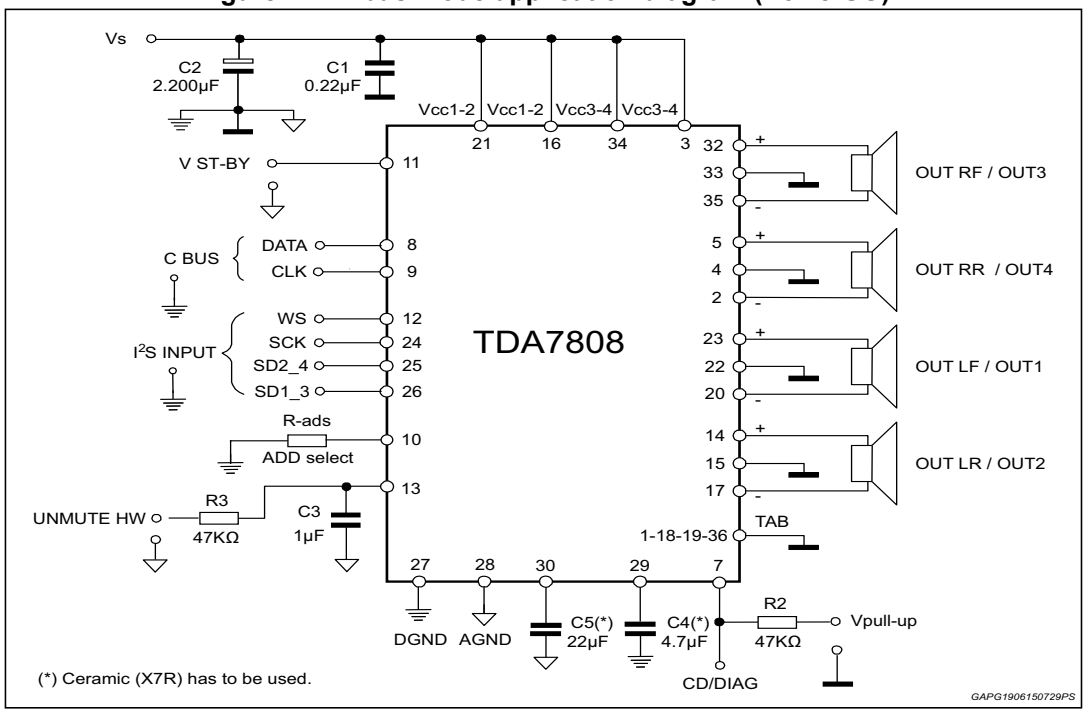


Figure 4. I²C bus mode application diagram (PowerSO)



3 Electrical specification

3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	DC supply voltage	-0.3 to 28	V
V_{peak}	Transient supply voltage for t = 100 ms	-0.3 to 50	V
V_{i2c}	I^2C bus pins voltage	-0.3 to 4.6	V
V_{i2s}	I^2S bus pins voltage	-0.3 to 4.6	V
V_{unmute}	Unmute hardware voltage (PSO36 only)	-0.3 to 4.6	V
V_{cd}	CD/Diag pin voltage	-0.3 to 20	V
V_{stby}	STBY pin voltage	-0.3 to 4.6	V
I_O	Output peak current (repetitive f > 10 Hz)	internally limited(1)	A
P_{tot}	Power dissipation T_{case} = 70 °C	85	W
T_{stg}, T_j	Storage and junction temperature	–55 to 150	°C
T_{amb}	Operative temperature range(2)	-40 to 105	°C
C_{max}	Maximum capacitor vs. ground connected to the output	4.7	nF
ESD_{HBM}	ESD protection HBM (3)	2000	V
ESD_{CDM}	ESD protection CDM (3)	500	V

1. Internally limited by overcurrent protection.
2. A suitable heatsink/dissipation system should be used to keep T_j inside the specified limits.
3. Conforming to Q100 ESD standard.

3.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}case}$	Thermal resistance junction-to-case (max.)	1	°C/W

3.3 Electrical characteristics

Referred to the test setup V_S = 14.4 V; R_L = 4 Ω; f = 1 kHz; tested at T_{amb} = 25 °C; functionality guaranteed for T_j = -40 °C to 150 °C; SB-I mode; unless otherwise specified.

Table 6. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
General						
V_S	Supply voltage range	R_L = 4 Ω	6	-	18.5	V
I_{SB}	Standby current	-	-	1	4	µA
I_q	Total quiescent current in amplifier mode	Mute condition	-	170	210	mA
I_{qECO}	Total quiescent current in ECO mode	ECO mode	-	35	40	mA
A_M	Mute attenuation	-	80	-	-	dB
V_{OS}	Offset voltage	Mute and play	-25	-	+25	mV
V_{lowM}	V_{CC} low supply mute threshold (Min I^2C setting - default)	Attenuation <0.5 dB, digital mute disabled	-	-	5.6	V
		Attenuation ≥60 dB, digital mute disabled	5	-	-	V
$V_{POWONRESET}$	Supply voltage of power-on reset	-	-	3.5	-	V
V_{highM}	High supply mute threshold	Attenuation = -6 dB	19	-	21	V
Audio performances						
P_O	Output power	R_L = 4 Ω; max power (1)	40	43	-	W
		THD = 10 %	25	27	-	W
		THD = 1 %	20	22	-	W
THD_{SB}	Total harmonic distortion (Standard bridge)	P_O = 4 W, f=1 kHz, G_{V1}	-	0.015	0.04	%
		P_O = 4 W, f=10 kHz, G_{V1}	-	0.15	0.5	%
		R_L =100 Ω input=-10 dBFS, f = 1 kHz, $G_{V1,2,3,4}$	-	0.01	0.02	%
THD	Total harmonic distortion (SBI mode)	P_O = 2 W, f = 1 kHz, G_{V1}	-	0.015	0.04	%
		P_O = 6 W, f =1 kHz, G_{V1}	-	0.02	0.06	%
C_T(2)	Cross talk	f = 1 kHz	-	100	-	dB
		f = 10 kHz	-	80	-	dB
G_{V1}	Voltage gain 1	@ Amplitude = -18 dBFs	2.3	2.5	-	Vp
G_{V2}	Voltage gain 2		1.25	1.35	-	Vp
G_{V3}	Voltage gain 3		0.9	1	-	Vp
G_{V4}	Voltage gain 4		0.4	0.55	-	Vp

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$DR^{(2)}$	Dynamic range	A-wtd values, G_{V1} gain	-	115	-	dB
E_{out1}	Output noise voltage $G_V = G_{V1}$ $G_V = G_{V4}$	A-wtd values	 - -	 27 18	 40 -	µV
E_{out2}	Output noise voltage $G_V = G_{V1}$ $G_V = G_{V4}$	ITU-R 468	 - -	 70 45	 96 -	µV
$SNR^{(2)}$	Signal to noise ratio	A-wtd values, G_{V1} gain	-	115	-	dB
ΔG_v	Channel Gain Mismatch	-	-0.5	-	0.5	dB
SSR	Supply slew rate	-	-	1	-	V/µs
PSRR	Power supply rejection ratio	f = 1 kHz; V_r = 1 Vpk;	60	70	-	dB
$\lvert\Delta V_{OITU}\rvert$	ITU Pop filter output voltage (standard bridge mode)	Eco mode to mute transition and vice versa	-	-	4	mV
		Mute to Play and Play to Mute transition$^{(3)}$	-	0	-	mV
Clipping detector						
CD_{LK}	Clip det high leakage current	CD off, V = 3.3 V	-	0	1	µA
CD_{SAT}	Clip det sat. voltage	CD on; I_{CD} = 1 mA	-	50	-	mV
$CD1_{THD}$	Clip det THD threshold 1	-	-	2	3	%
$CD2_{THD}$	Clip det THD threshold 2	-	4	6	8	%
$CD3_{THD}$	Clip det THD threshold 3	-	9	12	14	%
I^2C bus interface						
f_{SCL}	Clock frequency	-	-	-	400	kHz
V_{IL}	Input low voltage	-	-	-	0.8	V
V_{IH}	Input high voltage	-	1.3	-	-	V
V_{olmax}	Maximum I2C data pin low voltage when current Isink is sinked	I_{sink} = 2 mA	-	-	0.27	V
		I_{sink} = 8 mA	-	-	0.7	V
I_{limax}	Maximum input leakage current	V = 3.6 V	-	-	1	µA
STBY pin						
V_{ILSTBY}	Input low voltage	-	-	-	1.2	V
V_{IHSTBY}	Input high voltage	-	2.4	-	-	V
I_{ILSTBY}	Logic ‘0’ output current	V_{IN} = 0.45 V	-	-	1	µA
I_{IHSTBY}	Logic ‘1’ input current	V_{IN} = 2.3 V, IB0 D4 = 0	-	-	1	µA

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I^2S pins						
V_{IL-I2S}	Input low voltage	-	-	-	0.8	V
V_{IH-I2S}	Input high voltage	-	1.3	-	-	V
I_{IH}	Input high current	@ V_I = 3.3 V	-	-	1	µA
I_{IL}	Input low current	@ V_I = 0 V	-	-	1	µA
Unmute hardware (pin 13)						
V_{HW_UNMUTE}	Hardware unmute threshold (PSO36 only)	Attenuation ≥60 dB	-	-	1.2	V
		Attenuation <0.5 dB	2.6	-	-	V
I_{UNMUTE}	Input high current	@ V_I = 3.3 V	-	-	1	µA
	Input low current	@ V_I = 0 V	-	-	1	µA

1. Square-wave input / saturated output.
2. Evaluated at bench during product validation.
3. Guaranteed by design (intrinsically immune from any pop at mute to play and play to mute transitions)

3.4 Electrical characteristics typical curves

Figure 5. Quiescent current vs. supply voltage

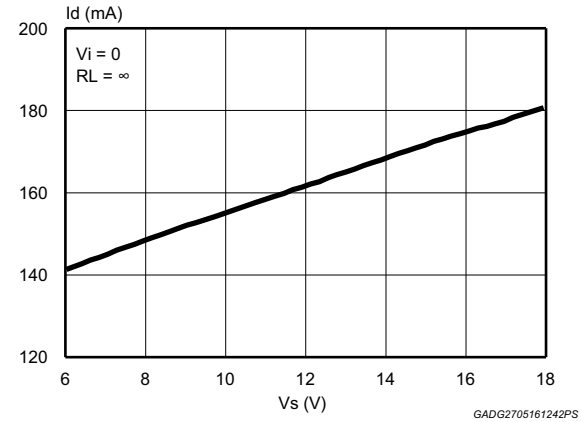


Figure 6. Output power vs. supply voltage (4 Ω)

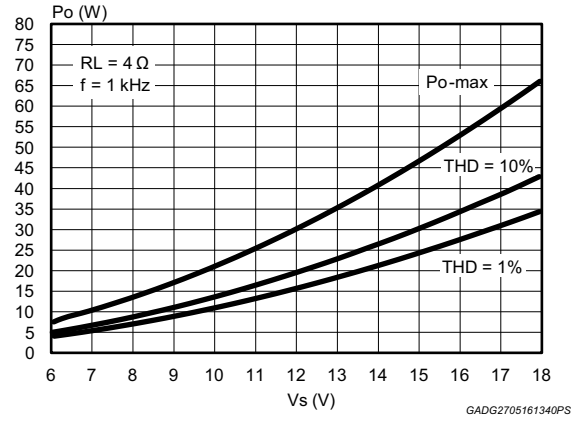


Figure 7. Distortion vs. output power (4 Ω, STD mode)

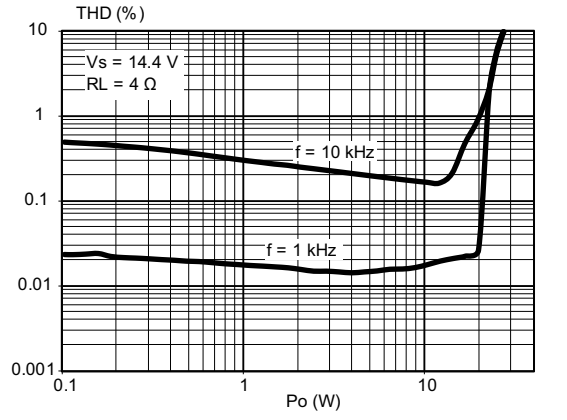


Figure 8. Distortion vs. output power (4 Ω, SBI mode)

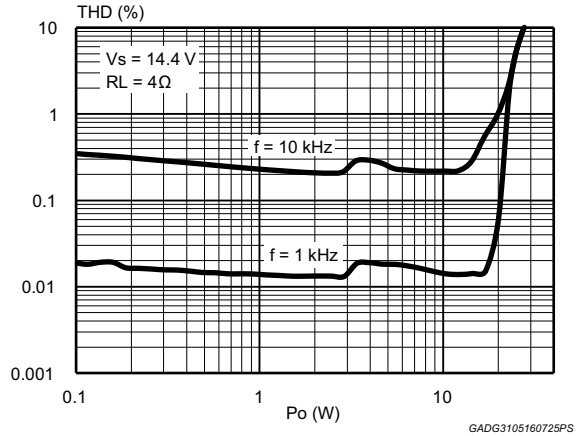


Figure 9. Distortion vs. frequency (4 Ω)

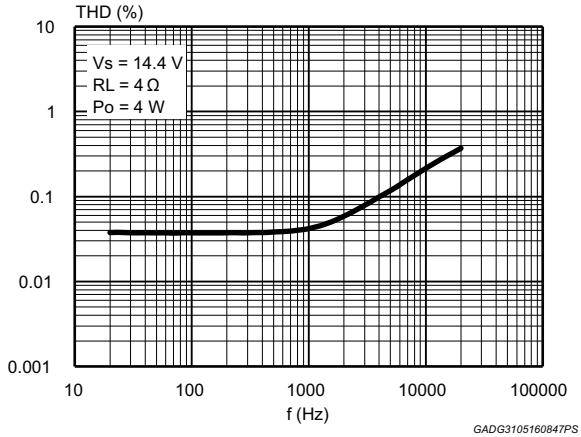


Figure 10. Distortion vs. output power (4 Ω, Vs = 6 V)

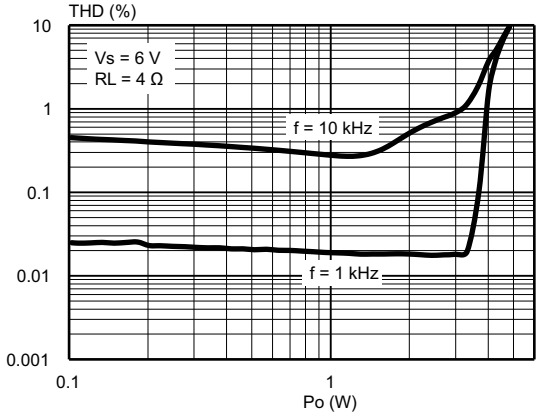


Figure 11. Vo vs. Vin (Gv1-2-3-4 settings)

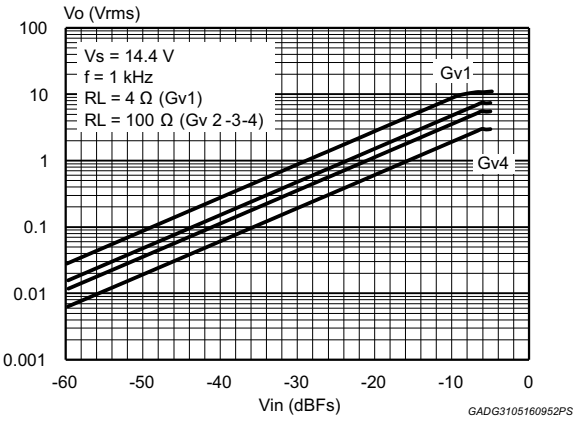


Figure 12. Vo vs. Vin (Gv1-2-3-4 settings + 6 dB dig. gain)

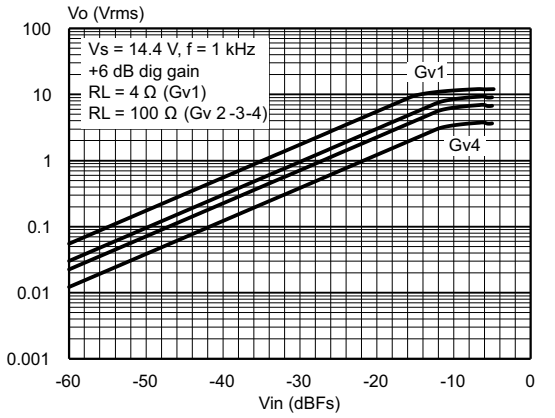


Figure 13. Distortion vs. output voltage (LD-Gv2)

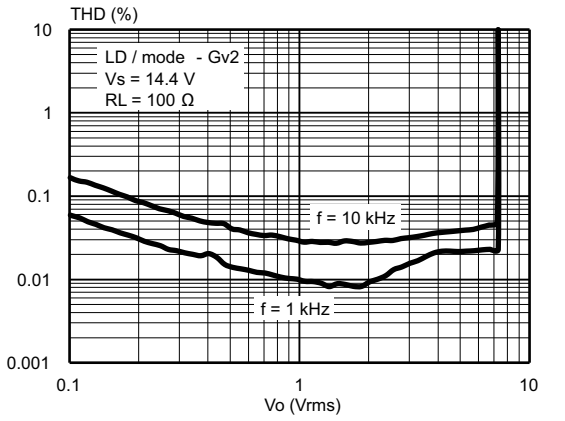


Figure 14. Distortion vs. output voltage (LD-Gv3)

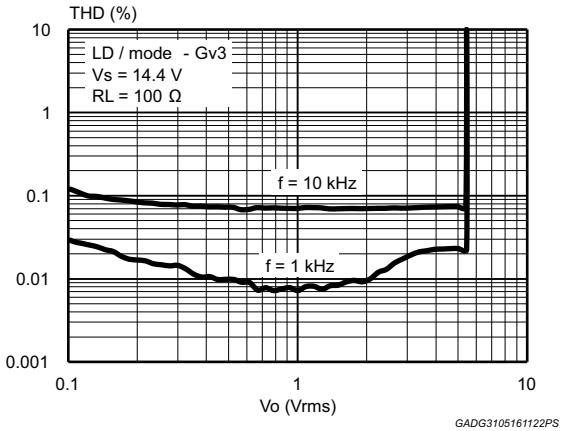


Figure 15. Distortion vs. output voltage (LD-Gv4)

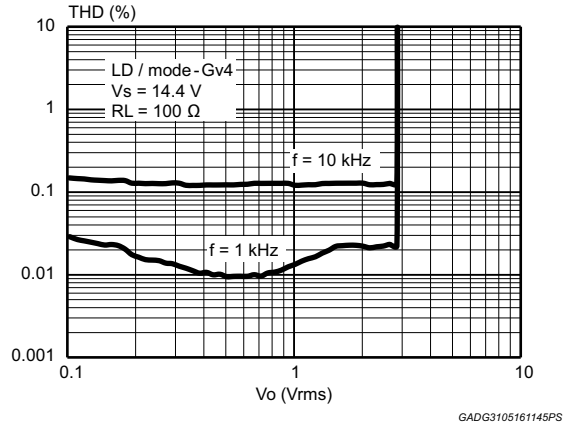


Figure 16. Output attenuation vs. supply voltage

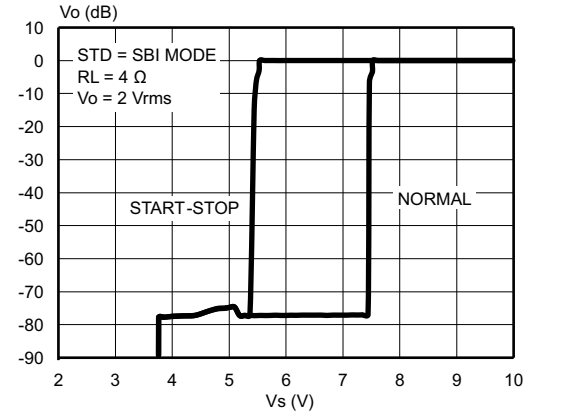


Figure 17. Crosstalk vs. frequency (STD mode)

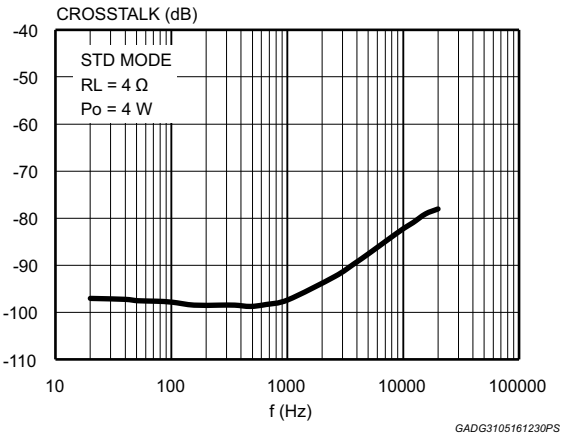


Figure 18. Crosstalk vs. frequency (SBI mode)

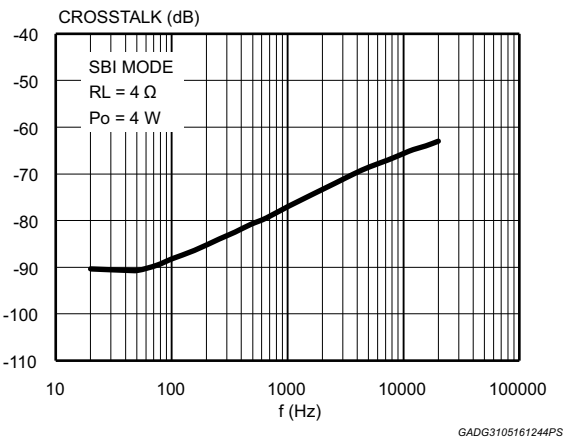


Figure 19. Supply voltage rejection vs. frequency

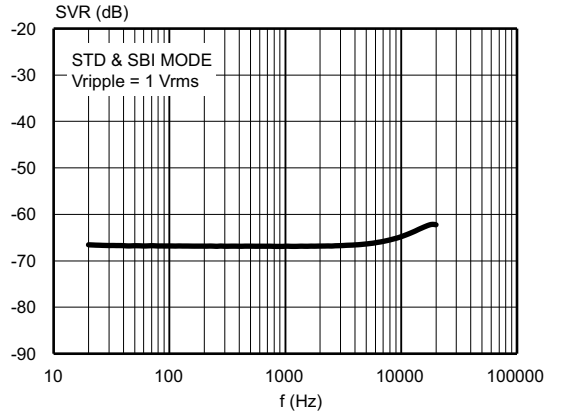


Figure 20. Total power dissipation & efficiency vs. Po (4 Ω, STD, Sine)

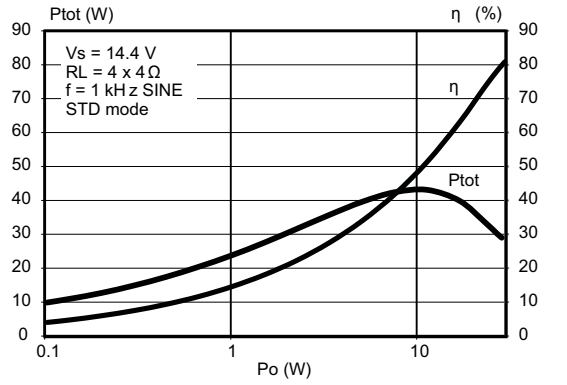


Figure 21. Total power dissipation & efficiency vs. Po (4 Ω, SBI, Sine)

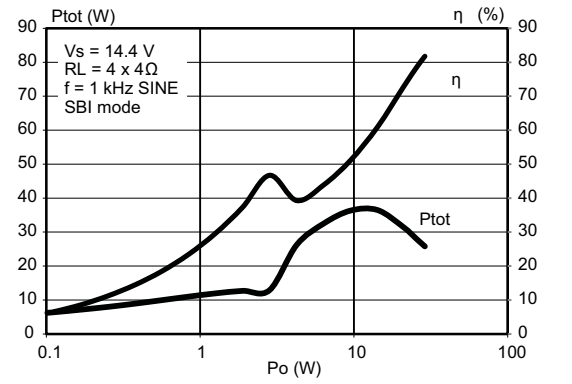


Figure 22. Power dissipation vs. average Po (audio program simulation, 4 Ω)

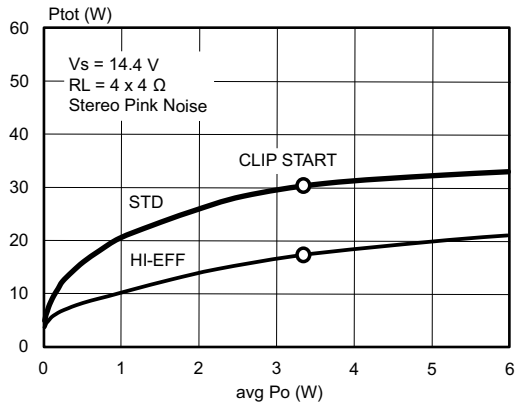
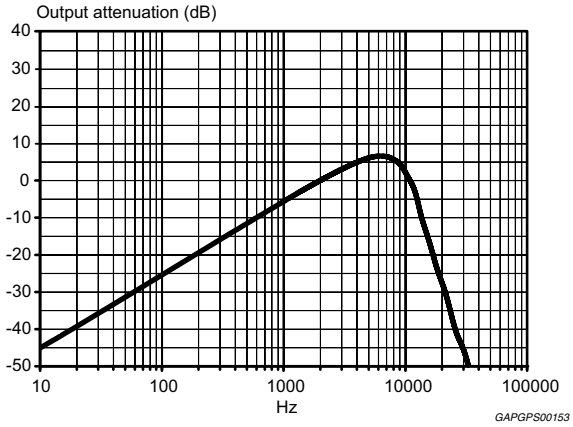


Figure 23. ITU R-ARM frequency response, weighting filter for transient pop



4 Operation states

TDA7808 functionality is regulated by means of a finite state machine.

Main states are:

- Standby
- ECO-mode
- Amplifier mode

4.1 Standby state

When STBY pin is under VILSTBY voltage the amplifier is in stand-by state and the current consumption is very low.

4.2 ECO-mode state

When STBY pin is over VIHSTBY the amplifier is in a state of low current absorption, the ECO-mode. The short circuit protections are active and the amplifier is ready for receiving commands from micro-controller through I^2C interface.

Outputs and A3V3 supply are biased at 0 V.

4.3 Amplifier-mode state

When TDA7808 is in ECO-mode state, IB3-d0 is set to "1", (Amplifier-ON), and I^2S clock is present the amplifier moves to Amplifier-mode state.

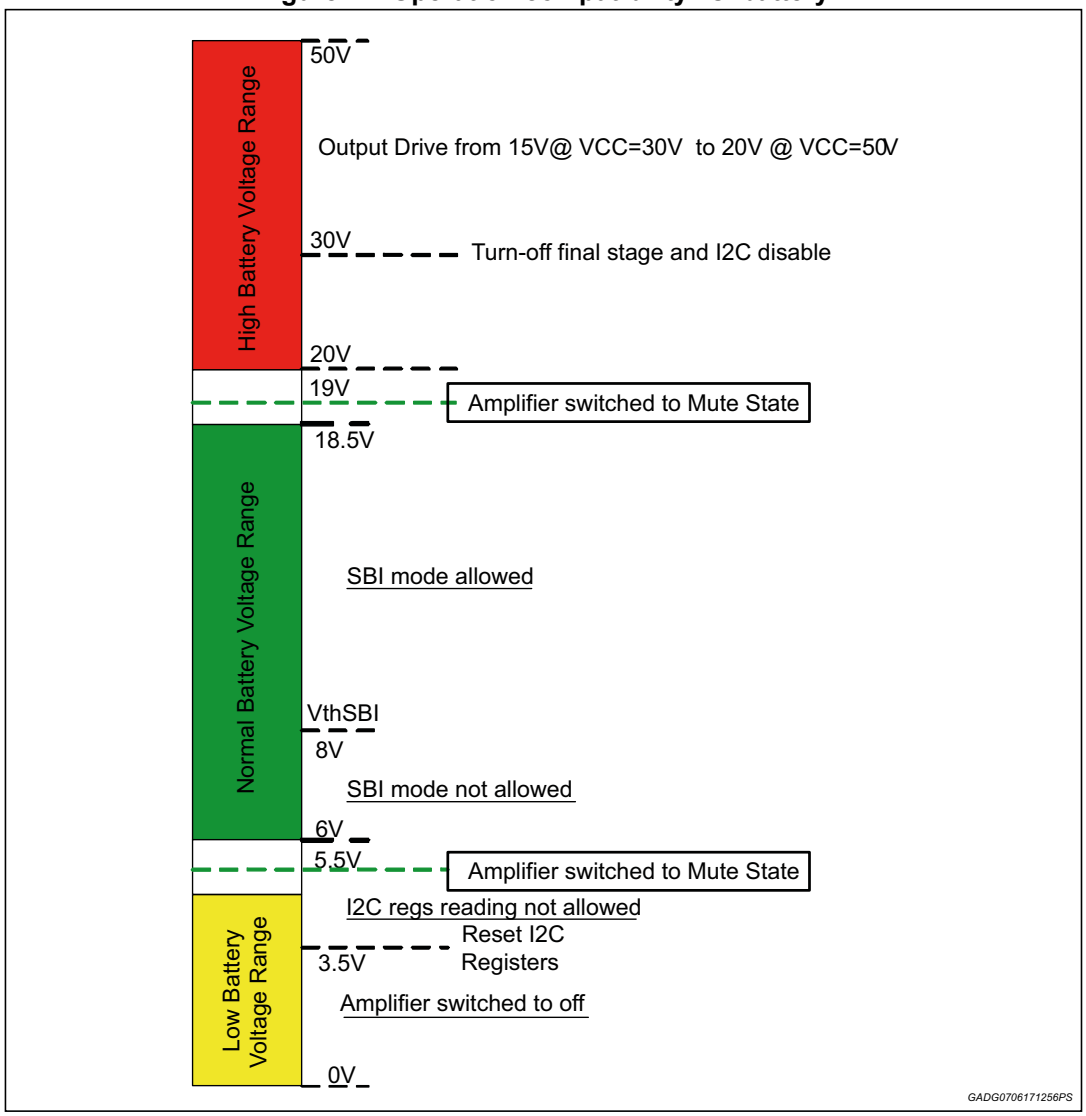
The outputs are biased from 0 V to Vcc/2 and the current consumption reaches "Iq" level until the amplifier is set in MUTE or in PLAY with low level signal. User can move the amplifier from MUTE to PLAY and viceversa acting on IB2-d4, d3 bits.

A hardware unmute pin is available in PSO36 package only.

5 Operation compatibility vs. battery

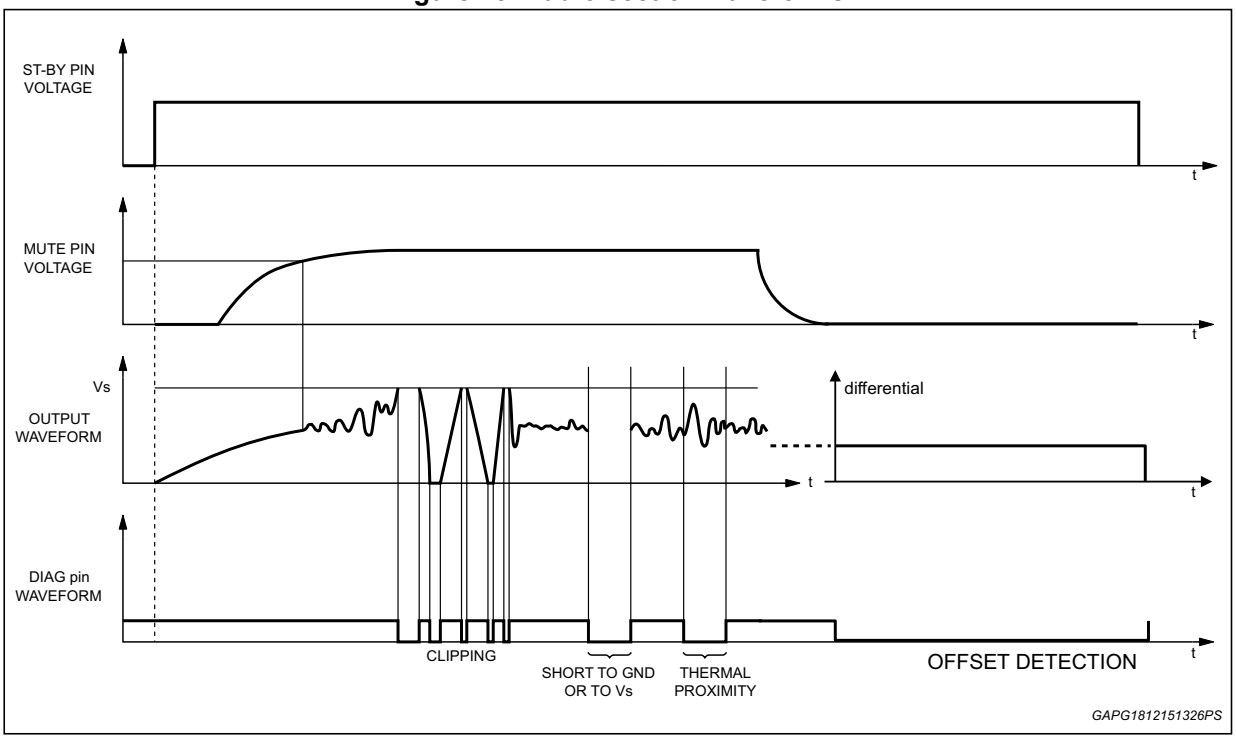
Here below the operation compatibility vs. the battery value is shown. For each battery voltage range, only a limited number of functions are available as it is shown below:

Figure 24. Operation compatibility vs. battery



6 Clipping detection and diagnostics (CD-DIAG pin)

Figure 25. Audio section waveforms



7 I²S and TDM bus interface

The audio input port is a three/four-wire synchronous serial interface that can operate only as Slave. Pins SD13 and SD24 are the serial data inputs. The audio data format accepted from TDA7808 is the I²S standard.

Input data can also be sent in time division multiplexed (TDM). Pins SCK (bit clock) and WS (frame select) complete the I²S interface.

Important note on I2S-clock: when I2S-clk is lost during amplifier operations a protection circuit acts and puts the amplifier in a safe condition: amplifier short circuit protections are guaranteed, dump protection is guaranteed, signal is muted and outputs bias is under control.

For avoiding other side effects user should put the amplifier in standby moving STBY pin to 0 V.

7.1 I²S and TDM input data frame format

The audio data word length for each channel may be up to 24 bit. Either for I2S or TDM mode, the frame for each channel has 32 bit length.

The following table summarizes the frequencies configurations.

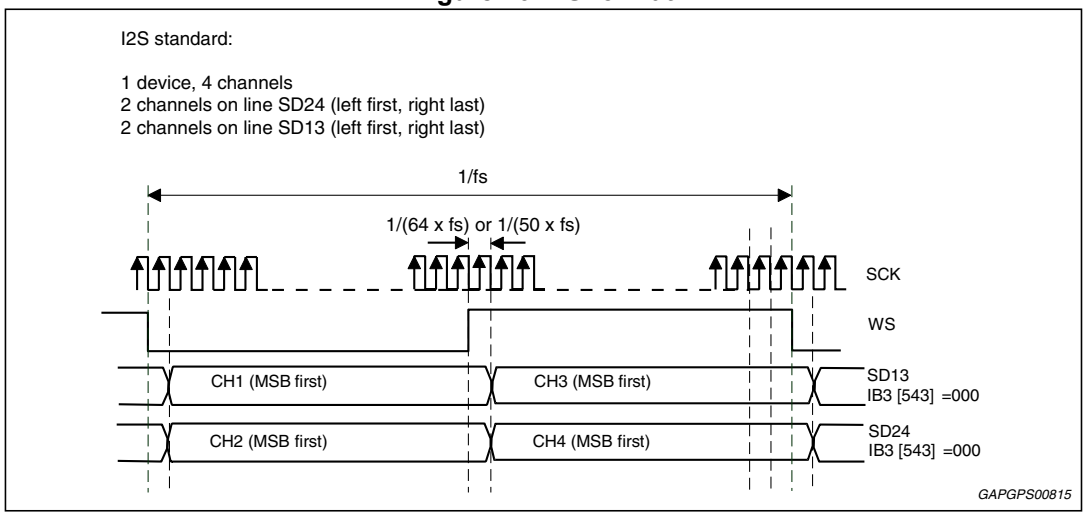
Table 7. System input frequencies

Frequency sampling (Fs)	System clock frequency (f_{SCK}), (MHz)		
	I²S standard	TDM 4ch	TDM 8ch/8+8ch
44.1 (kHz)	2.8224	5.6448	11.2896
48 (kHz)	3.072	6.144	12.288
96 (kHz	6.144	12.288	24.576
192 (kHz	12.288	24.576	N.A.

7.2 I²S input data format

The TDA7808 accepts I²S standard interface format as in *Figure 26* and the I²C bit configuration is IB3 [D5,D4,D3] = "000".

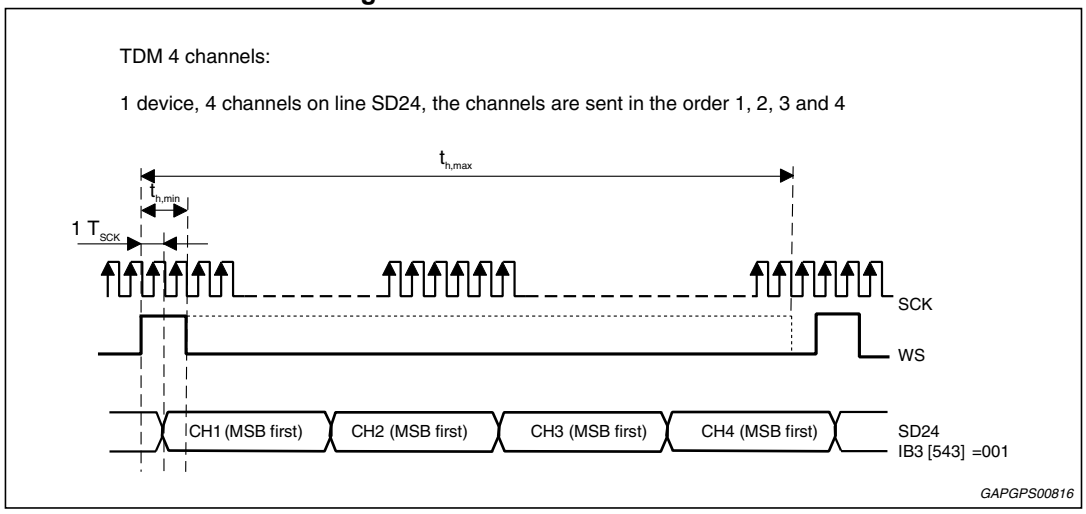
Figure 26. I²S format



7.3 TDM input data format

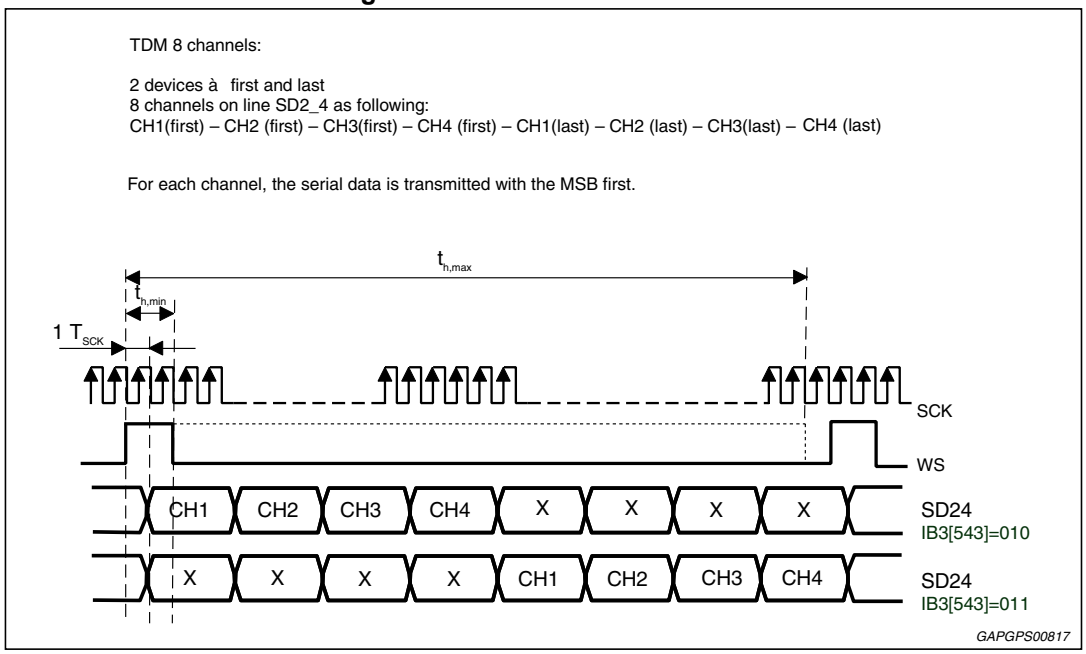
TDM 4-channel is allowed for TDA7808 and it is as in *Figure 27*. All the channels are sent on the audio data line SD24. The channel's order is 1, 2, 3 and 4. The I²C bit configuration is IB3 [D5, D4, D3] = "001".

Figure 27. TDM 4-channel format



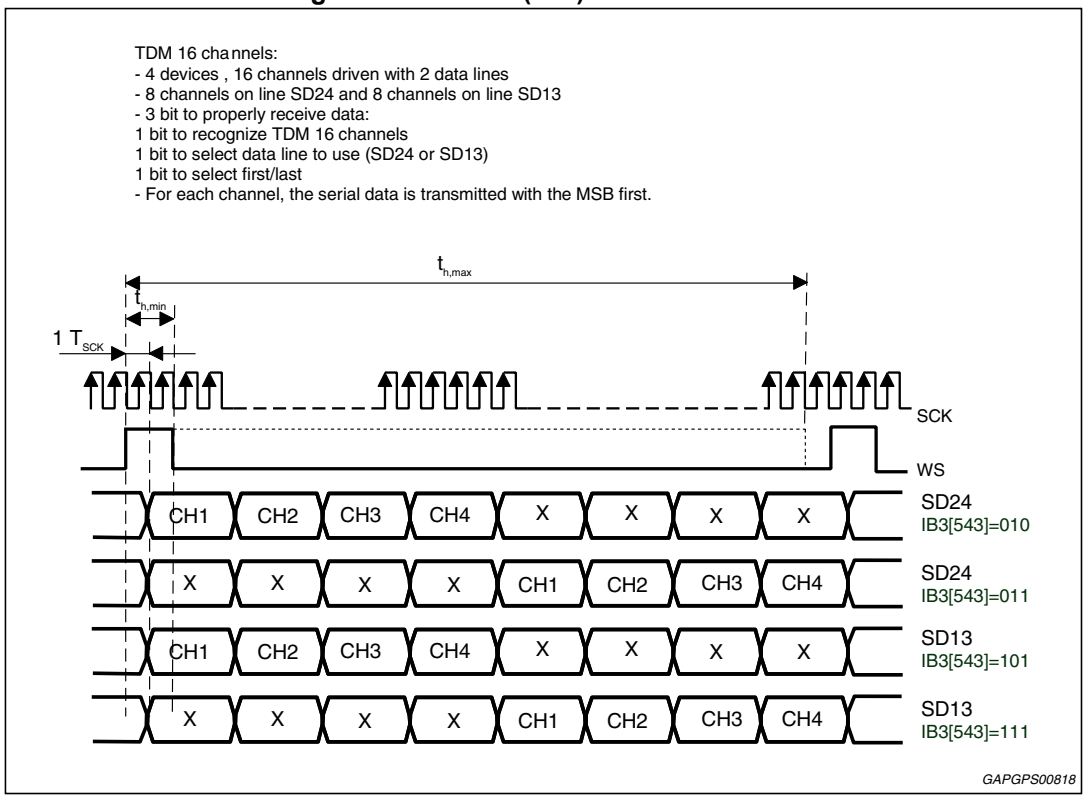
TDM 8-channel is also allowed and two devices (device 1 and device 2) can be driven by using just one serial data line SD24. There are two selectable options
When IB3 [D5,D4,D3] = "010" device 1 is first sent; when IB3 [D5,D4,D3] = "011" device 2 is first sent. In *Figure 28* TDM 8-channel format is showed.

Figure 28. TDM 8-channel format



The TDM 8 channel is expansible to TDM 16 channel (*Figure 29*) where both SD24 and SD13 data lines are used. All the configurations are selectable via I²C.

Figure 29. TDM 16 (8+8) - channel format



7.4 Timings requirements

Figure 30. Audio interface timing

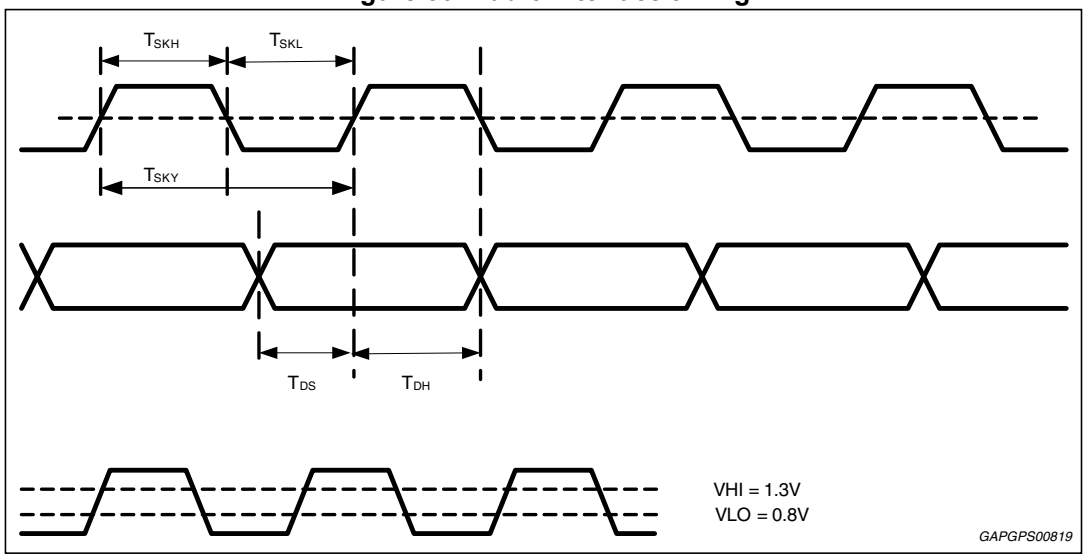


Table 8. I²S interface timing

Symbol	Parameter	note	min	max	unit
Fsck0	SCK (bit clock) frequency	-	-	49.152	MHz
-	SCK (bit clock) frequency tolerance	-	0.9Fsck0	1.1Fsck0	MHz
Tsck	SCK period	-	20	-	ns
-	SCK duty cycle	-	40	60	%
Tsckh	SCK high time	-	6	-	ns
Tsckl	SCK low time	-	6	-	ns
-	SCK transition time	-	-	4	ns
-	WS (word select) frequency	-	-	192	KHz
Twsh	WS high time	I2S standard	25 or 32 Tsck (duty cycle=50%)		ns
Twsh	WS high time	TDM 4-channel	1 Tsck	127 Tsck	ns
Twsh	WS high time	TDM 8-16-channel	1 Tsck	255 Tsck	ns
Tws	WS setup time	-	5	-	ns
Twh	WS hold time	-	6	-	ns
Tds	SD13 SD24 (data inputs) setup time before SCK rising edge	-	5	-	ns
Tdh	SD13 SD24 (data inputs) hold time after SCK rising edge	-	6	-	ns

For TDM mode:

- WS changes at SCK falling edge, on clock period before the MSB is transmitted
- WS does not need to be symmetrical. It need to stay high for at least 2 SCK period clock. The maximum duration is:
  - T_{h_max} = 127 T_{SCK} in TDM 4-channel
  - T_{h_max} = 255 T_{SCK} in TDM 8-channel and TDM 16 (8+8)-channel
- The other timings are like in *Table 8*.

7.5 Group delay

The group delay is due to the FIR filter of first interpolator and it is T_{delay} = 32/Fs.

8 Functional description

8.1 Voltage regulators timing

Pins D3V3 and A3V3 are respectively the digital and analog internal regulators. The D3V3 rises right after the STBY pin is at the logical value "1" and its rising time depends on the filter capacitor; the value suggested for this filter is of min 4.7 µF.

The A3V3 rises after any command that moves the amplifier from low quiescent current mode; the rising time depends on the combined effect of the external capacitor on the pin and of an internal 2 ms ramp: if the capacitor value is 22 µF or lower, the internal ramp effect is dominant and the rising time will be about 2 ms. On the other hand, when the capacitor has a higher value, the rise time will be higher as well. The suggested value for this capacitor is 22 µF (47 µF) at least.

8.2 SB-I Improved high efficiency principle

The TDA7808 embeds an improved high efficiency feature that minimizes the power dissipated through the heat sink basing on the musical signal characteristic. All bridges are connected to a common bar by means of four power switches. When an input signal goes under a threshold that depends on the Vs level, the switch will short the corresponding output to the common bar in such a way that it can exchange current with the other channel. The dissipation reduction can be up to 50% compared to standard AB class.

The TDA7808 sets the high efficiency mode by default, but it can be changed through the bits IB0 D3, D2, D1 and D0.

8.3 Input offset detector

Input offset detector aim is to avoid any possible offset that could come from the audio signal source through I2S/TDM input stream.

For this purpose the TDA7808 input offset detector performs an evaluation of the input signal and calculates if an offset with values higher than -19.5 dBFs is present.

Moreover, if high pass filter function is selected by means of IB3-d2, the TDA7808 will eliminate the input offset giving a complete robustness to any disturbance or malfunction coming from the previous audio chain blocks.

The input offset detector and high-pass filtering can be used during PLAY mode.

9 I²C bus interface

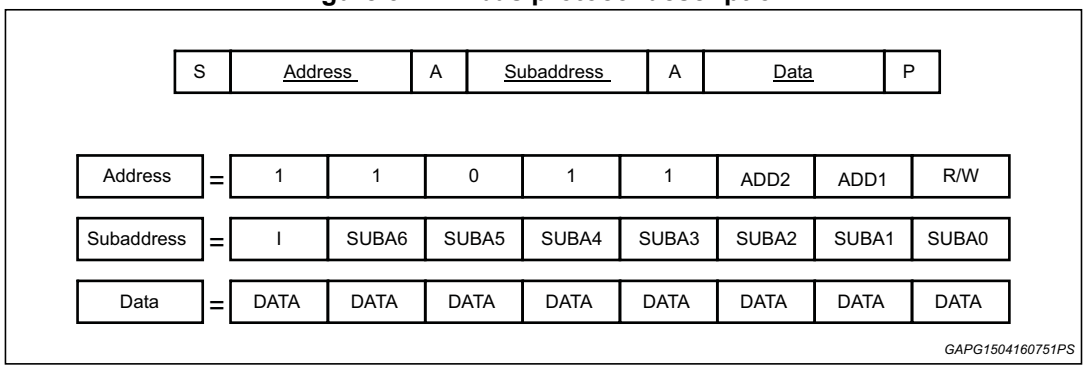
Data transmission from microprocessor to the TDA7808 and viceversa takes place through the 2 wires I²C bus interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected).

When I²C bus is active, the user can select the IC's operating mode.

The protocol used for the bus is depicted in *Figure 31* and comprises:

- a start condition (S)
- a chip Address byte (the LSB bit determines read/write transmission)
- a Subaddress byte
- a sequence of Data (N-bytes + acknowledge)
- a stop condition (P)

Figure 31. I²C bus protocol description



Description:

- S = Start
- R/W = '0' => Receive-Mode (Chip could be programmed by uP)
- I = Auto increment; when 1, the address is automatically incremented for each byte transferred
- A = Acknowledge
- P = Stop
- MAX CLOCK SPEED 400kbit/sec

There are four I²C addresses for PowerSO36 package: 1101100, 1101101, 1101110, 1101111.

For Flexiwatt package only the 1101111 is available.

9.1 Writing procedure

There are two possible procedures:

1. without increment: the I bit is set to 0 and the register to be written is addressed by the subaddress SUB A. Only this register is written by the DATA byte following the subaddress byte.
2. with increment: the I bit is set to 1 and the first register to be written is the one addressed by subaddress SUB A. Then all the registers from SUB A up to stop bit or the reaching of last register are written.

9.2 Data validity

The data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

9.3 Start and stop conditions

A start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH.

The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

9.4 Byte format

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

9.5 Acknowledge

The transmitter* puts a resistive HIGH level on the SDA line during the acknowledge clock pulse. The receiver** has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse.

* **Transmitter**

= master (µP) when it writes an address or instruction byte to the TDA7808
= slave (TDA7808) when the µP reads a data byte from TDA7808

** **Receiver**

= slave (TDA7808) when the µP writes an address or instruction byte to the TDA7808
= master (µP) when it reads a data byte from TDA7808

9.6 Address selection

To select the proper I²C address a resistor must be connected to ADD pin as follows:

Table 9. Address threshold

ADD2	ADD1	Rload
0	0	120K < R
0	1	56K < R < 64K

Table 9. Address threshold (continued)

ADD2	ADD1	Rload
1	0	30K < R < 38K
1	1	R < 15K

9.7 I²C bus timings

This paragraph describes more in detail the I²C bus protocol used and its timings. *Figure 32* and *Table 10* include the timings that need to be respected in order to correctly write into/ read from the I²C registers.

Figure 32. I²C bus interface timing

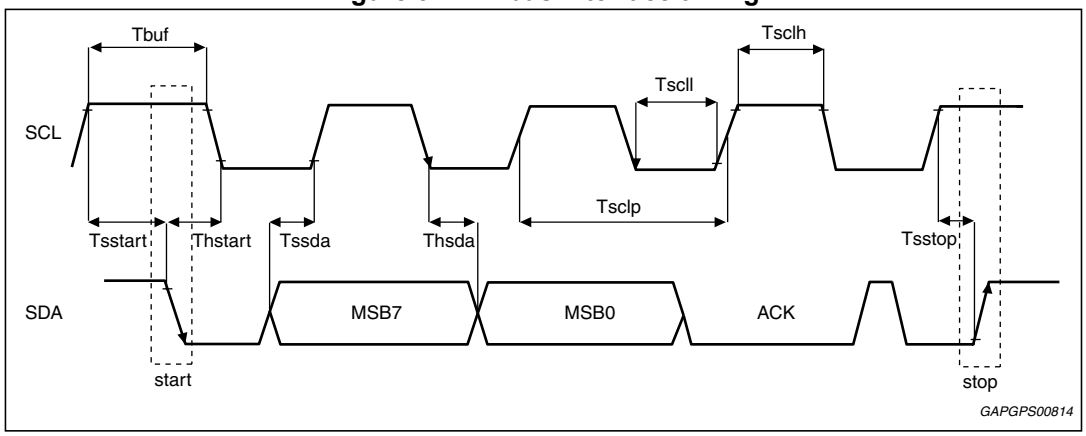


Table 10. I²C bus interface timing

Symbol	Parameter	Min	Max	Unit
Fscl	SCL (clock line) frequency	-	400	kHz
Tscl	SCL period	2500	-	ns
Tsclh	SCL high time	0.6	-	µs
Tscll	SCL low time	1.3	-	µs
Tsstart	Setup time for start condition	0.6	-	µs
Thstart	Hold time for start condition	0.6	-	µs
Tsstop	Setup time for stop condition	0.6	-	µs
Tbuf	Bus free time between a stop and a start condition	1.3	-	µs
Tssda	Setup time for data line	100	-	ns
Thsda	Hold time for data line	0(1)	-	ns
Tf	Fall time for SCL and SDA	-	300	ns

1. Device must internally provide a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the falling edge of SCL.

10 I²C registers

10.1 Instruction byte

10.1.1 IB0 - Subaddress "I0000000h" - default = "00000000"

Table 11. IB0 - Subaddress "I0000000h" - default = "00000000"

Bit	Instruction decoding bit
D7-D6	Clipping detection level for front channels **D7 D6** **0 0 2% for all channel 1 and 3** 0 1 5% for all channel 1 and 3 1 0 10% for all channel 1 and 3 1 1 no clipping for channel 1 and 3
D5-D4	Clipping detection level for rear channels **D5 D4** **0 0 2%for all channel 2 and 4** 0 1 5% for all channel 2 and 4 1 0 10% for all channel 2 and 4 1 1 no clipping for channel 2 and 4
D3	Channel 4 Amplifier Mode **0: High Efficiency Mode** 1: Standard Class AB Mode
D2	Channel 3 Amplifier Mode **0: High Efficiency Mode** 1: Standard Class AB Mode
D1	Channel 2 Amplifier Mode **0: High Efficiency Mode** 1: Standard Class AB Mode
D0	Channel 1 Amplifier Mode **0: High Efficiency Mode** 1: Standard Class AB Mode

10.1.2 IB1 - Subaddress "I0000001h" - default = "00000000"

Table 12. IB1 - Subaddress "I0000001h" - default = "00000000"

Bit	Instruction decoding bit
D7	Not used
D6	Not used
D5 D4	Digital gain selection **D5 D4 Digital gain** **0 0 default** 0 1 +6 dB 1 0 +12 dB 1 1 Not used
D3 D2	Gain Channel 1 & 3 **D3 D2 Gain** **0 0 GV1** 0 1 GV2 1 0 GV3 1 1 GV4
D1 D0	Gain Channel 2 & 4 **D1 D0 Gain** **0 0 GV1** 0 1 GV2 1 0 GV3 1 1 GV4

10.1.3 IB2 - Subaddress "I0000010h" - default = "00000000"

Table 13. B2 - Subaddress "I0000010h" - default = "00000000"

Bit	Instruction decoding bit
D7	Sample frequency range (Word select frequency) **D7 D6 Sample frequency** **0 0 44.1 kHz** 0 1 48 kHz(1) 1 0 96 kHz 1 1 192 kHz
D6	
D5	Digital Input Format **D5 D4 D3** **0 0 0 I2S standard** 0 0 1 TDM – 4ch 0 1 0 TDM – 8ch (SD2_4 input, device 1) 0 1 1 TDM – 8ch (SD2_4 input device 2) 1 0 0 TDM – 16ch (SD2_4 input – device 1) 1 0 1 TDM – 16ch (SD2_4 input – device 2) 1 1 0 TDM – 16ch (SD1_3 input – device 3) 1 1 1 TDM – 16ch (SD1_3 input – device 4)
D4	
D3	
D2	Mute 1&3 **0: Channels 1&3 Muted** 1: Channels 1&3 un-Muted
D1	Mute 2&4 **0: Channels 2&4 Muted** 1: Channels 2&4 un-Muted
D0	Disable digital mute **0: Digital mute ON** 1: Digital mute OFF

1. Byte IB3 settings can be changed only if the amplifier is in Low quiescent current state, otherwise the command is ignored.

10.1.4 IB3 - Subaddress "I0000011h" - default = "00000000"

Table 14. IB3 - Subaddress "I0000011h" - default = "00000000"

Bit	Instruction decoding bit
D7-D3	Not used
D2	Digital High pass filter enable/disable **0: enable** 1: disable
D1	Input offset detection **0: enable** 1: disable
D0	Amplifier on/off **0: off** 1: on

11 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

ECOPACK® is an ST trademark.

11.1 PowerSO-36 (slug up) package information

Figure 33. PowerSO-36 (slug up) package outline

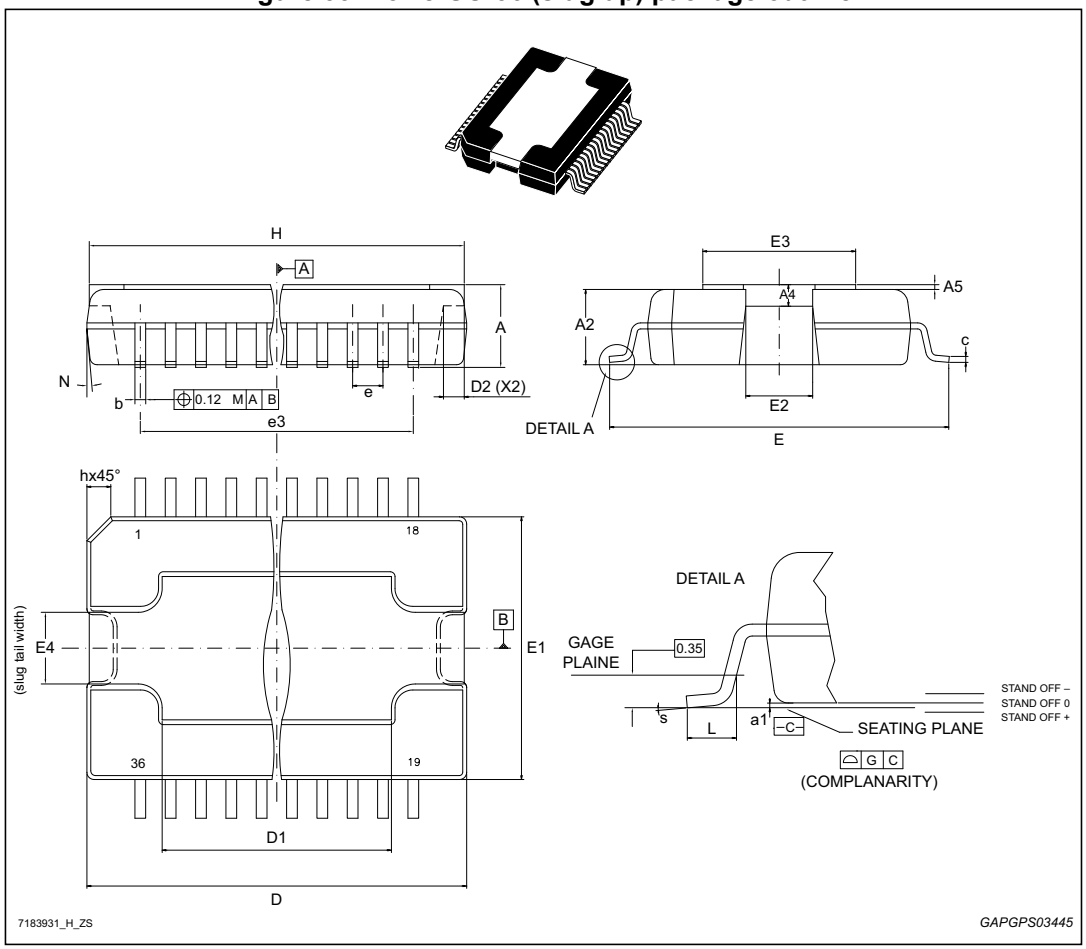


Table 15. PowerSO-36 (slug up) package mechanical data

Ref	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	3.27	-	3.41	0.1287	-	0.1343
A2	3.1	-	3.18	0.1220	-	0.1252
A4	0.8	-	1.0	0.0315	-	0.0394
A5	-	0.2	-	-	0.0079	-
a1	0.03	-	-0.04	0.0012	-	-0.0016
b	0.22	-	0.38	0.0087	-	0.0150
c	0.23	-	0.32	0.0091	-	0.0126
D[2]	15.8	-	16.0	0.6220	-	0.6299
D1	9.4	-	9.8	0.3701	-	0.3858
D2	-	1.0	-	-	0.0394	-
E	13.9	-	14.5	0.5472	-	0.5709
E1[2]	10.9	-	11.1	0.4291	-	0.4370
E2	-	-	2.9	-	-	0.1142
E3	5.8	-	6.2	0.2283	-	0.2441
E4	2.9	-	3.2	0.1142	-	0.1260
e	-	0.65	-	-	0.0256	-
e3	-	11.05	-	-	0.4350	-
G	0	-	0.075	0	-	0.0031
H	15.5	-	15.900	0.6102	-	0.6260
h	-	-	1.1	-	-	0.0433
L	0.8	-	1.1	0.0315	-	0.0433
N	-	-	10°	-	-	10°
s	-	-	8°	-	-	8°

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. ‘D’ and ‘E1’ do not include mold flash or protusions.
Mold flash or protusions shall not exceed 0.15mm (0.006”).

11.2 Flexiwatt 27 (vertical) package information

Figure 34. Flexiwatt 27 (vertical) package outline

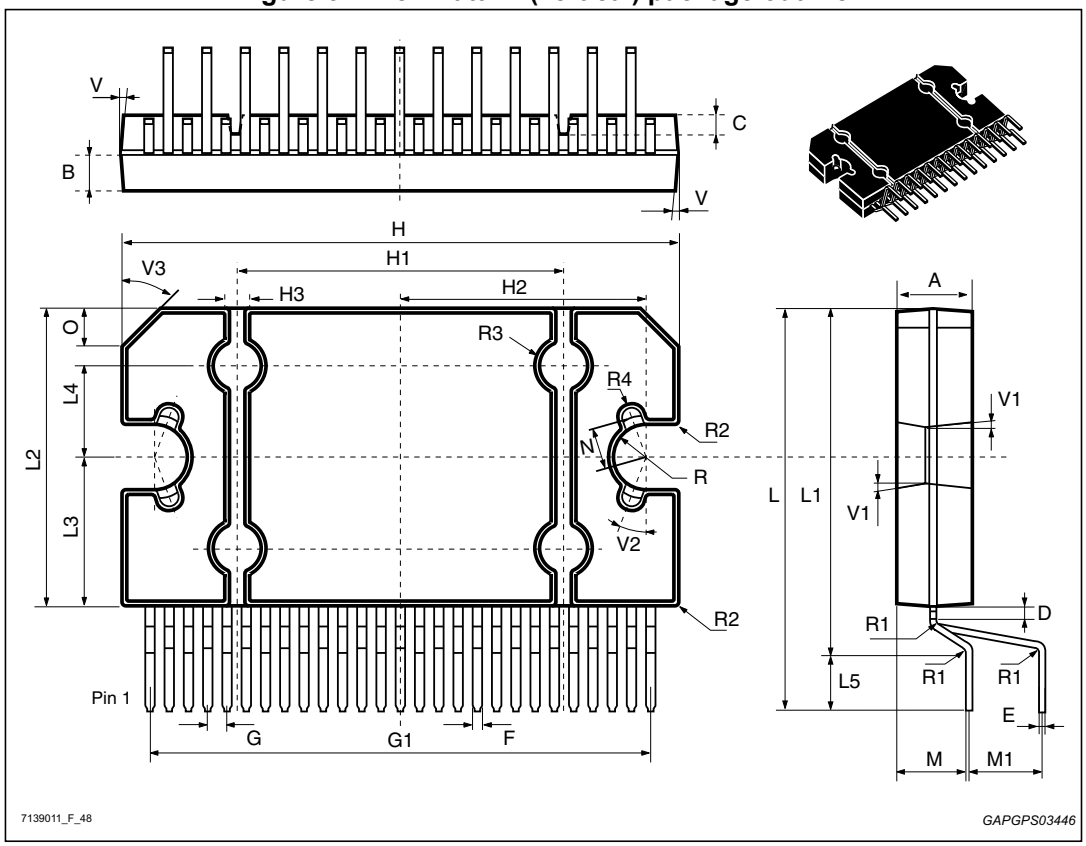


Table 16. Flexiwatt 27 (vertical) package mechanical data

Ref	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.45	4.50	4.65	0.1752	0.1772	0.1831
B	1.80	1.90	2.00	0.0709	0.0748	0.0787
C	-	1.40	-	-	0.0551	-
D	0.75	0.90	1.05	0.0295	0.0354	0.0413
E	0.37	0.39	0.42	0.0146	0.0154	0.0165
F[2]	-	-	0.57	-	-	0.0224
G	0.80	1.00	1.20	0.0315	0.0394	0.0472
G1	25.75	26.00	26.25	1.0138	1.0236	1.0335
H [3]	28.90	29.23	29.30	1.1378	1.1508	1.1535
H1	-	17.00	-	-	0.6693	-
H2	-	12.80	-	-	0.5039	-

Table 16. Flexiwatt 27 (vertical) package mechanical data (continued)

Ref	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
H3	-	0.80	-	-	0.0315	-
L [3]	22.07	22.47	22.87	0.8689	0.8846	0.9004
L1	18.57	18.97	19.37	0.7311	0.7469	0.7626
L2 [3]	15.50	15.70	15.90	0.6102	0.6181	0.6260
L3	7.70	7.85	7.95	0.3031	0.3091	0.3130
L4	-	5	-	-	0.1969	-
L5	3.35	3.5	3.65	0.1319	0.1378	0.1437
M	3.70	4.00	4.30	0.1457	0.1575	0.1693
M1	3.60	4.00	4.40	0.1417	0.1575	0.1732
N	-	2.20	-	-	0.0866	-
O	-	2	-	-	0.0787	-
R	-	1.70	-	-	0.0669	-
R1	-	0.5	-	-	0.0197	-
R2	-	0.3	-	-	0.0118	-
R3	-	1.25	-	-	0.0492	-
R4	-	0.50	-	-	0.0197	-
V	5°			5°		
V1	3°			3°		
V2	20°			20°		
V3	45°			45°		

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. dam-bar protusion not included.
3. molding protusion included.

11.3 Package marking information

Figure 35. Flexiwatt 27 marking information

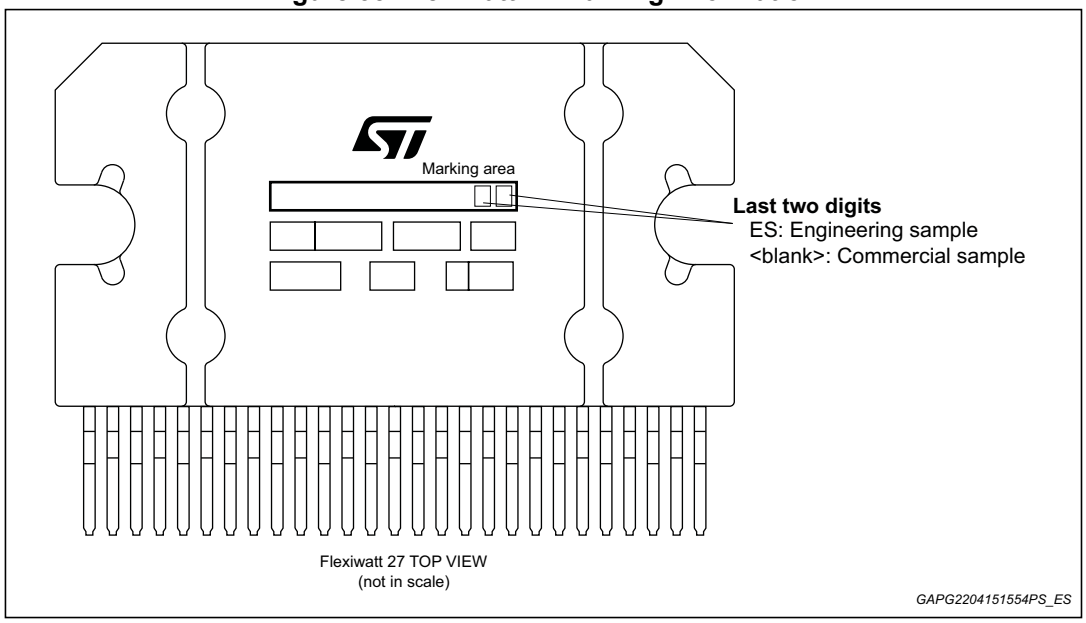
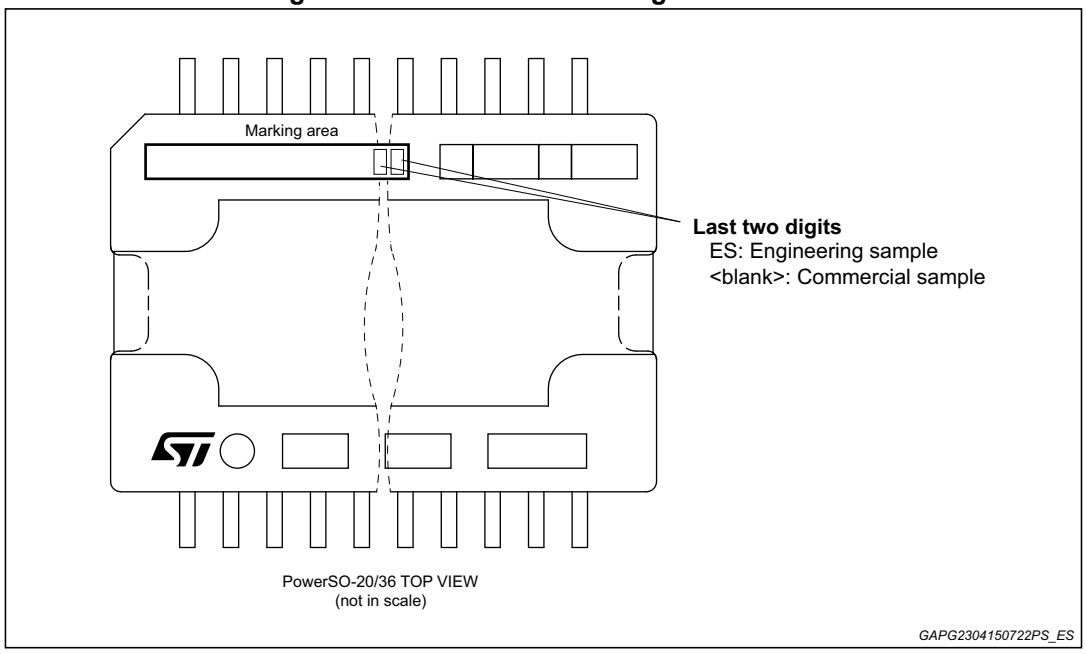


Figure 36. PowerSO-36 marking information



Parts marked as ‘ES’ are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

12 Revision history

Table 17. Document revision history

Date	Revision	Changes
06-Jul-2017	1	Initial release.
27-Mar-2018	2	Removed in cover page and in the whole document any reference to the CPN 'TDA7808-HLX' packaged in Flexiwatt27. Updated *Figure 4: I^2C bus mode application diagram (PowerSO) on page 9*.
06-Apr_2018	3	Datasheet changed from Confidentiality level to Public.
15-Jan-2019	4	Updated: – *Table 1: Device summary on page 1*; – *Section 1.2: Pins description*; – *Section 2: Application diagrams*; – In *Table 4: Absolute maximum ratings* for the parameter "C_{max} Maximum capacitor vs. ground connected to the output" the value ichange from 10 nF to 4.7 nF. – *Section 9: I^2C bus interface*; – *Table 9: Address threshold on page 27*; – *Section 10: I^2C registers*; – *Section 11: Package information* added "Flexiwatt 27 (vertical) package information".