



## TE0725LP TRM

Revision: v.45

Exported on: 06/29/2018

# 1 Table of Contents

1	Table of Contents.....	2
2	Overview.....	4
2.1	Key Features.....	4
2.2	Block Diagram.....	4
2.3	Main Components.....	5
2.4	Initial Delivery State.....	6
3	Boot Process.....	7
4	Signals, Interfaces and Pins.....	8
4.1	I/Os on Pin Headers .....	8
4.2	PL I/O-Banks.....	8
4.3	JTAG Interface.....	8
4.3.1	XMOD FTDI JTAG-Adapter Header JB1 .....	8
4.4	UART Interface .....	9
4.5	QSPI Interface .....	9
4.6	I2C Interface .....	10
4.7	Differential Analog Input .....	10
5	On-board Peripherals .....	11
5.1	Quad SPI Flash Memory.....	11
5.2	HyperFlash™ Memory.....	11
5.3	EEPROM .....	11
5.4	System Clock Oscillator.....	11
5.5	On-board LEDs .....	11
5.6	Connectors .....	11
6	Power and Power-On Sequence .....	12
6.1	Power Supply .....	12
6.2	Power Consumption .....	12
6.3	Power-On Sequence .....	12
6.4	Voltage Monitor Circuit.....	12
6.5	Power Rails.....	13
6.6	Bank Voltages.....	13
7	Variants Currently In Production .....	14
8	Technical Specifications.....	15
8.1	Absolute Maximum Ratings.....	15
8.2	Recommended Operating Conditions .....	15
8.3	Physical Dimensions .....	15

9	Revision History .....	17
9.1	Hardware Revision History .....	17
9.2	Document Change History .....	17
10	Disclaimer.....	18
10.1	Data privacy .....	18
10.2	Document Warranty.....	18
10.3	Limitation of Liability.....	18
10.4	Copyright Notice .....	18
10.5	Technology Licenses.....	18
10.6	Environmental Protection .....	18
10.7	REACH, RoHS and WEEE .....	18

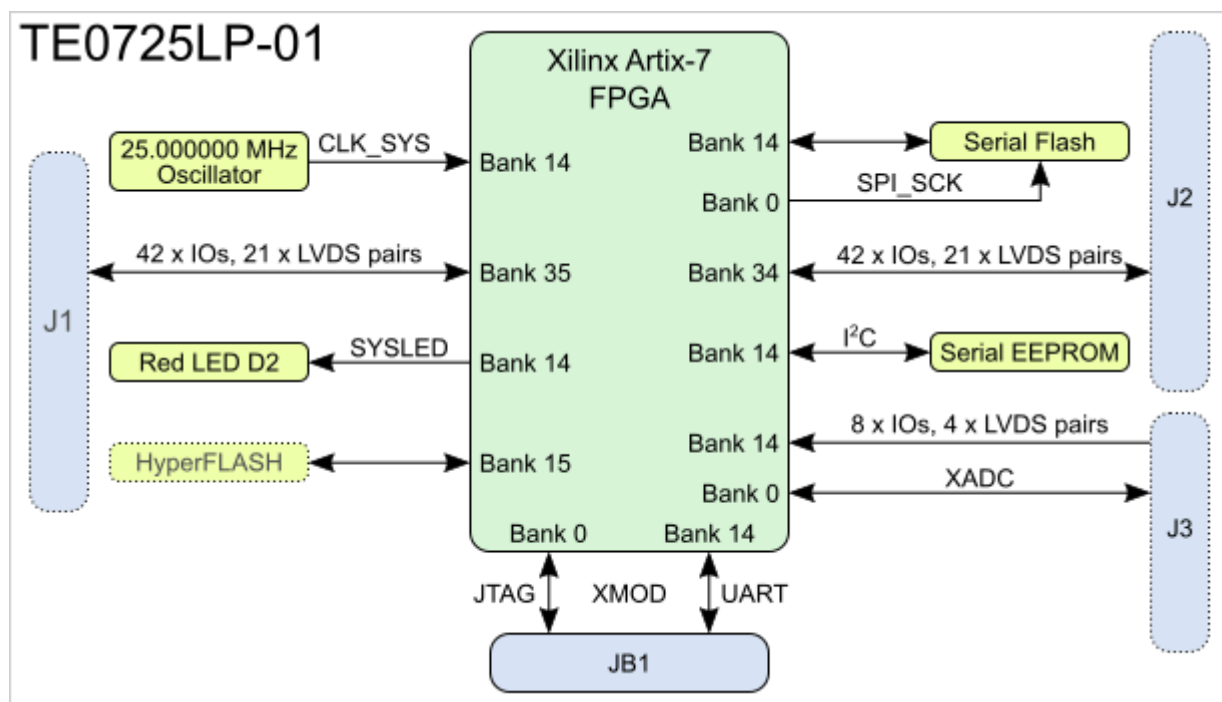
## 2 Overview

The Trenz Electronic TE0725LP is a low cost small-sized FPGA module integrating a Xilinx Artix-7 and 32 MByte Flash memory for configuration and operation. Refer to <http://trenz.org/te0725LP-info> for online version of this manual and the rest of available documentation of the product.

### 2.1 Key Features

- Xilinx Artix-7 XC7A100T FPGA
- 32 MByte QSPI Flash memory
- 2 x 50-pin headers with 2,54mm pitch, ideal for breadboard use
- 92 x GPIOs (42 + 42 + 8)
- 25.000000 MHz system clock
- 128 KBit (16 KByte) I<sup>2</sup>C EEPROM
- 3.3V single power supply with on-board voltage regulators
- JTAG/UART connector
- 1 user LED
- Optional HyperRAM (8 to 32 MByte)
- Commercial temperature grade (Industrial on Request)
- Size 73 x 35 mm

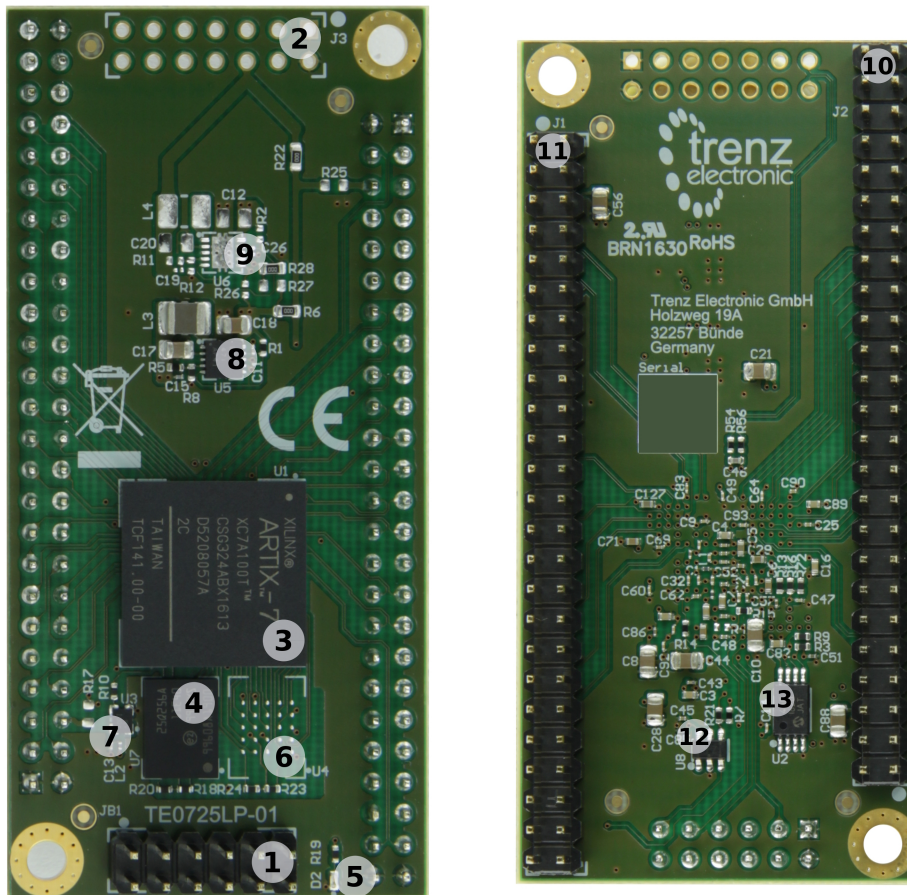
### 2.2 Block Diagram



**Figure 1:** TE0725LP-01 Block Diagram.



## 2.3 Main Components



**Figure 2:** TE0725LP-01 FPGA module (Variant TE0725LP-01-100-2D depicted).

1. XMOD header, JB1
2. 14-pin header placeholder for connector, J3
3. Xilinx Artix-7 FPGA, U1
4. 1.8V, 256 MBit (32 MByte) quad SPI serial flash memory, U7
5. Red LED (SYSLED), D2
6. Cypress S26KS512S 512 MBit (64 MByte) 1.8V HyperFlash™ memory, U4 (optional)
7. Low-power programmable oscillator @25.000000 MHz, U3
8. Low VIN high-efficiency step-down converter (1.5A max.), U5
9. Low VIN high-efficiency step-down converter (1.5A max.), U6 (optional)
10. 50-pin header placeholder for breadboard connector, J1
11. 50-pin header placeholder for breadboard connector, J2
12. Ultra-low supply-current voltage monitor with optional watchdog, U8
13. 128KBit I<sup>2</sup>C CMOS serial EEPROM, U2

## 2.4 Initial Delivery State

<b>On-board Programmable Device</b>	<b>Content</b>	<b>Notes</b>
Quad SPI Flash (U7) OTP area	Empty	-
I <sup>2</sup> C EEPROM, U2	Empty	-
HyperFlash™ memory, U4	Empty	-

**Table 1:** Module initial delivery state of programmable on-board devices.

## 3 Boot Process

By default the configuration mode pins of the FPGA are set to Master SPI mode, hence the FPGA is configured from serial QSPI flash memory at system start-up. The JTAG interface of the module is provided for storing the initial FPGA configuration data to the QSPI flash memory.

## 4 Signals, Interfaces and Pins

### 4.1 I/Os on Pin Headers

I/O signals of the FPGA SoC's I/O banks connected to the board's pin headers:

Bank	Type	Pin Header	I/O Signal Count	Bank Voltage
14	HR	J3	8 I/O's, 4 LVDS pairs	1.8V
34	HR	J2	42 I/Os, 21 LVDS pairs	VCCIO34
35	HR	J1	42 I/Os, 21 LVDS pairs	VCCIO35

**Table 2:** General overview of single ended and LVDS I/O signals connected to pin headers

### 4.2 PL I/O-Banks

Bank	VCCIO	Used I/O's	Available On Connectors	Notes
0	1.8V	7	4	4 I/O's used for JTAG interface, 3 control signals (DONE, PROG_B, INIT).
14	1.8V	22	11	8 I/O's (4 LVDS pairs) connected to J3, 3 I/O's to XMOD header JB1 (2 UART I/O's, 1 user I/O), 1 I/O to LED D2.
15	1.8V	18	-	Used for optional HyperFlash™ U4.
34	User select	42	42	0-Ohm resistor R17 option to select 1.8V I/O-bank VCCIO.
35	User select	42	42	0-Ohm resistor R25 option to select 1.8V I/O-bank VCCIO.

**Table 3:** General overview of PL I/O-bank signals.

### 4.3 JTAG Interface

JTAG access to the Xilinx Artix-7 device is provided through XMOD header JB1.

Header JB1 (2 x 6 pin) is compatible with XMOD-JTAG adapter TE0790. This adapter can be inserted from top onto the TE0725LP, if JB1 is fitted with male pin header. Optionally JB1 can be fitted with pin header from bottom, in that case the JTAG connector must be on the base board.

#### 4.3.1 XMOD FTDI JTAG-Adapter Header JB1

The JTAG interface of the FPGA can be accessed via XMOD header JB1, so in use with the XMOD-FT2232H adapter-board TE0790 the FPGA can be configured via USB2.0 interface. The TE0790 board provides also an UART interface to the FPGA device which can be accessed by the USB2.0 interface of the adapter-board while the signals between these serial interfaces will be converted.

Following table describes the signals and interfaces of the XMOD header JB1:

Pin Schematic Name	XMOD Header JB1	Pin Note
F_TCK	C (pin J3-4)	-

Pin Schematic Name	XMOD Header	JB1 Pin	Note
F_TDO	D (pin J3-8)	-	-
F_TDI	F (pin J3-10)	-	-
F_TMS	H (pin J3-12)	-	-
UART_RXD	A (pin J3-3)		UART receive line, connected to PL I/O-bank 14.
UART_TXD	B (pin J3-7)		UART transmit line, connected to PL I/O-bank 14.
XMOD_E	E (pin J3-9)		User configurable, connected to PL I/O-bank 14, pin M17.
NRST	G (pin J3-11)		Assigned to 'PROG_B' (configuration-reset signal of FPGA) via IC U8.


**Table 4:** XMOD header JX1 signals and connections.

When using XMOD FTDI JTAG Adapter TE0790, the adapter-board's VCCIO will be sourced by the FPGA module's supply voltage (1.8V). The adapter board's VCC has to be sourced by the USB Host interface.

For this configuration, set the XMOD DIP-switch as follows in table below:

XMOD DIP-switches	Position
Switch 1	ON
Switch 2	OFF
Switch 3	OFF
Switch 4	ON

**Table 5:** XMOD adapter board DIP-switch positions for voltage configuration.

 Use Xilinx compatible TE0790 adapter board (designation TE-0790-xx with out 'L') to program the Xilinx Zynq devices.

The TE0790 adapter board's CPLD have to be configured with the **Standard** variant of the firmware. Refer to the TE0790 Resources Site for further information and firmware download.

## 4.4 UART Interface

UART interface is available on B2B connector JM2. With the TE0790 XMOD USB2.0 adapter, the UART signals can be converted to USB2.0 interface signals:

UART Signal Schematic Name	B2B	XMOD Header	JX1 Pin	Header J3	Note
B14_L0	JM2-99	JX1-7		J3-7	UART-TX (transmit line)
B14_L25	JM2-97	JX1-3		J3-3	UART-RX (receive line)

**Table 6:** UART interface signals.

## 4.5 QSPI Interface

The QSPI interface of the FPGA device is routed to and used by the on-module QSPI flash IC U7:

SD IO Signal Schematic Name	FPGA I/O	Flash Memory (U7) Pin	Note
SPI-DQ0	Bank 14, pin K17	D3	QSPI data
SPI-DQ1	Bank 14, pin K18	D2	QSPI data
SPI-DQ2	Bank 14, pin L14	C4	QSPI data
SPI-DQ3	Bank 14, pin M14	D4	QSPI data
SPI_SCK	Bank 0, pin E9	B2	QSPI clock
SPI-CS	Bank 14, pin L13	C2	QSPI chip select

**Table 7:** QSPI interface signals.

## 4.6 I<sup>2</sup>C Interface

The I<sup>2</sup>C interface of the FPGA device is routed to and used by the on-module EEPROM IC U2:

I <sup>2</sup> C Signal Schematic Name	FPGA I/O	EEPROM (U2) Pin	Notes
I2C_SDA	Bank 14, pin U185		I <sup>2</sup> C data line, 1.8V reference voltage
I2C_SCL	Bank 14, pin U176		I <sup>2</sup> C clock line, 1.8V reference voltage
I2C_WP	Bank 14, pin T187		Write-protect signal of EEPROM

**Table 8:** I<sup>2</sup>C interface signals.

## 4.7 Differential Analog Input

The TE0725LP FPGA module provides access to the XADC (Analog-to-Digital Converter) unit of the Xilinx FPGA via connector J3:

I <sup>2</sup> C Signal Schematic Name	FPGA I/O	Connector J3 Pin	Notes
XADC_P	Bank 0, pin J10 (VP_0)	J3-14	-
XADC_N	Bank 0, pin K9 (VN_0)	J3-13	-

**Table 9:** XADC interface signals.

## 5 On-board Peripherals

### 5.1 Quad SPI Flash Memory

On-module QSPI flash memory (U7) is provided by Micron Serial NOR Flash Memory N25Q256A with 256 MBit (32 MByte) storage capacity. This non volatile memory is used to store initial FPGA configuration. Besides FPGA configuration, remaining free flash memory can be used for user application and data storage. All four SPI data lines are connected to the FPGA allowing x1, x2 or x4 data bus widths. Maximum data rate depends on the selected bus width and clock frequency used.

### 5.2 HyperFlash™ Memory

On the TE0725LP FPGA module is optionally available a Cypress S26KS512S 512 MBit (64 MByte) 1.8V HyperFlash™ memory IC (U4). This flash memory IC is connected to the FPGA bank 15 via the Cypress specific HyperBus interface, which offers read bandwidth up to 333MByte/s.

### 5.3 EEPROM

A Microchip 24AA128 128 KBit (16 KByte) CMOS Serial EEPROM (U2). The device is organized as eight blocks of 16 KBit memory with a 2-wire serial interface connected on FPGA bank 14. The memory as is available for application use. It is accessible over I<sup>2</sup>C bus with slave device address 0x50.

### 5.4 System Clock Oscillator

A low-power SiTime programmable oscillator (U3) @25.000000 MHz configured on-module is connected to PL I/O-bank 14 and provides the system reference clock signal.

### 5.5 On-board LEDs

There is one red LED connected to the FPGA bank 14, pin M16. This LED is user configurable to indicate for example any system status.

LED	Color	Signal	Schematic Name	FPGA	Notes
D2	Red	'SYSLED'		Pin M16-	

**Table 10:** LEDs of the module.

### 5.6 Connectors

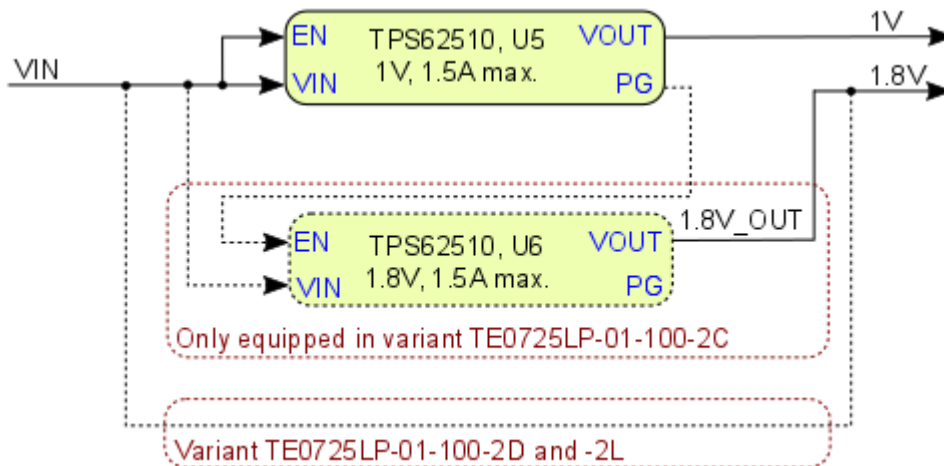
All connectors are for 100mil headers, all connector locations are in 100mil (2.54mm) grid. The module's PCB provides footprints to mount and solder optional (B2B connector) headers, if those are not factory-fitted on module.

## 6 Power and Power-On Sequence

To power-up a module, power supply with minimum current capability of 1A is recommended.

### 6.1 Power Supply

TE0725LP needs one single power supply with nominal of 3.3V at the variant TE0725-01-100-2C or 1.8V at the variants TE0725LP-01-100-2D and TE0725LP-01-100-2L. Following diagram shows the dependencies of the power supply:



**Figure 3:** Module power supply dependencies

### 6.2 Power Consumption

FPGA	Design	Typical Power, 25C ambient
XC7A100T-2CSG324C	Not configured	TBD*

**Table 11:** Module power consumption

\*TBD - To Be Determined.

Actual power consumption depends on the FPGA design and ambient temperature.

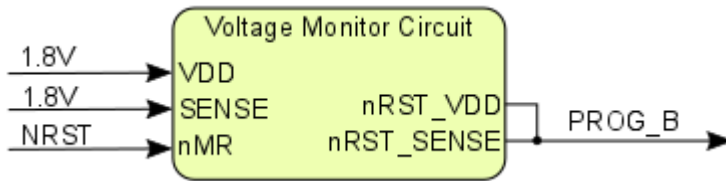
### 6.3 Power-On Sequence

There is no specific or special power-on sequence, single power source is needed as VIN.

### 6.4 Voltage Monitor Circuit

The 1.8V voltage level is monitored by the voltage monitor circuit U8, which generates the PROG\_B signal to begin a new configuration sequence after reset of the FPGA. A manual reset is also possible by driving the connector pin JB1-11 ('NRST') to GND. Hence, by this pin a mounted XMOD adapter board can perform a reset on the FPGA module.





**Figure 4:** Voltage monitor circuit

## 6.5 Power Rails

Power Rail Name	J1 Pins	J2 Pins	J3 Pins	JB1 Pin	Direction	Notes
VIN	5	5	5	-	Input	Power supply voltage
1.8V	-	-	-	6	Output	JTAG VCCIO
1.8V_OUT	-	-	-	6	Output	-
VCCIO34	-	6, 45	-	-	Input	Bank voltage
VCCIO35	6, 45	-	-	-	Input	Bank voltage

**Table 13:** Board power rails

## 6.6 Bank Voltages

Bank	Bank I/O Voltage	VCCO Voltage Range
0 (config)	1.8V	fixed
14 (HR)	1.8V	fixed
15 (HR)	1.8V	fixed
34 (HR)	VCCIO34	1.2V ... 3.3V
35 (HR)	VCCIO34	1.2V ... 3.3V

**Table 14:** Board bank voltages

## 7 Variants Currently In Production

**Trenz shop TE0725LP overview page**

[English page](#)

[German page](#)

**Table 12:** Module variants production

## 8 Technical Specifications

### 8.1 Absolute Maximum Ratings


Parameter	Min	Max	Unit	Reference document
VIN supply voltage (Variant TE0725LP-01-100-2C)	-0.3	4	V	TI TPS62510 data sheet
VIN supply voltage (Variant TE0725LP-01-100-2D and -2L)	-0.3	2	V	Xilinx datasheet <a href="#">DS181</a> / TI TPS62510 datasheet
HR I/O banks supply voltage (VCCO)	-0.5	3.6	V	Xilinx datasheet <a href="#">DS181</a>
HR I/O banks input voltage (VCCIO single ended)	-0.4	VCCO + 0.55	V	Xilinx datasheet <a href="#">DS181</a>
Storage Temperature	-40	+100	°C	LED SML-P11x series datasheet

**Table 13:** Absolute maximum ratings

### 8.2 Recommended Operating Conditions

Parameter	Min	Max	Unit	Reference document
VIN supply voltage (Variant TE0725LP-01-100-2C)	1.8	3.8	V	TI TPS62510 data sheet
VIN supply voltage (Variant TE0725LP-01-100-2D and -2L)	1.8	1.89	V	Xilinx datasheet <a href="#">DS181</a> / TI TPS62510 datasheet
HR I/O banks supply voltage (VCCO)	1.14	3.465	V	Xilinx datasheet <a href="#">DS181</a>
HR I/O banks input voltage (VCCIO single ended)	-0.2	VCCO + 0.20	V	Xilinx datasheet <a href="#">DS181</a>
Operating Temperature	0	+85	°C	Xilinx datasheet <a href="#">DS181</a>

**Table 14:** Recommended operating conditions

 Please check Xilinx datasheet [DS181](#) for complete list of absolute maximum and recommended operating ratings for the Artix-7 device.

### 8.3 Physical Dimensions

Please note that two different units are used on the figures below, SI system millimeters (mm) and imperial system thousandths of an inch (mil). This is because of the 100mil pin headers used, see also explanation below. To convert mils to millimeters and vice versa use formula  $100\text{mil's} = 2,54\text{mm}$ .

- Board size: PCB 72.9mm × 34.8mm
- PCB thickness: ca. 1.65mm



## 9 Revision History

### 9.1 Hardware Revision History

Date	Revision	Notes	PCN	Documentation Link
-	01	First production release	-	<a href="#">TE0725LP-01</a>


**Table 15:** Module hardware revision history

Hardware revision number is printed on the PCB board together with the module model number separated by the dash.



**Figure 6:** Module hardware revision number

### 9.2 Document Change History

Date	Revision	Contributors	Description
 2018-06-29	45	Ali Naseri, Jan Kumann	• First TRM release

**Table 16:** Document change history

## 10 Disclaimer

### 10.1 Data privacy

Please also note our data protection declaration at <https://www.trenz-electronic.de/en/Data-protection-Privacy>

### 10.2 Document Warranty

The material contained in this document is provided “as is” and is subject to being changed at any time without notice. Trenz Electronic does not warrant the accuracy and completeness of the materials in this document. Further, to the maximum extent permitted by applicable law, Trenz Electronic disclaims all warranties, either express or implied, with regard to this document and any information contained herein, including but not limited to the implied warranties of merchantability, fitness for a particular purpose or non infringement of intellectual property. Trenz Electronic shall not be liable for errors or for incidental or consequential damages in connection with the furnishing, use, or performance of this document or of any information contained herein.

### 10.3 Limitation of Liability

In no event will Trenz Electronic, its suppliers, or other third parties mentioned in this document be liable for any damages whatsoever (including, without limitation, those resulting from lost profits, lost data or business interruption) arising out of the use, inability to use, or the results of use of this document, any documents linked to this document, or the materials or information contained at any or all such documents. If your use of the materials or information from this document results in the need for servicing, repair or correction of equipment or data, you assume all costs thereof.

### 10.4 Copyright Notice

No part of this manual may be reproduced in any form or by any means (including electronic storage and retrieval or translation into a foreign language) without prior agreement and written consent from Trenz Electronic.

### 10.5 Technology Licenses

The hardware / firmware / software described in this document are furnished under a license and may be used / modified / copied only in accordance with the terms of such license.

### 10.6 Environmental Protection

To confront directly with the responsibility toward the environment, the global community and eventually also oneself. Such a resolution should be integral part not only of everybody's life. Also enterprises shall be conscious of their social responsibility and contribute to the preservation of our common living space. That is why Trenz Electronic invests in the protection of our Environment.

### 10.7 REACH, RoHS and WEEE

#### **REACH**

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of [REACH](#). The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release