UM10514

GreenChip TEA1755DB1100 90 W power supply

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User manual

COMPANY PUBLIC

Document information

Information	Content
Keywords	TEA1755DB1100, TEA1755T GreenChip SR, TEA1792TS, control IC, TEA1703TS, PFC, flyback, synchronous rectification, high efficiency, power-down functionality for very low standby power, adapter, notebook, PC power
Abstract	This user manual provides the specification, performance measurements, schematics, bill of materials and PCB layout of the TEA1755DB1100 90 W board. See the associated data sheets and application notes for information on the TEA1792TS, TEA1792TS and TEA1703TS ICs.

Table 1. Revision history

Rev	Date	Description
v.4	20170913	new version
Modifications	• Text and graphics have been updated throughout the document.	
v.3	20150112	new version
v.2	20131118	new version
v.1.1	20130118	updated issue
v.1	20121210	first issue

1 Introduction

Warning	
 	The non-insulated high voltages that are present when operating this product, constitute a risk of electric shock, personal injury, death and/or ignition of fire. This product is intended for evaluation purposes only. It shall be operated in a designated test area by personnel qualified according to local requirements and labor laws to work with non-insulated mains voltages and high-voltage circuits. This product shall never be operated unattended.

This user manual describes the TEA1755DB1100 demo board. The demo board is a universal input, 19.5 V, 90 W single output power supply using the GreenChip device TEA1755T together with the TEA1703TS and TEA1792TS.

It contains the following content:

- Specification of the power supply
- The circuit diagram
- The component list
- The PCB layout and component positions
- Documentation of the PFC choke and flyback transformer
- Test data and oscilloscope pictures of the most important waveforms

The GreenChip combines the control and drive for both the PFC and the flyback stages into a single device. The TEA1755T provides SMPS control functionality to comply with the IEC61000-3-2 harmonic current emission requirements. It enables a significant reduction of components, save PCB space and BOM cost.

It offers low-power consumption in no-load condition, which is attractive for the consumer products where it is a requirement. The built-in green functions ensure high efficiency at all power levels. This efficiency results in a design that can easily meet all existing and proposed energy efficiency standards such as: CoC (Europe), ENERGY STAR (U.S), CEC (California), MEPS (Australian and New Zealand), and CECP (China).

The TEA1703 in combination with the TEA1755T provides a very low-power consumption performance in standby mode.

The TEA1792 is a synchronous rectification control IC that requires no external components to set the timing. The GreenChip SR can be applied to a wide V_{CC} operating range between 8.5 V and 38 V, minimizing the number of external components required and enabling simpler designs. The high driver output voltage (10 V) makes the GreenChip SR compatible with all brands of MOSFETs.

Figure 1 shows the assembled top board view and bottom view of the TEA1755DB1100 demo board.

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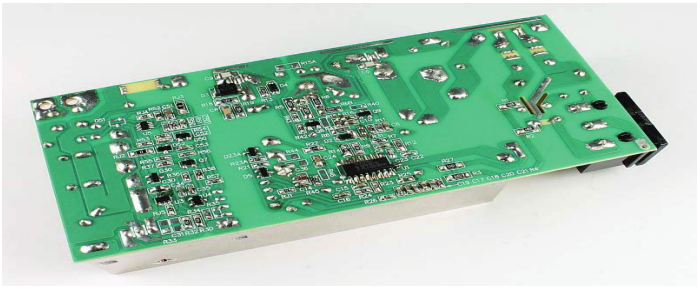
a. Top view



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b. Bottom view

Figure 1. TEA1755DB1100 demo board

1.1 Features

- Universal mains supply operation
- Integrated PFC and flyback controller
- Accurate PFC on/off control
- Burst mode operation for high efficiency with low audible noise
- OverCurrent Protection (OCP)
- OverPower Protection (OPP)
- OverTemperature Protection (OTP)
- Open control loop protection for both converters (the open-loop protection for the flyback converter is safe restart; TEA1755LT version only)
- Excellent load step performance
- Ultra-low-power consumption in standby mode (Erp lot 6 compliant)
- High/low line output power compensation
- High efficiency (ENERGY STAR and Erp lot 6 compliant)
- EMI CISPR22 compliant

2 Configuration

There are two versions of the TEA1755DB1100 demo board

- APBADC068(A) - with TEA1703TS
- APBADC068(B) - without TEA1703TS

The configuration is marked on the back side of the demo board. The performance data refer to the (A) version, unless otherwise specified. More information about the differences between the two versions and other alternative circuit options can be found in Section 10.

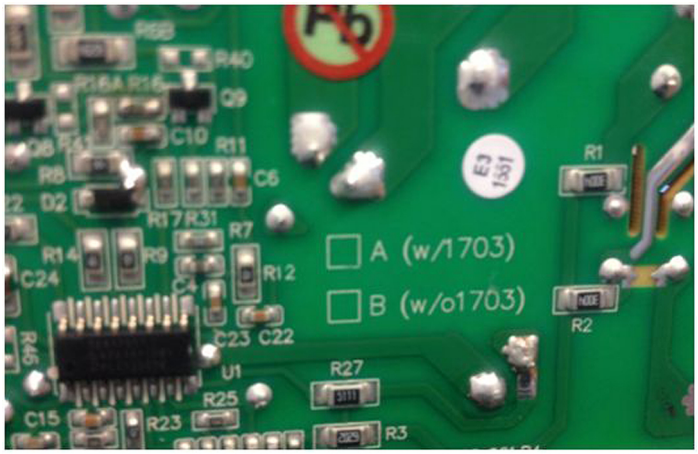

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Figure 2. TEA1755DB1100 demo board configuration marking

3 Power supply specifications

Table 2. Input specifications

Symbol	Description	Condition	Specification			Units
			A		B	
V_i	mains input voltage	-		90 to 264		V
f_i	mains input frequency	-		47 to 64		Hz
$P_{i(no-load)}$	no-load input power	230 V/50 Hz	< 50		< 100	mW

Table 3. Output specifications

Symbol	Description	Condition	Configuration			Units
			A		B	
V_o	output voltage	-		19.5		V
$V_{o(min)}$	minimum output voltage during standby operation	at 90 V; 60 Hz; no-load	≥ 12	-		V
$V_{o(ripple)(p-p)}$	output ripple and noise	20 MHz bandwidth		≤ 100		mV_{p-p}
I_o	continuous output current	90 V to 264 V		0 to 4.62		A
I_{OM}	peak output current	115 V; 60 Hz		5.6		A
t_{holdup}	hold-up time	115 V; 60 Hz; full-load		5		ms
$V_{line(reg)}$	output voltage regulation as a function of mains voltage	90 V to 264 V		±1		%
$V_{L(reg)}$	output voltage regulation as a function of load	0 A to 4.62 A		±2		%
$t_{startup}$	start-up time	115 V; 60 Hz		≤ 2		s
η	efficiency	according to ENERGY STAR (EPS2)		≥ 89.5		%
-	EMI	CISPR22 compliant		pass		-
-	immunity against ESD	EN61000-4-2 compliant (≥ ±12 kV air discharge)		pass		-
SCP	short-circuit protection	-		P_{in} < 1.2		W
OCP	overcurrent protection	-		P_{in} < 2.2		W
OVP	latched output overvoltage protection	-		< 24		V

Symbol	Description	Condition	Configuration			Units
			A		B	
OTP	overtemperature protection	-		≤ 120		°C
FLR	fast latched reset	Disconnect mains voltages		< 2		s

4 Performance data

4.1 Test setup

Performance figures are based on the following PCB design:

- Schematic version: APBADC068 TEA1755 plus TEA1792 plus TEA1703, 90 W adapter (see Figure 25 or Figure 26).

4.1.1 Test equipment

- AC source: Agilent 6812B
- Power meter: Yokogawa WT210 with harmonics option
- DC electronic load: Chroma, model 6310
- Digital oscilloscope: Yokogawa DLM 2024
- Current probe: Yokogawa 701933 30 A; 50 MHz
- 100 MHz, high-voltage differential probe: Yokogawa 700924
- 500 MHz, low voltage differential probe: Yokogawa 701920
- Multimeter: Keithley 2000
- EMC receiver: Rohde & Schwarz ESPI-3 + LISN ENV216

4.1.2 Test conditions

- Adapter on the lab-table with the heat sinks downwards
- The adapter has no casing
- Ambient temperature between 20 °C and 25 °C
- Measurements are made after stabilization of the temperature. These measurements are according to "test method for calculating the efficiency of single-voltage external AC-DC and AC-AC power supplies" of ENERGY STAR

4.2 Efficiency

Efficiency measurements are executed using an automated test program containing a temperature stability detection algorithm. The output voltage and current are measured using a 4-wire current sense configuration directly at the PCB connector.

The measurement results for a selection of mains input voltages are shown in Table 4.

Table 4. TEA1755DB1100 demo board efficiency results

Condition	ENERGY STAR 2.0 Efficiency requirement (%)	Average	100 % load	75 % load	50 % load	25 % load	500 mW load	250 mW load	100 mW load
90 V/60 Hz	> 87	90.5	89.87	90.74	90.79	90.63	81.41	72.99	54.61
100 V/50 Hz	> 87	90.9	90.41	91.14	91.11	90.94	81.49	72.88	54.13
115 V/60 Hz	> 87	91.4	90.98	91.60	91.47	91.53	81.29	72.41	53.34
230 V/50 Hz	> 87	91.1	91.72	91.37	90.01	91.33	77.11	66.12	45.27
264 V/50 Hz	> 87	91	91.92	91.53	89.96	90.76	75.27	63.71	42.78

Notes:

Warm-up time is 10 minutes.

There is an efficiency loss of 1 % when measured at the end of a 1 m output cable.

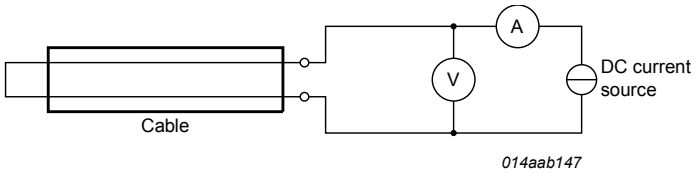


Figure 3. DC resistance output cable

The DC resistance output cable produces a two-way resistance of:

$$\frac{voltage\ drop}{current} = \frac{0.217}{3.01} = 72\ \ m\Omega\ (two\text{-}way) \quad (1)$$

4.3 PFC on/off level

To measure the PFC on/off tripping point, slowly increase/decrease the output current and check the power factor.

The measurement results for a selection of mains input voltages are shown in Table 5.

Table 5. PFC on and off level as a function of the mains input voltage

Condition	Output current (A)	
	PFC ON level	PFC OFF level
90 V/60 Hz	1.8	1.25
100 V/50 Hz	1.82	1.25
115 V/60 Hz	1.82	1.25
230 V/50 Hz	1.76	1.22
264 V/50 Hz	1.76	1.22

4.4 No-load power consumption

Power consumption performance of the total application without load connected is measured using an automated test program containing a temperature stability detection algorithm.

The measurement results for a selection of mains input voltages are shown in Table 6.

Table 6. Output voltage and power consumption: no-load

Condition	ENERGY STAR 2.0 requirement (mW)	No-load power consumption (mW)	
		Configuration A	Configuration B
90 V/60 Hz	≤ 300	4	69
100 V/50 Hz	≤ 300	5	70
115 V/60 Hz	≤ 300	6	72
230 V/50 Hz	≤ 300	27	97
264 V/50 Hz	≤ 300	34	112

Configuration (A) containing the IC combination TEA1755 and TEA1703, results in a standby power consumption far below the requirements of ENERGY STAR EPS2.0. It reflects the extra low standby power consumption that is required in the market for certain products.

4.5 Minimum output current for normal operation

This measurement is valid only for configuration (A). This application can function in two modes:

- Normal mode: TEA1755 is active and output voltage is in regulation.
- Standby mode: TEA1755 is set to power-down mode by TEA1703; output voltage is not in regulation and is a saw tooth waveform with an amplitude between V_o and $V_{o(min)}$

The minimum current to leave standby operation and enter normal operation is measured for 90 V/60 Hz and 264 V/50 Hz. The measurement results are shown in Table 7.

Table 7. Minimum current for normal operation

Condition	Output current (mA)
90 V/60 Hz	1.73
264 V/50 Hz	1.78

4.6 Power factor and THD

The total harmonic distortion for voltage and current is measured according to the IEC standard. Power factor and THD are measured using the Yokogawa power meter at the mains input with an automated test program containing a temperature stability detection algorithm. Measurements are performed for full load (4.62 A) condition.

The measurement results for a selection of mains input voltages are shown in Table 8.

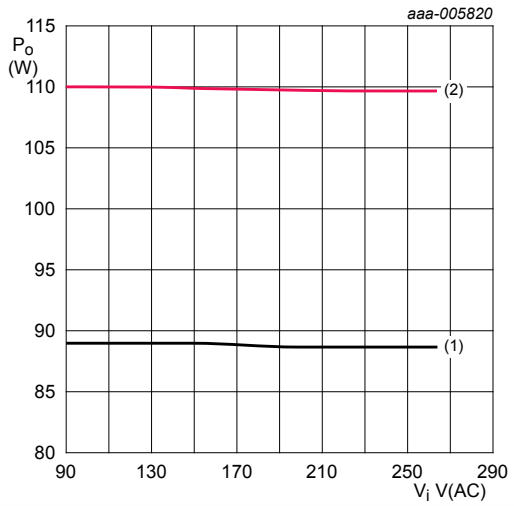
Table 8. Power factor and THD

Condition	Power factor (%)	THD I (%)
90 V/60 Hz	0.99	11.65
100 V/50 Hz	0.99	13.29
115 V/60 Hz	0.98	16.44
230 V/50 Hz	0.92	36.73
264 V/50 Hz	0.89	40.28

4.7 High/low line output power compensation

Nominal output power is measured directly at the output connector for various mains input voltages.

Figure 4 shows the nominal and peak output power as function of mains voltage.



(1) Nominal P_o (W)
(2) Peak P_o (W)

Figure 4. Normal and peak output power as a function of mains voltage

4.8 VCC voltage

The voltage on the VCC pin is measured for both no-load and full-load conditions. The minimum output current of 5 mA prevents switching to standby mode for configuration (A).

Table 9. VCC voltage configuration (A)

Condition	No-load (5 mA)	Full-load (4.62 A)
115 V/60 Hz	21.2	28.6
230 V/50 Hz	21.2	28

Table 10. VCC voltage configuration (B)

Condition	No-load (0 mA)	Full-load (4.62 A)
115 V/60 Hz	15.8	28.6
230 V/50 Hz	15.8	28

Note: *The VCC voltage at no-load condition is* $VCC_{(min)}$.

4.9 Timing and protection

4.9.1 Switch-on delay and output rise time

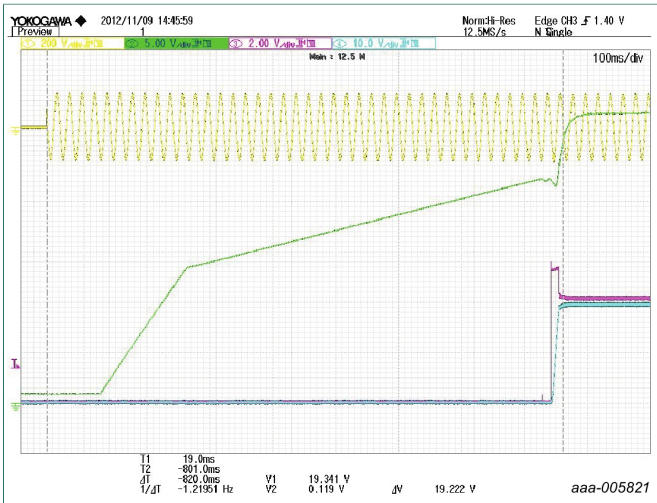
Test conditions

The electronic load is set to Constant Current (CC) mode and V_O = 0 V. The electronic load is set to the maximum continuous output current.

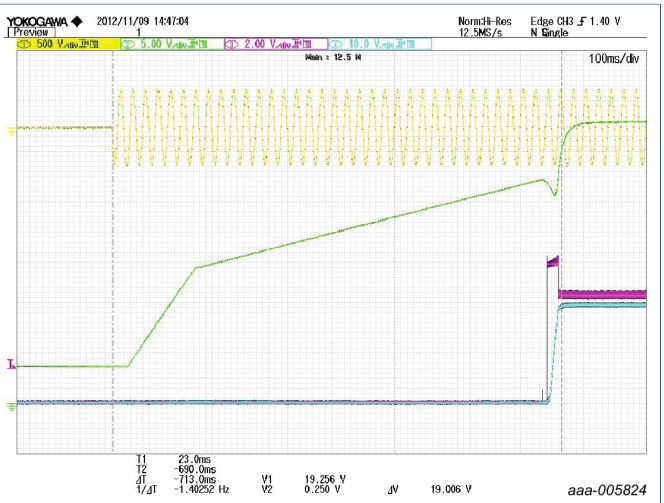
Criteria to pass

- Switch-on delay:
  2 s maximum after the AC mains voltage is applied to the time when the output is within regulation
- Output rise time:
  The output voltage rises from 10 % of the maximum to the regulation limit within 30 ms. The ramp-up of the output voltage is smooth and continuous. No voltage with a negative polarity is present at the output connector during start-up
- No output voltage bounce or hiccup is allowed during switch-on
- There is sufficient margin between the FBCTRL signal and the 7.75 V timeout trigger level. This margin avoids false triggering of the timeout protection due to component tolerances

Figure 5 shows the delay between switch-on and output regulation. Figure 6 shows the output rise time at full load start-up.



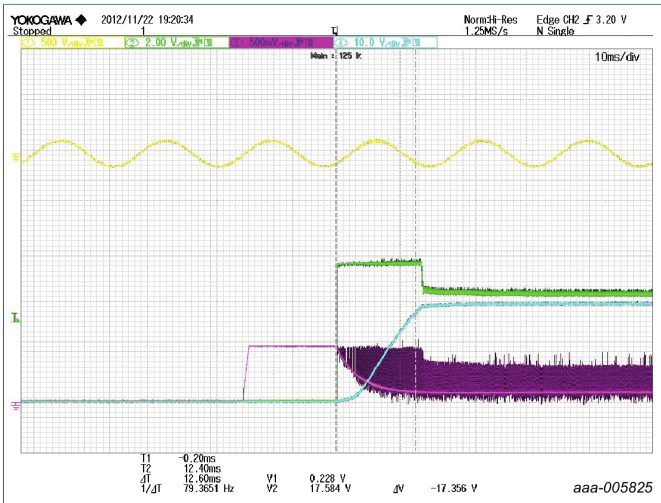
a. Mains input 90 V/60 Hz; delay time: 820 ms



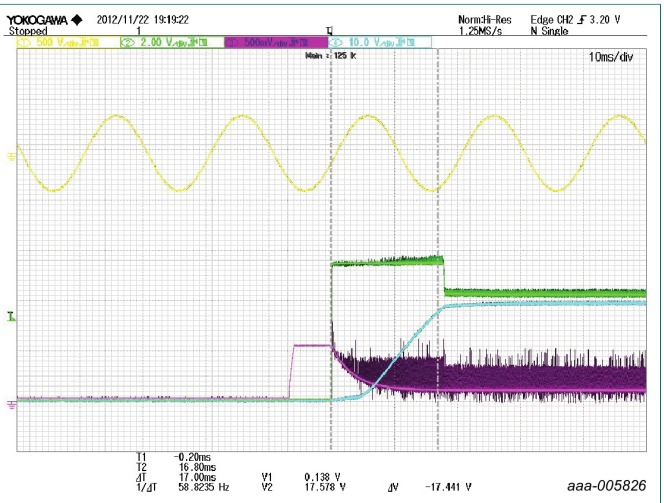
b. Mains input 264 V/50 Hz; delay time: 713 ms

(1) Load = 4.62 A
(2) Ch1 (yellow): mains input
(3) Ch2 (green): VCC pin TEA1755
(4) Ch3 (magenta): FBCTRL pin TEA1755
(5) Ch4 (cyan): output voltage

Figure 5. Delay between switch-on and output regulation



a. Mains input 90 V/60 Hz; output rise time: 13 ms



b. Mains input 264 V/50 Hz; output rise time: 17 ms

(1) Load = 4.62 A
(2) Ch1 (yellow): mains input
(3) Ch2 (green): FBCTRL pin TEA1755
(4) Ch3 (magenta): FBSENSE pin TEA1755
(5) Ch4 (cyan): output voltage

Figure 6. Output rise time at full-load start-up

4.9.2 Brownout and brownout recovery

When the VINSENSE voltage is less than the $V_{stop(VINSENSE)}$, the PFC driver output is switched off to prevent the PFC from operating at very low mains input voltages. The flyback driver output is switched off when driver $t_{on(fb)max}$ is reached.

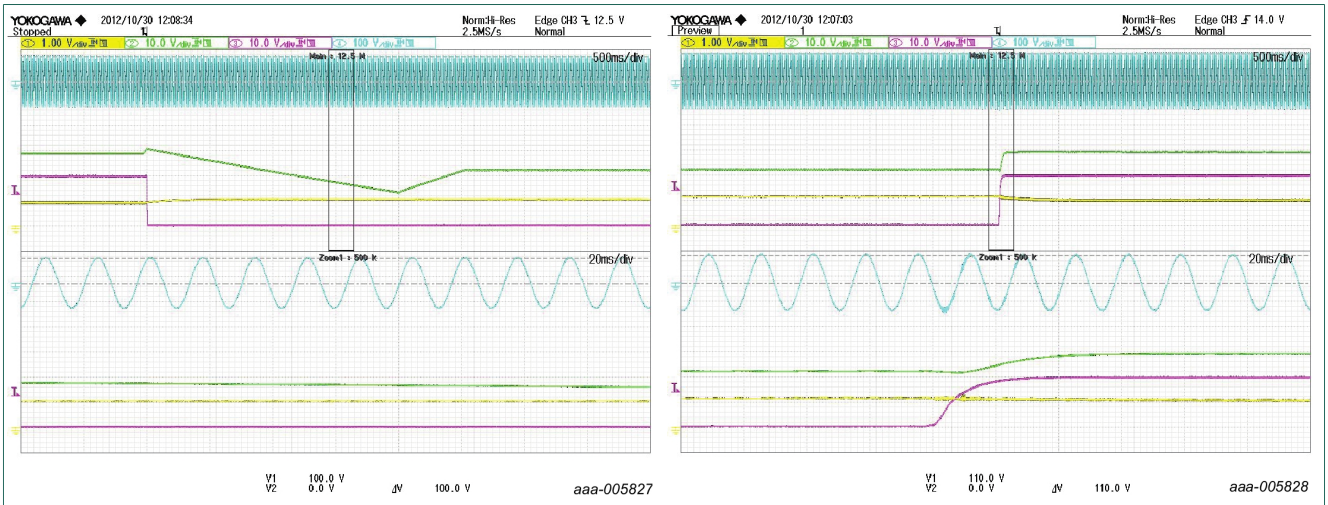
Test conditions

The mains input voltage is decreased from 90 V down to 0 V and then increased from 0 V to 90 V. The electronic load is set to Constant Current (CC) mode and V_{on} = 0 V. The electronic load is set to the maximum continuous output current (4.62 A).

Criteria to pass

- The adapter survives the test without damage and excessive heating of component
- The output voltage remains within the specified regulation limits or switch-off
- No output bounce or hiccup is allowed during switch-on or switch-off
- The adapter powers up before the AC line input voltage reaches 85 V (maximum)

Figure 7 shows the graphs for brownout and brownout recovery.



a. AC mains input from 90 V to 0 V; brownout recovery voltage = 100 / (√2) = 71 V.

b. AC mains input from 0 V to 90 V; brownout recovery voltage = 110 / (√2) = 78 V.

(1) Load = 4.62 A
(2) Ch1 (yellow): VINSENSE pin TEA1755
(3) Ch2 (green): VCC pin TEA1755
(4) Ch3 (magenta): output voltage
(5) Ch4 (cyan): mains input voltage

Figure 7. Brownout and brownout recovery

4.9.3 Output short circuit protection

To protect the adapter and application against an output short circuit or a single fault open (flyback) feedback loop, timeout protection is implemented. When the voltage on the FBCTRL pin rises above 4.5 V (typical), a fault is assumed and switching is blocked.

The timeout protection must not trigger during a normal start-up with the maximum continuous output current.

Test conditions

There are two test conditions:

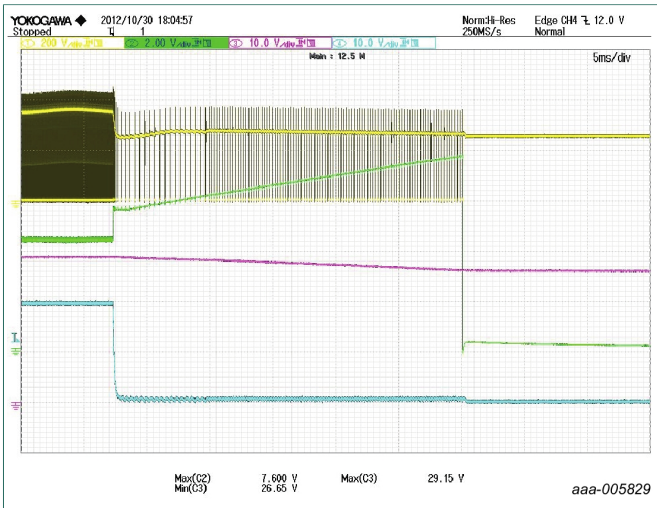
- The adapter is switched on with 4.62 A output load. After start-up a short circuit is applied manually at the end of the output cable
- Before the adapter is switched on, a short circuit is applied at the end of the output cable

Note: *An output short circuit is defined as an output impedance less than 0.1 Ω.*

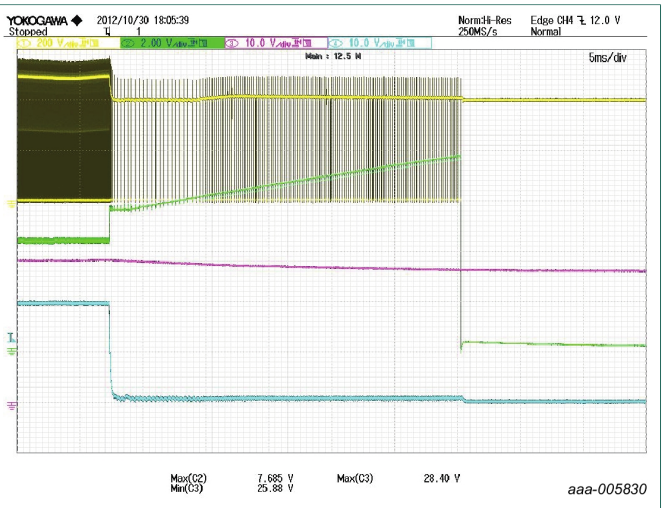
Criteria to pass

- The adapter can withstand a continuous short circuit at the output without damaging or overstressing the adapter under any input conditions
- The average input power is less than 3 W during the short circuit test
- After removal of the short circuit, the adapter recovers automatically

Figure 8 to Figure 10 show the graphs for output short circuit protection.



a. Mains input 90 V/60 Hz

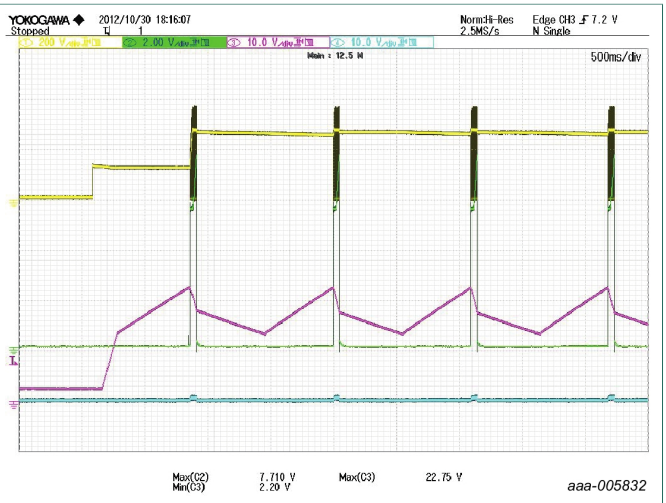


b. Mains input 264 V/50 Hz

(1) Load before short circuit = 4.62 A
(2) Ch1 (yellow): drain flyback MOSFET
(3) Ch2 (green): FBCTRL pin TEA1755
(4) Ch3 (magenta): VCC pin TEA1755
(5) Ch4 (cyan): output voltage

Figure 8. Output short circuit triggering of the timeout protection

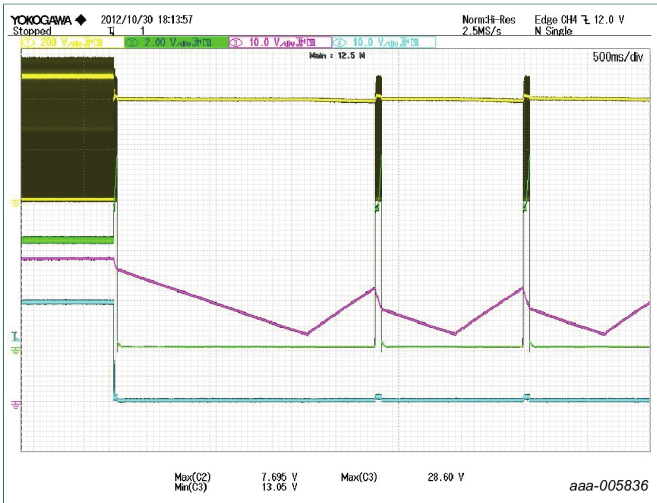
a. Output short circuit during normal operation



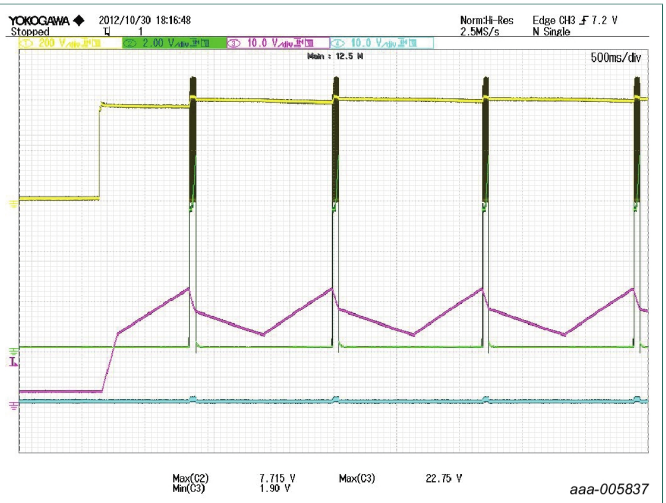
b. Output short circuit applied before start-up

(1) Load before short circuit = 4.62 A
(2) Ch1 (yellow): drain flyback MOSFET
(3) Ch2 (green): FBCTRL pin TEA1755
(4) Ch3 (magenta): VCC pin TEA1755
(5) Ch4 (cyan): output voltage

Figure 9. Output short circuit 90 V/60 Hz



a. Output short circuit during normal operation



b. Output short circuit applied before start-up

(1) Load before short circuit = 4.62 A
(2) Ch1 (yellow): drain flyback MOSFET
(3) Ch2 (green): FBCTRL pin TEA1755
(4) Ch3 (magenta): VCC pin TEA1755
(5) Ch4 (cyan): output voltage

Figure 10. Output short circuit 264 V/50 Hz

Table 11. Output short circuit input power

Output short circuit input power at different mains input voltages

Condition	Input power P_i (mW)	Power meter current range (mA)
90 V/60 Hz	404	100
100 V/50 Hz	412	100
115 V/60 Hz	424	100
230 V/50 Hz	530	200
264 V/50 Hz	568	500

Note: *P_i integrated over 6 minutes.*

4.9.4 OverCurrent Protection (OCP)

Test conditions

- The electronic load is set in Constant Current (CC) mode
- The load is increased from the maximum continuous value in small steps until the overcurrent protection is triggered. The input power is measured after triggering the overcurrent protection without changing the load setting. P_i is integrated during a 6-minute interval. The input current range of the power meter is set to indicate in range when the controller is switching (burst on state).

Criteria to pass

- The output power is limited to less than 150 W, before triggering of the overcurrent protection
- The average input power is less than 3 W when the overcurrent protection has been triggered

Table 12. Maximum output power at different mains input voltages

Condition	Output voltage (V)	OCP trigger level (A)	Output power $P_{o(max)}$ (W)
90 V/60 Hz	19.25	6.7	129
100 V/50 Hz	19.25	6.7	129
115 V/60 Hz	19.25	6.7	129
230 V/50 Hz	19.23	6.4	123
264 V/50 Hz	19.23	6.4	123

Table 13. Input power in OCP state at different mains input voltages

Condition	P_i (W)	Power meter current range (A)
90 V/60 Hz	2.2	2
100 V/50 Hz	2.2	1
115 V/60 Hz	2.2	1
230 V/50 Hz	2.1	0.5
264 V/50 Hz	2.1	0.5

4.9.5 OverVoltage Protection (OVP)

Test conditions

Applying a short circuit across the opto-LED of the optocoupler (U2) creates an output overvoltage condition. The output voltage and VCC pin voltage is measured directly at the output connector. The minimum output current of 15 mA prevents entering standby mode.

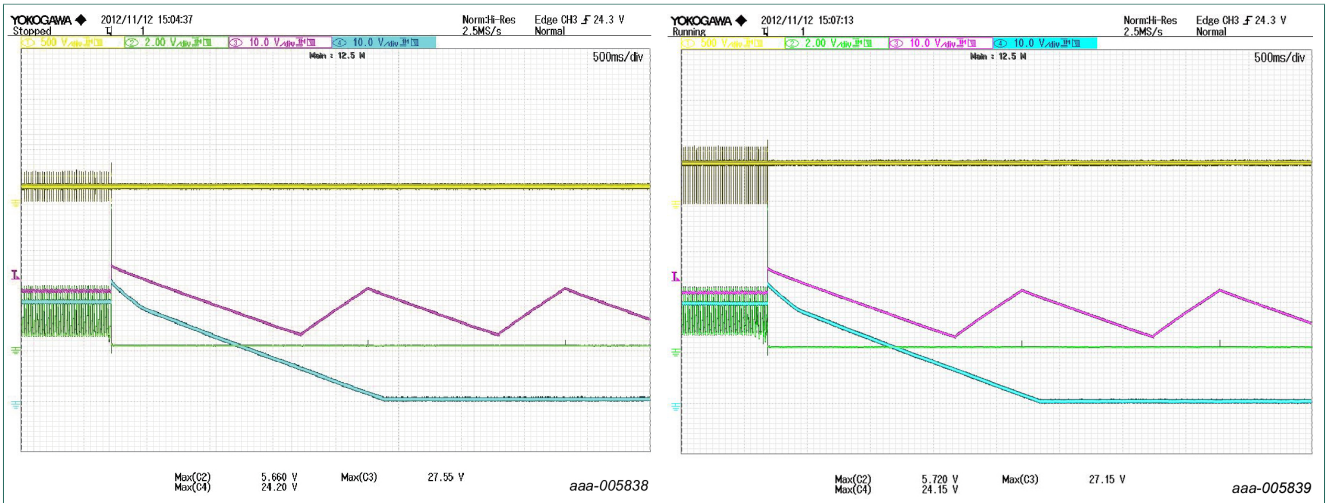
Criteria to pass

- The output voltage does not exceed 25 V or stabilizes between 25 V and the rated output voltage
- The voltage on the TEA1755 VCC pin does not exceed the absolute maximum rating of 38 V
- When OVP is triggered, the primary side controller shuts down and stays in a latched mode
- A single point fault must not cause a sustained overvoltage condition at the output

Table 14. VCC and output voltage in case of OVP as a function of mains input voltage

Condition	V_O (V)	VCC (V)
90 V/60 Hz	24.2	27.55
100 V/50 Hz	24.28	27.45
115 V/60 Hz	24.38	27.48
230 V/50 Hz	24.13	27.30
264 V/50 Hz	24.15	27.15

Figure 11 shows the graphs for output overvoltage protection.



a. Mains input 90 V/60 Hz

b. Mains input 264 V/50 Hz

(1) Output current before short circuit of the optocoupler = 0.015 A

(2) Ch1 (yellow): drain flyback MOSFET

(3) Ch2 (green): FBCTRL pin TEA1755

(4) Ch3 (magenta): VCC pin TEA1755

(5) Ch4 (cyan): output voltage

Figure 11. Output overvoltage protection

4.9.6 OverTemperature Protection (OTP)

An accurate external overtemperature protection (TEA1755 LATCH pin, RT2, R26, and C19) is provided on the TEA1755DB1100 demo board. This measure protects the flyback transformer against overheating (see Figure 12). Normally, the flyback transformer is the hottest component on the board.

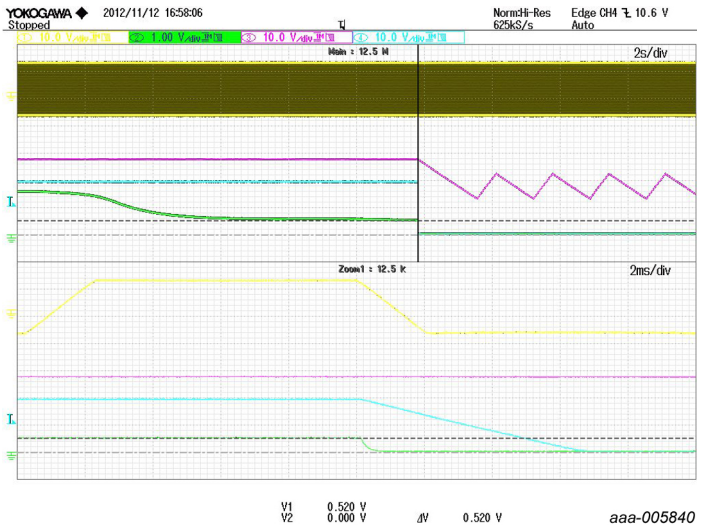
Test conditions

The NTC temperature sensor, glued to the transformer, is heated using hot air.

Criteria to pass

The IC latches off the output at a V_{LATCH} trip level of 0.494 V. No output bounce or hiccup is allowed.

Note: *For this demo board, the NTC is mounted on the heat sink. This place is not the hottest spot of the adapter. It is better to mount the NTC on the transformer.*



(1) OTP trigger temperature 140 °C
(2) Load = 4.62 A before OTP is triggered; Mains input: 230 V/50 Hz
(3) Ch1 (yellow): mains input voltage
(4) Ch2 (green): LATCH pin TEA1755
(5) Ch3 (magenta): VCC pin TEA1755
(6) Ch4 (cyan): output voltage

Figure 12. External overtemperature protection

4.9.7 Fast Latch Reset (FLR)

A fast latch reset function enables latched protection to be reset without discharging the bulk electrolytic capacitor. The latch protection is reset when the voltage on the VINSENSE pin drops below 0.75 V and is then raised to 0.86 V. This voltage variation is done by disconnecting the mains voltage.

Test conditions

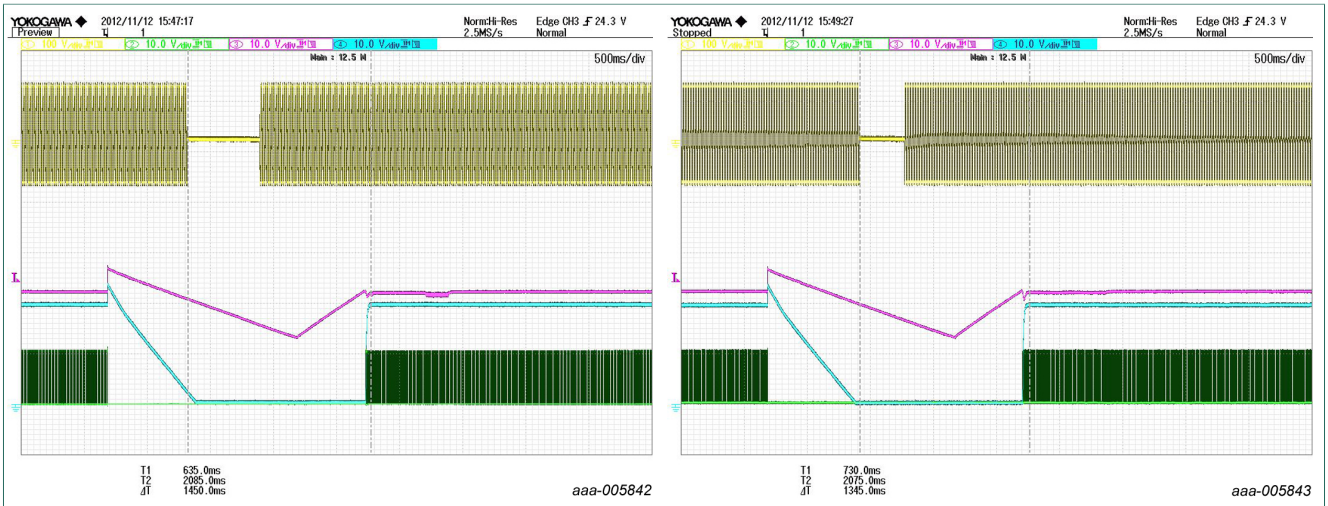
- The output is loaded (I_o = 50 mA)
- The test sequence is as follows:
  - A short circuit across the OPTO-led provides an OVP to trigger the latch protection (see also Section 4.9.5)
  - The mains input is switched off and the voltage on the VINSENSE pin drops below 0.75 V
  - The mains input is switched on and, when the voltage on the VINSENSE pin rises above 0.86 V, the latch protection is released

Note: *Switching of both live and neutral is required.*

Criteria to pass

The latch is reset within 3 s after switching of the mains input voltage.

Figure 13 shows the graphs for Fast Latch Reset (FLR).



a. Mains input 90 V/60 Hz; FLR = 1.5 s

b. Mains input 264 V/50 Hz; FLR = 1.3 s

(1) Ch1 (yellow): mains input voltage
(2) Ch1 (green): FBDRIVER pin TEA1755
(3) Ch2 (magenta): VCC pin TEA1755
(4) Ch3 (cyan): output voltage

Figure 13. Fast latch reset

4.10 Output regulation

4.10.1 Load regulation

The output voltage as a function of load current is measured using a 4-wire current sense configuration at the end of the cable. The minimum current of 15 mA prevents switching to standby mode. Measurements are performed for 90 V/60 Hz and 264 V/50 Hz.

Criteria to pass

The output voltage deviation must be less than 2 %. The load regulation is calculated using Equation 2.

$$\frac{V_{o(max)} - V_{o(min)}}{V_{o(nom)}} \times 100\ \% \quad (2)$$

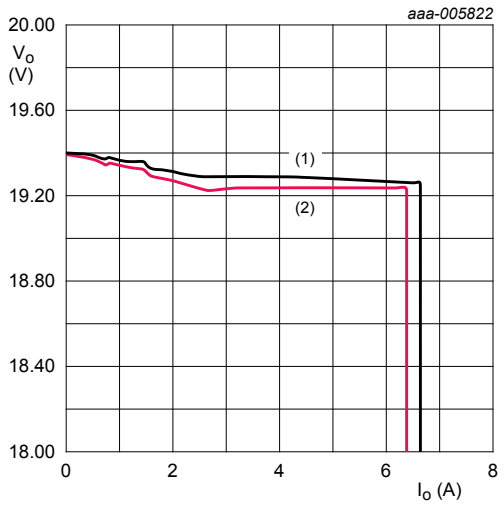
Where:

- $V_{o(nom)}$ = 19.5 V

The results are shown in Table 15.

Table 15. Load regulation

Condition	No load		Full load		Load regulation (%)
	V_o (V)	I_o (A)	V_o (V)	I_o (A)	
90 V/60 Hz	19.40	0.015	19.29	4.62	0.56
264 V/50 Hz	19.40	0.015	19.24	4.62	0.82



(1) 115 V (AC)/60 Hz
(2) 230 V (AC)/50 Hz

Figure 14. Output voltage regulation as a function of load

4.10.2 Line regulation

The output voltage as a function of mains input voltage is measured using a 4-wire current sense configuration at the end of the cable for full-load (4.62 A) condition.

Table 16 and Figure 15 show the results.

Criteria to pass

The output voltage deviation must be less than 0.05 %. The load regulation is calculated using Equation 3.

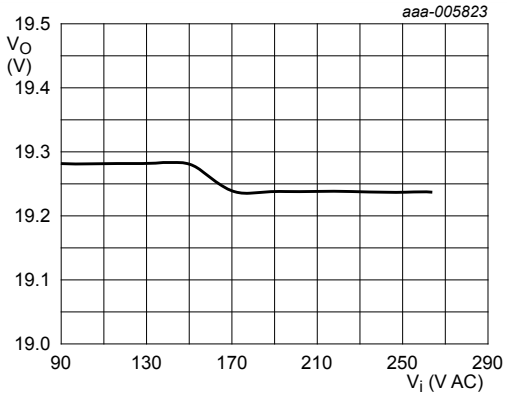
$$\frac{Vo(mainsmin) - Vo(mainsmax)}{Vo(nom)} \times 100\ \% \quad (3)$$

Where:

- $V_{o(nom)}$ = 19.5 V

Table 16. Line regulation

Condition	Full-load	
Mains	**V_o (V)**	**I_o (A)**
90 V/60 Hz	19.28	4.62
100 V/50 Hz	19.28	4.62
115 V/60 Hz	19.28	4.62
230 V/50 Hz	19.24	4.62
264 V/50 Hz	19.24	4.62



(1) Device name: 1

Figure 15. Output voltage as a function of mains voltage

4.10.3 Output voltage regulation in standby mode

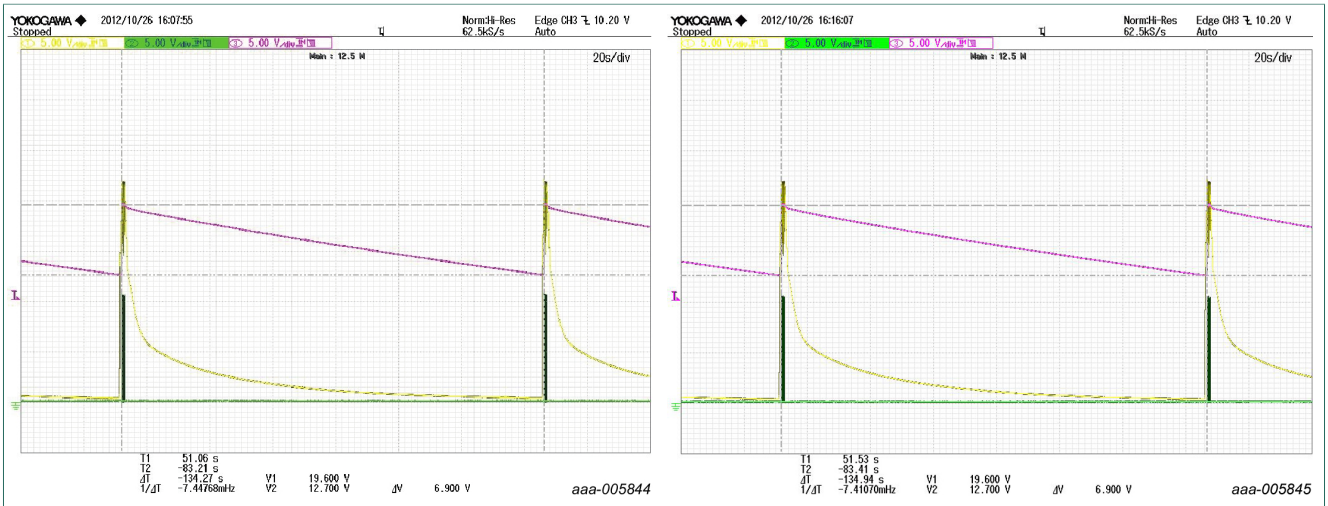
Measurement is only valid for configuration (A).

Table 17 shows the mains input voltages and results for output voltage regulation during no-load operation.

Table 17. Output voltage in standby mode (configuration A)

Condition	V_o maximum (V)	V_o minimum (V)	Repetition rate (s)
90 V/60 Hz	19.6	12.7	134.3
264 V/50 Hz	19.6	12.7	134.9

Figure 16 shows the graphs for output voltage regulation at no-load.



a. Mains input 90 V/60 Hz

b. Mains input 264 V/50 Hz

(1) Ch1 (yellow): VCC pin TEA1755
(2) Ch2 (green): FBDRIVER pin TEA1755
(3) Ch4 (cyan):output voltage

Figure 16. Output voltage regulation at no-load

4.10.4 No-load output ripple in burst mode

This measurement is only valid for demo board configuration (B). The output voltage ripple is measured when the TEA1755 controller is operating in burst mode. The output voltage ripple during no-load operation is measured for 90 V/60 Hz and 264 V/50 Hz (see Table 18).

Table 18. Output voltage in standby mode (configuration B)

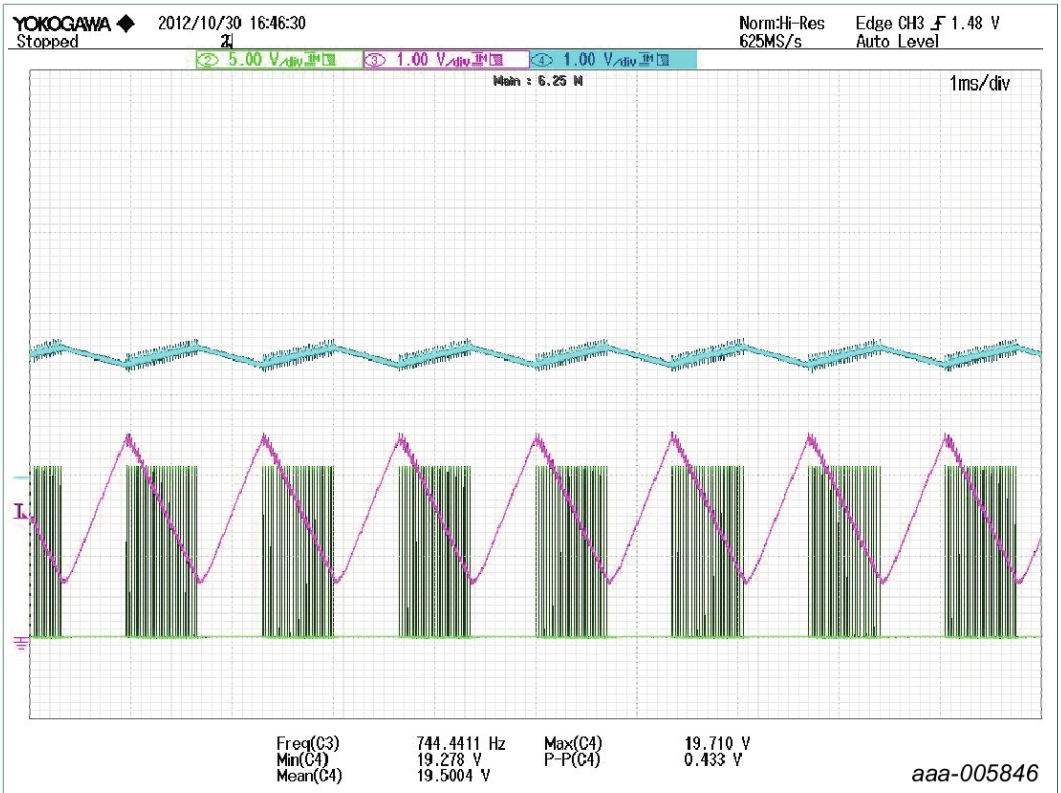
Condition	V_o maximum (V)	V_o minimum (V)	V_{p-p} (mV)	V_{mean} (mV)	Repetition rate (Hz)
90 V/60 Hz	19.6	19.2	363	19.4	5
264 V/50 Hz	19.6	19.3	363	19.4	5

4.10.5 Burst mode repetition rate

Burst repetition rate is measured when the burst on/off duty cycle is 50 %.

Criteria to pass

Burst repetition rate must be lower than 800 Hz to prevent the risk of audible noise.



Ch2 (green): FBDRIVER pin TEA1755
Ch3 (magenta): CTRL pin TEA1755
Ch4 (cyan): V_o

Figure 17. Burst mode repetition rate at 230 V/50 Hz; I_o = 0.45 A

Table 19 shows the mains input voltages and results for burst mode repetition rate and output current.

Table 19. Burst mode repetition rate

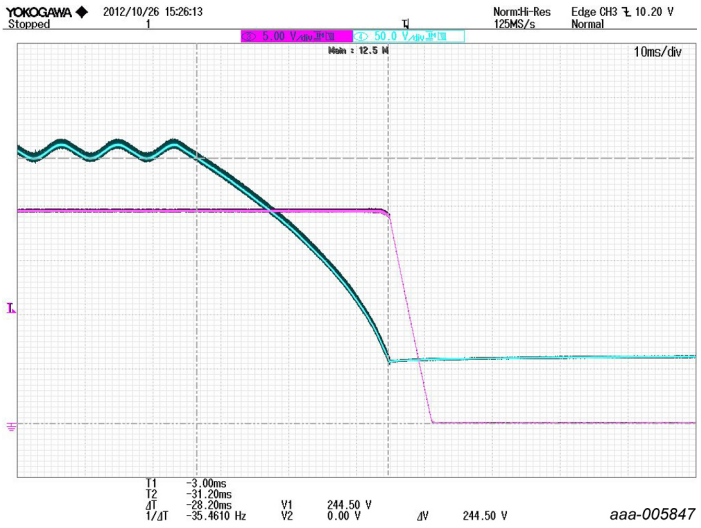
Condition	Burst mode repetition rate (Hz)	Output current for 50 % duty cycle (A)
90 V/60 Hz	776	0.46
115 V/60 Hz	754	0.44
230 V/50 Hz	745	0.43
264 V/50 Hz	749	0.43

4.10.6 Hold-up time

Hold-up time is defined as the time between the following events:

- After mains switch-off
- When the lowest bulk capacitor voltage during a mains cycle is crossed
- When the output voltage starts to drop

The hold-up time at 115 V/60 Hz is 28.2 ms.



(1) Ch3: V_O

(2) Ch4: bulk cap voltage

Figure 18. Full load: Hold-up time at 115 V/60 Hz

4.11 Dynamic loading

Test conditions

- The adapter is subjected to a load change from 0.33 % to 100 % at a slew rate of 2.5 A/µs. The minimum output current of 15 mA (0.33 %) prevents that the device enters standby mode
- The frequency of change is set to give the best readability of the deviation and setting time
- The output voltage is measured at the end of the cable

Criteria to pass

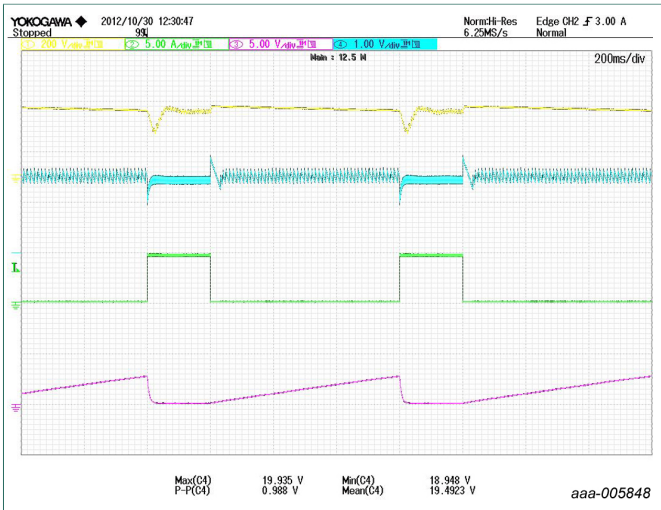
The output voltage must not overshoot or undershoot beyond the specified limits (+1 V and −0.5 V) after a load change.

Figure 19 and Figure 20 show the graphs for dynamic load response.

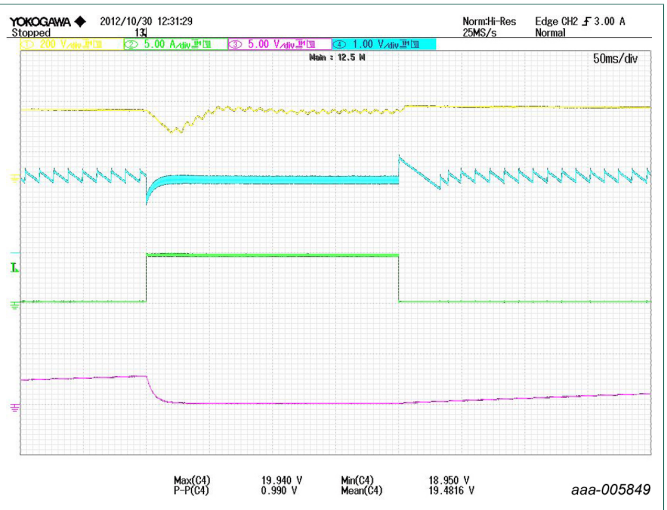
Table 20. Dynamic loading test condition and results

Deviation of the output voltage at a load step from 4.62 A to 0.015 A and from 0.015 A to 4.62 A.

Condition	Loading	$V_{o(max)}$ (V)	$V_{o(min)}$ (V)	Deviation	
				$V_{o(max)} - V_{o(nom)}$ (mV)	$V_{o(nom)} - V_{o(min)}$ (mV)
90 V/47 Hz	I_o: 0.33 % to 100 %; f: 1.25 Hz; duty cycle: 25 %	19.94	18.95	435	552
264 V/63 Hz	I_o: 0.33 % to 100 %; f: 1.25 Hz; duty cycle: 25 %	19.93	18.98	443	520



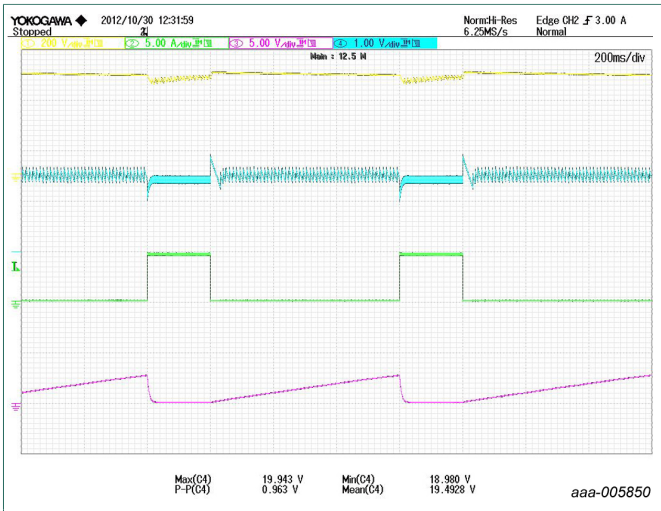
a. Mains input



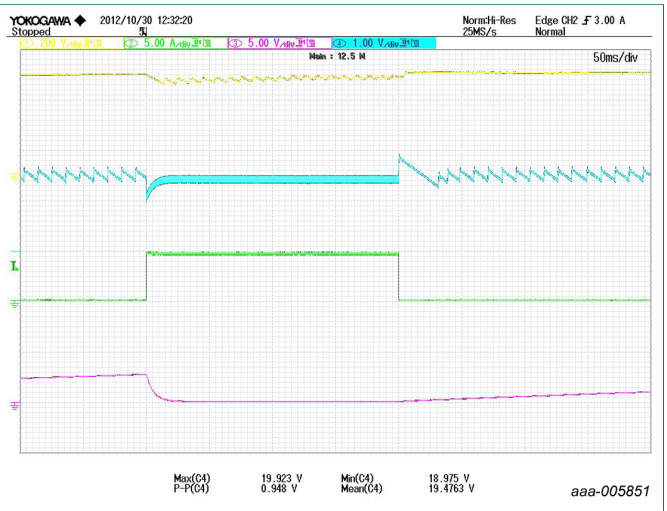
b. Mains input (detailed view)

(1) Ch1 (yellow): PFC bus voltage
(2) Ch2 (green): output current
(3) Ch3 (magenta): PFC timer pin TEA1755
(4) Ch4 (cyan):output voltage

Figure 19. Dynamic load response 90 V/60 Hz



a. Mains input 264 V/50 Hz



b. Mains input 264 V/50 Hz (detailed view)

(1) Ch1 (yellow): PFC bus voltage
(2) Ch2 (green): output current
(3) Ch3 (magenta): PFC timer pin TEA1755
(4) Ch4 (cyan):output voltage

Figure 20. Dynamic load response 264 V/50 Hz

4.12 Output ripple and noise

Test conditions

Output ripple and noise are defined as periodic or random signals over a frequency band of 10 Hz to 20 MHz.

Output ripple and noise are measured at the end of the cable using the measurement set-up shown in Figure 21. An oscilloscope probe is connected to the end of the adapter cable using a probe tip.

100 nF and 1 µF capacitors are added between plus and minus to reduce high-frequency noise. The input channel bandwidth of the oscilloscope is limited to 20 MHz.

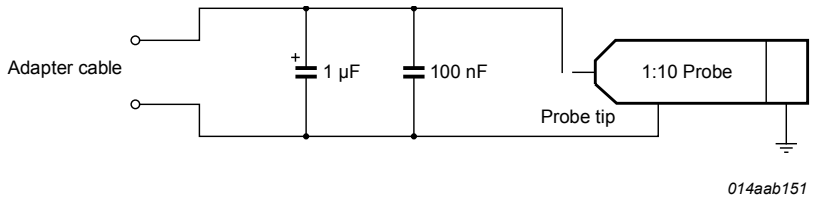


Figure 21. Output ripple and noise measurement setup

Criteria to pass

The output ripple and noise must remain within the specified limits 100 mV (peak-to-peak) for the full load (4.62 A) condition.

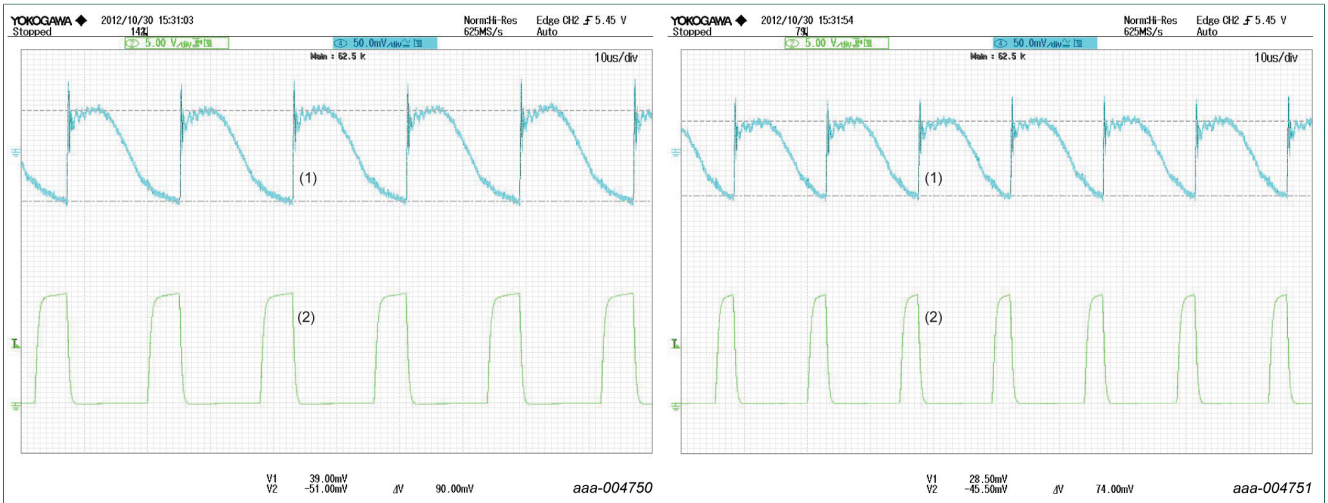
Table 21 shows the measurement results for a selection of mains input voltages.

Table 21. Output ripple and noise measurements

Ripple and noise (at maximum load) as a function of the mains input voltage

Condition	$V_{o(ripple)(p-p)}$ (mV)
90 V/47 Hz	90
100 V/50 Hz	79
115 V/60 Hz	79
230 V/50 Hz	74
264 V/63 Hz	74

Figure 22 shows the graphs for output ripple and noise.



a. Mains input 90 V/60 Hz

b. Mains input 264 V/50 Hz

(1) Ch4 (cyan): output voltage (AC coupled)

(2) Ch2 (green): FBDRIVER pin TEA1755

Figure 22. Output ripple and noise

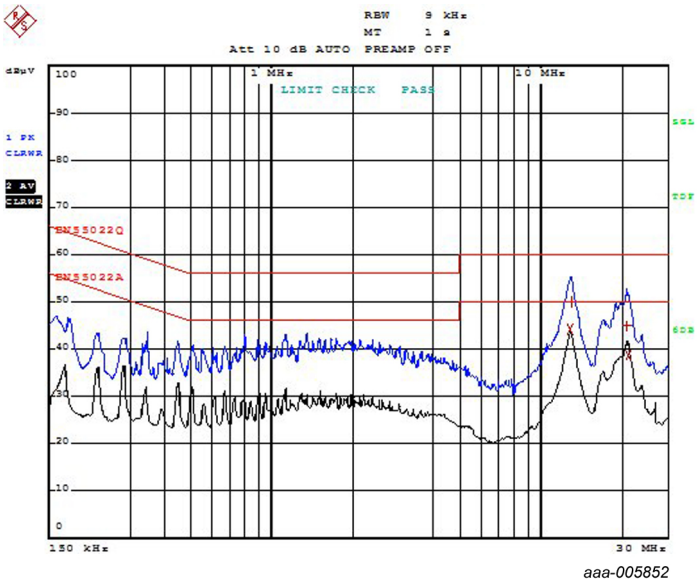
5 ElectroMagnetic Compatibility (EMC)

5.1 Conduction emission

5.1.1 Conditions

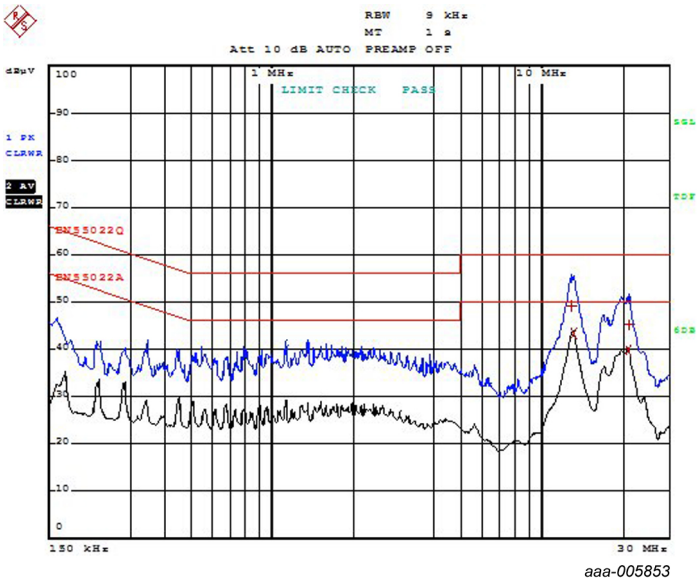
- Type: Conducted Electromagnetic Compatibility (EMC) measurement
- Frequency range: 150 kHz to 30 MHz
- Output power: full load condition
- Supply voltage: 115 V and 230 V
- Margin: 6 dB below limit
- Secondary ground connected to earth ground
- Measurements performed by NXP Semiconductors Nijmegen (The Netherlands)

In the graphs shown in Figure 23 and Figure 24, the blue line is the quasi-peak measurement result and the black line is the average measurement result.



aaa-005852

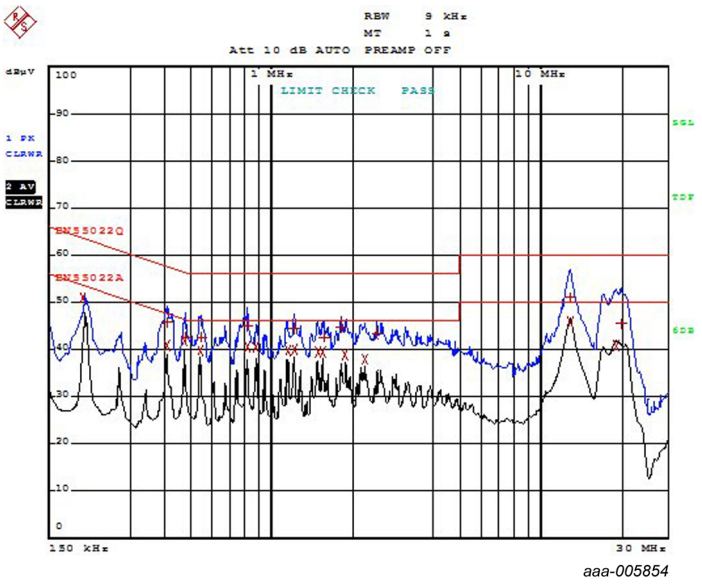
a. Phase N



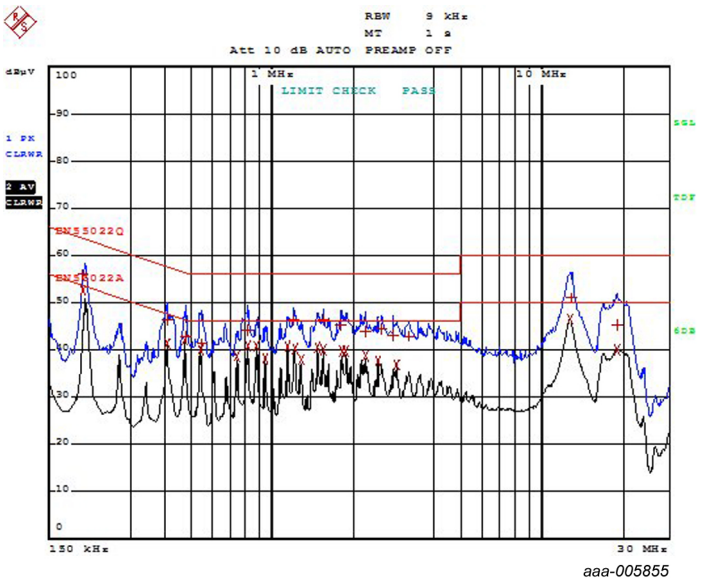
aaa-005853

b. Phase L

Figure 23. Conduction emission 115 V



a. Phase N



b. Phase L

Figure 24. Conduction emission 230 V

5.2 Immunity against lighting surges

Test conditions

- Combination wave: 1.2/50 µs open-circuit voltage and 8/20 µs short circuit current
- Test voltage: 2 kV
- L1 to L2: 2 Ω; L1 to PE, L2 to PE and L1 + L2 to PE: 12 Ω
- Phase angle: 0°, 90°, 180° and 270°
- Number of tests: 5 positive and 5 negative
- Pulse repetition rate: 20 s

Test result

There is no disruption of functionality.

5.3 Mains harmonic reduction

Test conditions

- The adapter is set to the maximum continuous load of 4.62 A
- The input voltage is 230 V/50 Hz

Criteria to pass

Compliance with EN61000-3-2 A14 class D.

Test result

Passed, see Table 22.

Table 22. MHR according to EN61000-3-2 A14, class D

Harmonic nr.	Measured (mA)	Limit (mA)	Harmonic nr.	Measured (mA)	Limit (mA)
1	427.7	-	21	9.6	20.1
3	149.7	338.1	23	2.6	18.2
5	21.3	189	25	1.4	16.7
7	8.1	99.4	27	6.5	15.3
9	14.0	49.7	29	7.1	14.2
11	6.6	34.8	31	1.9	13.2
13	5.5	34.8	33	2.8	12.4
15	3.9	29.5	35	4.0	11.6
17	3.0	25.5	37	1.7	10.9
19	2.1	22.5	39	2.0	10.3

6 Schematic TEA1755DB1100 demo board

Figure 25 shows the schematic for configuration A.

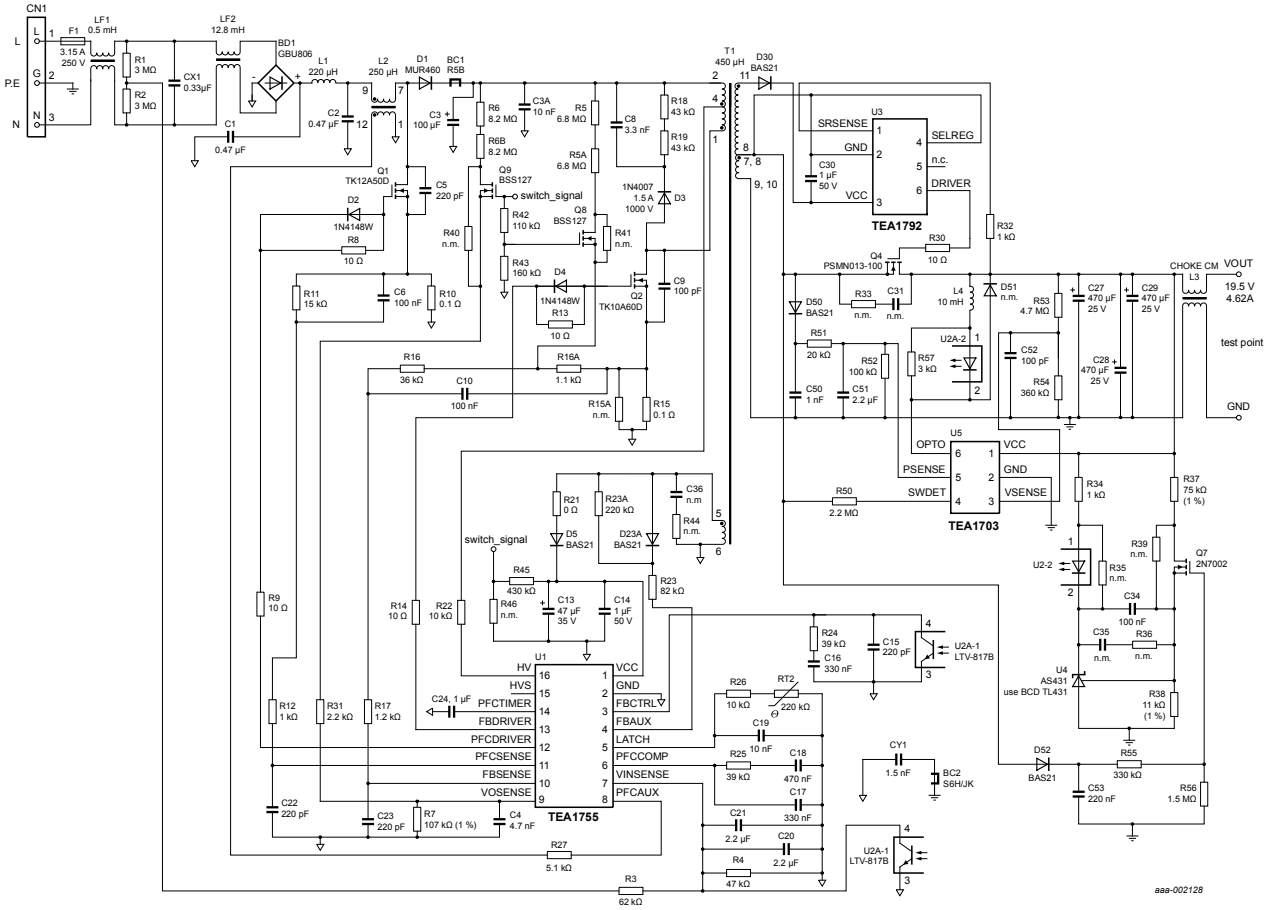


Figure 25. Schematic: TEA1755DB1100 demo board (configuration A)

Figure 26 shows the schematic for configuration B.

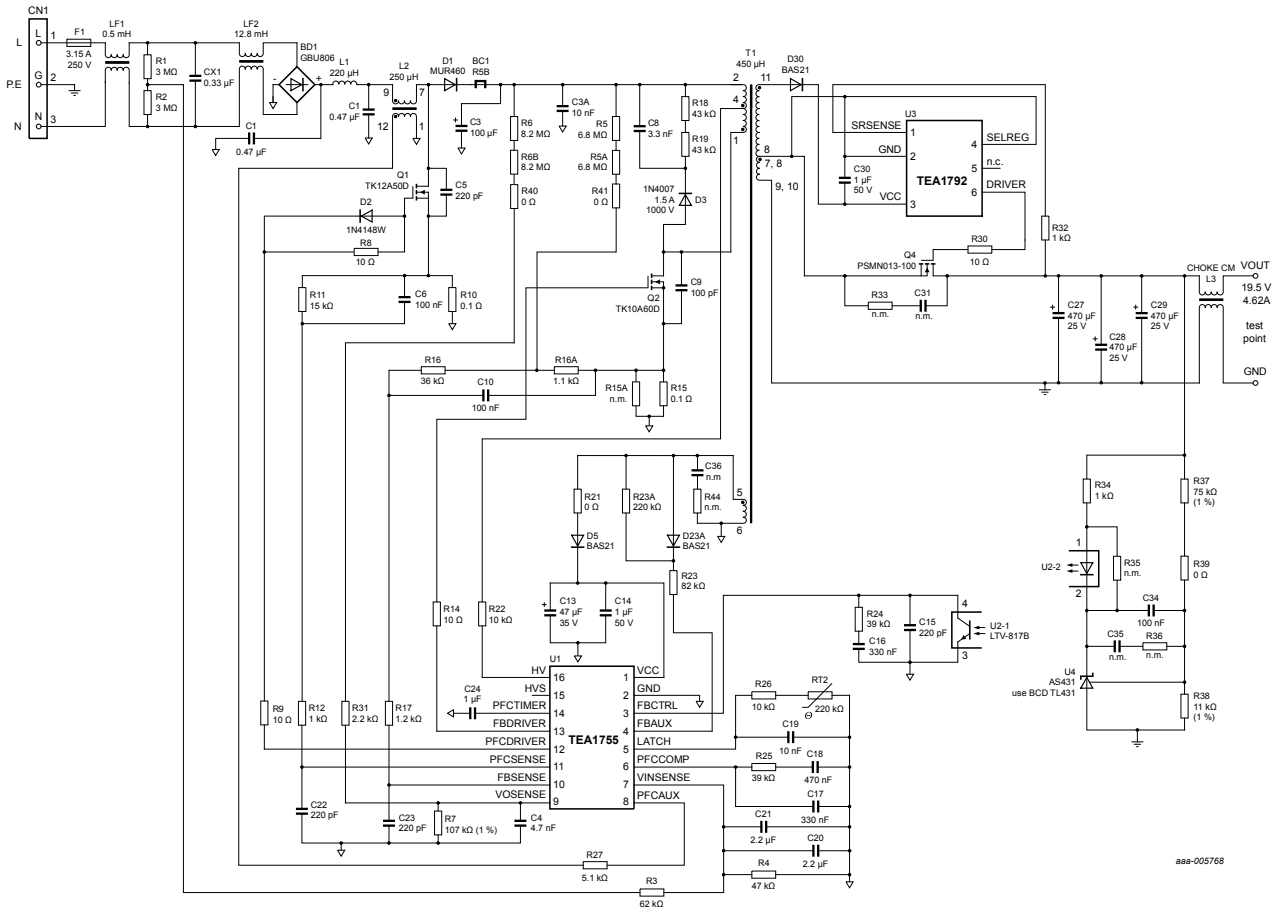


Figure 26. Schematic: TEA1755DB1100 demo board (configuration B)

7 Bill of Materials (BOM)

Table 23. TEA1755DB1100 demo board BOM

Reference	Description and values	Part number/ package	Manufacturer	Board version
BC1	bead; core; RH 4 × 6 × 2, R5B (King Core)/XP; for D1	N4/AMAX	-	A and B
BC2	bead; core; RH 3.5 × 4.2 × 1.3; S6H/JK; for CY1	N6/AMAX	-	A and B
BD1	bridge diode; Flat/Mini; 8 A; 600 V	GBU806	Lite-On	A and B
cable	cable; 16AWG/1571; 2.5 × 5.5 × 12 (kk, fk); L = 1200 mm	-	-	A and B
C1	capacitor; film; axial lead; 0.47 µF; 450 V; P = 10 mm	MFTD/HJC	-	A and B
C2	capacitor; film; axial lead; 0.47 µF; 450 V; P = 10 mm	MFTD/HJC	-	A and B
C3	capacitor; electric; radial lead; 100 µF; 400 V; 105 °C; 16 × 30 mm	KMG/NCCC	-	A and B
C3A	capacitor; ceramic, disc, D = 11.5; 10000 pF; 1 KV	Z5U	-	A and B
C4	capacitor; MLCC; 4700 pF; 50 V; X7R	SMD 0603	-	A and B
C5	capacitor; MLCC; 220 pF; 630 V; NPO	SMD 1206	-	A and B
C6	capacitor; MLCC; 0.1 µF; 50 V; X7R	SMD 0603	-	A and B
C8	capacitor; MLCC; 3300 pF; 630 V; X7R	SMD 1206	-	A and B
C9	capacitor; MLCC; 100 pF; 630 V; NPO	SMD 1206	-	A and B
C10; C34	capacitor; MLCC; 0.1 µF; 50 V; X7R	SMD 0603	-	A and B
C13	capacitor; electric; radial lead; 5 × 11 mm; 47 µF; 35 V; 105 °C	-	ZLH Rubycon	A and B
C14; C30	capacitor; MLCC; 1 µF; 50 V; Y5V	SMD 0805	-	A and B
C15	capacitor; MLCC; 220 pF; 50 V; X7R	SMD 0603	-	A and B
C16; C17	capacitor; MLCC; 0.33 µF; 16 V; X7R	SMD 0603	-	A and B
C18	capacitor; MLCC; 0.47 µF; 16 V; X7R	SMD 0603	-	A and B
C19	capacitor; MLCC; 0.01 µF; 50 V; X7R	SMD 0603	-	A and B
C20; C21	capacitor; MLCC; 2.2 µF; 10 V; X7R	SMD 0603	-	A and B
C22; C23	capacitor; MLCC; 220 pF; 50 V; X7R	SMD 0603	-	A and B
C24	capacitor; MLCC; 1 µF; 50 V; X7R	SMD 0805	-	A and B
C27; C28; C29	capacitor; electric; radial lead; 10 × 12.5 mm; 470 µF; 25 V; 105 °C	-	KZH/NCC	A and B
C35	capacitor; not mounted	SMD 0805	-	-
C36	capacitor; not mounted	SMD 0805	-	-
C50	capacitor; MLCC; 1 nF; 50 V; X7R	SMD 0603	-	A
C51	capacitor; MLCC; 2.2 µF; 10 V; X7R	SMD 0805	-	A

Reference	Description and values	Part number/ package	Manufacturer	Board version
C52	capacitor; MLCC; 100 pF; 50 V; NPO	SMD 0603	-	A
C53	capacitor; MLCC; 0.22 µF; 10 V; X7R	SMD 0603	-	A
CX1	capacitor; X2 cap; axial lead; 0.33 µF; 275 V	MKP/R46	KEMET	A and B
CY1	capacitor; ceramic; D = 8.5; Y1 cap; 1500 pF; 400 V	-	CD/TDK	A and B
D1	diode; ultra fast; axial lead; DO-201AD; 4 A; 600 V	MUR460	Vishay	A and B
D2; D4	diode; switching; SMD; 0.15 A; 75 V	1N4148W; SOD-123	Diodes	A and B
D3	diode; general purpose; SMB; 1.5 A; 1000 V	S2M	Lite-On	A and B
D5; D23A	diode; ultra fast; SMD; 0.2 A; 250 V	BAS21; SOD-123	NXP Semiconductors	A and B
D30	diode; ultra fast; SMD; 0.2 A; 250 V	BAS21; SOD-123	NXP Semiconductors	A and B
D50	diode; ultra fast; SMD; 0.2 A; 250 V	BAS21; SOD-123	NXP Semiconductors	A
D52	diode; ultra fast; SMD; 0.2 A; 250 V	BAS21; SOD-123	NXP Semiconductors	A
F1	fuse; axial lead; time-lag; T 3.15 A; 250 V	LT-5	Littelfuse	A and B
heat sink for Q1, Q2, BD1	I-Shape; 109 × 25 mm; t = 3 mm; Cu-tinned; WD	-	-	A and B
Heat sink for Q4	I-Shape; 90 × 25 mm; t = 3 mm; Cu-tinned; WD	-	-	A and B
Inlet	Inlet; S3P	TU-333-BZ-315-P3D	TECX	A and B
J1; J2	jumper wire; D = 0.6 taping	-	-	A and B
J3; J4	jumper wire; D = 0.6 × 27.5 mm with PVC	-	-	A and B
J5	jumper wire; D = 0.6 × 20 mm with PVC	-	-	A and B
J7	jumper wire; D = 0.6 × 12.5 mm with PVC	-	-	A and B
LF1	inductor; choke; T12*6*4C A10/R10K; 10T; minimum 380 µH	LF-TR120-001R	BELTA	A and B
LF2	inductor; line choke; T16*12*8C A10/R10K; 56 Ts; minimum 7 mH	TF-TR160-002R	BELTA	A and B
L1	inductor; choke; T50-52/KST50-52; 80 Ts; 211 µH	LI-TR050-214R	BELTA	A and B
L2	inductor; PFC choke; RM-10; 40:2; 250 µH	SP08Z187; TF-RM100-213R	SENDPOWER; BELTA	A and B
L3	inductor; choke; T10 x 6 x 5C A10/R10K; 8 Ts; minimum 140 µH	TF-TR100-202R	BELTA	A and B

Reference	Description and values	Part number/ package	Manufacturer	Board version
L4	inductor; choke; 10 mH; 0.5 W	ZAL-0410-101K	ZenithTek	A
Nut For Q1, Q2, Q4	nut; HEX/GW; M3; NI Shouh Pin; LF	-	-	A and B
PCB	single side; CEM-1; 2-OZ; 125.5 × 59 × 1.6 mm	APBADC052	-	A and B
Q1	transistor; n-channel MOSFET; 0.45 Ω; 500 V; 12 A; 15p-typ	TK12A50D; TO-220F	Toshiba	A and B
Q2	transistor; n-channel MOSFET; 0.58 Ω; 600 V; 10 A; 15p-typ	TK10A60D; TO-220F	Toshiba	A and B
Q4	transistor; n-channel MOSFET; 13.9 Ω; 100 V; 67 A; 220p-typ	PSMN013-100PS; TO-220F	NXP Semiconductors	A and B
Q7	transistor; n-channel MOSFET; 60 V; 18 A	2N7002; SOT-23	NXP Semiconductors	A
Q8	transistor; n-channel MOSFET; 600 V; 0.023 A	BSS127; SOT-23	Infineon	A
Q9	transistor; n-channel MOSFET; 600 V; 0.023 A	BSS127; SOT-23	Infineon	A
R1; R2	resistor; thin film chip; 3 MΩ; 1 %	SMD 1206	-	A and B
R3	resistor; thin film chip; 62 kΩ; 1 %	SMD 1206	-	A and B
R4	resistor; thin film chip; 47 kΩ; 5 %	SMD 0603	-	A and B
R5; R5A	resistor; thin film chip; 6.8 MΩ; 1 %	SMD 1206	-	A and B
R6; R6B	resistor; thin film chip; 8.2 MΩ; 1 %	SMD 1206	-	A and B
R7	resistor; thin film chip; 107 kΩ; 1 %	SMD 0603	-	A and B
R8; R9; R13; R14; R30	resistor; thin film chip; 10 Ω; 5 %	SMD 0805	-	A and B
R10; R15	resistor; axial lead; MOF; 0.1 Ω; 1 W (S); 5 %	-	-	A and B
R11	resistor; thin film chip; 15 kΩ; 5 %	SMD 0603	-	A and B
R12; R32	resistor; thin film chip; 1 kΩ; 5 %	SMD 0805	-	A and B
R16	resistor; thin film chip; 36 kΩ; 5 %	SMD 0603	-	A and B
R16A	resistor; thin film chip; 1.1 kΩ; 5 %	SMD 0603	-	A and B
R17	resistor; thin film chip; 1.2 kΩ; 5 %	SMD 0603	-	A and B
R18; R19	resistor; thin film chip; 43 kΩ; 1 %	SMD 1206	-	A and B
R21	resistor; thin film chip; 0 Ω; 5 %	SMD 0603	-	A and B
R22; R26	resistor; thin film chip; 10 kΩ; 5 %	SMD 0603	-	A and B
R23	resistor; thin film chip; 82 kΩ; 1 %	SMD 0603	-	A and B
R23A	resistor; thin film chip; 220 kΩ; 1 %	SMD 0603	-	A and B
R24; R25	resistor; thin film chip; 39 kΩ; 5 %	SMD 0603	-	A and B
R27	resistor; thin film chip; 5.1 kΩ; 5 %	SMD 1206	-	A and B
R31	resistor; thin film chip; 2.2 kΩ; 5 %	SMD 0603	-	A and B

Reference	Description and values	Part number/ package	Manufacturer	Board version
R35; R36	resistor; not mounted	SMD 0603	-	-
R37	resistor; thin film chip; 75 kΩ; 1 %	SMD 0603	-	A and B
R38	resistor; thin film chip; 11 kΩ; 1 %	SMD 0603	-	A and B
R39; R40; R41	resistor; thin film chip; 0 Ω; 5 %	SMD 0805	-	B
R42	resistor; thin film chip; 110 kΩ; 5 %	SMD 0603	-	A
R43	resistor; thin film chip; 160 kΩ; 5 %	SMD 0603	-	A
R44; R46	resistor; not mounted	SMD 0805	-	-
R45	resistor; thin film chip; 430 kΩ; 5 %	SMD 0603	-	A
R50	resistor; thin film chip; 2.2 MΩ; 5 %	SMD 0603	-	A
R51	resistor; thin film chip; 20 kΩ; 1 %	SMD 0603	-	A
R52	resistor; thin film chip; 100 kΩ; 1 %	SMD 0603	-	A
R53	resistor; thin film chip; 4.7 MΩ; 1 %	SMD 0603	-	A
R54; R55	resistor; thin film chip; 360 kΩ; 1 %	SMD 0603	-	A
R56	resistor; thin film chip; 1.5 MΩ; 5 %	SMD 0603	-	A
R57	resistor; thin film chip; 3 kΩ; 5 %	SMD 0603	-	A
RJ1; RJ2; RJ3; RJ4; RJ5	resistor; thin film chip; 0 Ω; 5 %	SMD 0603	-	A and B
RT2	resistor; NTC; axial lead; D = 5; 220 kΩ; 5 %	TTC05104	Thinking Electronic Industrial Co., LTD	A and B
screw for BD1, Q1, Q2, Q4	screw; M3 × 8; flat head 5.0; NI Shouh pin	-	-	A and B
T1	transformer; PQ-3220; 450 µH	SP08Z142 TF-PQ320-290R	SENDPOWER BELTA	A and B
Tube for LF2	heat shrink tube; 20 D × 20 mm	-	Fujikura, Sumitomo/LC	A and B
Tube for RT2	silicone tube; 1 D × 15 mm	-	A(Kurabe)/LC	A and B
U1	GreenChip SMPS control IC	TEA1755T; SO-16	NXP Semiconductors	A and B
U2	IC optocoupler; CTR = 130 % to 260 %	LTV-817B	Lite-On	A and B
U2A	IC optocoupler; CTR = 130 % to 260 %	LTV-817B	Lite-On	A
U3	IC synchronous rectifier controller	TEA1792TS; TSOP-6	NXP Semiconductors	A and B
U4	IC adjustable precision shunt regulator	AS431I – ANTR-GL; SOT-23	BCD	A and B
U5	IC; SMPS standby control	TEA1703TS; TSOP-6	NXP Semiconductors	A

8 Transformer specifications

8.1 Flyback transformer (T1)

8.1.1 Flyback transformer T1 specification

Table 24. Electrical characteristics

Item	Winding	Specification
Inductance	P1-2	450 µH; ±5 %; 50 kHz; 1 V
Leakage Inductance	P1-2	6 µH maximum
DC Resistance	P1-2	maximum 300 mΩ at 25 °C
High-voltage test	PRI to SEC	3000 V; 3 s; 5 mA
	PRI to CORE	1500 V; 3 s; 5 mA
	SEC to CORE	600 V; 3 s; 5 mA

Table 25. Material specifications

Item	Description	Manufacturer
Core	FERRITE Mn-Zn PQ32/20	JFE
Bobbin	PQ32/20 12P PHENOLIC	CHANG CHUN
Tape	#1350F1	3M
Wire	2UEW; 130 °C TIW TLW-B × 130 °C	JUNG SHING DAHJIN
Cu foil	0.025 mm thickness × 7 mm width	EXCELLENCE
Tube	PTFE (TFLON)	GREAT HOLDING
Varnish	BC-359	DOLPH
Tin	D9930C/SN100	DAI HYUI

Manufacturers:

- Axis Power Electronics, Taiwan (http://www.axispower.com.tw)
- Shenzhen Belta Electronics Co., Ltd. (http://www.belta.cn)

Figure 27 shows the schematic for the flyback transformer. Figure 28 shows its dimensions. Figure 29 shows its winding structure and order.

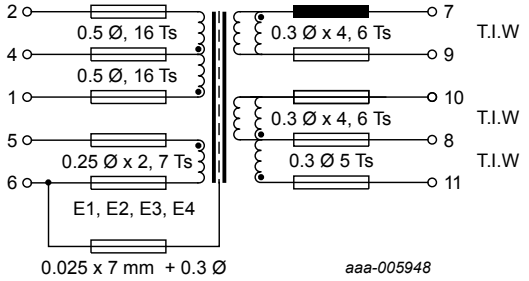


Figure 27. Flyback transformer schematic

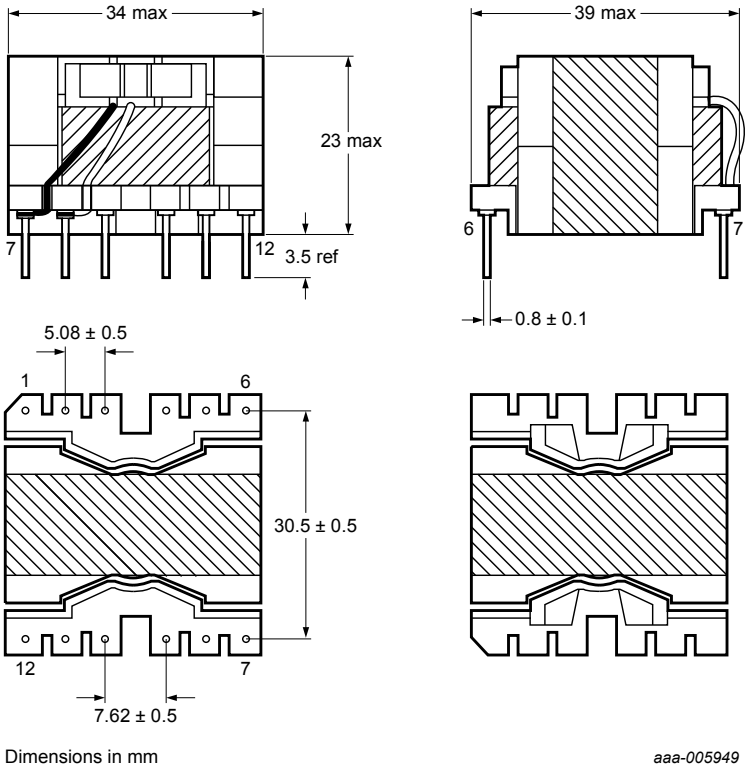


Figure 28. Flyback transformer dimensions

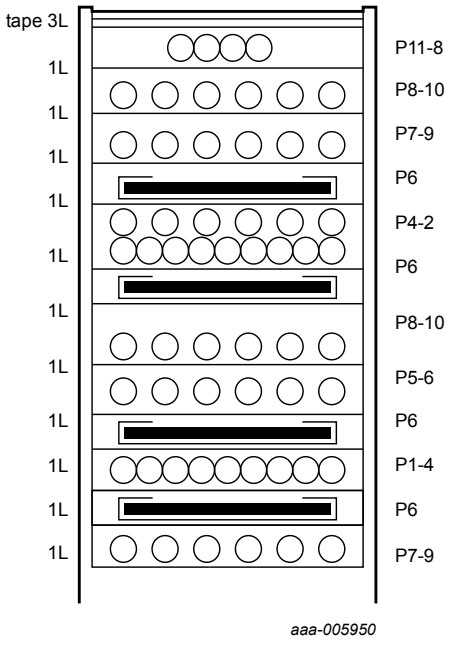


Figure 29. Flyback transformer winding structure and order

8.1.2 Flyback transformer T1 winding specifications

Table 26. Winding specifications

Winding order	Pin number		Wire type	Number of wires	Number of turns		Remarks
	Start	Finish			Winding	Mylar tape	
N1	7	9	TIW 0.3 Ø	2	6	1	-
E1	-	6	Copper foil 0.025 T × 7 mm	-	1	1	finished with wire 0.3 Ø
N2	1	4	2UEW 0.5 Ø	1	16	1	-
E2	-	6	Copper foil 0.025 T × 7 mm	-	1	1	finished with wire 0.3 Ø
N3	5	6	2UEW 0.25 Ø	2	7	1	-
N4	8	10	TIW 0.3 Ø	2	6	1	-
E3	-	6	Copper foil 0.025 T × 7 mm	-	1	1	finished with wire 0.3 Ø
N5	4	2	2UEW 0.5 Ø	1	16	1	-
E4	-	6	Copper foil 0.025 T × 7 mm	-	1	1	finished with wire 0.3 Ø
N6	7	9	TIW 0.3 Ø	2	6	1	-
N7	8	10	TIW 0.3 Ø	2	6	1	-
N8	11	8	TIW 0.3 Ø	1	5	1	-

8.2 PFC inductor (L2)

8.2.1 PFC inductor L2 Specification

Table 27. Electrical characteristics

Item	Winding	Specification
Inductance	P9-7	250 µH; ±10 %; 50 kHz; 1 V
DC Resistance	P9-7	maximum 170 mΩ at 25 °C
	P12-1	maximum 55 mΩ at 25 °C

Table 28. Material specification

Item	Description	Manufacturer
Core	FERRITE Mn-Zn PQ32/20	JFE
Bobbin	RM10 PHENOLIC	CHANG CHUN
Tape	#1350F1	3M
Wire	2UEW; 130 °C	JUNG SHING DAHJIN
Cu foil	0.05 mm thickness × 14 mm width	SCHLENK
Tube	PTFE (TFLON)	GREAT HOLDING
Varnish	BC-359	DOLPH

Item	Description	Manufacturer
Tin	D99300C/SN100	DYFENCO

Manufacturers:

- Axis Power Electronics, Taiwan (http://www.axispower.com.tw)
- Shenzhen Belta Electronics Co., Ltd. (http://www.belta.cn)

Figure 30 shows the schematic for the PFC inductor. Figure 31 shows its dimensions. Figure 32 shows its winding structure and order.

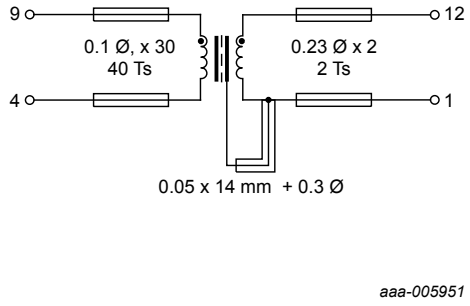


Figure 30. PFC inductor schematic

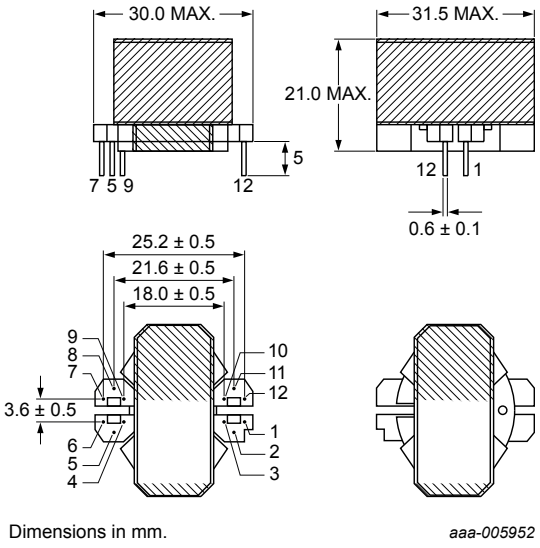


Figure 31. PFC inductor dimensions

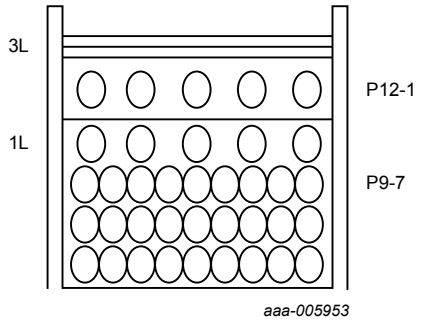


Figure 32. PFC inductor winding structure and order

8.2.2 PFC inductor L2 winding specifications

Table 29. Winding specifications

Winding order	Pin number		Wire type	Number of wires	Number of turns		Remarks
	Start	Finish			Winding	Mylar tape	
N1	9	7	2UEW 0.1 Ø	30	40	1	-
N2	12	1	2UEW 0.23 Ø	2	2	3	-

9 90 W TEA1755DB1100 demo board layout

The SMPS printed-circuit board is a single-sided board. The dimensions are 125 mm × 59 mm. The PCBs material is 1.6 mm FR2 with a single-sided 2 oz. copper (70 µm) layer. The Gerber file set for production of the PCB is available on the NXP website (www.nxp.com) or through the local NXP Semiconductors sales office.

Figure 33 shows the copper layout. Figure 34 the component placing of the demo board.

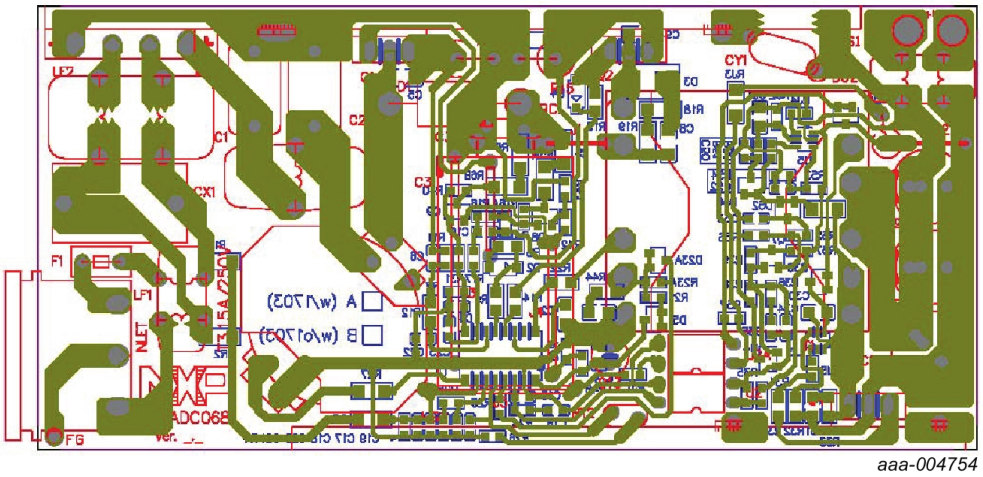
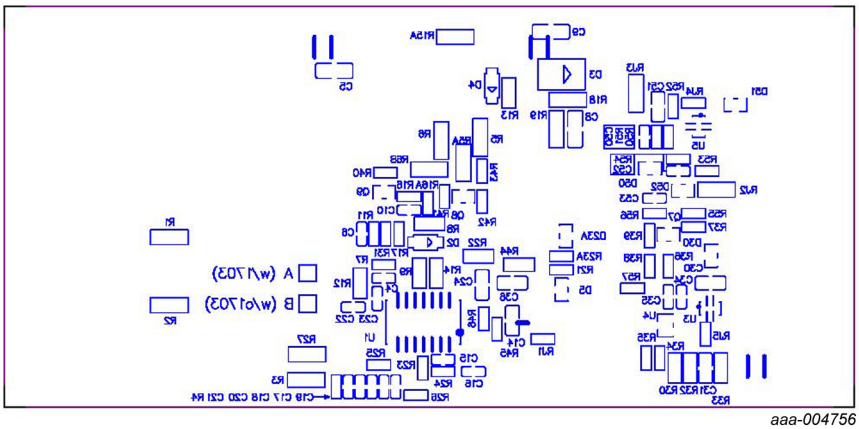


Figure 33. TEA1755DB1100 demo board copper layout bottom side (top view)



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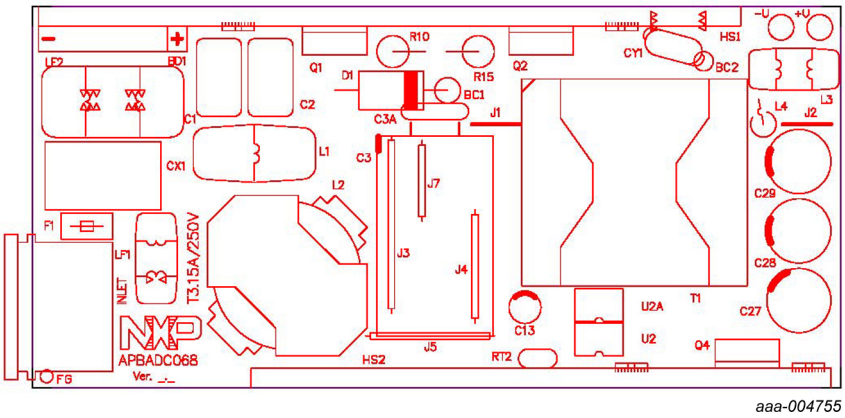
a. Bottom side (top view)



aaa-004755

b. Top side (top view)

Figure 34. TEA1755DB1100 demo board component placing

10 Alternative circuit options

10.1 Changing the output voltage

By changing the following components, the output voltage can be changed (±30 %). For more information on this topic, see the TEA1755T/LT application note. Ensure that the auxiliary voltage remains within its operation limits (13.4 V to 38 V typical) and it is high enough to start up (22.3 V typical).

R37/R38

The resistor divider R37 and R38 determines the output voltage. The total value of the two resistors is a compromise between no-load standby power dissipation and V_o accuracy. For configuration (A), there is no such compromise. The TEA1703 switches off the resistor divider in no-load standby mode.

- Higher value (R37 + R38): Power no-load standby power dissipation plus more tolerance on V_o
- Higher value (R37 + R38): Higher no-load standby power dissipation plus less tolerance on V_o

$$V_o = 2.5\ V \times \frac{(R37+R38)}{R38} \quad (4)$$

C27, C28, C29

The voltage rating of the electrolytic capacitor must be higher than the output voltage. For lower output currents, the capacity can be decreased.

10.2 TL431 selection

The selection of the TL431 is critical for the following performance parameters:

- Output voltage regulation
- No-load standby power consumption
- Stability of the control loop
- Start-up profile of the output voltage

The minimum cathode current for regulation must be met under all conditions. When at full-load, the current through the TL431 becomes too low and results in a drop of the output voltage at full-load. This current can be increased by changing R35 = 5.6 kΩ or by changing the TL431 for a type that requires a lower minimum cathode current for regulation.

10.3 VOSENSE pin resistors values

The VOSENSE pin senses the PFC output voltage. The VOSENSE pin has an integrated protection circuit to detect an open and short-circuited pin. The VOSENSE pin can also sense if one of the resistors of the voltage divider is open.

Based on calculations, the value of R7 must be less than 104.4 kΩ to guarantee the correct working of these protections. Selecting a too large value for R7 can override PFC open-loop protection when the current path to the bulk electrolytic capacitor C3 is lost (fault condition).

For more information about this subject, see the application note of the TEA1755 (AN11142, Section 4.1.1).

11 Abbreviations

Table 30. Abbreviations

Acronym	Description
CC	Constant Current
EMC	ElectroMagnetic Compatibility
FLR	Fast Latch Reset
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NTC	Negative Temperature Coefficient (?)
OCP	OverCurrent Protection
OPP	OverPower Protection
OTP	OverTemperature Protection
OVP	OverVoltage Protection
PCB	Printed-Circuit Board
PFC	Power Factor Correction (?)
SCP	Short Circuit Protection
SMPS	Switched Mode Power Supplies
SR	Synchronous Rectification

12 References

1 **TEA1755T data sheet** HV start-up DCM/QR flyback controller with integrated DCM/QR PFC controller; 2013, NXP Semiconductors

2 **TEA1792TS data sheet** GreenChip synchronous rectifier controller; 2014, NXP Semiconductors

3 **TEA1703TS data sheet** GreenChip SMPS standby control IC; 2012, NXP Semiconductors

4 **AN11142 application note** GreenChip TEA1755 integrated PFC and flyback controller; 2016, NXP Semiconductors

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