UM11024

TEA1998DB1453 synchronous rectifier controller demo board

Rev. 1 — 25 July 2016 **User manual**

Document information

Information	Content
Keywords	TEA1998DB1453, TEA1998TS, flyback converter, Synchronous Rectifier (SR) driver, TSOP-6, high efficiency, power supply, demo board
Abstract	This user manual describes the TEA1998DB1453 demo board. The TEA1998DB1453 demo board can be connected to a flyback converter. The TEA1998DB1453 demo board contains a TEA1998TS SR controller in a TSOP-6 package. Additionally, the TEA1998DB1453 demo board contains two possible options to place power MOSFETs. It replaces the secondary rectification part of the flyback converter.

Table 1. Revision history

Rev	Date	Description
v.1	20160725	first issue

1 Introduction

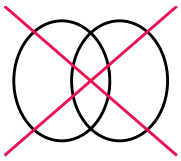
Warning	
 	The non-insulated high voltages that are present when operating this product, constitute a risk of electric shock, personal injury, death and/or ignition of fire. This product is intended for evaluation purposes only. It shall be operated in a designated test area by personnel qualified according to local requirements and labor laws to work with non-insulated mains voltages and high-voltage circuits. This product shall never be operated unattended.

This document describes the TEA1998DB1453 demo board. A functional description is provided, including instructions about how to connect the board, for the best results and performance. The TEA1998DB1453 demo board contains the secondary part of a single output flyback converter, excluding the output capacitors and the feedback control hardware. To use the TEA1998DB1453 demo board correctly, a flyback converter board in which the demo board can replace the secondary rectifier part is required.

2 Safety warning

The board application is AC mains voltage powered. Avoid touching the board while it is connected to the mains voltage and when it is in operation. An isolated housing is obligatory when used in uncontrolled, non-laboratory environments. Galvanic isolation from the mains phase using a fixed or variable transformer is always recommended. Figure 1 shows the symbols on how to recognize these devices.

a. Isolated

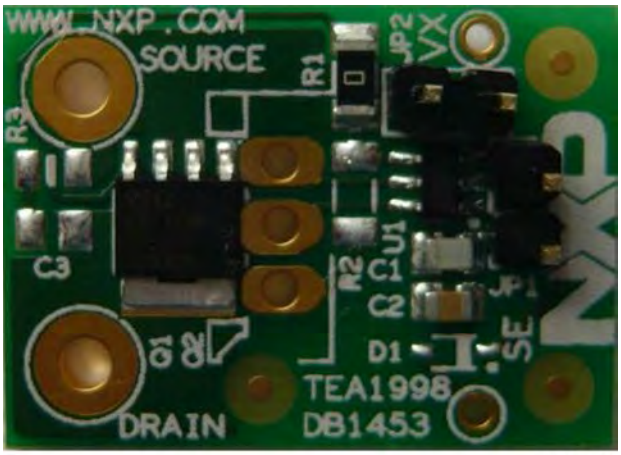


b. Not isolated

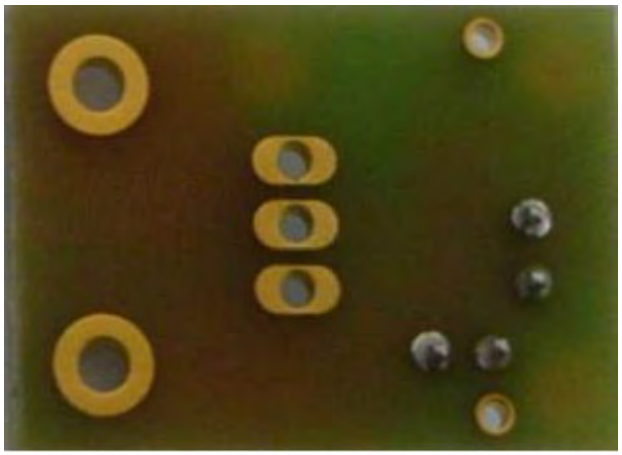
Figure 1. Isolation symbols

3 Board photographs

The TEA1998DB1453 demo board incorporates the TEA1998TS in TSOP-6 package and a MOSFET in LFPAK with a typical R_{DSon} of 1.8 mΩ. Figure 2 shows the front side and back side of the TEA1998DB1453 demo board. The TEA1998DB1453 demo board is a single layer board, which includes plated-through vias for external connections and the TO-220 MOSFET.



a. Front side



b. Back side

Figure 2. TEA1998DB1453 demo board photographs

4 TEA1998TS SR controller

The TEA1998TS is a dedicated controller IC for synchronous rectification on the secondary side of flyback converters. It incorporates the sensing stage and driver stages for driving the SR MOSFET. The SR MOSFET rectifies the output of the secondary transformer winding.

The TEA1998TS can generate its own supply voltage for battery charging applications with low output voltage or for applications with high-side rectification.

The TEA1998TS can be used in all power supplies that require a high efficiency, like:

- Chargers
- Adapters
- Flyback power supplies with very low and/or variable output voltages

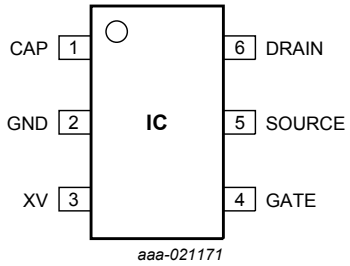


Figure 3. TEA1998TS pin configuration

5 TEA1998DB1453 demo board setup

5.1 Connected at low-side SR

The TEA1998DB1453 demo board is incorporated in an existing flyback power supply.

Figure 4 shows the connection of the TEA1998DB1453 demo board to the secondary side of a flyback controller board as low-side SR.

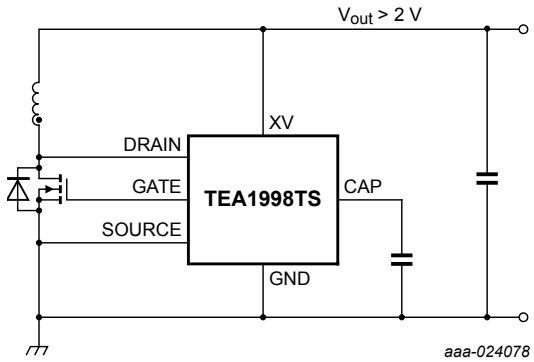


Figure 4. TEA1998DB1453 demo board configuration with low-side rectification

1. Supply via DRAIN pin (2 V to 4 V)
2. Supply via V_{out} (> 4 V)

Figure 4 shows the configuration for SR low-side applications that include CC mode (e.g. USB BC specification for an operation between 2 V and 5 V). When $V_{out} \geq 4.7$ V, the TEA1998DB1453 uses the voltage on the XV pin as supply. The resulting voltage on the CAP pin is typically 0.1 V below the voltage on the XV pin. It is used as supply voltage for the gate drive output to the external MOSFET.

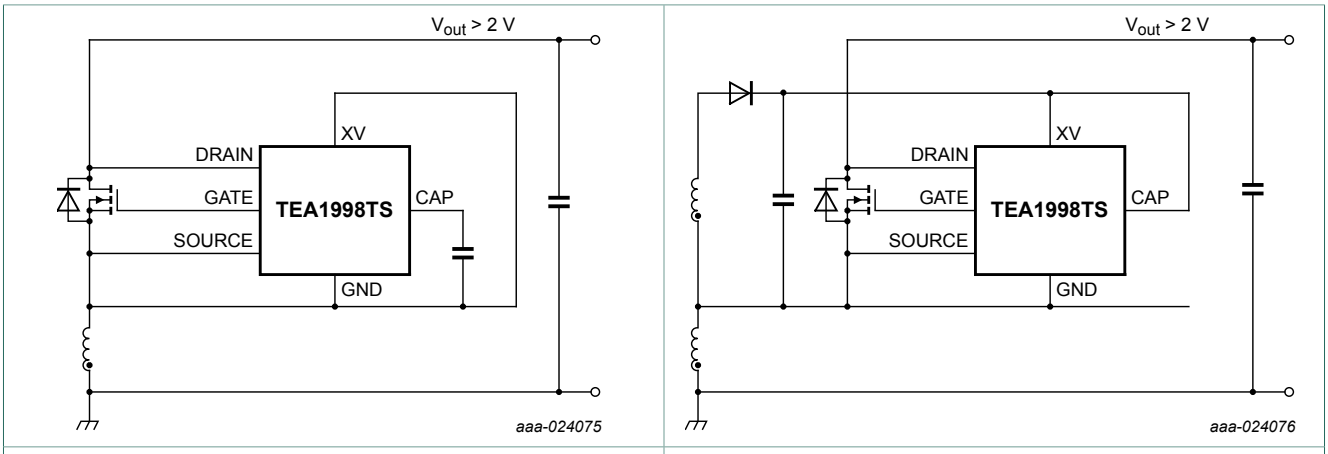
When $V_{out} < 4.7$ V (CC mode), the TEA1998TS uses the pulsed voltage on the drain input to generate the voltage for the CAP pin. When $0 V < V_{out} < 4.7$ V, the regulated voltage on the CAP pin is 4.7 V (typical).

Maximum voltage ratings for TEA1998TS pins:

- Pins XV and CAP: 10 V
- Pin DRAIN: 60 V

5.2 Connected at high-side SR

Figure 5 shows the connection of the TEA1998DB1453 demo board to the secondary side of a flyback controller board as high-side SR.



a. Self-supply via the DRAIN input (> 2 V)

b. Supply via the auxiliary winding

Figure 5. TEA1998DB1453 demo board with high-side rectification

Figure 5(a) shows the configuration for SR high-side applications with self-supply. In this case, the TEA1998TS retrieves its supply from the pulsed voltage on the DRAIN input. The regulator inside the TEA1998TS converts these pulses to an approximately 9 V regulated DC voltage. If the XV pin is connected to the IC ground, the TEA1998TS generates 9 V. This voltage is present on the CAP pin. It is the reference voltage for the gate drive of the external MOSFET.

Figure 5(b) shows the configuration for SR high-side application which is supplied by an additional auxiliary winding. This configuration can deliver the best possible efficiency for high-side application.

If, in a multiple-outputs application, the auxiliary voltage drops below the 4.7 V for the lower output voltages, the TEA1998TS generates its own supply voltage. It maintains a minimum supply of 4.7 V on the CAP pin. The auxiliary voltage can then be optimized for the higher output voltages. In this way, maximum efficiency at maximum power is achieved.

Maximum voltage ratings for TEA1998TS pins:

- Pins XV and CAP: 10 V
- Pin DRAIN: 60 V

6 Schematic

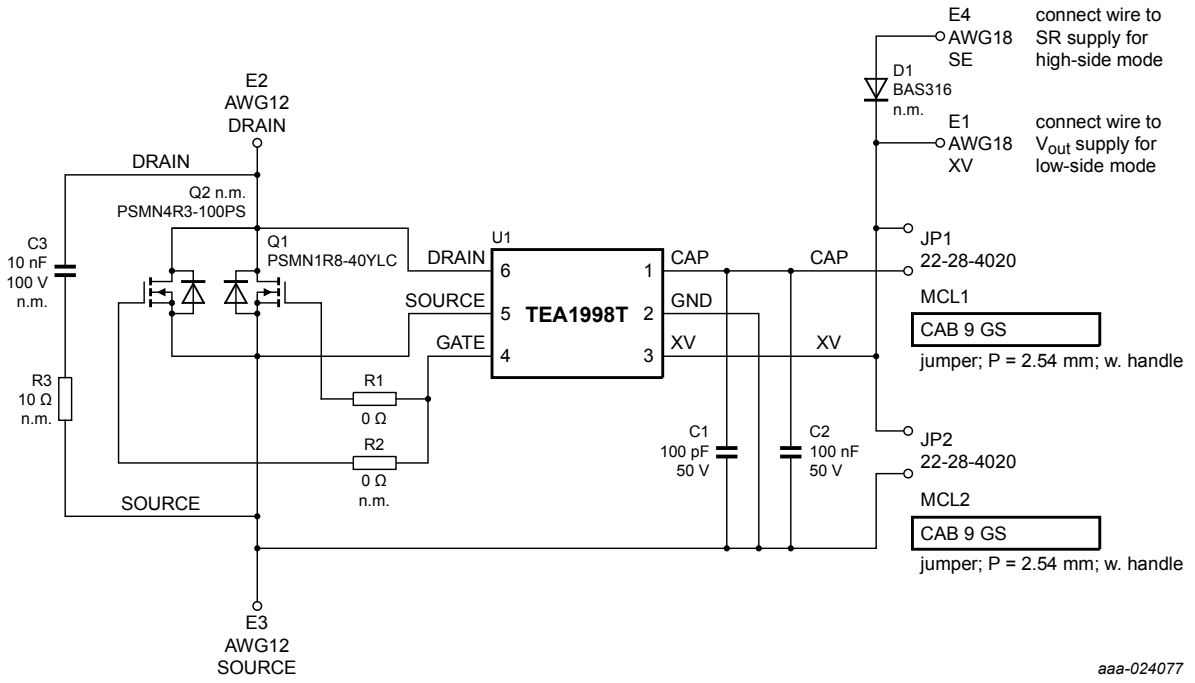


Figure 6. TEA1998DB1453 demo board schematic

Figure 6 shows the schematic diagram of the TEA1998DB1453 demo board. The board incorporates the TEA1998TS controller and a power MOSFET. The TEA1998TS acts as a controlled amplifier. The input is the voltage difference between the DRAIN and the SOURCE pin. The corresponding gate driver signal is the output. The amplifier regulates the source-to-drain voltage difference to 35 mV in the rectification phase.

To facilitate easy layout design for a single-sided board, resistors R1 and R2 are added. They must be between 0 Ω and 10 Ω. For the fastest turn-off time, use the lowest value. By default, the LFPAK MOSFET Q1 is mounted with a 0 Ω gate resistor (R1). It is also possible to mount a TO220 MOSFET Q2 with gate resistor R2. Capacitors C1 and C2 are decoupling capacitors for the V_{CC} of the TEA1998TS. Connect these capacitors close to the IC.

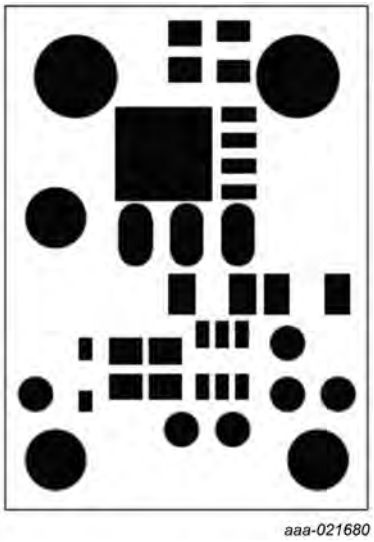
To ensure sufficient charge power during the secondary stroke to drive the external MOSFET, a value of 100 nF is used for capacitor C2. To prevent unwanted oscillation of the V_{CC} supply, capacitor C1 is added. A provision is made for snubber R3/C3. The components are not mounted. However, if high-voltage spikes occur on the drain-source connections of the MOSFETs, they can be added. To facilitate optimal configurations for either the low-side or the high-side connection, jumpers JP1 and JP2 are added (see the diagrams in Section 5).

7 Bill Of Materials (BOM)

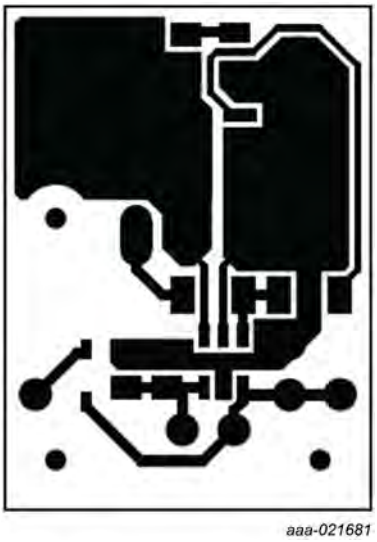
Table 2. TEA1998DB1453 demo board BOM

Reference	Description and values	Part number	Manufacturer
C1; C2	capacitor; 100 pF; 50 V; 0805	-	-
C3	capacitor; not mounted; 10 nF; 100 V; 0805	-	-
D1	diode; not mounted; SOD323	BAS316	NXP Semiconductors
JP1; JP2	header; straight; 1 × 2-way	22-28-4020	Molex
MCL1; MCL2	jumper; with handle; P = 2.54 mm	CAB 9 GS	Fischer
R1	resistor; 0 Ω; 1206	-	-
R2	resistor; not mounted; 0 Ω; 1206	-	-
R3	resistor; not mounted; 10 Ω; 0805	-	-
Q1	MOSFET; LFPAK	PSMN1R8-40YLC	NXP Semiconductors
U1	SR controller; TEA1998TS	TSOP-6	NXP Semiconductors

8 Layout



a. Front side



b. Back side

Figure 7. TEA1998DB1453 demo board layout

Some important guidelines for a good layout:

- Keep the trace from the DRAIN pin to the MOSFET drain as short as possible
- Keep the trace from the SOURCE pin to the MOSFET source as short as possible
- Keep the area of the loop from the DRAIN pin, to the MOSFET drain, to the MOSFET source, and to the SOURCE pin as small as possible. Make sure that the overlap of this loop over the power drain track or the power source track is as small as possible. Take care that the two loops do not cross each other.
- Keep the track from the GATE pin to the gate of the MOSFET as short as possible
- Use separate clean tracks for the XV and the GND pins. If possible, use a small ground plane underneath the IC, which improves the heat dispersion.

9 NXP Semiconductors power MOSFETs

Table 3. Extract from the NXP Semiconductors power MOSFET selection guide

Type number	Package name	$V_{DS(max)}$ (V)	$R_{DSon(max)}$ at V_{GS} = 10 V (mΩ)	$I_{D(max)}$ (A)	Q_{GD} (typical; nC)	$Q_{G(tot)}$ (typical; nC)
PSMN2R4-30MLD	LFPAK33	30	2.4	70	5.6	16
PSMN1R0-30YLD	LFPAK56	30	1.02	100	11	38
PSMN1R0-40YLD	LFPAK56	40	1.1	100	17	59
PSMN1R4-40YLD	LFPAK56	40	1.4	100	13	45
PSMN1R5-40ES	I2PAK	40	1.6	120	32	136
PSMN1R5-40PS	TO-220AB	40	1.6	150	32	136
PSMN1R6-40YLC	LFPAK56	40	1.55	100	15.3	59
PSMN1R8-40YLC	LFPAK56	40	1.8	100	10.9	45
PSMN1R9-40PL	TO-220AB	40	1.7	150	40.9	230
PSMN2R1-40PL	TO-220AB	40	2.2	150	29.6	168.9
PSMN2R2-40PS	TO-220AB	40	2.1	100	25	110
PSMN2R6-40YS	LFPAK56	40	2.8	100	14	63
PSMN2R8-40PS	TO-220AB	40	2.8	100	17	71
PSMN3R3-40YS	LFPAK56	40	3.3	100	11.2	49
PSMN4R0-40YS	LFPAK56	40	4.2	100	7	38
PSMN4R5-40PS	TO-220AB	40	4.6	100	8.8	35
PSMN5R8-40YS	LFPAK56	40	5.7	90	7.8	28.8
PSMN8R0-40PS	TO-220AB	40	7.6	77	3.8	17
PSMN8R3-40YS	LFPAK56	40	8.6	70	4.5	20
PSMN2R0-60ES	I2PAK	60	2.2	120	32	137
PSMN2R0-60PS	TO-220AB	60	2.2	120	32	137
PSMN2R5-60PL	TO-220AB	60	2.6	150	41.2	223
PSMN2R6-60PS	TO-220AB	60	2.6	150	43.7	140
PSMN3R0-60ES	I2PAK	60	3	100	28	130
PSMN3R0-60PS	TO-220AB	60	3	100	28	130
PSMN3R3-60PL	TO-220AB	60	3.4	130	31	175
PSMN3R9-60PS	TO-220AB	60	3.9	130	33	103
PSMN4R2-60PL	TO-220AB	60	3.9	130	27	151
PSMN4R6-60PS	TO-220AB	60	4.6	100	14.8	70.8
PSMN5R5-60YS	LFPAK56	60	5.2	100	11.2	56
PSMN7R0-60YS	LFPAK56	60	6.4	89	9.6	45
PSMN7R6-60PS	TO-220AB	60	7.8	92	10.6	38.7
PSMN8R5-60YS	LFPAK56	60	8	76	7.7	39

Type number	Package name	$V_{DS(max)}$ (V)	$R_{DSon(max)}$ at V_{GS} = 10 V (mΩ)	$I_{D(max)}$ (A)	Q_{GD} (typical; nC)	$Q_{G(tot)}$ (typical; nC)
PSMN3R3-80ES	I2PAK	60	3.3	120	27	139
PSMN3R3-80PS	TO-220AB	60	3.3	120	27	139
PSMN3R5-80ES	I2PAK	80	3.5	120	27	139
PSMN3R5-80PS	TO-220AB	80	3.5	120	27	139
PSMN4R3-80ES	I2PAK	80	4.3	120	28	111
PSMN4R3-80PS	TO-220AB	80	4.3	120	28.4	111
PSMN4R4-80PS	TO-220AB	80	4.1	100	25	112
PSMN5R0-80PS	TO-220AB	80	4.7	100	21	87
PSMN6R5-80PS	TO-220AB	80	6.9	100	16	71
PSMN8R2-80YS	LFPAK56	80	8.5	82	12	55
PSMN8R7-80PS	TO-220AB	80	8.7	90	11	52
PSMN4R3-100ES	I2PAK	100	4.3	120	49	170
PSMN4R3-100PS	TO-220AB	100	4.3	120	49	170
PSMN5R0-100ES	I2PAK	100	5	120	49	170
PSMN5R0-100PS	TO-220AB	100	5	120	49	170
PSMN5R6-100PS	TO-220AB	100	5.6	100	43	141
PSMN7R0-100ES	I2PAK	100	6.8	100	36	125
PSMN7R0-100PS	TO-220AB	100	6.8	100	36	125
PSMN8R5-100ES	I2PAK	100	8.5	100	33	111
PSMN8R5-100PS	TO-220AB	100	8.5	100	33	111
PSMN6R3-120ES	I2PAK	120	6.7	70	61.9	207.1
PSMN6R3-120PS	TO-220AB	120	6.7	70	61.9	207.1
PSMN7R8-120ES	I2PAK	120	7.9	70	50.5	167
PSMN7R8-120PS	TO-220AB	120	7.9	70	50.5	167

10 Abbreviations

Table 4. Abbreviations

Acronym	Description
CC	Constant Current
CV	Constant Voltage
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
SR	Synchronous Rectifier

11 References

TEA1998TS data sheet

GreenChip synchronous rectifier controller; 2016, NXP Semiconductors

12 Legal information

12.1 Definitions

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