



TEP0006 TRM

Revision v.24

Exported on 2019-11-07

Online version of this document:

<https://wiki.trenz-electronic.de/display/PD/TEP0006+TRM>

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4 Overview

The Trenz Electronic TEP0006 is an Ultra96 LS Expansion to Pmod adapter.

Refer to <http://trenz.org/tep0006-info> for the current online version of this manual and other available documentation.

4.1 Key Features

- **On Board:**
 - 4x Voltage Level Translators
 - 2x Voltage Regulators
- **Interface:**
 - 1x Ultra96 LS Expansion Header (40 Pins)
 - 3x Pmod Connectors
 - 3x Jumpers
- **Power:**
 - 5V
 - VCC_PSAUX
- **Dimension:**
 - 85 mm x 17 mm

4.2 Block Diagram

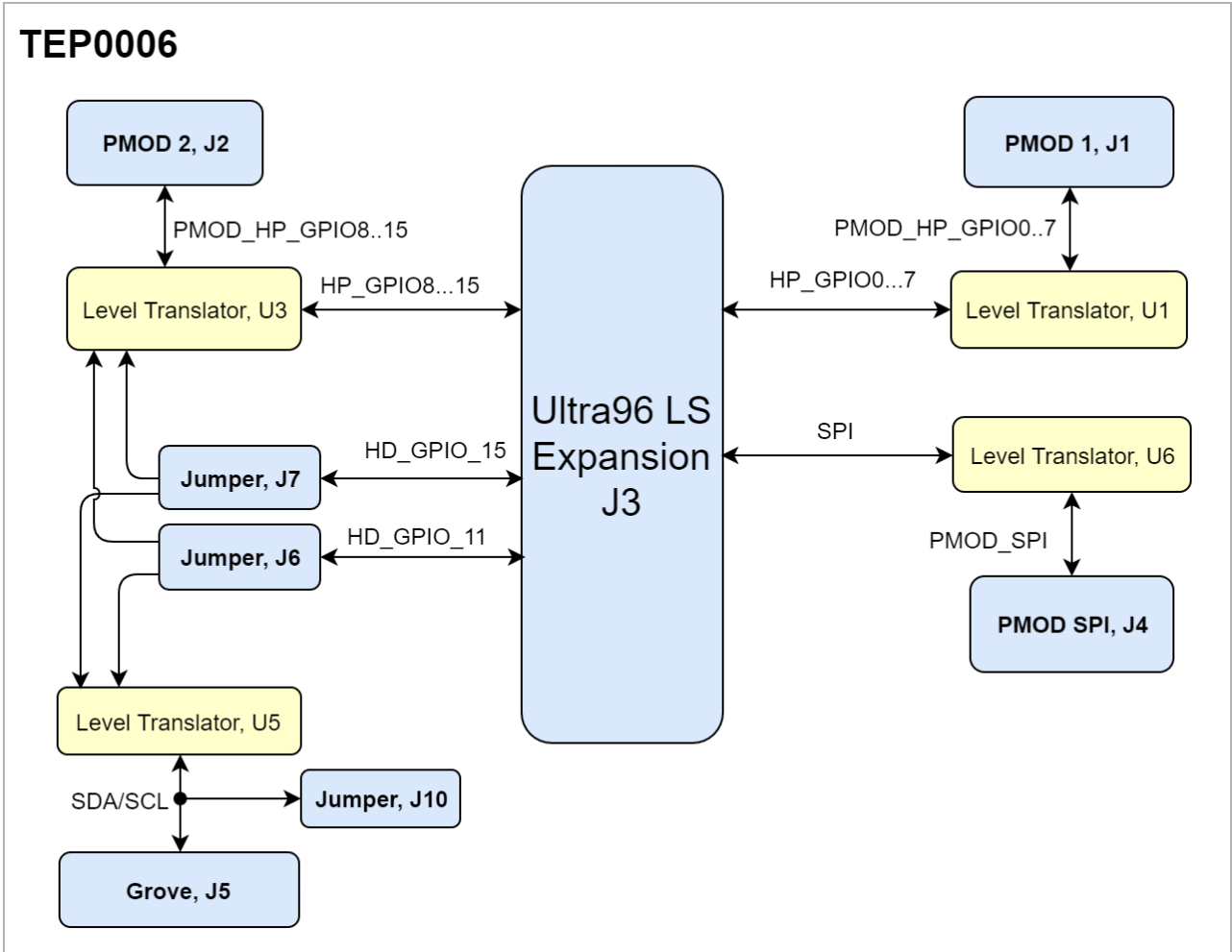


Figure 1: TEP0006 block diagram

4.3 Main Components

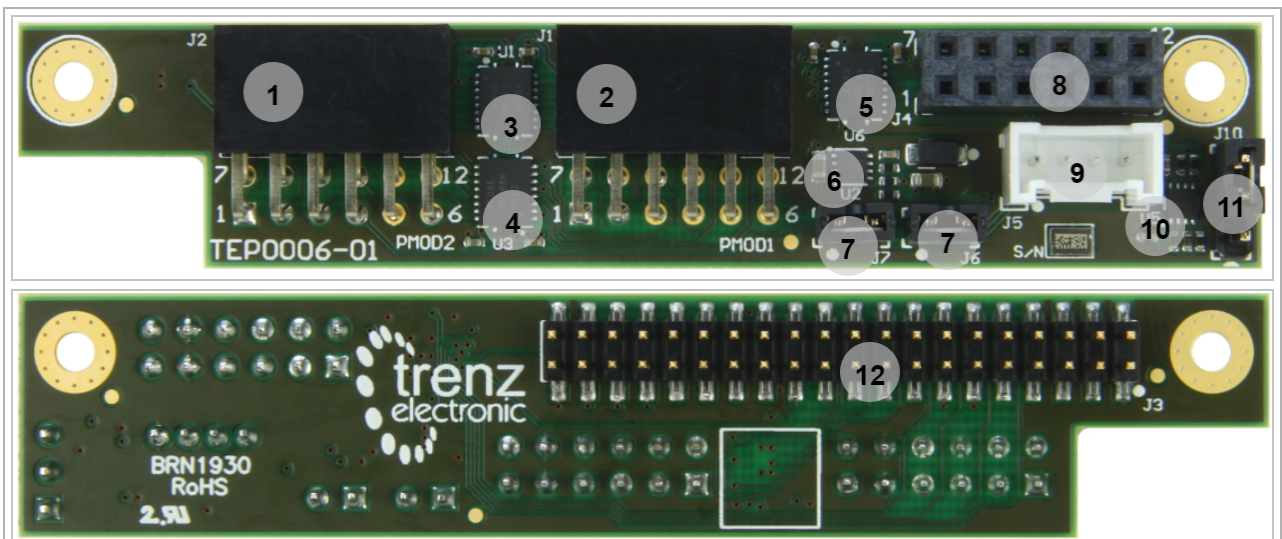


Figure 2: TEP0006 Main Components

1. PMod 2x6 Host Socke (PMOD 2) ,J2
2. PMod 2x6 Host Socke (PMOD 2) ,J1
3. Level Translator (HP_GPIO[0..7]) ,U1
4. Level Translator (HP_GPIO[8..15]),U3
5. Level Translator PMOD(SPI),U6
6. Linear Voltage Regulator,U2
7. Jumper,J6-J7
8. PMod 2x6 Host Socke (SPI),J4
9. GROVE,J5
10. Level Translator (GROVE) ,U5
11. Jumper (Voltage select),J10
12. Ultra96 LS Expansion Header (40 Pos),J3

4.4 Initial Delivery State

Storage device name	Content	Notes
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Table 1: Initial delivery state of programmable devices on the module

4.5 Configuration Signals

5 Signals, Interfaces and Pins

5.1 Low Speed Expansion Connector

The SMD Header J3 has 40 pin (20x2) and it is compatible with Ultra96 LS Expansion Connector. You can find General information about the LS Expansion connector in the following table.

Schematic	Connected to	Notes
HD_GPIO0...7	Level Translator HP_GPIO[0...7], U1	GPIO0...7
HD_GPIO8...15	Level Translator HP_GPIO[8...15], U3	GPIO8...15
MIO36...37	Level Translator PMOD(SPI)	PS_GPIO_0...1
MIO38, MIO41...43	Level Translator PMOD(SPI)	SPI
VCC_PSAUX	Level Translator, U1-U3-U5-U6 Voltage Regulator, U2	1.8 V nPOK
5V	Voltage Regulator, U2 Jumper, J10	Vin Pull up Voltage

Table 2: Ultra96 LS Expansion information

5.2 Pmod Connectors

The TEP0006 is equipped with three Pmod connectors. Pmod Connectors are the expanded outputs from Ultra96 Board.

Pin	Connected to			Notes
	Pmod 1, J1	Pmod 2, J2	Pmod SPI, J4	
1	PMOD_HD-GPIO0	PMOD_HD-GPIO8	SS	
2	PMOD_HD-GPIO1	PMOD_HD-GPIO9	MOSI	
3	PMOD_HD-GPIO2	PMOD_HD-GPIO10	MISO	

Pin	Connected to			Notes
	Pmod 1, J1	Pmod 2, J2	Pmod SPI, J4	
4	PMOD_HD-GPIO3	PMOD_HD-GPIO11	SCK	
5	GND	GND	GND	
6	3.3 V	3.3 V	3.3 V	
7	PMOD_HD-GPIO4	PMOD_HD-GPIO12	INIT	
8	PMOD_HD-GPIO5	PMOD_HD-GPIO13	RESET	
9	PMOD_HD-GPIO6	PMOD_HD-GPIO14	Not Connected	
10	PMOD_HD-GPIO7	PMOD_HD-GPIO15	Not Connected	
11	GND	GND	GND	
12	3.3 V	3.3 V	3.3 V	

Table 3: Pmod Connectors information

5.3 Jumpers

Designator	Functionality	Connection Between	Notes
J6	HD_GPIO_15	Level Translator U3 and U5	If you install the jumper HD_GPIO_15 will be driven through Level Translator (U5) and Grove (J5) otherwise it goes to Level Translator (U3).
J7	HD_GPIO_11	Level Translator U3 and U5	If you put the jumper HD_GPIO_11 will be driven through Level Translator (U5) and Grove (J5) otherwise it goes to Level Translator (U3).
J10	Voltage select	5 V, 3.3 V	Pull up Voltage

Table 4: Pmod Connectors information

6

On-board Peripherals

Chip/Interface	Designator	Notes
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Table 5: On board peripherals

7 Power and Power-On Sequence

7.1 Power Supply

Power is supplied by Ultra96 Board through SMD Header J3.

7.2 Power Consumption

Power Input Pin	Typical Current
5V	TBD
VCC_PSAUX	TBD

Table 6: Power Consumption

* TBD - To Be Determined

7.3 Power Distribution Dependencies

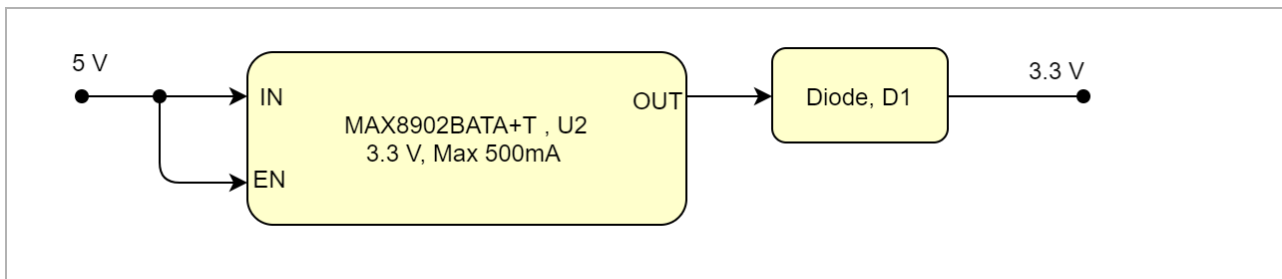


Figure 3: Power Distribution

7.4 Power-On Sequence

There is no specific power on sequence, after power on the Ultra96 Board all electrical components on TEP0006 will be enabled.

7.5 Power Rails

Power Rail Name	LS Expansion Connector Pin	Direction	Notes
+5V	37	Input	Supplied by Ultra96

Power Rail Name	LS Expansion Connector Pin	Direction	Notes
VCC_PSAUX	35	Input	Supplied by Ultra96

Table 7: Module power rails.

7.6 Technical Specifications

7.7 Absolute Maximum Ratings

Symbols	Description	Min	Max	Unit
T_STG	Storage Temperature	-55	150	°C

Table 8: PS absolute maximum ratings

7.8 Recommended Operating Conditions

Operating temperature range depends also on customer design and cooling solution. Please contact us for options.

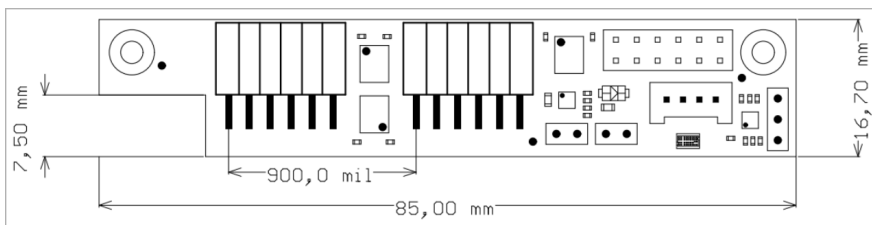
Parameter	Min	Max	Units	Reference Document
T_OPT	-40	+85	°C	

Table 9: Recommended operating conditions.

7.9 Physical Dimensions

- Module size: 85 mm × 17 mm. Please download the assembly diagram for exact numbers.

PCB thickness: 1.6 mm.


Figure 4: Physical Dimension

8 Currently Offered Variants

Trenz shop TEP0006 overview page	
English page¹	German page²

Table 10: Trenz Electronic Shop Overview

¹ <https://shop.trenz-electronic.de/en/search?sSearch=TEP0006>

² <https://shop.trenz-electronic.de/de/search?sSearch=TEP0006>

9 Revision History

9.1 Hardware Revision History

Date	Revision	Changes	Documentation Link
2019-07-19	01	Initial Release	REV01 ³

Table 11: Hardware Revision History

Hardware revision number can be found on the PCB board together with the module model number separated by the dash.

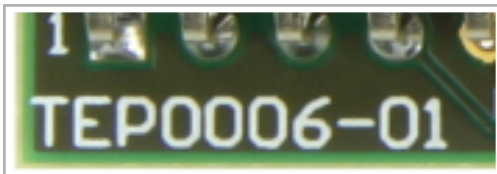


Figure 5: Board hardware revision number.

9.2 Document Change History

Date	Revision	Contributor	Description
 2019-11-07	v.24(see page 6)	John Hartfiel ⁴	<ul style="list-style-type: none"> Initial release
--	all	Pedram Babakhani ⁵ , John Hartfiel ⁶	<ul style="list-style-type: none"> --

Table 12: Document change history.

³ https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Pmods/TEP0006/REV01

⁴ <https://wiki.trenz-electronic.de/display/~j.hartfiel>

⁵ <https://wiki.trenz-electronic.de/display/~P.Babakhani>

⁶ <https://wiki.trenz-electronic.de/display/~j.hartfiel>

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10.7 REACH, RoHS and WEEE

REACH