TGA2237

0.03 – 2.5 GHz 10 W GaN Power Amplifier

Product Overview

Qorvo's TGA2237 is a wideband distributed amplifier fabricated on Qorvo's production 0.25 um GaN on SiC process (QGaN25). The TGA2237 operates from 0.03 – 2.5 GHz and provides 10 W of saturated output power with 13 dB of large signal gain and greater than 52% power-added efficiency.

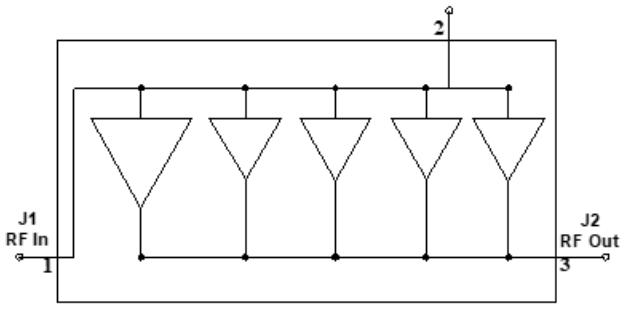
The broadband performance supports both radar and communication applications across defense and commercial markets as well as electronic warfare. The TGA2237 is fully matched to 50 Ω at both RF ports allowing for simple system integration. DC blocks are required on both RF ports and the drain voltage must be injected through an off chip bias-tee on the RF output port.

Lead-free and RoHS compliant.

Key Features

- Frequency Range: 0.03 – 2.5 GHz
- P_{SAT}: 40 dBm (P_{IN} = 27 dBm)
- P1dB: 32 dBm
- PAE: 52% (P_{IN} = 27 dBm)
- Large Signal Gain: 13 dB
- Small Signal Gain: 19 dB
- IM3 (120 mA, P_{OUT} < 33 dBm/tone): −30 dBc
- IM5 (120 mA P_{OUT} < 33 dBm/tone): −30 dBc
- Bias: V_D = 30 V, I_{DQ} = 360 mA
- Chip Dimensions: 2.40 x 1.80 x 0.10 mm

Functional Block Diagram



Applications

- Commercial and military radar
- Communications
- Electronic Warfare

Ordering Information

Part No.	Description
TGA2237	0.03 – 2.5GHz 10W GaN Power Amplifier
TGA2237EVBP01	TGA2237 Evaluation Board

Absolute Maximum Ratings

Parameter	Rating
Drain Voltage (V_D)	40 V
Gate Voltage Range (V_G)	−8 to 0 V
Drain Current (I_D)	1350 mA
Gate Current (I_G)	Refer to plot on page 9
Power Dissipation (P_{DISS}), 85°C	19 W
Input Power (P_{IN}), CW, 50Ω, 85°C,	33 dBm
Input Power (P_{IN}), CW, VSWR 10:1, V_D = 30V, 85°C	30 dBm
Mounting Temperature	320 °C
Storage Temperature	−55 to 150 °C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Typ.	Units
Drain Voltage (V_D)	30	V
Drain Current (I_{DQ})	360	mA
Drain Current w/RF Drive (I_{D_Drive})	660	mA

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

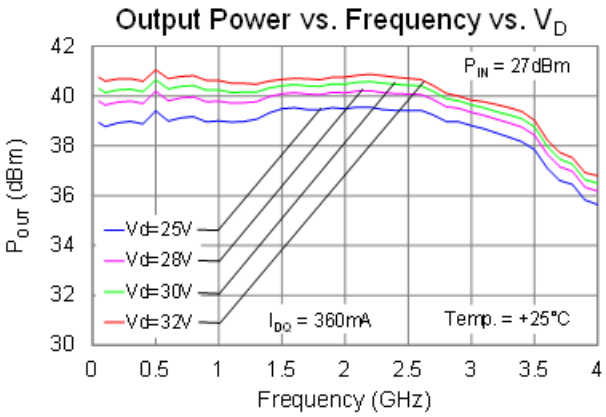
Electrical Specifications

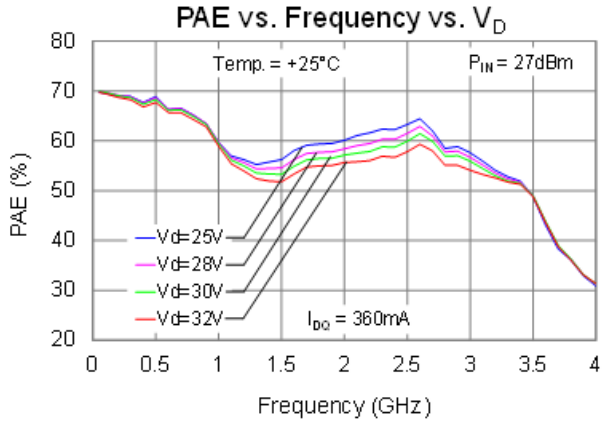
Parameter	Min	Typ	Max	Units
Operational Frequency Range	0.03		2.5	GHz
Small Signal Gain		19		dB
Input Return Loss		> 10		dB
Output Return Loss		> 12		dB
Output Power (Pin = 27 dBm)		40		dBm
Power Added Efficiency (Pin = 27 dBm)		> 52		%
Power @ 1dB Compression (P1dB)		> 32		dB
IM3 @ 120 mA P_{OUT}/Tone < 33 dBm		−30		dBc
IM5 @ 120 mA P_{OUT}/Tone < 33 dBm		−30		dBc
Small Signal Gain Temperature Coefficient		−0.02		dB/°C
Output Power Temperature Coefficient		−0.002		dBm/°C
Recommended Operating Voltage:	25	30	32	V

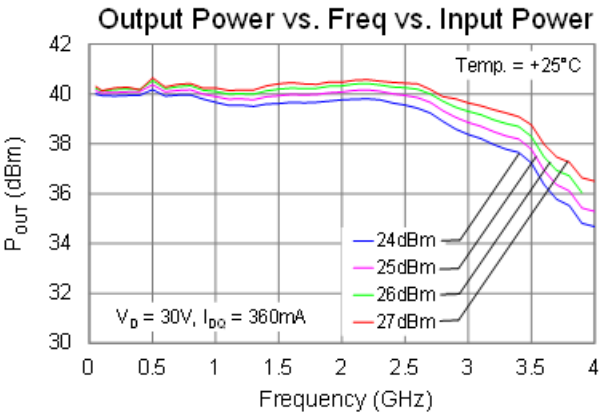
Test conditions unless otherwise noted: 25 °C, V_D = 30 V, I_{DQ} = 360 mA

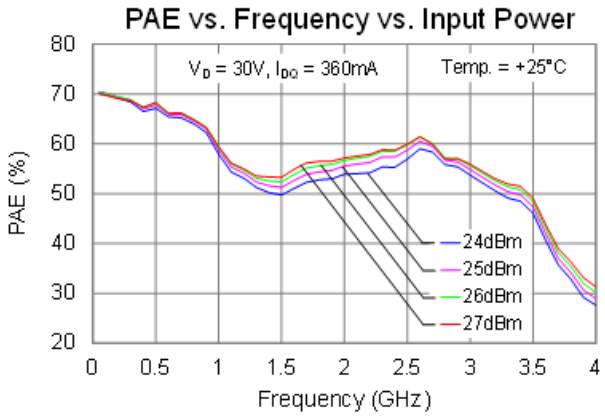
Performance Plots – Large Signal

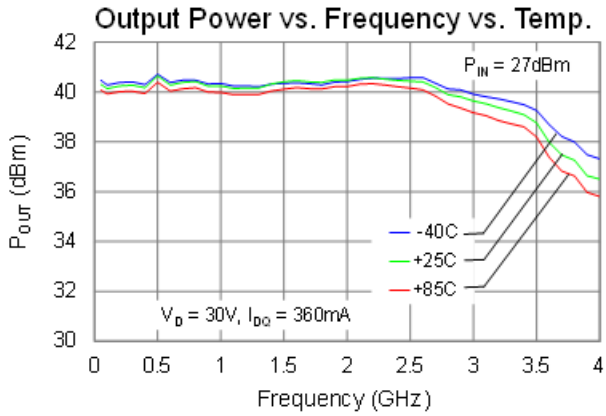
The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on pages 10-11)

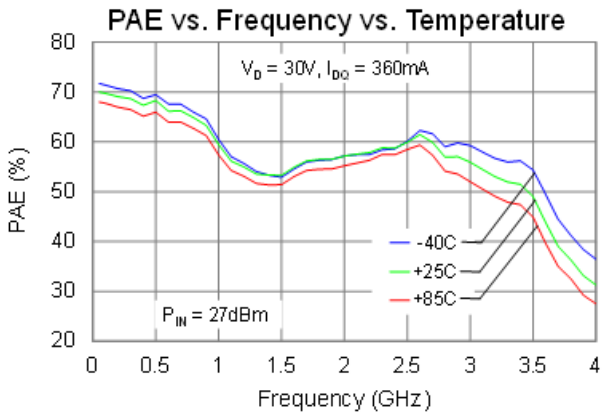






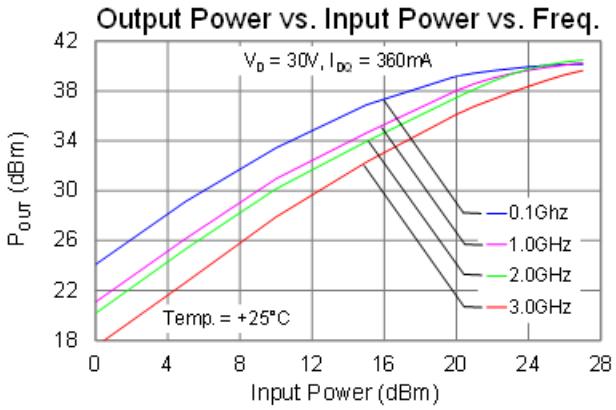


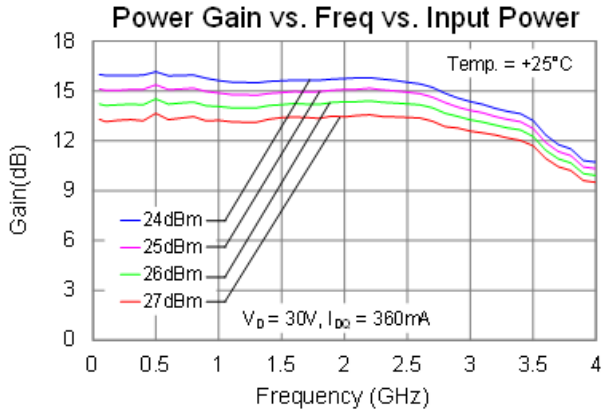


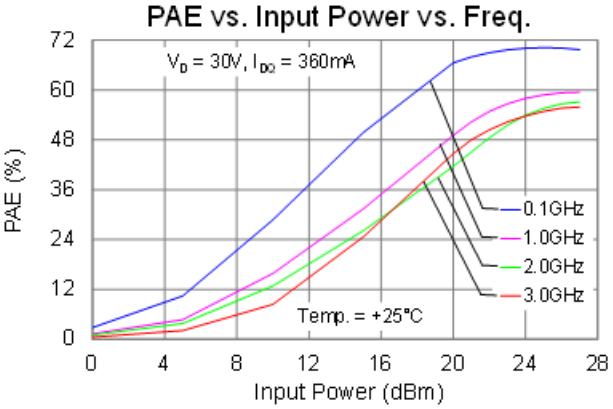


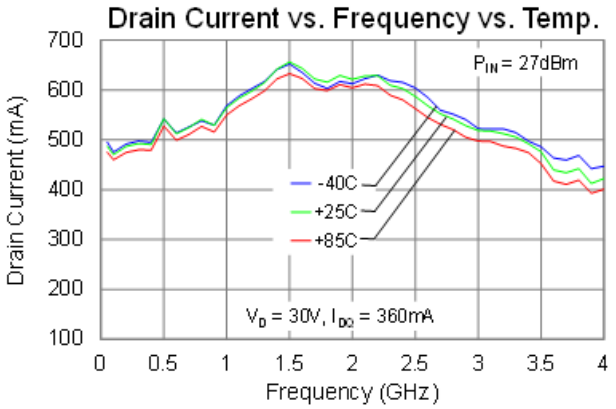
Performance Plots – Large Signal

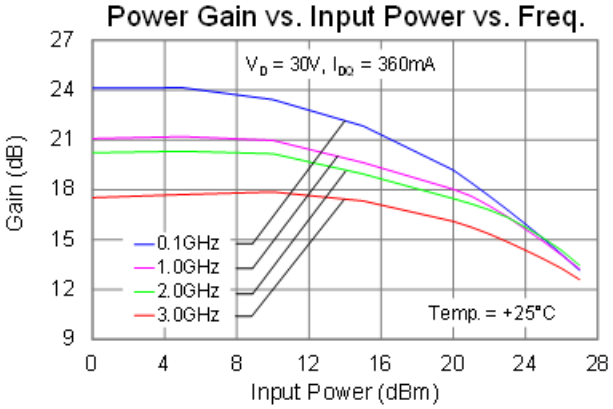
The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on pages 10-11)

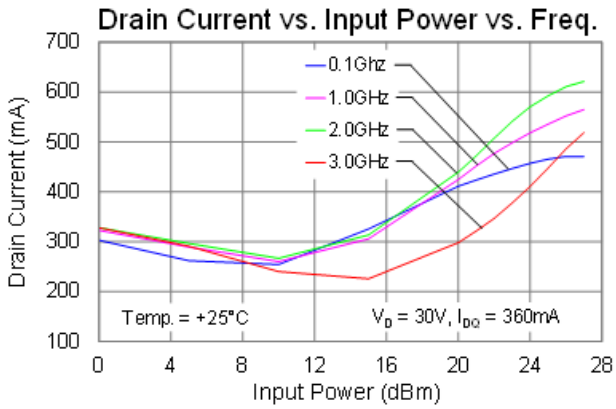






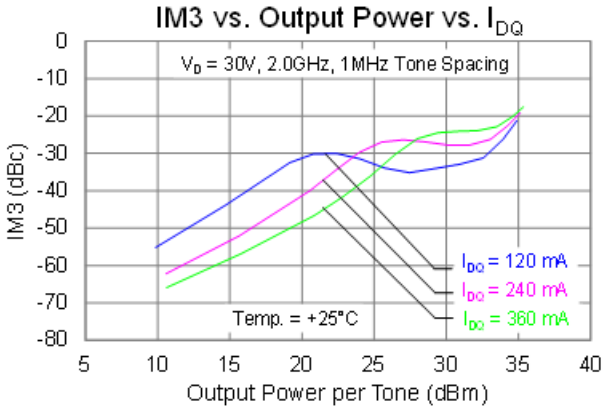


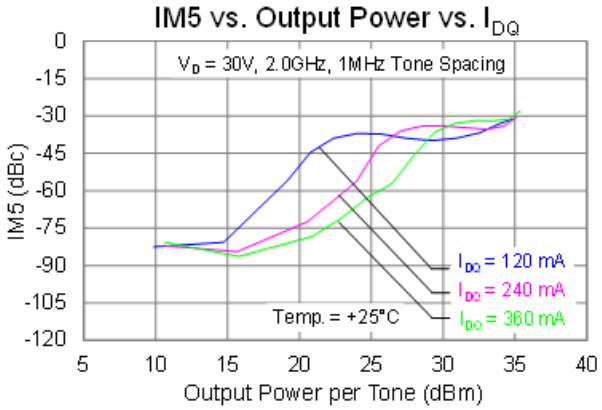


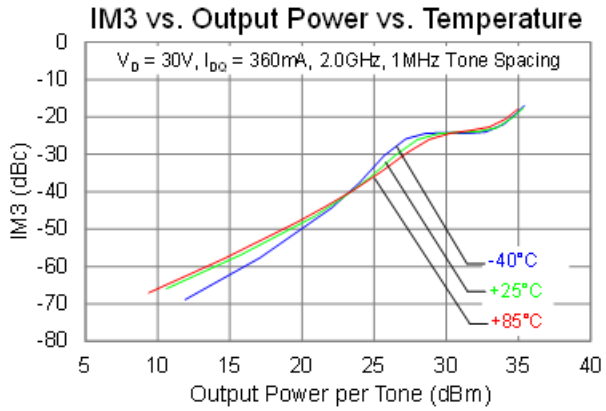


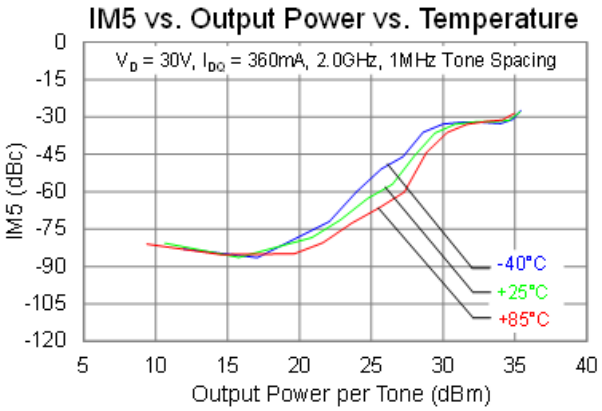
Performance Plots – Linearity

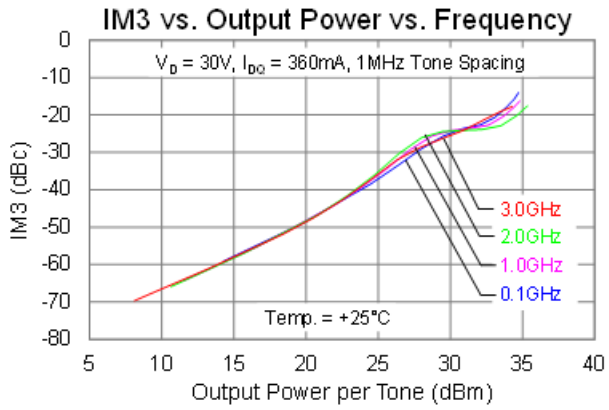
The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on pages 10-11)

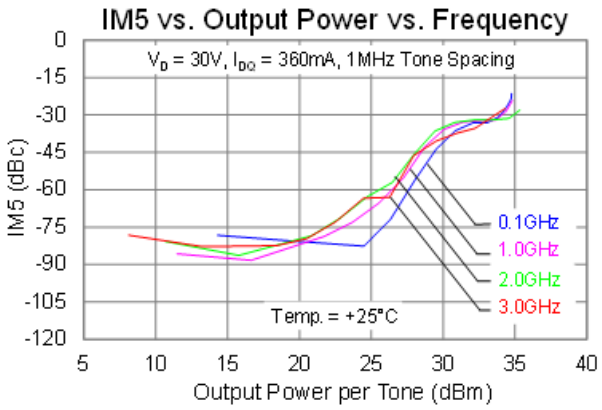






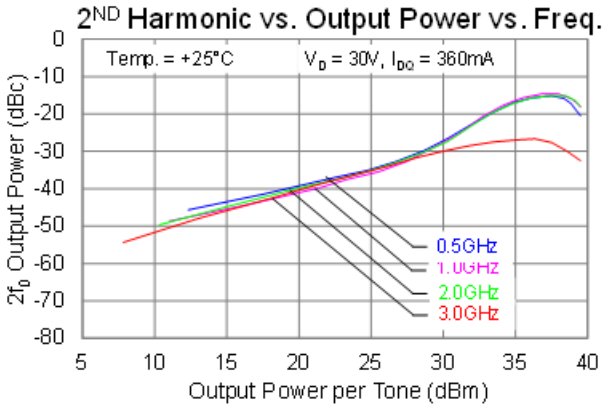


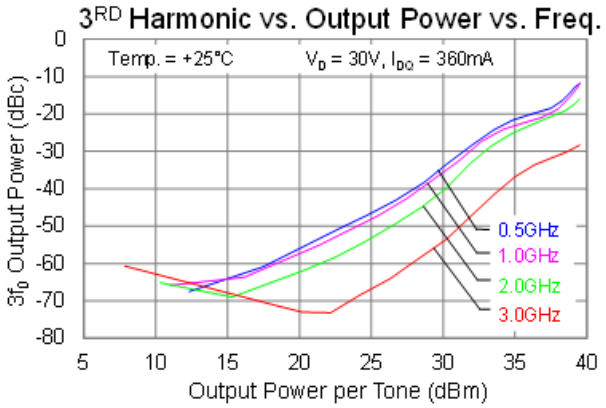


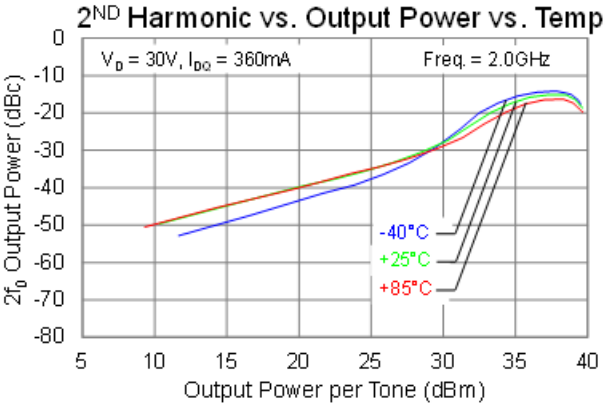


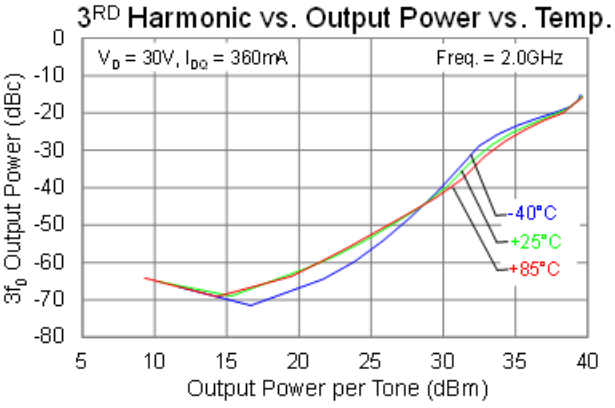
Performance Plots – Harmonics

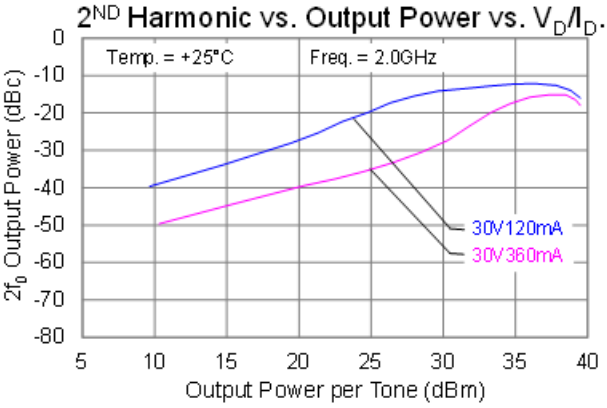
The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on pages 10-11)

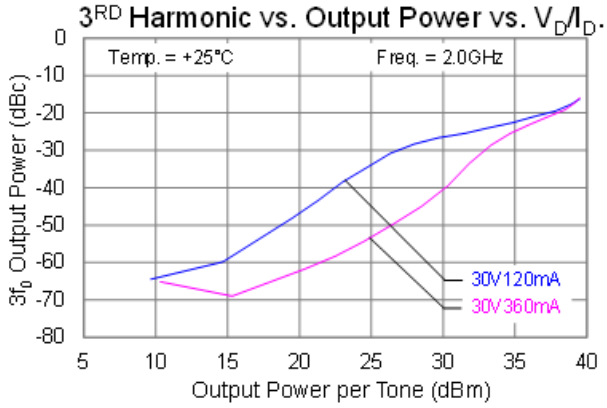






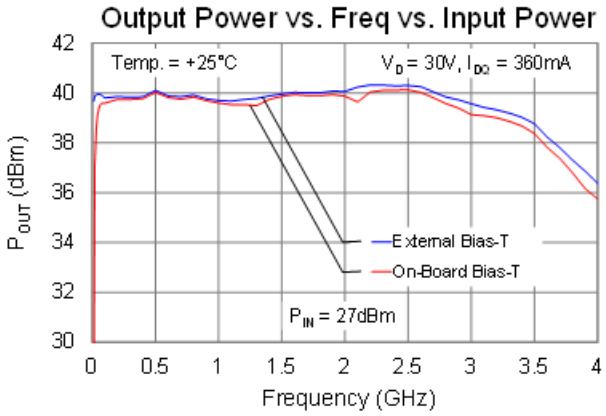


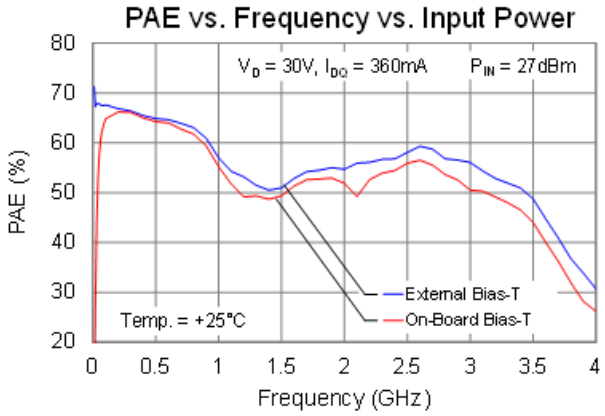




Performance Plots – External Bias-Tee vs. On-Board Bias-Tee

The plots below reflect performance measured between using an external bias tee and an on-board bias tee
(See application circuit on pages 10-11 and 12-13)

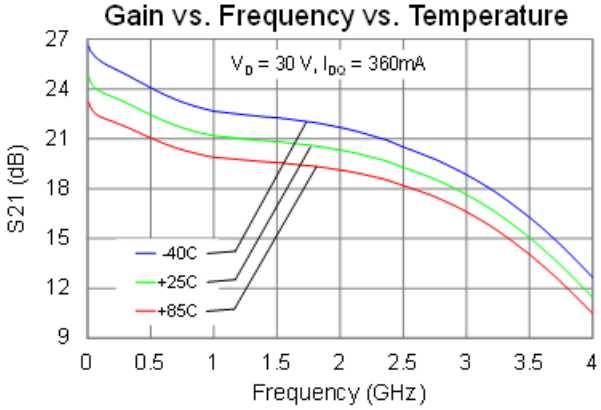




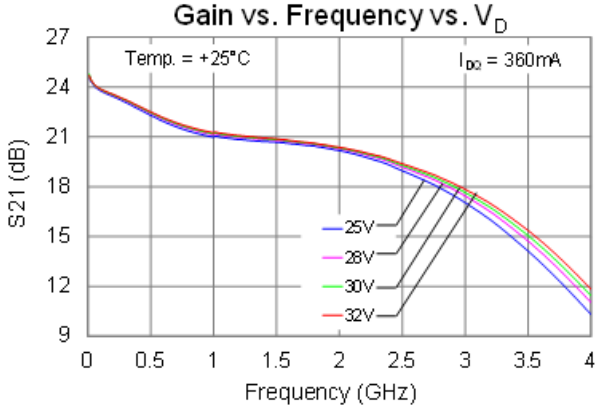
Performance Plots – Small Signal

The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on pages 10-11)

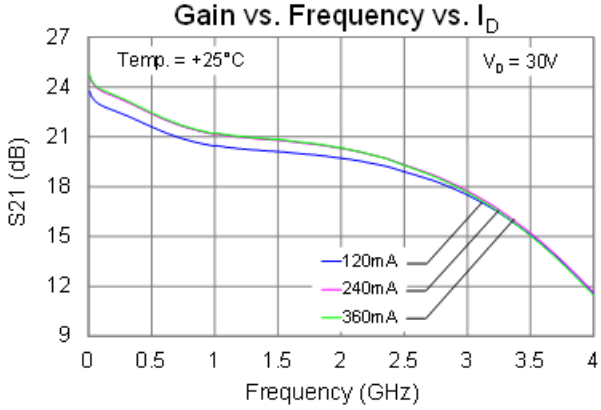
Gain vs. Frequency vs. Temperature



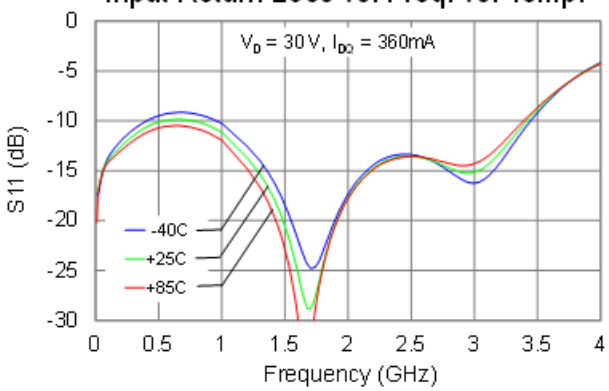
Gain vs. Frequency vs. V_D



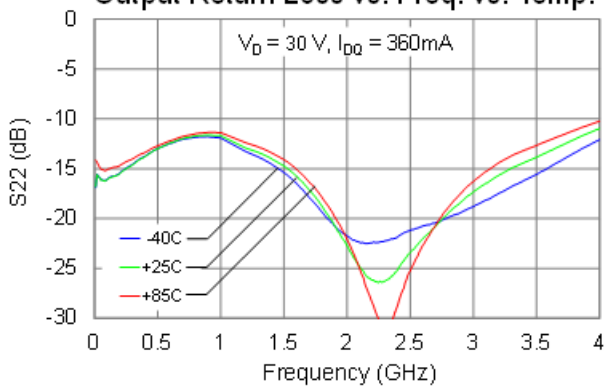
Gain vs. Frequency vs. I_D



Input Return Loss vs. Freq. vs. Temp.



Output Return Loss vs. Freq. vs. Temp.

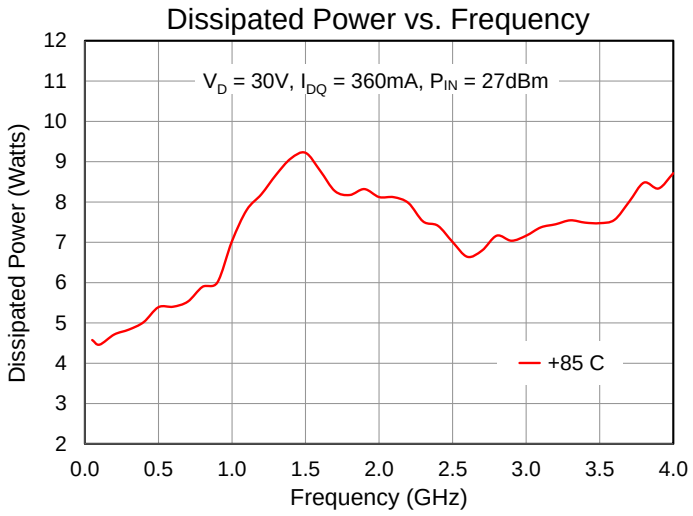


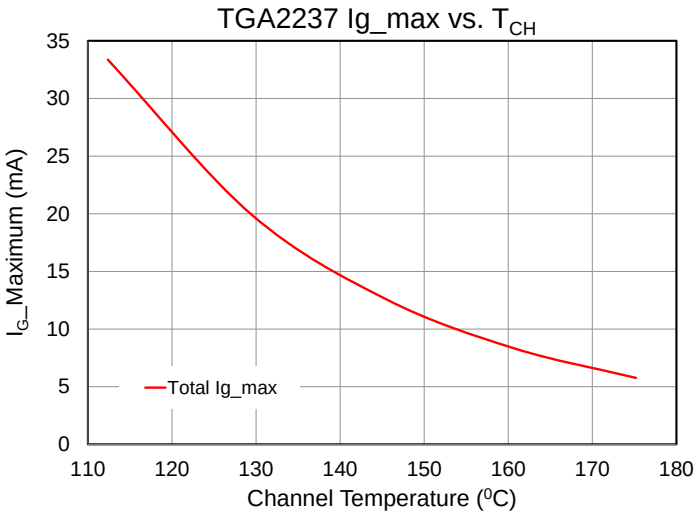
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = 85 °C, V_D = 30 V, I_{DQ} = 360 mA, P_{DISS} = 10.8 W (No RF Drive)	6.664	°C/W
Channel Temperature T_{CH} (Quiescent) (1,2)		157.0	°C
Thermal Resistance (θ_{JC}) (1)	T_{BASE} = 85 °C, V_D = 30 V, I_{DQ} = 360 mA, I_{D_Drive} = 633 mA, P_{OUT} = 40 dBm, P_{DISS} = 9.22 W	6.545	°C/W
Channel Temperature T_{CH} (RF Drive) (1,2)		145.3	°C

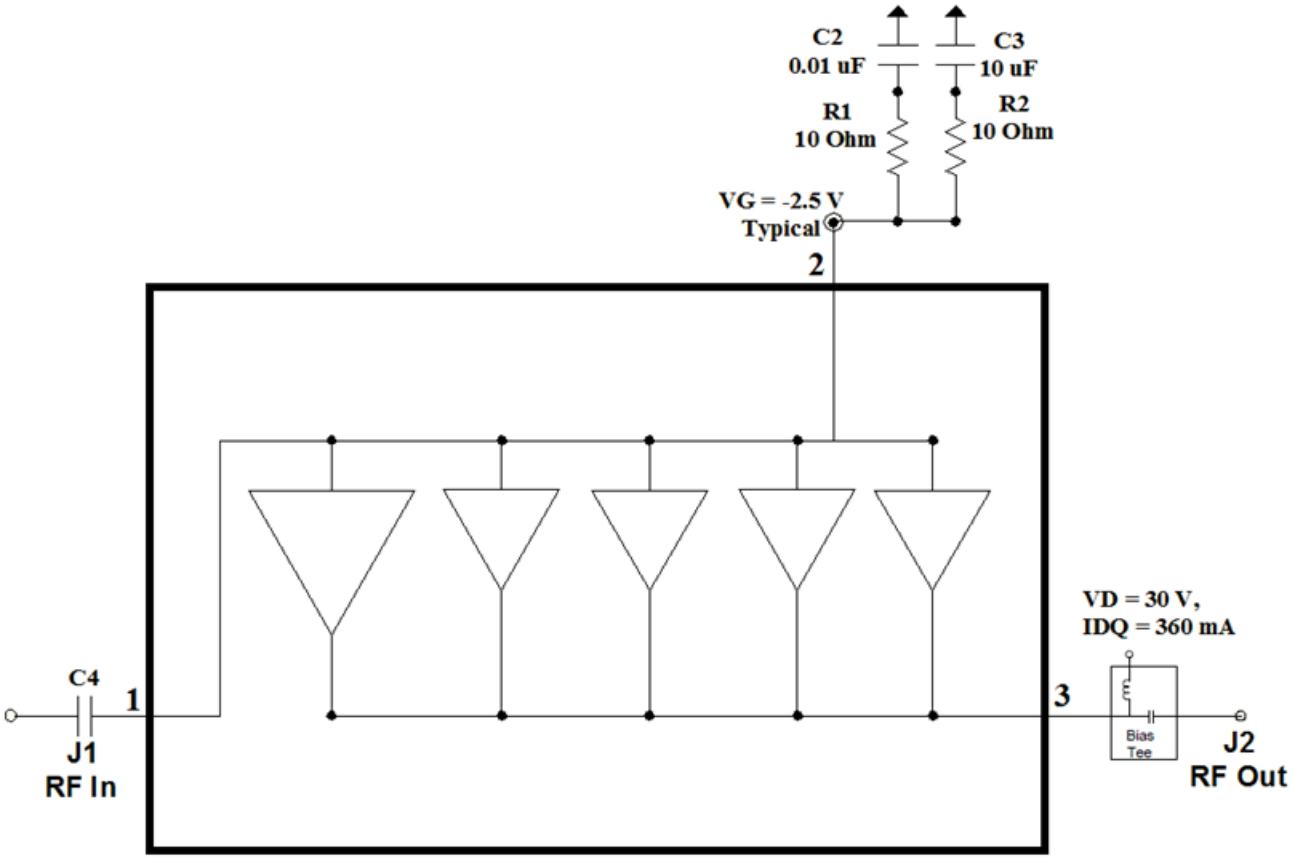
Notes:
1. Die mounted to 20 mil CuMo carrier plate with AuSn solder. Thermal resistance determined to the back of carrier at 85 °C.
2. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

Power Dissipation and Maximum Gate Current





Applications Information – Coax Input DC Block and Coax Output Bias-Tee



Notes:

1. This configuration was used for DVT and is provided here for reference only. This configuration is not provided for customer use.
2. Coaxial input DC block (C4) is used for input port (RF In)
3. External wide bandwidth Bias-Tee is used for output port (RF Out). V_D is applied through the output Bias-Tee

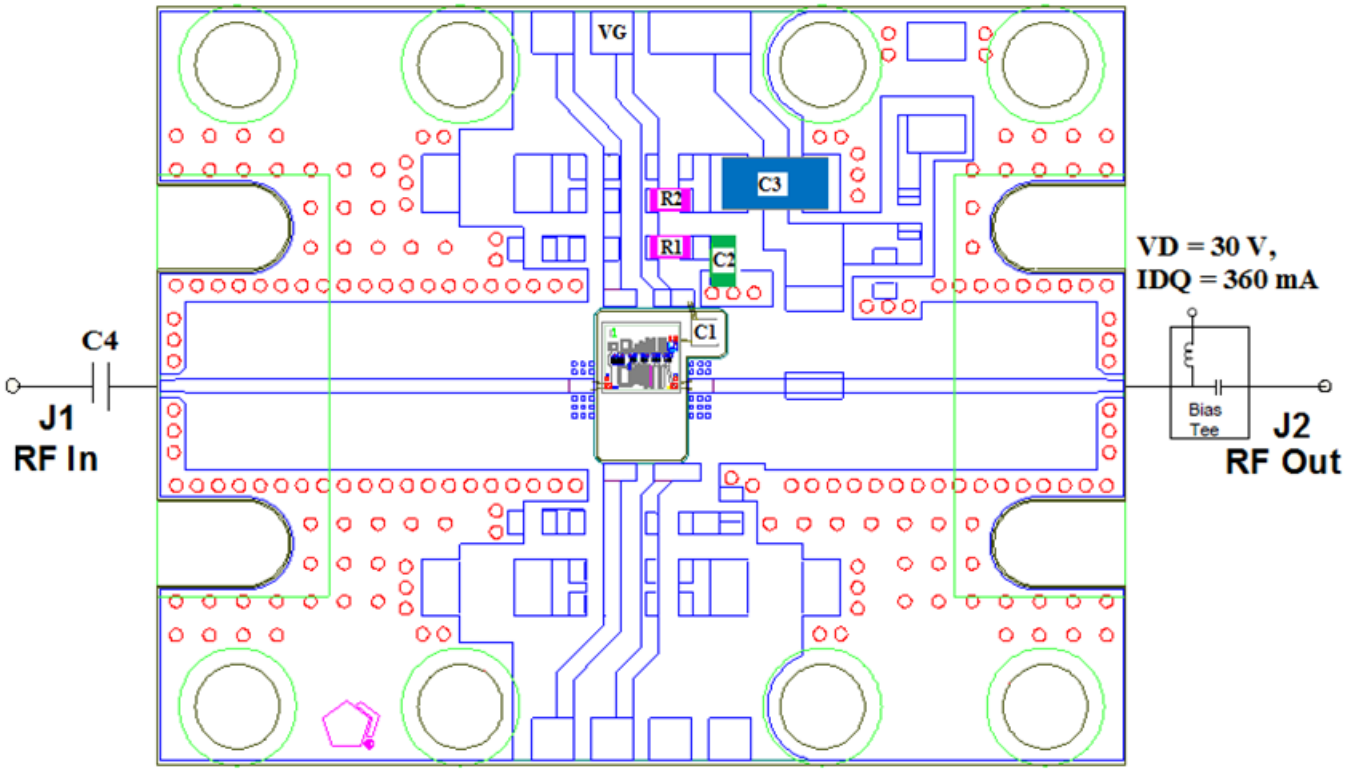
Bias-Up Procedure

1. Set I_D limit to 700 mA, I_G limit to 5 mA
2. Set V_G to -5.0 V
3. Set VD +3 0V
4. 4. Adjust V_G more positive until I_{DQ} = 360 mA
5. Apply RF signal

Bias-Down Procedure

1. Turn off RF signal
2. Reduce V_G to -5.0 V. Ensure I_{DQ} ~ 0 mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

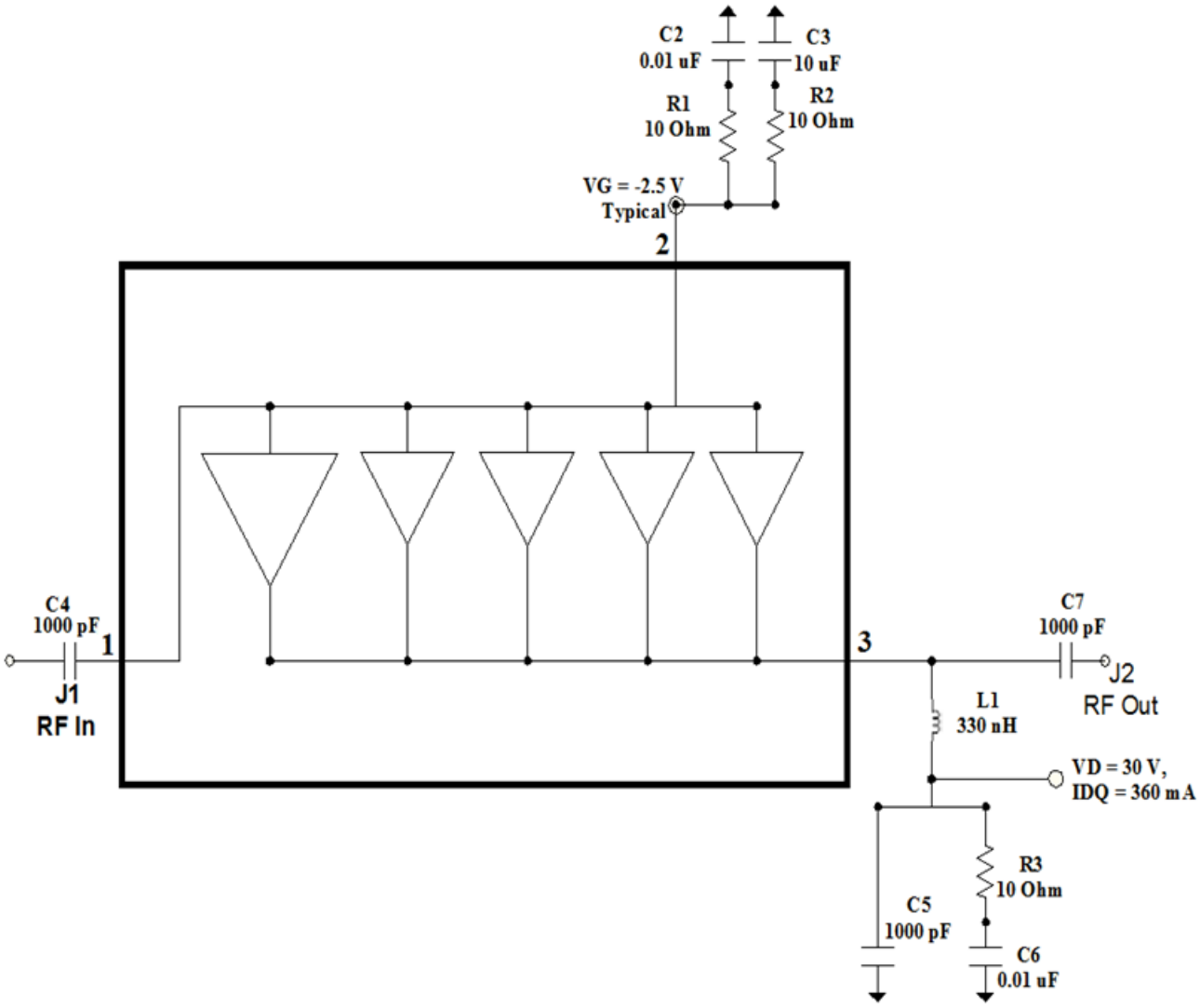
Evaluation Board Assembly – Coax Input DC Block and Coax Output Bias-Tee



Bill of Materials

Reference Des.	Value	Description	Manuf.	Part Number
C1	1000pF	SLC, 50V	Various	
C2	0.01uF	Cap, 0402, 50V, 10%, X7R	Various	
C3	10uF	Cap, 1206, 50V, 10%, X7R	Various	
C4		DC Block	Various	
R1 – R2	10Ω	Res, 0402	Various	

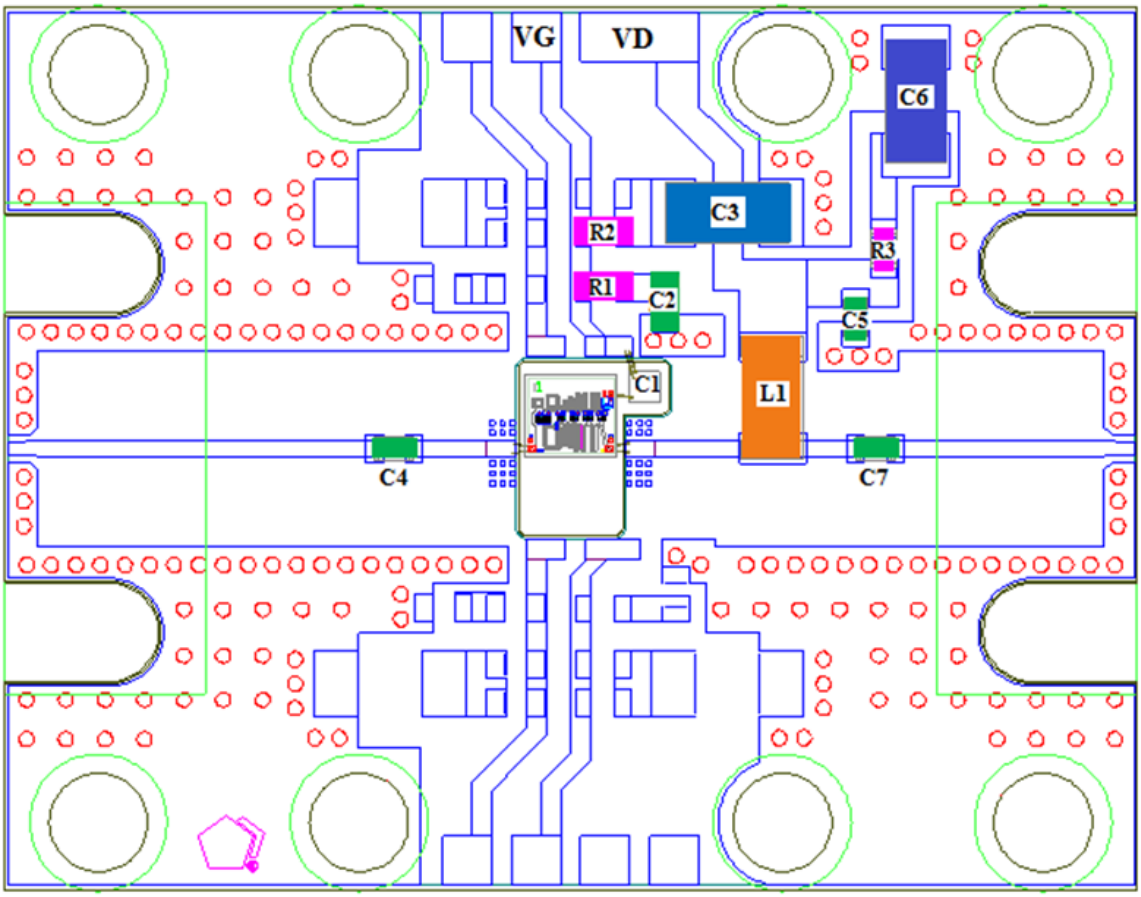
Applications Information – On-Board DC Blocks and Bias-Tee



Note:

1. This configuration is provided for customer use.
2. Performance of the MMIC with surface mount DC blocks and bias tee components may be degraded relative to the coaxial option. These components should be optimized for the desired operational bandwidth.

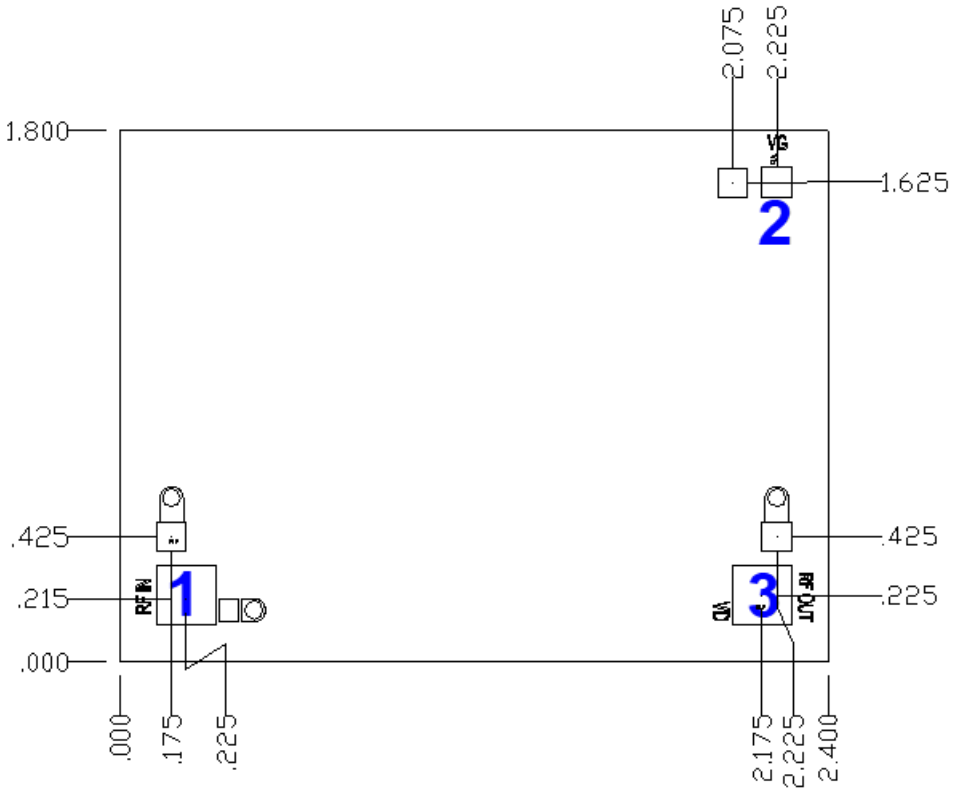
Evaluation Board Assembly – On-Board DC Blocks and Bias-Tee



Bill of Materials (On-Board Bias-Tee)

Reference Des.	Value	Description	Manuf.	Part Number
C4, C5, C7	1000pF	Cap, 0402, 100V, 10%, X7R	Various	
C6	0.01uF	Cap, 1206, 100V, 10%, X7R	Various	
L1	330nH	Ind, 1206, 100V, 10%, X7R	Various	
R3	10Ω	Res, 0402	Various	

Mechanical Information and Bond Pad Description



Units: millimeters
Thickness: 0.100
Die x,y size tolerance: ± 0.050
Chip edge to bond pad dimensions are shown to center of pad
Ground is backside of die

Bond Pad Description

Pad No.	Symbol	Pad Size (mm)	Description
1	RF In	0.198 x 0.198	RF Input; DC block is required.
2	V_G	0.100 x 0.100	Gate voltage: Bias network is required; see Application Circuit on pages 10 and 12 as examples.
3	RF Out/V_D	0.198 x 0.198	Output and Drain voltage: Bias network is required; see Application Circuit on pages 10 and 12 as examples.

Assembly Notes

Component placement and die attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Conductive epoxy attachment may be used for small-signal low power dissipation die.

Reflow process assembly notes:

- Use AuSn (80/20) solder and limit exposure to temperatures above 300°C to 3-4 minutes, maximum.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonic are critical parameters.
- Aluminum wire should not be used.