

### Product Overview

Qorvo’s TGA2598 is a broadband MMIC driver amplifier fabricated on Qorvo’s production 0.25um GaN on SiC process (QGaN25). Covering 6-12GHz, the TGA2598 provides more than 33dBm of saturated output power and 21dB of small signal gain while achieving more than 31% power-added efficiency.

The TGA2598 is an ideal choice to drive Qorvo’s high performing x-band GaN HPAs allowing the user to run both driver and HPA off the same voltage rail.

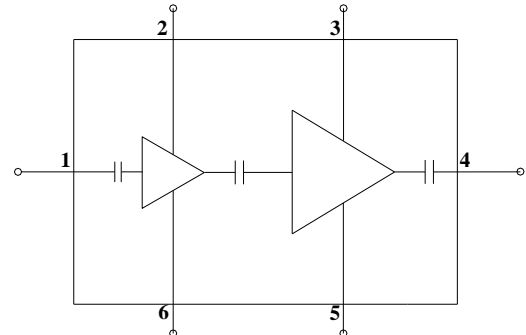
Fully matched to 50Ω with integrated DC blocking capacitors on both I/O ports, the TGA2598 is ideally suited for both military and commercial radar and communications applications.



### Key Features

- Frequency Range: 6 – 12 GHz
- P<sub>SAT</sub>: >33 dBm
- PAE: >31%
- Small Signal Gain: >21 dB
- Input Return Loss: >9 dB
- Output Return Loss: >11 dB
- Bias: V<sub>D</sub> = 25 V, I<sub>DQ</sub> = 100 mA, V<sub>G</sub> = - 2.6 V Typical
- Chip Dimensions: 2.14 x 1.11 x 0.10 mm

### Functional Block Diagram



### Applications

- Commercial and military radar
- Communications
- Electronic Warfare (EW)

### Ordering Information

Part No.	Description
TGA2598	6 – 12 GHz 2W GaN Driver Amplifier
1110980	TGA2598 Evaluation Board

## Recommended Operating Conditions

Parameter	Values	Units
Drain Voltage	25	V
Drain Current (quiescent, $I_{DQ}$ )	100	mA
Gate Voltage (typical)	- 2.6	V
Operating Temperature Range	- 40 to 85	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

## Electrical Specifications

Test conditions unless otherwise noted:  $V_D = + 25$  V,  $I_{DQ} = 100$  mA,  $V_G = - 2.6$  V typical, CW Mode, 25 °C.  
Data de-embedded to MMIC bond wires

Parameter	Min	Typ	Max	Units
Operational Frequency Range	6		12	GHz
Small Signal Gain		21		dB
Input Return Loss		9		dB
Output Return Loss		11		dB
Output Power ( $P_{SAT}$ , CW)		33		dBm
Power Added Efficiency ( $P_{SAT}$ , CW)		31		%
Small Signal Gain Temperature Coefficient		-0.05		dB/°C
Output Power Temperature Coefficient		-0.01		dBm/°C
Recommended Operating Voltage:		25	30	V

## Absolute Maximum Ratings

Parameter	Range / Value	Units
Drain Voltage ( $V_D$ )	40	V
Gate Voltage Range ( $V_G$ )	-8 to 0	V
Drain Current ( $I_{D1}$ )	128	mA
Drain Current ( $I_{D2}$ )	260	mA
Gate Current ( $I_{G1}$ )	1.4	mA
Gate Current ( $I_{G2}$ )	2.8	mA
Power Dissipation ( $P_{DISS}$ ), 85°C	6	W
Input Power ( $P_{IN}$ ), CW, 50 $\Omega$ , $V_D=25V$ , $I_{DQ}=100mA$ , 85°C,	30	dBm
Input Power ( $P_{IN}$ ), CW, VSWR 10:1, $V_D=25V$ , $I_{DQ}=100mA$ , 85°C	30	dBm
Mounting Temperature (30 Seconds)	320	°C
Storage Temperature	-55 to 150	°C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

## Thermal and Reliability Information

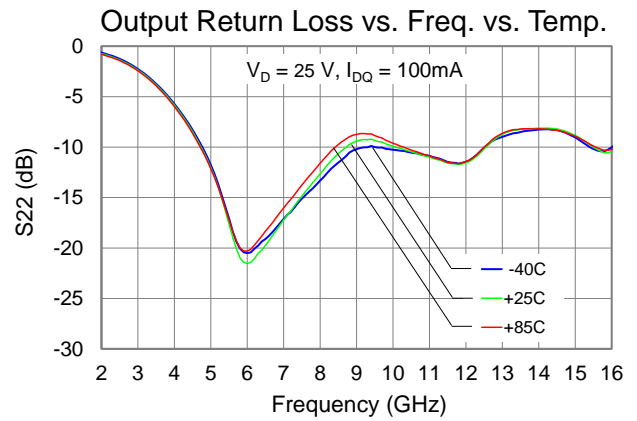
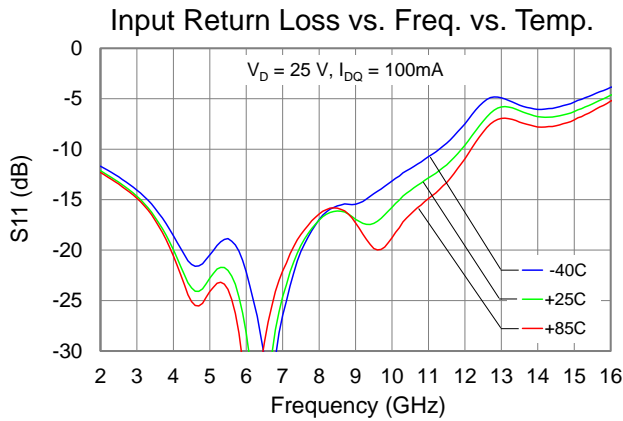
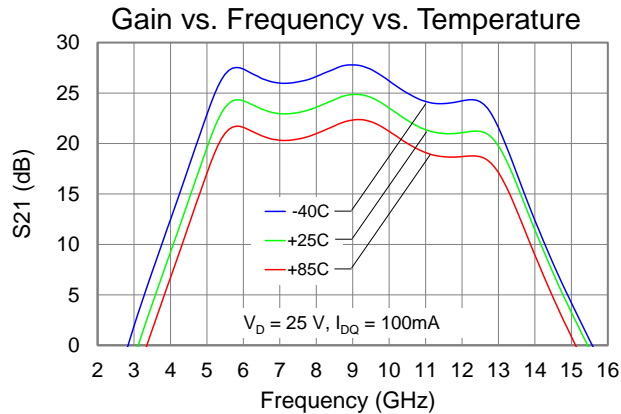
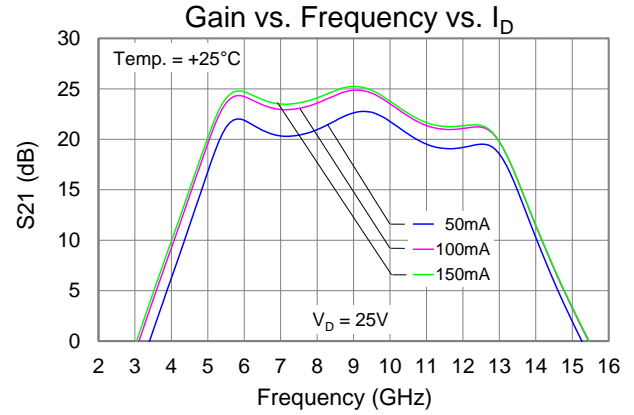
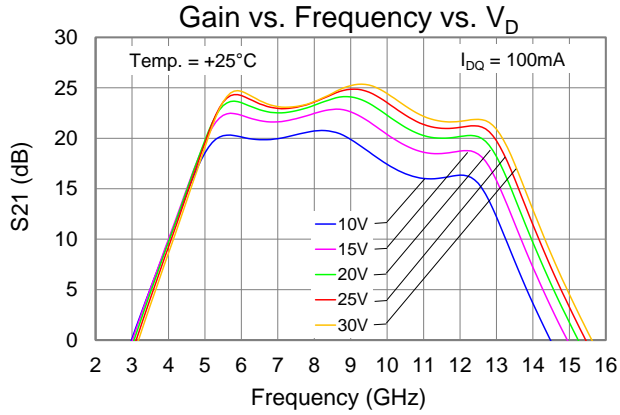
Parameter	Values	Units	Conditions
Under Drive, Thermal Resistance ( $\theta_{JC}$ ) <sup>(1,2,3)</sup>	14.52	°C/W	$T_{BASE} = 85^\circ C$ , $V_D = +25V$ , CW $I_{DQ} = 100mA$ , $I_{D\_DRIVE} = 285mA$ $P_{IN} = +20dBm$ , $P_{OUT} = +33.5dBm$ , $P_{DISS} = 4.8W$
Channel Temperature ( $T_{CH}$ )	154.69	°C	

Notes:

1. Thermal resistance is measured to package backside
2. Base or ambient temperature is 85 °C
3. Refer to the following document: [GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates](#)

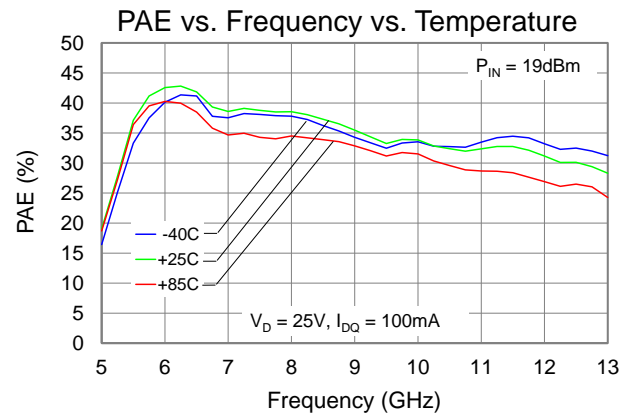
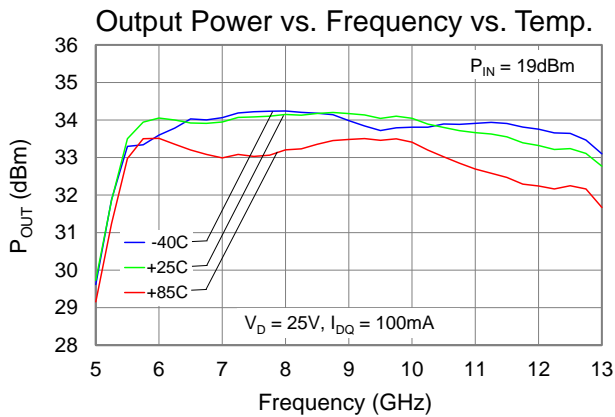
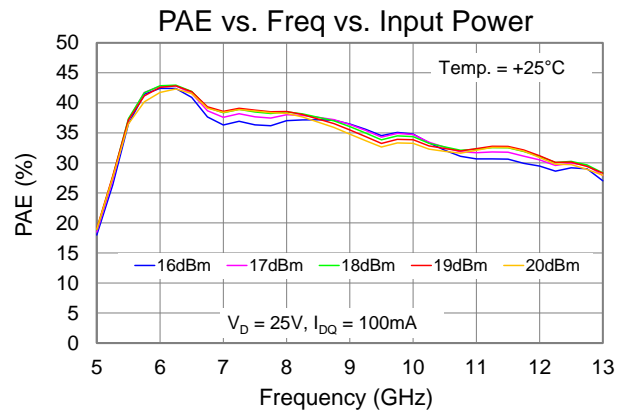
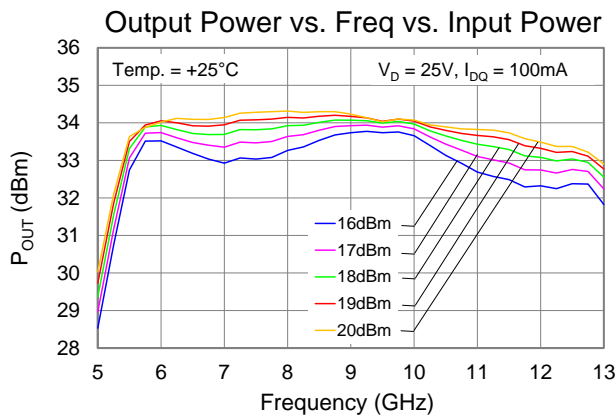
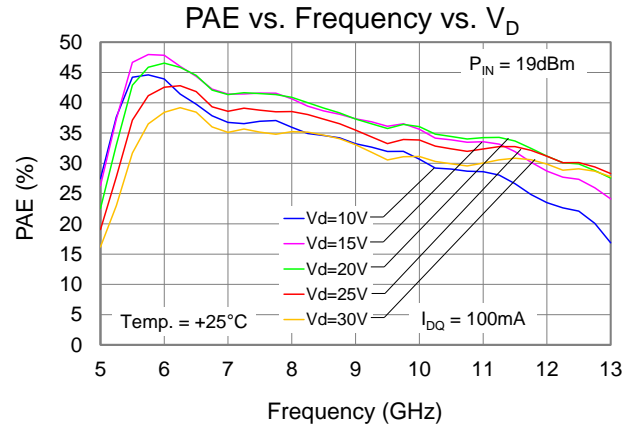
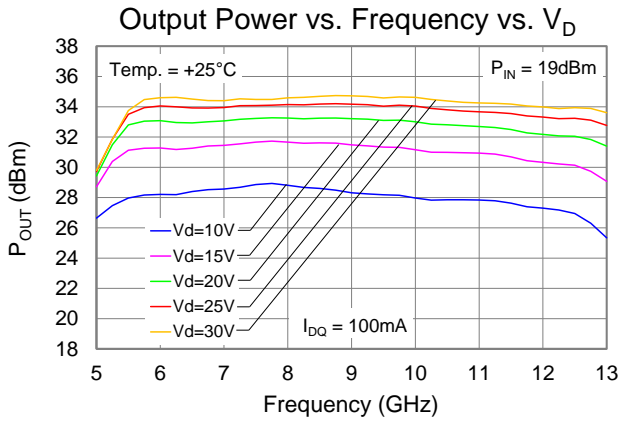
Performance Plots – Small Signal

Test conditions unless otherwise noted:  $V_D = +25\text{ V}$ ,  $I_{DQ} = 100\text{ mA}$ , Temp. =  $+25\text{ }^\circ\text{C}$



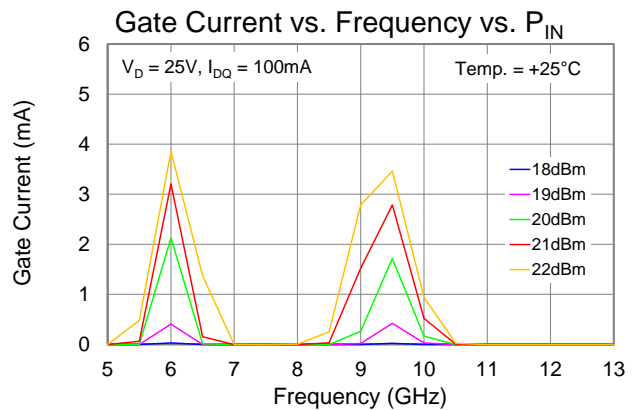
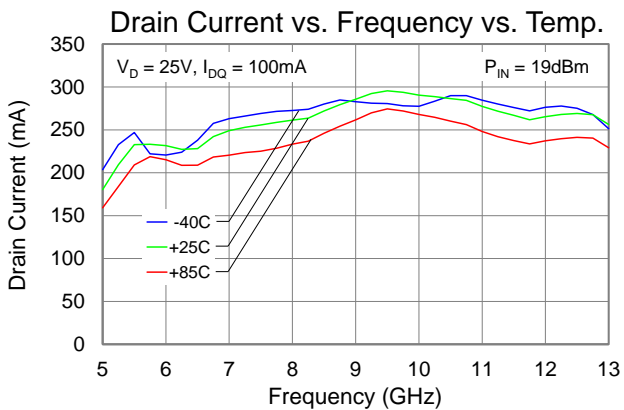
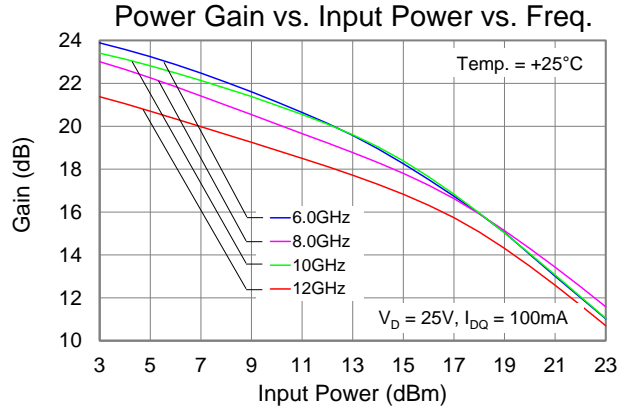
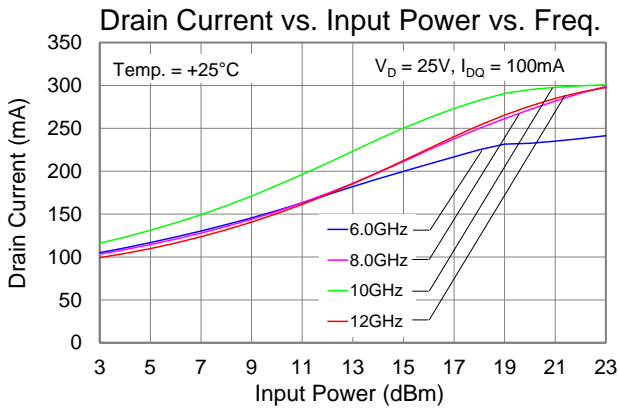
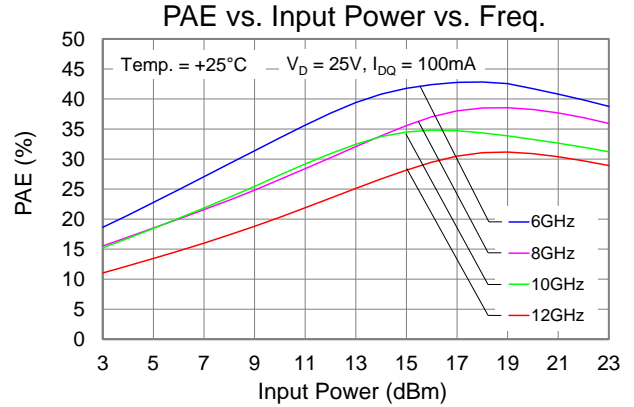
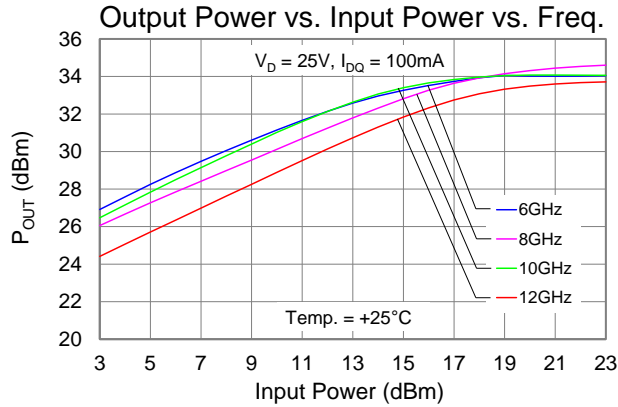
## Performance Plots – Large Signal

Test conditions unless otherwise noted:  $V_D = +25\text{ V}$ ,  $I_{DQ} = 100\text{ mA}$ , CW, Temp. =  $+25\text{ }^\circ\text{C}$



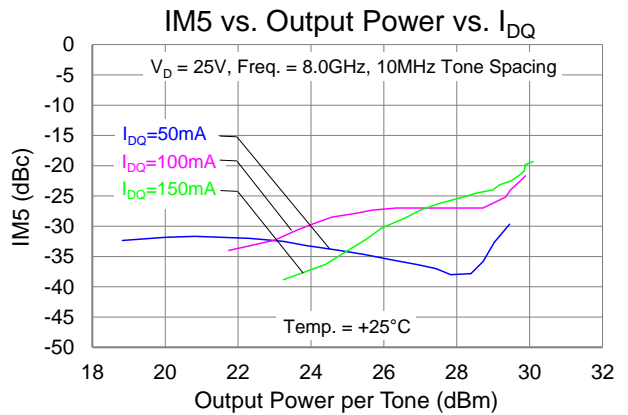
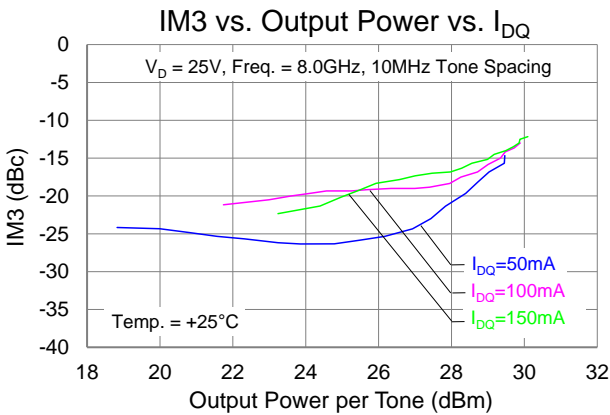
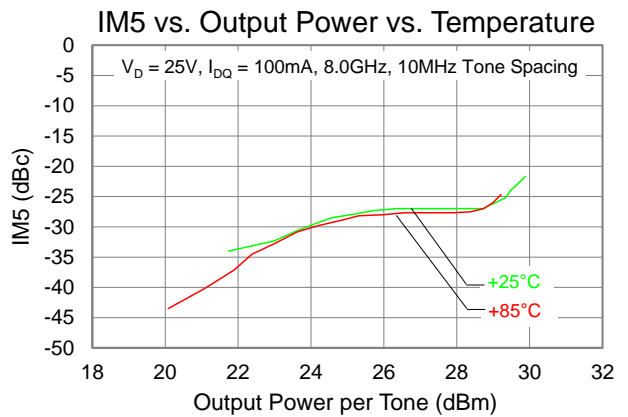
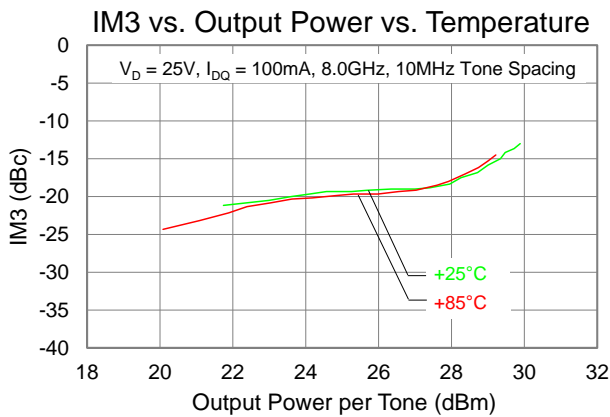
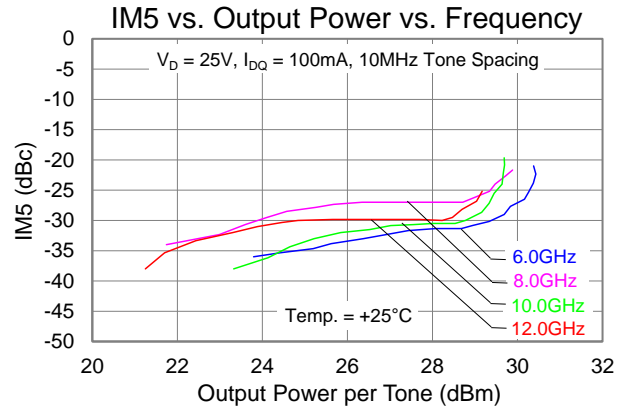
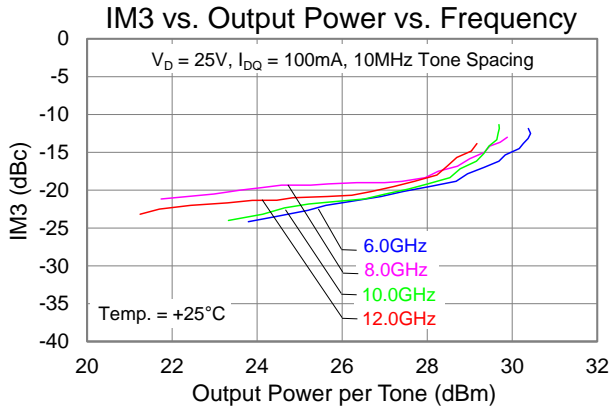
## Performance Plots – Large Signal

Test conditions unless otherwise noted:  $V_D = +25\text{ V}$ ,  $I_{DQ} = 100\text{ mA}$ , CW, Temp. =  $+25\text{ }^\circ\text{C}$



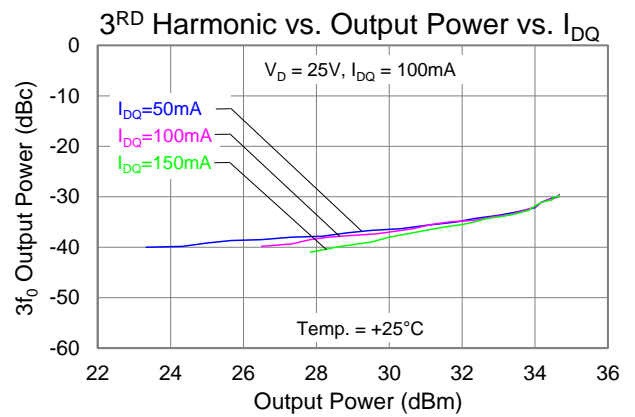
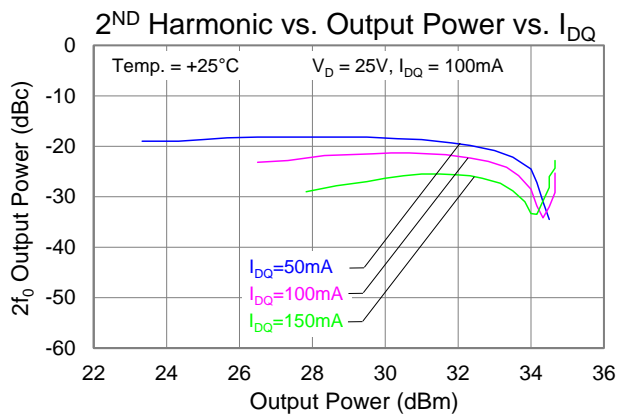
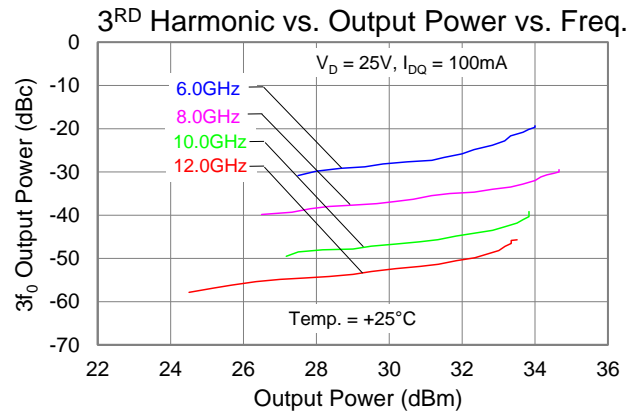
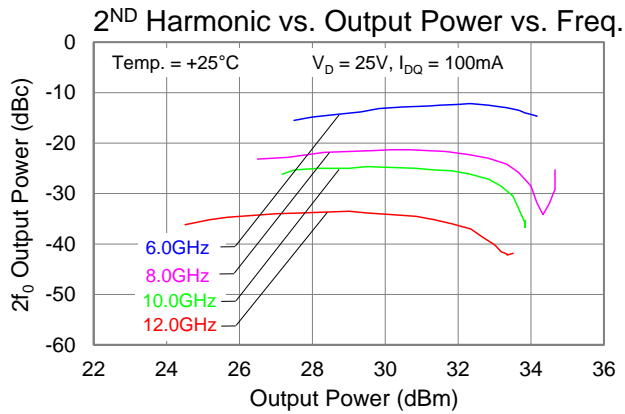
Performance Plots – Linearity

Test conditions unless otherwise noted:  $V_D = +25\text{ V}$ ,  $I_{DQ} = 100\text{ mA}$ ,  $\text{Temp.} = +25\text{ }^\circ\text{C}$



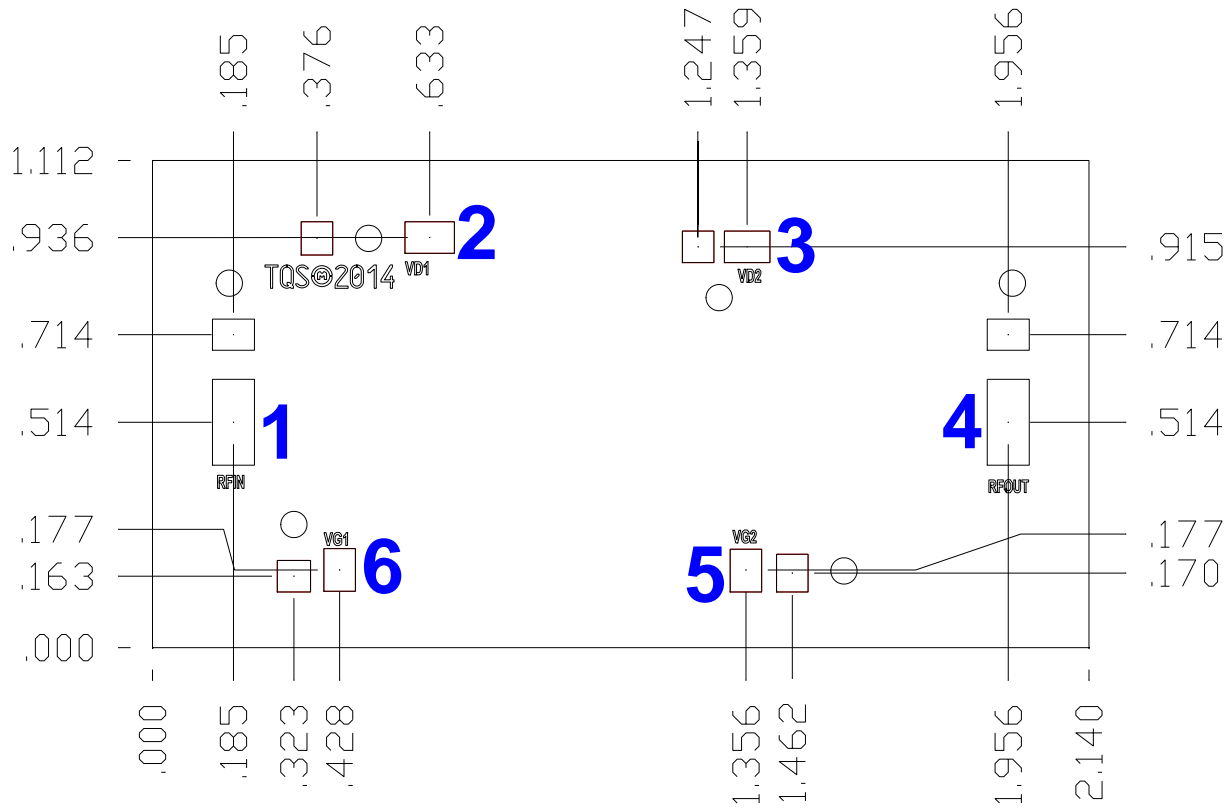
Performance Plots – Harmonics

Test conditions unless otherwise noted:  $V_D = +25\text{ V}$ ,  $I_{DQ} = 100\text{ mA}$ ,  $\text{Temp.} = +25\text{ }^\circ\text{C}$





**Mechanical Drawing and Bond Pad Description**



Dimensions in mm, Die Thickness: 0.10, Die x, y size tolerance: +/- 0.050  
Chip edge to bond pad dimensions are shown to center of pad

Bond Pad No.	Symbol	Pad Size	Description
1	RF IN	0.096 x 0.196	Input; matched to 50 ohms; DC blocked.
2	VD1	0.113 x 0.072	Drain voltage 1, bias network is required; see Application Circuit as an example
3	VD2	0.104 x 0.072	Drain voltage 2, bias network is required; see Application Circuit as an example
4	RF OUT	0.096 x 0.196	Output; matched to 50 ohms; DC blocked.
5	VG2	0.072 x 0.098	Gate voltage 2, bias network is required; see Application Circuit as an example
6	VG1	0.072 x 0.098	Gate voltage 1, bias network is required; see Application Circuit as an example

## Assembly Notes

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### **Component placement and adhesive attachment assembly notes:**

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment (i.e., conductive epoxy) can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.

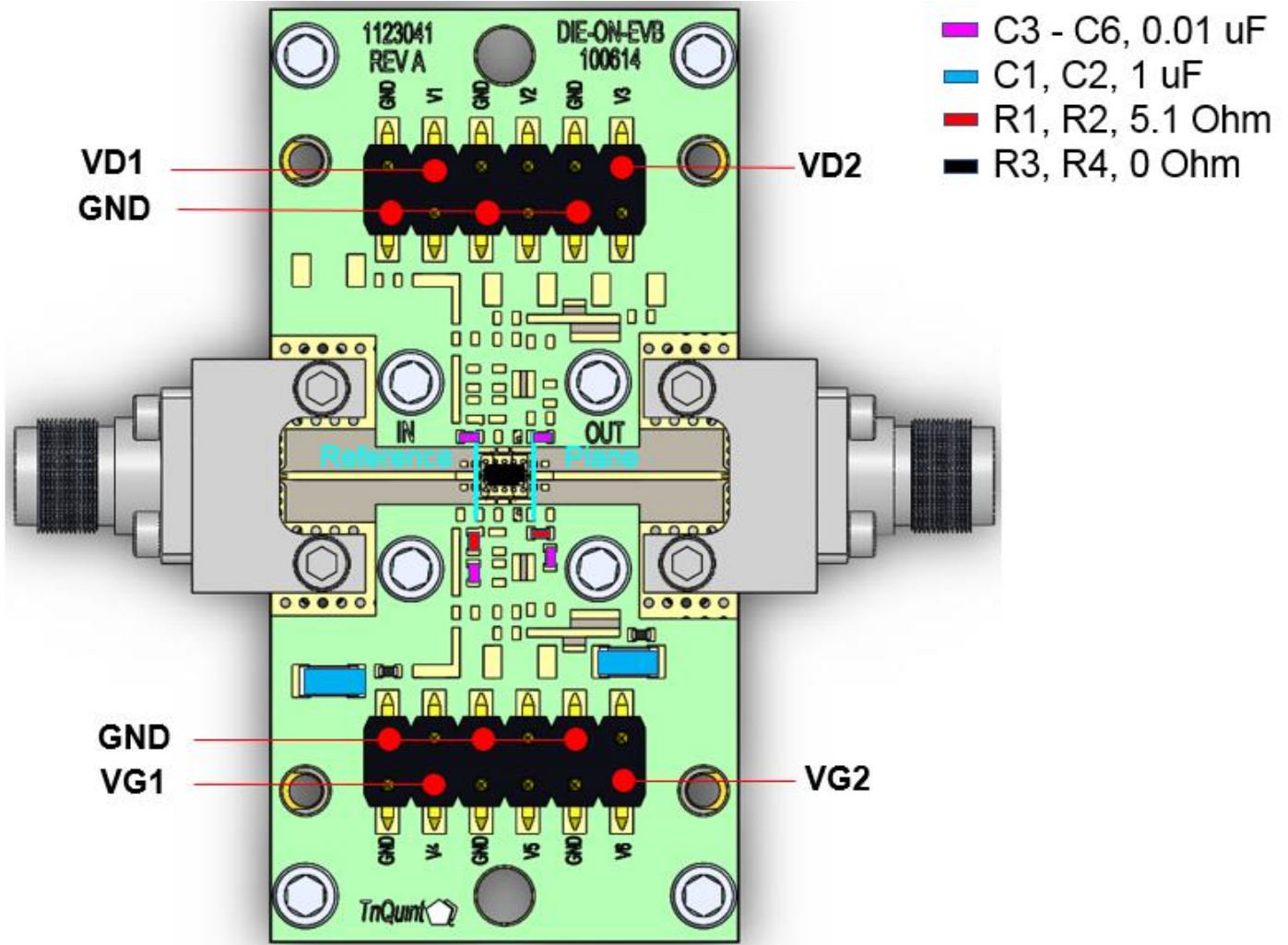
### **Reflow process assembly notes:**

- Use AuSn (80/20) solder and limit exposure to temperatures above 300°C to 3-4 minutes, maximum.
- Conductive epoxy die attach is recommended for PCB mounting.
- Bonding pads plating: Au.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

### **Interconnect process assembly notes:**

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonic are critical parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.

Evaluation Board and BOM



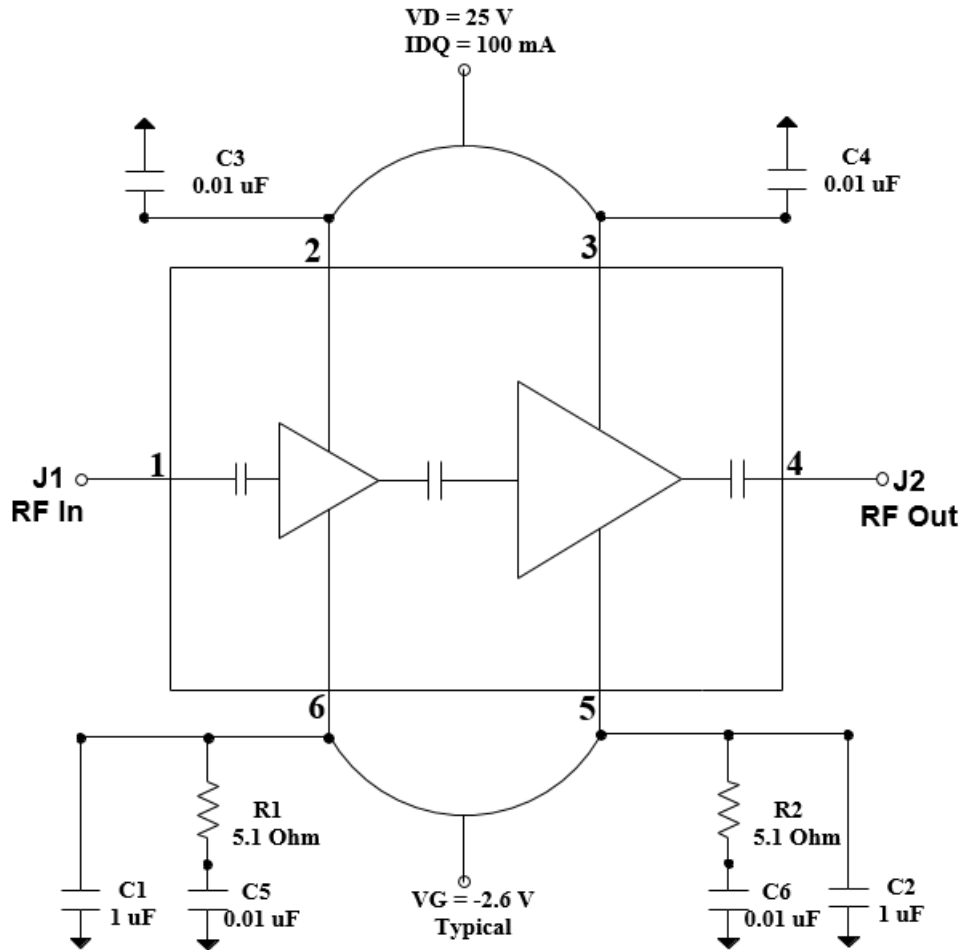
- C3 - C6, 0.01 uF
- C1, C2, 1 uF
- R1, R2, 5.1 Ohm
- R3, R4, 0 Ohm

RF Layer is 0.008" thick Rogers Corp. RO4003C ( $\epsilon_r = 3.35$ ). Metal layers are 0.5 oz. copper. The microstrip line at the connector interface is optimized for the Southwest Microwave end launch connector 1092-01A-5.

Bill of Material – Evaluation Board

Ref. Des.	Value	Description	Manuf.	Part Number
C1 – C2	1uF	Cap, 1206, 16V, 20%, X5R	Various	
C3 – C6	0.01uF	Cap, 0402, 50V, 10%, X7R	Various	
R1 – R2	5.1Ω	Res, 0402, 5%	Various	
RF IN, RF OUT	2.92 mm	2.92 MM END LAUNCH CONNECTOR	Southwest Microwave	1092-01A-5

Application Circuit and Biasing Sequence



Notes:

1. Can use separate gate and drain for individual stage controls.

**Bias-up Procedure**

1. Set  $I_D$  limit to 320mA,  $I_G$  limit to 4mA
2. Apply -5.0V to  $V_G$
3. Apply +25V to  $V_D$
4. Adjust  $V_G$  more positive until  $I_{DQ} = 100\text{mA}$  ( $V_G \sim -2.6\text{ V Typical}$ )
5. Apply RF signal

**Bias-down Procedure**

1. Turn off RF signal
2. Reduce  $V_G$  to -5.0V. Ensure  $I_{DQ} \sim 0\text{mA}$
3. Set  $V_D$  to 0V
4. Turn off  $V_D$  supply
5. Turn off  $V_G$  supply